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# Combining the best of bulk and surface micromachining using Si {111} substrates

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## ABSTRACT

This process combines the best features of bulk and surface micromachining. It enables the production of stress free, thick, virtually arbitrarily shaped structures with well defined, thick or thin sacrificial layers, high sacrificial layer selectivity and large undercuts using IC compatible, processes. The basis of this approach is the use of readily available {111} oriented substrates, anisotropic Si trench etching, SiN masking and KOH etching.

**Keywords:** {111} Si, Bulk Micromachining, Trench Etch, KOH, Surface Micromachining.

## 1. INTRODUCTION

Most micromachined devices can be split into two major classes, those formed by bulk micromachining and those formed by surface micromachining. The attraction of bulk micromachining is that it can produce parts, which have high stiffness in the "Z" dimension and relatively high masses for inertial sensors. However, there are only a limited number of possible shapes since the processes used are typically highly orientation dependent. On the other hand, using surface micromachining it is possible to fabricate parts with arbitrary lateral shapes. However these devices are limited in their vertical dimension and this limits both their mass and "Z" dimension stiffness. The approach described here combines the flexibility in patterning offered by surface micromachining with the potential for thick layers offered by bulk micromachining.

One of the cornerstones of bulk micromachining is KOH etching. The high selectivity of {111} planes and masking layers such as silicon nitride and silicon dioxide during KOH etching enables the inexpensive batch fabrication of holes and relatively bulky structures such as proof masses. A major disadvantage of this process is that it is dependent upon crystallographic orientation. This makes design of complicated structures difficult. Furthermore there are problems associated with the presence of "outside corners". While the selectivity of the etch to {111} planes is high, when two {111} planes intersect to create an outside corner the line of intersection is not a {111} plane and will therefore be rapidly eroded. This makes the fabrication of arbitrarily shaped structures impossible. In the last several years fluorine based, high rate reactive ion etching processes have become available which enable the fabrication of arbitrarily shaped features with vertical side walls [1]. However, the majority of applications require that at least portions of the part are freed from the substrate and this remains a problem.

The second major class of micromachining is surface micromachining. This rapidly evolving field leverages techniques developed for the silicon based semiconductor industry. The foundation of this approach is the use of low stress poly silicon as a structural material and deposited films of silicon dioxide as sacrificial layers. Since the sheets are patterned by photolithography they can be very accurately defined and have essentially arbitrary lateral shapes. However, the thickness of both the structural and sacrificial layers are limited to roughly 6 and 3 microns respectively due to problems of stress and low silicon deposition rates. This limits the force of the resulting actuators and the mass of the inertial plates. Furthermore, the

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fabrication of low stress poly silicon requires the use of a high temperate anneal step. This anneal greatly complicates the problem of integration of surface micromachined structures with integrated circuits since the anneal temperature is far greater then the melting point of the commonly used aluminum metallization.

The process described here combines the best features of bulk and surface micromachining. The basis of this approach is the use of readily available {111} oriented substrates. {111} surfaces have very low etch rates in KOH [2] relative to other orientations and we use this property to our advantage. In the first step the desired pattern is transferred into the {111} silicon substrate using photolithography and silicon trench etching. The sidewalls are then protected by a silicon nitride fillet. A second silicon trench etch is then performed, followed by a KOH release etch. Both the thickness of the part, and that of the sacrificial layer, are determined by the depth of a silicon trench etch. In this manner, well defined, thick parts can be fabricated for inertia masses and high force actuators. Large separations from the substrate can be obtained to reduce parasitic capacitances. If desired, the parts can be anchored to the substrate using silicon nitride or silicon dioxide plugs that extend into the substrate deeper than the sum of the structural and sacrificial layer thickness.

## 2. EXPERIMENTAL

The process is schematically shown in Fig 1. The starting material used for this study was {111} oriented, n-type, 150 mm wafers. The degree of misorientation from the {111} was 3.5°. In the first step, a 100nm layer of silicon nitride was deposited onto the wafer. The desired pattern was then photolithographically defined. The patterned photo resist was used as a mask for both the silicon nitride and the silicon etches. The silicon nitride was etched using a chlorine-based chemistry. The silicon was trench etched using an $SF_6/O_2$ chemistry in a electrostatically chucked ECR (electron cyclotron resonance) etcher. The etching chemistry of 100 sccm of $SF_6$ and 20 sccm of $O_2$ was run at -30°C at a pressure of 14 mTorr with 250mAmps of current incident on the wafer and a power on the wafer of 15 watts. The etch depth was varied between 5 and 20 microns. A 3 minute etch resulted in an etch depth of 10 microns on trenches with aspect ratio of ~2. The resist was then stripped. The sidewalls of the structure were then protected by the deposition of 100 nm of thermal SiN. The silicon nitride was cleared from the bottom of the trenches using an end-pointed, chlorine-based reactive ion etch. A second $SF_6$ etch was then used to partially trench into the substrate. The wafers were then exposed to an 85C, 4M KOH solution for a variety of etch times to undercut the structures. The SiN etch masks were then removed using a concentrated HF solution.

## 3. RESULTS

Examples of various structures are shown in Figure 2. The ability to form complex, released parts is clearly demonstrated. On these particular structures, the devices are anchored to the substrate only by a relatively wide pad which was not completely undercut during the etch process. It is also possible to anchor the structures using silicon dioxide or silicon nitride pillars which extend into the substrate deeper than the sum of the structural layer thickness plus the sacrificial layer thickness. Figure 3 shows the amount of undercut under one of the structures. The edge was not parallel to any of the 3 <111> directions running along the plane of the wafer. In this case the undercut is rapid since outside corners are continuously being exposed.

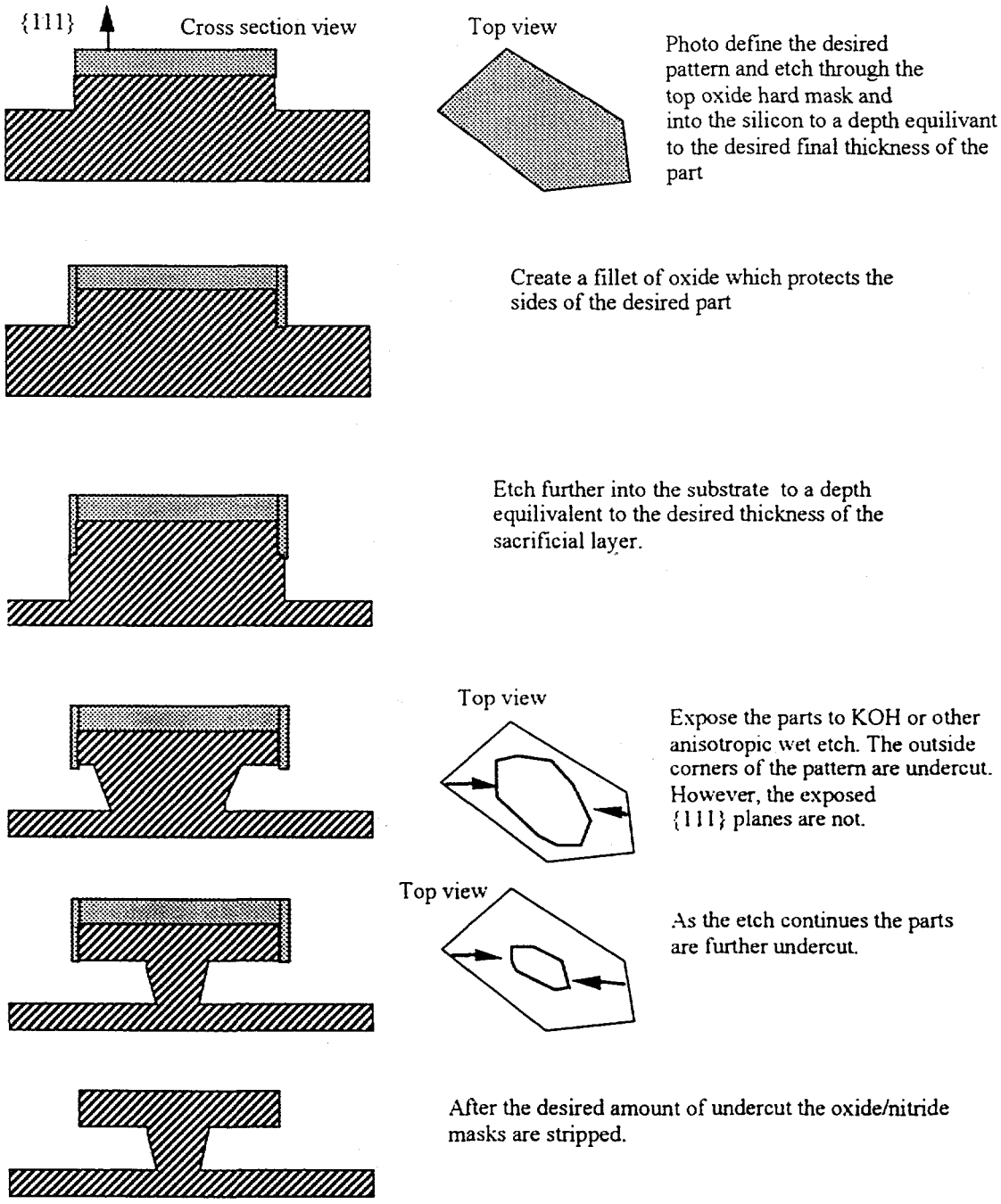


Fig. 1 Schematic of the process flow.

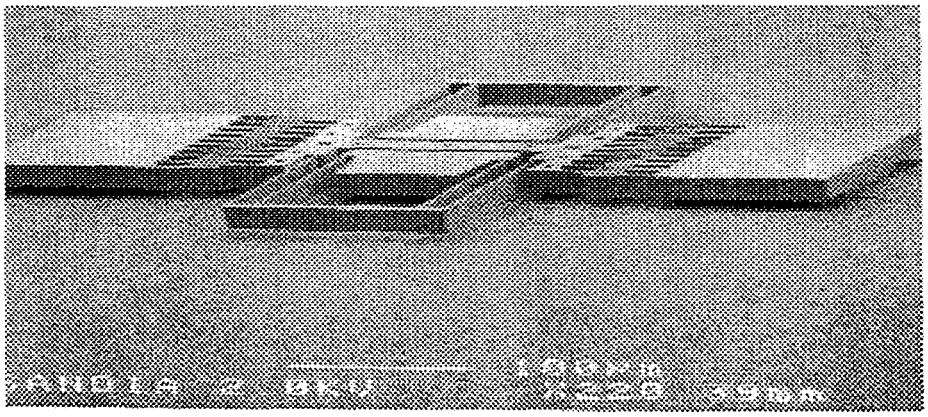

Fig. 2a.

Example of a part formed by this process.

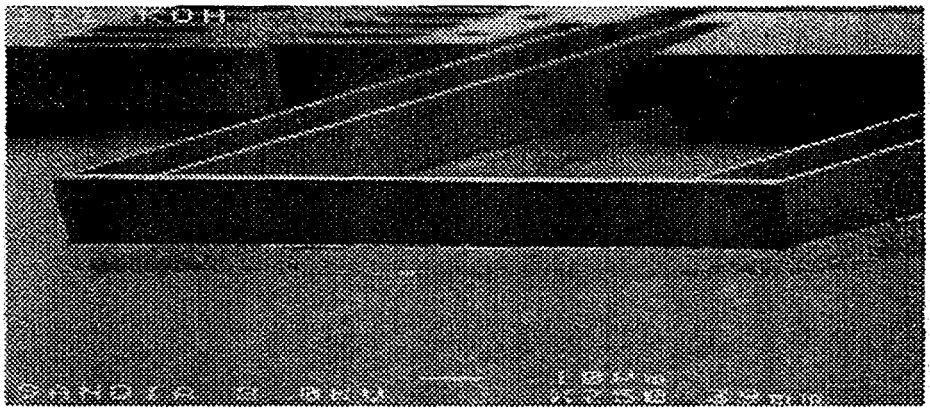

Fig. 2b

Close up of the folded spring in Fig. 2a. The structure is ~25 microns thick and the sacrificial layer thickness is ~8 microns. The spring and fingers have clearly been released.

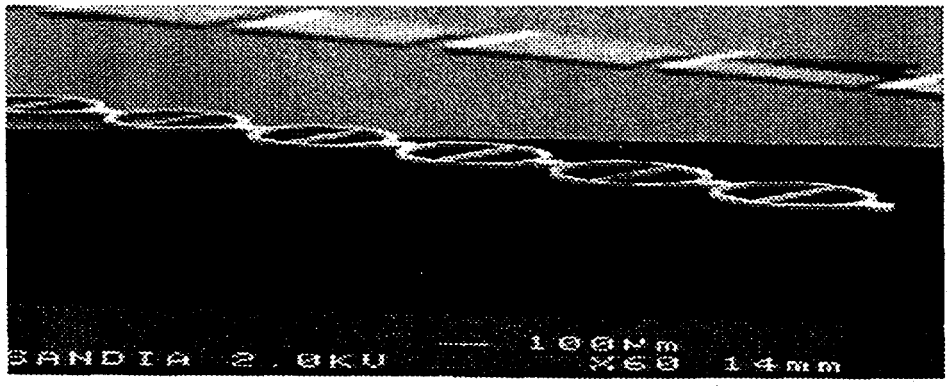

Fig. 2c

Example of release ring stress measurement structures extending over the edge of the cleaved, completed wafer. The rings have clearly been released from the substrate.

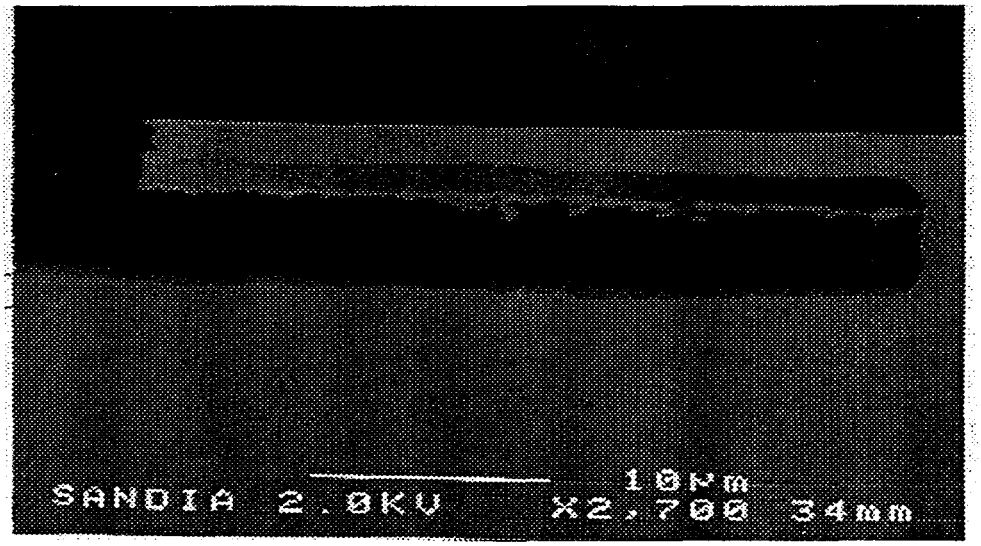


Fig. 3

Cross section of a plate undercut during the KOH release process. Since the wafer was not precisely aligned to the {111} direction, the plate is also being thinned during the etch.

There are no outside corners along directions aligned along one of the (111) planes intersecting the surface, Figure 4. In this case it is possible to form a series of stable inside corners. Such structures are released only through the propagation of outside corners, which may be present at the ends of the features. This problem can be overcome in several ways. The first is to ensure that the second, release, SF6 etch is sufficiently deep that the two sides intersect. The second approach is to align the parts so that the majority of the edges do not align with a <110> direction. Since the surface <110> directions are at 120 degrees to each other this is typically not a significant problem. Since the KOH etch selectivity's are extremely high, it is possible to simply release the structure through the continued erosion of outside corners as long as the wafer surface is aligned closely to the {111}. Figure 4 also shows problems associated with the wafer being 3.5° off the {111} and with aspect ratio dependent etching of the silicon during the SF6/O2 etches. Due to the misalignment the surface of the {111} wafer is continually being etched as a result of the exposed outside corners. This results in thinning of the part and eventual undercut of any insulation pillars. This problem can be addressed by the use of wafers with surfaces more closely aligned to the {111}. The other problem illustrated in Figure 4 is that of aspect ratio dependent etching during the SF6/O2 etch [3]. These phenomena gives rise to different aspect ratio structures having different etch rates. Because of this the semi-infinite edges of the part are etched faster than the silicon in the trenches.

## 4. DISCUSSION

There are many attractive features to this approach. The first is that the thickness of both the structural and sacrificial layers are determined by the depth of a reactive ion etch. With the commercialization of various trench etch technologies, these thickness' can be on the order of tens of microns. This is far thicker that those possible using conventional surface micromachining. For example, the process required for the creation of low stress silicon for surface micromachined structures requires almost 8 hours to deposit 2 microns of material. The standard process also requires a high temperature anneal. It is possible to deposit relatively low stress silicon dioxide sacrificial films. However, after any high temperature processing the stress in the films increases. The approach described here offers advantages in producing actuators with greater torque; motion sensors with heavier proof masses, structures with greater stiffness in the "Z"

direction and reduced capacitive coupling to the substrate. However, it must be kept in mind that these fluorine based trench etches suffer from aspect ratio dependent etching. Undercut of the structures can be rapid when the etched features are not aligned to the <110> directions, or if the separation between the two sides of the structure is small relative to the depth of the sacrificial etch depth.

In the work done here the etch masks used consisted of silicon nitride deposited by chemical vapor deposition at temperatures of ~800°C. However, low temperature (300°C) plasma enhanced CVD silicon nitride is also an effective KOH mask. Since the structural material consists of single crystalline silicon it is stress-free as formed and there is no need for the high temperature anneals required by polysilicon based structures. Since all the processing can be low temperature the integration of electronics may be simpler. However, {111} silicon is typically used for bipolar, and not CMOS based electronics.

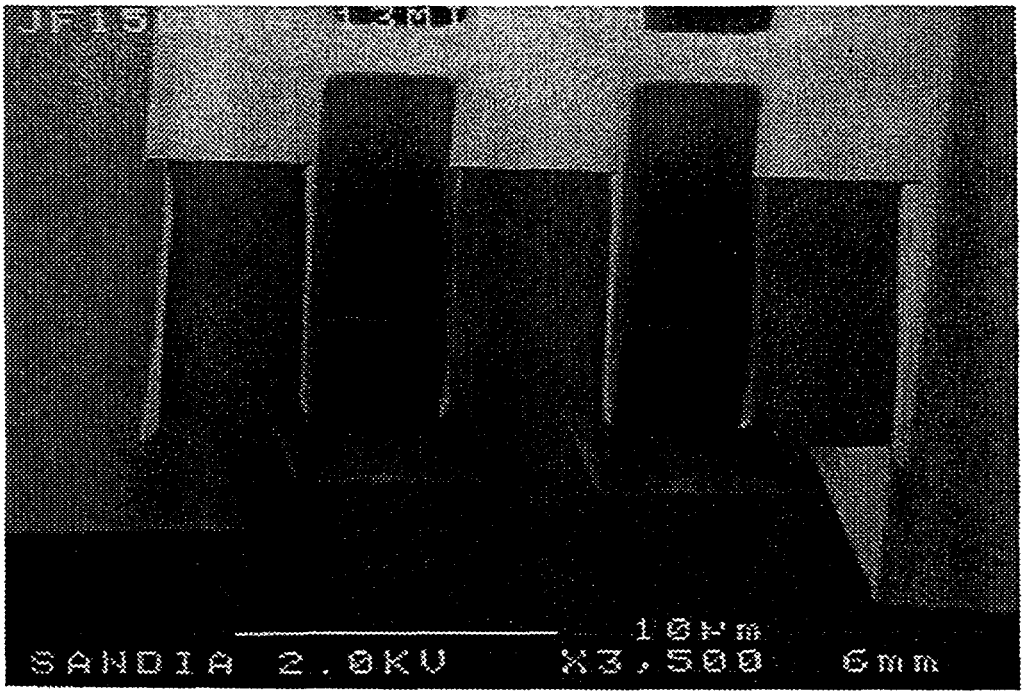


Fig. 4

Oblique view cross section of a partially released structure illustrating potential problems with aspect ratio dependent etching, alignment of the part edges along a <110> direction and missorientation of the wafer surface to the {111} plane. Since the field region is etching faster than the trenches, the depth of etch in the field is greater than that in the trench. Since the part was aligned to a <110> direction stable inside {111} corners are created and the parts are undercut only through the propagation of external outside corners. The misalignment of the wafer to the {111} results in variations in the fields on either side of the part. There are process, design or materials solutions to all these problems.

## 4. SUMMARY

A novel process has been developed for the fabrication of single crystalline sheets of silicon with nearly arbitrary shapes. The thickness of the structure and the sacrificial layer are defined by the depths of silicon trench etch processes. Both of these dimensions can be considerably greater than those attainable using conventional surface micromachining. Since the structures are of single crystalline silicon, they have low stress and their mechanical properties are well defined. The basis of the process is the use of readily

available {111} substrates combined with silicon trench etching, silicon nitride masking layers and KOH etching. All of the processes used are potentially low temperature compatible, and this may offer advantages for integration with electronics.

## 5. ACKNOWLEDGEMENTS

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