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NCMS PWB SURFACE FINISHES TEAM PROJECT SUMMARY

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ABSTRACT

The NCMS PWB Surface Finishes Consortium is just about at the end of the five year program. Dozens of projects related to surface finishes and PWB solderability were performed by the team throughout the program, and many of them are listed in this paper. They are listed with a cross reference to where and when a technical paper was presented describing the results of the research. However, due to time and space constraints, this paper can summarize the details of only three of the major research projects accomplished by the team. The first project described is an "Evaluation of PWB Surface Finishes", it describes the solderability, reliability, and wire bondability of numerous surface finishes. The second project outlined is an "Evaluation of PWB Solderability Test Methods". The third project outlined is the "Development and Evaluation of Organic Solderability Preservatives".

INTRODUCTION

The Advanced Technology Program (ATP) PWB Interconnect Systems is a five year research project which began in April of 1991. The program is sponsored by the National Institute of Standards and Technology (NIST) and is managed by the National Center for Manufacturing Sciences (NCMS). The consortium of companies was formed to pool their resources to perform research in four general areas of PWB fabrication; board materials, imaging, surface finishes, and product integration. The focus of this paper is on the research performed by the Surface Finishes Team. As is evident from the list of authors, who make-up the Surface Finishes Team, a good cross section of the industry is represented, as the participating companies are manufacturers of aerospace, telecommunications and computer products. This manufacturing contingency is enhanced by the membership and resources of Sandia National Laboratories. Appendix 1 contains a list of papers that have been publicly presented by the team.

PROJECT SUMMARY

The Surface Finishes Team project plan consists of five major areas of research. Some of the projects were performed by one member company, and others were carried out by combinations of companies. The following list is a brief outline of a number of the projects that were completed in each of these 5 areas.

1. Solderability Assessments

- The effects of surface roughness on solderability were demonstrated. Research was performed to optimize the concentrations and exposure times of several chemical etchants.
- A study was performed to determine if Sequential Electrochemical Reduction Analysis (SERA) could be used to differentiate varying degrees of copper roughness.
- The effects of grooves on wetting were characterized and modeled.
- The surface chemistry of solder on copper was investigated and characterized.
- The oxidation behavior of tin/lead and Imidazole coated copper finishes was examined.
- The kinetics of copper aging were characterized.
- The effects of oxide/sulfide film thicknesses on tin/lead solderability were determined.
- The effects of roughness on aging and solderability were performed with both bare and OSP treated copper.
- A number of PWB solderability tests were evaluated, several emerging technology tests were characterized, and one new test, the capillary flow test vehicle was developed by Sandia with the aid of team members.

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2. Solderable Finish Stressing

- A study to define the connection between storage conditions and time on PWB solderability was performed.
- The effects of steam aging time and temperature on PWB solderability was studied in cooperation with the IPC.
- The degree of temperature variability in steam aging equipment was characterized in cooperation with the IPC.
- A study was performed to determine the shelf life of Imidazole coated copper PWBs.

3. Baseline and Benchmarking

- An extensive evaluation of alternative surface finishes was performed.
- A PWB solderability survey was performed, collecting data from 21 plants.
- A study was performed to evaluate the performance of 5 Liquid Photo Imageable Solder Masks (LPISM).

4. Surface Finish Improvements

- Extensive process development work was performed to develop and implement Imidazole Organic Solderability Preservative (OSP).
- Evaluations of numerous commercially available OSPs were performed.
- The effects of no-clean and aggressive flux soldering processes on OSPs were evaluated.
- Two processes were developed for detecting the presence of OSP coatings on bare copper.
- The Reduced Oxide Soldering Activation (ROSA) process was evaluated.
- The use of plasma as a flux replacement was evaluated.
- An electroplated palladium over nickel process was developed and characterized.
- A DOE was performed to optimize the stencil aperture and solder paste for bumping flip chip pads using a stencil printing process.
- Sequential electrochemical reduction analysis (SERA) was characterized and developed as a process evaluation and trouble-shooting tool.
- "Engineering" solder flow on copper was performed by mechanical and chemical roughening of surfaces.

5. Surface Finishes for New Assembly Technologies

- The SF Team has collaborated with the NCMS Conductive Polymer and Lead-Free Alloy teams to evaluate Lead-Free PWB surface finishes..
- Mechanical reliability testing before and after environmental stressing was performed on the 12 benchmark surface finishes.
- A wire bondability evaluation was performed on a number of gold and palladium chemistries and thicknesses. The boards were subjected to various

simulated assembly environments prior to wire bonding to evaluate compatability and robustness.

EVALUATION OF PWB SURFACE FINISHES

INTRODUCTION

Tin-lead solder coatings have been the industry standard surface finish for Printed Wiring Boards for many years. However, alternative PWB surface finishes have been receiving renewed interest by the electronics industry in response to external and internal factors. With a variety of environmental (CFC and lead elimination), new packaging technologies (finer pitch devices, chip-on-board, flip chip, etc.), design (pad co-planarity), cost (global competition) and metallurgical (solder wetting) issues facing PWB fabricators, future PWB surface finishes will most likely need to be different from the current tin-lead finishes. To help address these needs, the Surface Finishes Team has evaluated 4 major performance criteria of alternative surface finishes, solderability, cost, reliability, and wire bondability. The objective of this study was to identify potential alternative surface finishes and compare these candidate finishes with the finishes currently being used by the project participants.

The surface finishes being evaluated as part of this project included a number of baseline and benchmark finishes. The baseline finishes consisted of Organic Solderability Preservative (OSP) coatings, tin-lead Hot Air Solder Leveled (HASL) surfaces, and reflowed electroplated tin-lead surfaces. The benchmark finishes included two immersion gold over electroless nickel chemistries, immersion tin-lead solder, a modified OSP coating, a lead-free HASL solder, immersion tin, electroplated tin, electroless gold over electroless nickel, electroplated gold over electroplated nickel, non-reflowed electroplated tin-lead, electroless palladium over electroless nickel, electroplated palladium over electroplated nickel, and two tin-bismuth alloys.

SOLDERABILITY

Phase I of the solderability testing involved a screening process of the aforementioned surface finishes using 40 hole, plated through hole (PTH) coupons. The rationale was to determine the solderability of the baseline finishes, and to screen the benchmark finishes against the baseline to determine their potential for further evaluation. The coupons were subjected to accelerated stresses to increase the sensitivity of the test. Based on this Phase I testing, it was decided to not pursue further testing of three of the benchmark finishes due to poor performance. The 3 finishes were electroplated tin and the two tin/bismuth

alloys (10% and 30% bismuth). The remaining twelve finishes continued to Phase II of the testing.

Phase II of the testing involved using a test vehicle called the Solderability Test Vehicle (STV), see Figure 1. This test vehicle is a double sided epoxy-glass board. It was designed to have a broad representation of components that are currently in use today. Most of the components are daisy chained, thus allowing them to be electrically monitored during any functional or environmental testing. With this test vehicle, the surface finishes could be evaluated in assembly and accelerated life environments. The STV assembly consists of the following components:

<u>Component</u>	<u>Qty.</u>
1206 Chip Capacitors (20 top/20 bottom)	40
SOT-23 (8 top side/8 bottom side)	16
SOIC 20	7
LCCC 44	1
PLCC 44	1
PLCC 84	1
132 QFP (0.025" pitch)	1
208 QFP (0.5mm pitch)	1

256 QFP (0.4mm pitch)	1
256 Ceramic BGA (0.05" pitch)	1
20 pin Ceramic DIP	2
20 pin Plastic DIP	3
68 pin PGA	1
Axial Resistors	65

The assembly evaluation involved four of the member companies assembling STV's in their production facilities. One of the companies assembled boards in two facilities, making a total of 5 participating assembly sites. Three of the production sites assembled 16 boards of their baseline finish and 4 boards of each of the 12 benchmark finishes. Two of the production sites assembled 16 boards of their baseline finish and 4 boards each of 5 of the benchmark finishes. All of the production sites assembled boards using their existing production processes. Table 1 shows a matrix of the processes used at each of the assembly sites. As you can see, a wide range of assembly material/processes, from aggressive water soluble, total immersion clean, to non-aggressive no-clean were used.

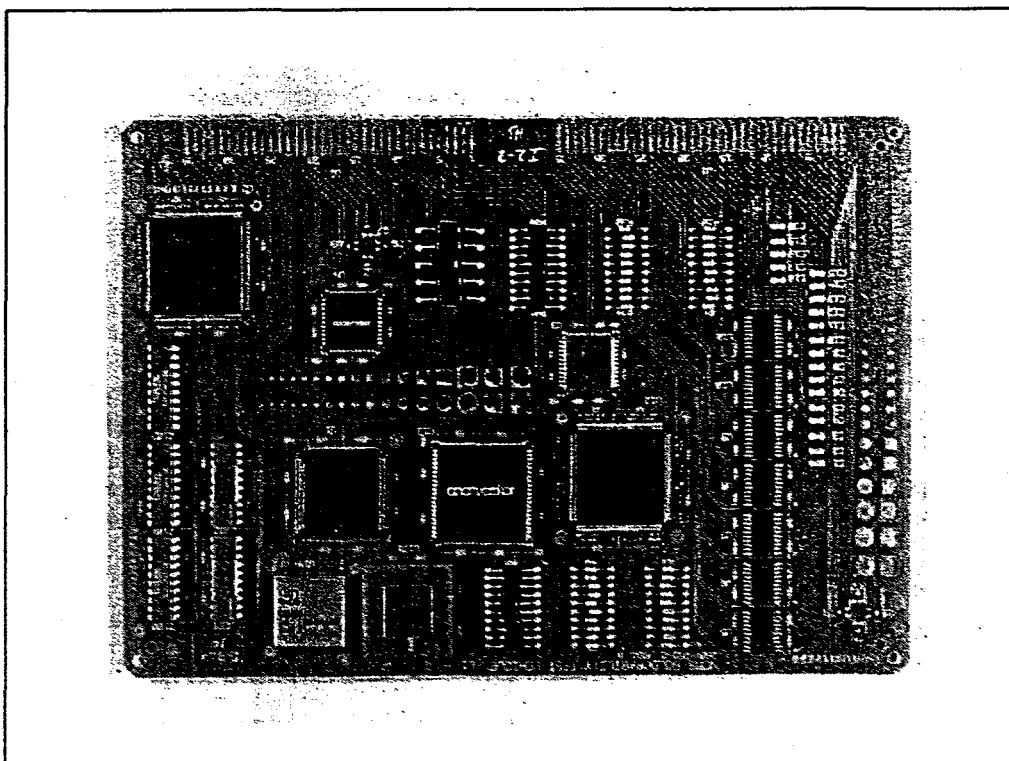
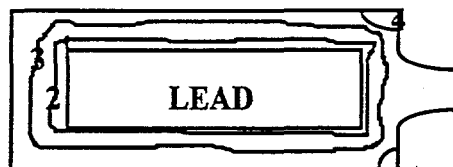


Figure 1 - Solderability Test Vehicle (STV)

MIXED TECHNOLOGY ASSEMBLY PROCESSES / MATERIALS	ASSEMBLY SITE A	ASSEMBLY SITE B	ASSEMBLY SITE C	ASSEMBLY SITE D	ASSEMBLY SITE E
Surface Mount Solder Paste Flux	RMA	RMA	WS	RMA	WS
Surface Mount Reflow Environment	Nitrogen	Air	Air	Nitrogen	Nitrogen
Cleaning After Surface Mount	None	Semi-Aqueous	Water	Semi-Aqueous	Water
Bottom Side Adhesive Cure Environment	Air	Air	Air	Air	Nitrogen
Wave Soldering Flux	LSF	RMA	WSF	RMA	WSF
Wave Soldering Flux Application Method	Spray	Wave	Foam	Wave	Foam
Wave Soldering Environment	Nitrogen	Air	Air	Air	Air
Cleaning After Wave Soldering	None	Semi-Aqueous	Water	Semi-Aqueous	Water

Table 1 - STV Assembly Site Processes

After assembly, all of the boards were inspected at the site assembling the boards. The inspection was performed and data collected on a common inspection sheet which described the defect criteria. This was an attempt to obtain some commonality in the gathering of the data. Surface mount components were inspected for bridges, opens, dewet leads, lead alignment and wetting rate. Wetting rate was assigned a factor from 1 - 5 as defined in the diagram below:



1. - No solder
2. - Insufficient solder
3. - Exposed area around pad
4. - Exposed corners of the pad
5. - Complete pad coverage

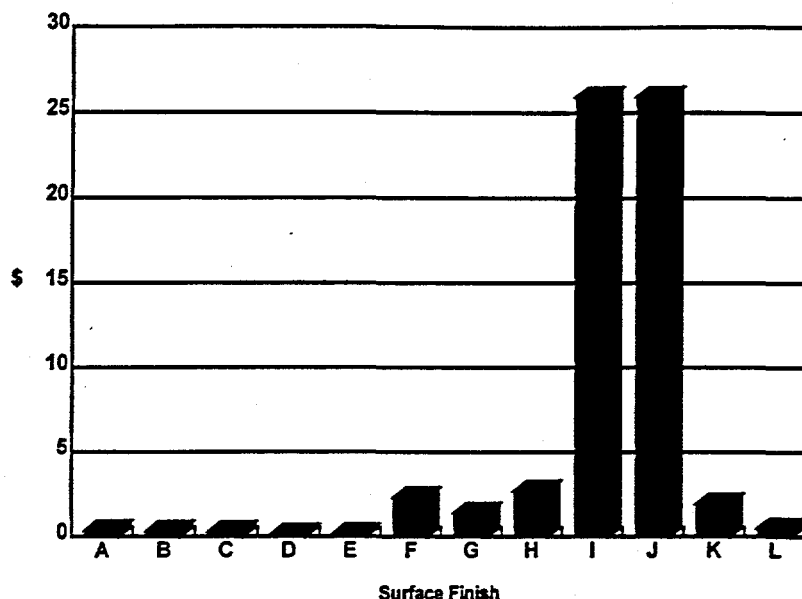
Plated through hole components were inspected for bridges, opens, dewet leads, dewet pads, excessive solder, and topside fillets.

The results of the inspection are summarized in Table 2 . Due to the large number of processes that are currently in use today, it is difficult to make any general conclusions from the data. It is more beneficial to look at the data as it is broken down, by assembly site process and board design (i.e. PTH or SMT). Based on that

analysis one might judge which surface finishes might hold the best potential for application or further evaluation for a specific design

SURFACE FINISH COST

Another important consideration in selecting a surface finish is its cost. Since it was found that many of the surface finishes selected were not in full scale production, a large cost disparity was found from board vendor to vendor. Because of this, only the chemistry costs for the different finishes were collected. The approximate cost for the various chemistries is shown in Figure 2. The approximate costs are in \$/square foot based upon 30% coverage on 2 sides. From this data, it is clear that the OSPs provide the lowest cost alternative. The metallic finishes reflect an increase in chemistry costs over the current tin-lead surfaces. It was left to each individual company to analyze the overall cost for a given surface finish. This analysis would include all PWB fabrication costs, assembly defect costs related to the surface finish, and other associated costs.



Legend: A = SnPb HASL; B = SnPb Plate & Reflow; C = Immersion SnPb; D = OSP#1; E = OSP#2; F = Electroless Pd over Ni; G = Electroless Pd over Cu; H = Immersion Au over Electroless Ni; I = Electroless Au over Ni; J = Electroplated Au over Ni; K = Electroplated Pd over Ni; L = Lead-Free HASL

Figure 2 - Approximate Surface Finish Chemistry Cost

SURFACE FINISH INTERCONNECT INTEGRITY/RELIABILITY/BONDABILITY

Many of the baseline surface finishes are noble metals. The intent was that the noble metal plated finishes should provide a flat solderable surface for fine pitch packages as well as be wire bondable. Phase I and II of the PWB surface finishes project only evaluated the solderability of these surfaces. For this reason, phase II was expanded to include both the wire bondability and the integrity/reliability of the solder interconnections made to the noble metal surface finishes. The selection of noble metal thickness was based on anticipated need for wire bondability and vendor recommendations. Although calculations indicated that the noble metal concentration in STV solder joints, for the surface finishes selected, was well below the 3 to 5 weight percent taken as the critical value for solder embrittlement, it was decided to assess the integrity of the interconnections by mechanical pull testing.

PWB SOLDER INTERCONNECTION INTEGRITY/RELIABILITY

The mechanical integrity of solder interconnections was measured by pull testing leads of surface mount packages soldered on STVs. The body of the surface mount packages were excised using a low speed diamond saw. Individual leads were grasped with a stainless steel clamp

mounted on a motorized micro-tensile tester. The leads were vertically pulled at a rate of 0.4 inches per minute and the mechanical failure strength recorded. Sufficient time and resources were not available to pull test all leads on each of the assembled STVs. A decision was made to pull test leads from three package styles:

- 256 I/O 0.4 mm Pitch PQFP Gull Wing Leads
- 84 I/O 50 mil Pitch PLCC J-Leads
- 20 I/O 50 mil Pitch SOIC Gull Wing Leads

Mechanical testing of the SOICs is ongoing and not included herein. However, the PLCCs are representative of standard surface mount packages and the 0.4 mm pitch PQFPs are representative of state-of-the art packages. It should be noted that the mechanical integrity testing was performed on STVs assembled at site "A" using non-aggressive "no-clean" assembly.

While pull testing "as assembled" STVs provides an adequate representation of the mechanical integrity of solder interconnections, additional evaluations are required for assessment of the interconnection reliability. Since four STVs of each surface finish were assembled for the benchmark evaluations, it was decided to mechanically pull test interconnections in the following conditions:

ASSEMBLY SITE/PROCESS	Sn/Pb	Sn/Pb NR	Sn/Pb HASL	ELS Sn/Pb	IMZ EP Cu	IMZ ES Cu	Thk OSP	BTA	Pb-free HASL	IMM Sn	IMM Au-1	IMM Au-2	ELP Au	ELS Au	ELP Pd	ELS Pd
SMT % DEFECTIVE																
Site A (rank/14)	n/a	0.0 (1)	n/a	0.83 (9)	0.01 (2)*	0.00 (1)	0.00 (1)	n/a	0.29 (7)	0.60 (8)	0.00 (1)	0.21 (4)	0.29 (7)	0.26 (5)	0.02 (3)	0.27 (8)
Site B (rank/14)	4.2 (13)*	2.59 (11)	n/a	2.16 (9)	1.41 (6)	0.25 (2)	2.28 (10)	n/a	17.84 (14)	3.31 (12)	0.56 (4)	0.28 (3)	0.23 (1)	1.89 (8)	1.13 (5)	1.44 (7)
Site C (rank/6)	2.4 (5)*	0.84 (3)	n/a	n/a	n/a	0.00 (1)	n/a	n/a	n/a	n/a	n/a	n/a	2.31 (4)	0.30 (2)	0.00 (1)	n/a
Site D (rank/6)	6.5 (4)*	1.23 (3)	n/a	n/a	n/a	1.15 (2)	n/a	n/a	n/a	n/a	n/a	n/a	18.18 (8)	10.26 (5)	0.38 (1)	n/a
Site E (rank/13)	n/a	0.0 (1)	4.97 (9)*	14.9 (12)	n/a	3.01 (4)	9.99 (11)	7.2 (10)*	4.91 (8)	15.84 (13)	0.00 (1)	3.77 (6)	0.16 (3)	3.80 (7)	3.55 (5)	0.08 (2)
SMT WETTING RATE/6																
Site A (rank/14)	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Site B (rank/14)	4.98 (4)*	3.91 (10)	n/a	5.00 (1)	4.366 (8)	4.194 (9)	4.530 (8)	n/a	4.424 (7)	4.686 (5)	4.99 (2)	4.990 (3)	5.00 (1)	5.000 (1)	3.26 (1)	3.102 (12)
Site C (rank/6)	4.53 (5)*	4.87 (4)	n/a	n/a	n/a	4.066 (8)	n/a	n/a	n/a	n/a	n/a	n/a	4.998 (2)	5.000 (1)	4.712 (3)	n/a
Site D (rank/6)	4.17 (4)*	4.79 (2)	n/a	n/a	n/a	4.328 (3)	n/a	n/a	n/a	n/a	n/a	n/a	5.00 (1)	5.000 (1)	3.970 (5)	n/a
Site E (rank/14)	n/a	4.73 (9)	4.81 (8)*	4.98 (5)	n/a	4.59 (10)	4.42 (11)	4.04 (12)*	5.00 (1)	4.91 (8)	5.00 (1)	4.98 (4)	4.98 (2)	4.98 (3)	4.83 (7)	5.00 (1)
BOTTOM SIDE WAVE																
%DEFECTIVE																
Site A (rank/14)	n/a	0.06 (1)	n/a	2.41 (7)	2.33 (6)*	1.86 (4)	2.90 (8)	n/a	4.41 (11)	5.93 (13)	2.27 (5)	3.98 (9)	3.8 (10)	4.69 (12)	0.13 (2)	1.17 (3)
Site B (rank/14)	1.5 (9)*	0.0 (1)	n/a	0.00 (1)	2.41 (10)	0.27 (4)	0.82 (7)	n/a	0.13 (3)	0.55 (5)	0.75 (6)	0.08 (2)	0.08 (2)	0.08 (2)	0.27 (4)	1.03 (8)
Site C (rank/6)	0.3 (1)*	1.31 (2)	n/a	n/a	n/a	5.80 (6)	n/a	n/a	n/a	n/a	n/a	n/a	5.04 (4)	5.45 (5)	3.17 (3)	n/a
Site D (rank/6)	2.2 (3)*	0.48 (1)	n/a	n/a	n/a	6.83 (6)	n/a	n/a	n/a	n/a	n/a	n/a	4.35 (5)	3.10 (4)	0.69 (2)	n/a
Site E (rank/14)	n/a	2.48 (2)	0.05 (1)*	4.83 (4)	n/a	36.7 (10)	14.43 (6)	0.05 (1)*	4.07 (3)	7.25 (5)	18.23 (7)	29.2 (9)	51 (13)	28.45 (8)	41.1 (12)	37.91 (11)
TOP SIDE WAVE SOLDER																
CLASS 1/2 % DEFECTIVE																
Site A (rank/14)	n/a	0.92 (3)	n/a	0.41 (2)	0.25 (1)*	1.09 (5)	1.84 (6)	n/a	8.64 (11)	2.34 (7)	0.25 (1)	7.88 (10)	1.00 (4)	3.60 (9)	2.34 (7)	3.02 (8)
Site B (rank/14)	0.0 (1)*	0.0 (1)	n/a	0.00 (1)	0.98 (6)	1.09 (7)	1.51 (9)	n/a	1.84 (10)	0.08 (2)	0.33 (4)	3.02 (11)	0.08 (2)	0.18 (3)	1.17 (8)	0.41 (5)
Site C (rank/6)	0.0 (1)*	0.0 (1)	n/a	n/a	n/a	0.00 (1)	n/a	n/a	n/a	n/a	n/a	n/a	0.58 (2)	0.00 (1)	0.00 (1)	n/a
Site D (rank/6)	0.0 (1)*	0.0 (1)	n/a	n/a	n/a	0.00 (1)	n/a	n/a	n/a	n/a	n/a	n/a	0.18 (2)	0.00 (1)	0.00 (1)	n/a
Site E (rank/14)	n/a	0.25 (3)	0.16 (2)*	0.00 (1)	n/a	9.06 (11)	0.50 (4)	1.34 (7)*	0.00 (1)	1.59 (9)	0.75 (6)	2.43 (10)	0.00 (1)	0.67 (5)	0.00 (1)	1.51 (8)
TOP SIDE WAVE SOLDER																
CLASS 3 %DEFECTIVE																
Site A (rank/14)	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Site B (rank/14)	0.04 (2)*	0.0 (1)	n/a	0.00 (1)	11.22 (9)	3.52 (5)	32.3 (11)	n/a	6.54 (8)	34.0 (12)	5.78 (7)	3.52 (5)	4.94 (6)	1.84 (4)	1.42 (3)	21.64 (10)
Site C (rank/6)	0.0 (1)*	0.16 (2)	n/a	n/a	n/a	32.38 (4)	n/a	n/a	n/a	n/a	n/a	n/a	48.65 (6)	28.35 (3)	35.08 (5)	n/a
Site D (rank/6)	0.0 (1)*	0.25 (2)	n/a	n/a	n/a	17.03 (5)	n/a	n/a	n/a	n/a	n/a	n/a	34.73 (6)	7.46 (4)	3.18 (3)	n/a
Site E (rank/14)	n/a	16.8 (5)	9.13 (3)*	4.78 (2)	n/a	51.6 (11)	15.9 (4)	23.5 (7)*	2.26 (1)	16.86 (5)	18.79 (6)	34.81 (8)	87.7 (13)	43.37 (9)	48.8 (10)	62.75 (12)

LEGEND

*Baseline Finish
Sn/Pb = Electroplated and reflowed Tin/Lead
Sn/Pb NR = Electroplated Tin/Lead, non-reflowed
Sn/Pb HASL = Hot air solder leveled Tin/Lead
ELS Sn/Pb = Electroless Tin/Lead
IMZ EP Cu = Imidazole OSP over electroplated Copper
IMZ ES Cu = Imidazole OSP over electroless Copper

Thk OSP = Thick Organic Solderability Preservative

BTA = Benzotriazole

Pb-free HASL = Lead-free hot air solder leveled

IMM Sn = Immersion Tin

IMM Au-1 = Immersion Gold supplier 1

Imm Au-2 = Immersion Gold supplier 2
ELP Au = Electroplated Gold over Nickel
ELS Au = Electroless Gold over Nickel
ELP Pd = Electroplated Palladium over Nickel
ELS Pd = Electroless Palladium over Nickel

Table 2 - Baseline and Benchmark Surface Finish Defect Rate Summary

- "As Assembled" (i.e., no accelerated aging)
- After 2500 temperature cycles of 0 °C to 100 °C (3 cycles per hour)
- After 5000 temperature cycles of 0 °C to 100 °C (3 cycles per hour)

Automatic electrical monitoring for open solder interconnections during temperature cycling was not possible. Upon completion of temperature cycling, manual electrical continuity measurements were made on all of the surface mount and through hole component solder interconnections. Temperature cycling did not create open solder interconnections on any of the peripheral leaded surface mount packages. Opens were detected on most of the 256 I/O ceramic BGAs after 5000 temperature cycles. All of the 44 I/O leadless ceramic chip carriers (LCCC) had open solder interconnections after 2500 temperature cycles and the LCCCs fell off the STVs after 5000 cycles. These thermal-fatigue induced open solder interconnections were determined to be a function of the package type rather than the surface finish.

The results of the mechanical strength tests are presented in Table 3. The values listed are the average and standard deviation for each set of measurements. Approximately 100 leads from each PQFP, and 80 leads from each PLCC, were pull tested. The remainder of the leads were left intact for metallurgical cross sectioning and evaluations. Although the surface finish project started out with only 12 baseline/benchmark surface finishes, additional finishes were included for various reasons. Table 3 gives the pull strength results for 24 surface finishes. The surface finishes are separated into four categories; non-noble metallic finishes, OSPs, gold (Au) finishes, and palladium (Pd) finishes. The thickness of each metallic surface finish was measured using X-Ray Florescence (XRF) and confirmed during metallographic cross sectioning.

In cooperation with the NCMS Pb-Free project, mechanical pull test measurements also were made on surface mount solder interconnections formed using a Pb-free alloy. STVs with various Pb-free surface finishes were surface mount assembled with SnAgCu solder paste and wave soldered using SnAgCu solder. Although the evaluation of these STVs is still in progress, the preliminary results for a "total SnAgCu" (i.e., surface finish, surface mount solder paste, and PTH wave solder) assembly is given in Table 3.

The average pull strength for 0.4mm pitch PQFP leads was about 1 pound, while the average for the bigger 50 mil pitch PLCC leads was over 3 pounds. A fracture in the solder fillet near the peripheral lead was the typical mode of failure when the leads were pulled vertically. The solder fillet usually remained on the STV surface mount land. Although the craters formed when the leads separate from the solder fillets appear to indicate a lead/solder interface separation, examination of the leads and fillets show the separation to

be a cohesive failure in the bulk solder. This was the case for the majority of the pull tests. However, many of the solder fillets formed on electroless copper STV lands remained attached to the leads. The quantity of these solder/PWB surface finish failures is given in the "% Def." column in Table 3. It should be noted that these failures also occurred on electroless Pd plated electrolytic copper lands. The root cause of this failure mechanism is currently under evaluation. For the case of Pd, there are preliminary indications of a "seeding" problem (i.e., adhesion of Pd to Cu).

The following summarizes the results of the mechanical integrity/reliability evaluations:

- The mechanical strength of surface mount solder interconnections is proportional to the land/lead/fillet size.
- Embrittlement of surface mount solder interconnections was not observed with noble metal surface finish thickness of 10 to 37 microinches.
- The strength of SnAgCu solder interconnections is notably greater than SnPb interconnections.
- With the exception of electroless Cu and electroless Pd surface finishes, solder interconnections to peripheral leaded packages survived 5000 temperature cycles of 0 °C to 100 °C
- Solder interconnections to 44 I/O leadless components (LCCC) cracked within 2500 temperature cycles
- Solder interconnections to 256 I/O ceramic BGAs were in tact after 2500 temperature cycles but cracked after 5000 cycles.

PWB SURFACE FINISH WIRE BONDABILITY

The NCMS STV was designed to evaluate surface finish solderability/soldering performance for fine pitch surface mount. Provisions on this test vehicle were not provided for chip-on-board (COB); i.e., flip-chip or wire bond. To validate the capability of combining COB with surface mount technology (SMT), an evolutionary test vehicle (ETV) design was undertaken by the Product Team. Fabrication of these ETVs is currently in progress. The Surface Finishes Team was asked to recommend appropriate surface finishes for the ETV. To do this, the SF Team expanded their program to include evaluations of wire bondability of noble metal surface finishes.

Rather than design a new test vehicle, a decision was made to use one of the NCMS member company's existing wire bond test vehicles (WBTv). The WBTv is about 0.5 inches wide by 1.5 inches long and contains two die sites each with seventy six (76) 3.5 mil wide by 8.5 mil long wire bond

STV SURFACE FINISH	FINISH THK. (in)	256 I/O 0.4mm PITCH PQFP GULL WING LEADS						84 I/O 50 mil PITCH PLCC J-LEADS					
		"AS ASSEMBLED"			5000 CYCLES			"AS ASSEMBLED"			2500 CYCLES		
		(lbsms)	(% Def.)	(lbsms)	(% Def.)	(lbsms)	(% Def.)	(lbsms)	(% Def.)	(lbsms)	(% Def.)	(lbsms)	(% Def.)
SnPb (HASL)	350	0.88 (.10)		1.38 (.14)				3.64 (.29)		3.79 (.27)			
SnPb (Non-Reflowed)	602	1.13 (.17)		1.02 (.16)		0.87 (.20)		3.73 (.32)		3.42 (.34)		2.81 (.31)	
SnPb (Immersion)	485	1.09 (.10)		1.03 (.14)		1.19 (.11)		2.59 (.34)		2.61 (.29)		2.23 (.41)	
SnAgCu (HASL)	306	1.08 (.14)		0.97 (.17)				3.50 (.34)		2.71 (.41)			
Sn (Immersion)	32	1.28 (.17)		1.15 (.19)		1.33 (.21)		3.71 (.38)		2.95 (.40)		2.83 (.38)	
Bi (Immersion)	3	1.16 (.14)		1.00 (.23)		1.14 (.15)		3.23 (.33)		3.35 (.27)		2.85 (.39)	
OSP "B"		1.08 (.10)		1.25 (.07)				3.57 (.32)				3.63 (.30)	
OSP "E"		1.28 (.13)		1.16 (.12)		1.11 (.10)		3.19 (.38)		3.11 (.31)			
OSP "C" on eCu		1.14 (.15)		0.35 (.36)	84%	0.36 (.40)	96%	2.95 (.24)		1.69 (1.14)	100%	1.17 (1.12)	79%
OSP "B" on eCu		1.18 (.14)		0.34 (.45)	100%			2.94 (.38)		1.90 (1.08)			
AuNi (Electroplated) "A"	27 / 95	1.16 (.10)		1.14 (.13)		1.20 (.13)		2.28 (.35)		2.29 (.37)		2.59 (.37)	
AuNi (Electroless) "A"	24 / 115	1.10 (.17)		1.02 (.14)		1.09 (.12)		2.97 (.41)		3.40 (.47)		3.81 (.38)	
AuNi (Immersion) "A"	2 / 129	1.30 (.29)		1.25 (.15)		1.38 (.21)		3.85 (.48)		3.85 (.36)		3.98 (.38)	
AuNi (Immersion) "B"	6 / 203	1.27 (.17)		1.05 (.17)		1.21 (.16)		3.04 (.32)		2.85 (.32)		3.28 (.39)	
AuNi (Immersion) "B"	5 / 200	1.15 (.07)		1.12 (.10)				3.60 (.31)		3.63 (.34)			
AuNi (Immersion) "B"	15 / 150	0.87 (.09)		0.93 (.17)		0.97 (.10)		2.52 (.29)		2.67 (.32)	51%	2.70 (.40)	17%
AuNi (Immersion) "C"	6 / 150	1.12 (.10)		0.97 (.09)		1.21 (.19)		2.93 (.27)		2.65 (.25)		2.93 (.32)	
PdNi (Electroless) "D" on eCu	9 / 159	1.06 (.13)		0.94 (.38)		1.00 (.15)		3.18 (.25)		3.10 (.30)		3.07 (.31)	
PdNi (Electroless) "B"	17 / 142	1.05 (.10)		1.08 (.17)				3.74 (.29)		3.54 (.29)			
PdNi (Electroplated) "E"	19 / 120	1.08 (.16)		1.03 (.12)		0.91 (.15)		3.36 (.27)		3.55 (.37)		3.28 (.32)	
Pd (Electroless) "D" on eCu	37	1.02 (.14)		0.91 (.19)		0.97 (.23)		2.97 (.18)		3.17 (.29)	5%	2.98 (.38)	
Pd (Electroless) "B"	14	1.06 (.18)	5%	0.70 (.33)	74%			3.22 (.28)		0.00 (.00)	100%		
AuPdNi (Electroplated) "G"	9 / 19 / 149							3.01 (.31)		3.84 (.43)			
SnAgCu (HASL & PASTE)	306	1.00 (.12)		1.49 (.22)				4.01 (.42)		4.31 (.28)			

LEGEND

"A", "B", "C", "D", "E", "F", "G" = seven commercial vendors of PWB chemistries

B* = Plating done at research lab

B** = Plating done at commercial plating site

B*** = Plating done at second commercial plating site using electroless Ni formulated for application to Al

Table 3 - NCMS STV Surface Mount Device Lead Average Pull Strength Test Results

lands. It would have been desirable to have the WBTVs plated along with the STV. However, this was not possible. Panels of WBTVs were plated with noble metals using the plating equipment and parameters used for the STVs. The surface finishes used for the wire bondability evaluations are listed in Table 4. Comparison of the XRF measured thickness of the noble metal and underlying Ni plating on the WBTV in Table 4 with the thickness of the STVs in Table 3 show similar values.

Immersion Au thickness of 6 +/- 3 microinches over 50 to 250 microinches of electroless Ni is the generally accepted surface finish for Al wire wedge bonding. Thicker (20 to 50 microinches) electrolytic or electroless Au is usually specified for Au wire ball bonding. More recently, vendors have been touting the use of immersion Au for ball bonding and Pd as a universal surface finish (i.e., solderable as well as wire bondable with Al or Au wire). To evaluate these claims, ultrasonic aluminum (Al) wire wedge bonding as well as thermo-sonic gold (Au) wire ball bonding was performed on the surface finishes listed in Table 4. In both evaluations a wire diameter of 1.25 mils was used. The heated stage for the thermo-sonic Au wire bond was maintained at 150 °C. Integrity of the wire bonds was determined using wire pull and ball shear. The average of 200 wire bond strength measurements and standard deviation in grams for each of the surface finishes is given in Table 4. Rather than a mid-span wire pull, the pull force was exerted near (i.e., within 25% of the wire length) the wedge bond. This "aggressive" pull was felt to give a more reliable indication of the wire bond integrity.

Wire bond evaluations were performed at assembly sites "A" and "E". Although both sites experienced similar

observations and agree on qualitative results, a compilation of the quantitative results for site "E" was not available when this paper was prepared. The following summarizes the baseline wire bond observations and conclusions drawn from the site "A" results:

- Successful Al wire bonding to Pd surface finishes was not obtained. Although some Al wires stuck to the Pd finishes, there were many "no-sticks".
- Successful Au wire bonding to Pd surface finishes was not obtained. Although the average pull strength of Au wires to the 37 microinch thick electroless Pd and the electroplated PdNi alloy were above 8 grams, there were many "no-sticks".
- Good wire bond strengths were achieved using the electroplated Au/Pd/Ni surface finish. However, these WBTVs were inadvertently plated with 9.2 microinches of Au rather than the requested Au flash.
- The electroplated Au (37.8 microinches), electroless plated Au (31.2 microinches), as well as one of the immersion Au (7.3 microinches) surface finishes had more than adequate Au wire strength values.
- While the thinner immersion Au (2.2 microinches) had a lower average and higher standard deviation value than the thicker immersion Au (7.3 microinches), the results were more encouraging than anticipated.

WBTV SURFACE FINISH	SURFACE FINISH THICKNESS (uin)			"AS PLATED" BASELINE STRENGTH (gms)		
	Au	Pd	Ni	AGGRESSIVE PULL		BALL SHEAR
				Al WIRE	Au WIRE	Au WIRE
Au/Ni (Electroplated) "A"	37.8		205		15.34 (2.86)	63.1 (4.1)
Au/Ni (Electroless) "A"	31.2		132		15.25 (2.54)	64.6 (3.8)
Au/Ni (Immersion) "A"	2.2		149	11.23 (1.97)	9.6 (3.86)	
Au/Ni (Immersion) "B"	7.3		316	12.48 (1.57)	14.8 (2.73)	
Pd/Ni (Electroless) "D"		9.2	159	< 1 gm	< 1 gm	< 1 gm
PdNi (Electroplated) "E"		7.3	120	< 1 gm	8.80 (2.37)	
Pd (Electroless) "D"		37.1		< 1 gm	8.42 (4.20)	63.1 (7.7)
Au/Pd/Ni (Electroplated) "G"	9.2	18.9	149	11.07 (1.34)		65.1 (5.1)
Values in parentheses are standard deviation						

Table 4 - NCMS WBTV Baseline Wire Bond Average Strength Results

These results are baseline values in that the wire bonding was done on "as plated" surface finishes. Although the surface finishes were plated 4 to 8 weeks prior to wire bonding and some handling was incurred during XRF thickness measurements, the WBTV had not been subjected to a surface mount assembly soldering process. From a surface contamination standpoint, it would be desirable to wire bond before surface mount soldering. Since this isn't a practical assembly scheme, wire bonding will need to be the latter rather than former process. To evaluate the effect of this assembly scenario, wire bonding was performed after simulated surface mount assembly processes. Assembly sites "A" and "E" subjected WBTVs to their simulated surface mount assembly soldering. This included stencil printing solder paste (RMA paste for site "A" and WS paste for site "E") on surface mount features which were within .250 inches of the wire bond lands and processing through a surface mount reflow soldering furnace. Because of the use of WS solder paste, the site "E" WBTVs were processed through an aqueous cleaner before wire bonding. Wire bonding was performed on the processed WBTVs as well as WBTVs subjected to an additional cleaning process. The additional cleaning for site "A" was EC-7 semi-aqueous, and plasma clean for site "E". The simulated surface mount assembly "No-Clean" and EC-7 clean wire bonding results for site "A" are given in Table 5, along with the baseline results. The following summarizes the after simulated surface mount solder assembly wire bond observations and conclusions drawn from the site "A" results:

- Simulated surface mount assembly decreased the average wire bond strength and increased the standard deviation for the electroplated and electroless Au surface finishes. The semi-aqueous EC-7 cleaning process provided some improvement to the wire bond strength values.
- Simulated surface mount assembly processing was detrimental (>65% pull strength decrease) to the wire bondability of the 2.2 microinch thick immersion Au surface finish. Semi-aqueous cleaning did not improve wire bond strength values.
- Simulated surface mount assembly processing was detrimental (>35% pull strength decrease) to the wire bondability of the 7.3 microinch thick immersion Au surface finish. Semi-aqueous cleaning significantly improved the wire bond strength values.

INTERCONNECTION INTEGRITY AND WIRE BONDABILITY SUMMARY

The results of the PWB surface finishes solder interconnection integrity/reliability and wire bondability evaluations can be summarized as follows:

- The integrity of the peripheral leaded package soldered interconnections for all of the non-noble metal, OSP, and Au surface finishes tested, with the exception of those on electroless copper, were "sound" (i.e., met or exceeded expectations).
- All of the Au surface finishes were Al wire wedge bondable.
- Simulated surface mount assembly processing degraded the bondability of noble metal surface finishes, but did not make wire bonding impossible.
- Gold wire bonding to the thicker electroplated and electroless Au surface finishes resulted in greater pull strengths than the thinner immersion Au. However, the Au wire pull strength values for the immersion Au surface finish showed considerable promise.
- The mechanical integrity of solder interconnections and wire bondability of Pd surface finishes was not as good as for the Au surface finishes.

PWB SOLDERABILITY TEST METHODS

INTRODUCTION

Evaluations of ten different solderability test methods were performed over the course of the project. Several of these test methods were developed by the team. The evaluations were performed in two phases. The first phase involved a team effort to assess 7 different tests for the purpose of defining the most effective one for use in baselining current surface finishes and benchmarking new finishes. The most effective test could also be used by the member companies in their production lines to provide an indication of assembly yield. The second phase involved individual companies developing and evaluating 3 additional tests.

PHASE I TEST METHOD DESCRIPTIONS

A test board (Figure 3) called the "Metal Wettability Test Vehicle" (MWTV), was designed to assess the 7 solderability tests evaluated in Phase I. The MWTV is a 10" x 7.5", .062" thick, 4 layer epoxy-glass board. It contains 2,400 PTHs for wave solder testing, 5,200 SMT pads (2,600/side), and 6 coupons in the middle to evaluate the various solderability tests. Four different member companies evaluated five groups of MWTV's. Each tester received four MWTV's from each process submitted. Each tester received two groups of HASL, two groups of reflow solder plate, and one group of OSP coated copper MWTV's. All tests were validated against the results from the simulated assembly trials. These 5 tests are described as follows:

WBTV SURFACE FINISH	WIRE BOND WIRE	BEFORE ASSEMBLY "AS PLATED" BASELINE	AFTER SIMULATED SOLDER ASSEMBLY	
			NO CLEAN	AFTER EC-7 CLEAN
Au/Ni (Electroplated) "A" (37.8 uin Au)	Al			
	Au	15.34 (2.85)	11.48 (4.72)	17.10 (2.27)
Au/Ni (Electroless) "A" (31.2 uin Au)	Al			
	Au	15.25 (2.54)	11.50 (3.65)	12.75 (2.27)
Au/Ni (Immersion) "A" (2.2 uin Au)	Al	11.23 (1.97)	9.50 (2.00)	10.85 (2.20)
	Au	9.6 (3.86)	3.29 (1.56)	2.69 (1.70)
Au/Ni (Immersion) "B" (7.3 uin Au)	Al	12.48 (1.57)	10.10 (2.18)	10.42 (1.86)
	Au	10.59 (5.01)	6.93 (2.57)	12.23 (4.41)
Pd/Ni (Electroless) "D" (9.2 uin Pd)	Al	< 1 gm		
	Au	< 1 gm		
PdNi (Electroplated) "E" (7.3 uin Pd)	Al	< 1 gm		
	Au	8.80 (2.37)		
Pd (Electroless) "D" (37.1 uin Pd)	Al	< 1 gm		
	Au	8.42 (4.20)		
Au/Pd/Ni (Electroplated) "G" (9.2 uin Au / 18.9 uin Pd)	Al	11.07 (1.34)		
	Au			
Pull strength values in parentheses are standard deviation				

Table 5 - NCMS WBTV Aggressive Wire Bond Average Pull Strength Results

The Spread Test (Sessile Drop) method involved placing a 17 milligram, RMA flux coated, Sn 63 alloy solder pre-form, in the center of the circular test coupon (Figure 3). The coupon with pre-form was placed on a 490 °F solder bath until the flux melted (color change). Ten seconds after the flux melted, the specimen was removed and the maximum wetting diameter was measured.

The PTH Wetting Balance test consisted of measurements taken from each of the specially designed 3 X 5 PTH (Figure 3) coupons. The force at 8 seconds was taken from the 10 second test. Only one Tester supplied data for this test. A special fixture was used to hold the coupon at approximately a 30° angle. After coating the specimen with type R flux, the edge was immersed to a depth of only 0.1 millimeters in a solder bath maintained at a temperature of 473 °F, just enough to cover the edge of the pads on the solder side. The change in weight was recorded against time for ten seconds. The force was measured after an eight second immersion and recorded.

The SMT Wetting Balance test consisted of measurements made on the 0.250 inch wide metal covered specimens (Figure 3). The Force at 2 seconds was reported after normalization for the wetting perimeter. Two testers reported data on this test. As in the case of the PTH test the surface specimen was dipped in type R flux and blotted before the immersion into the solder. However, in this test, the specimen entered the 473 °F solder vertically to a depth of 3 millimeters. The force (corrected for buoyancy) at two seconds was obtained and divided by the wettable perimeter (in this case 0.5 inches) to obtain the Force @2 seconds.

Electron Dispersive X-ray (EDX) analysis consisted of the average of three measurements taken from the PTH knee area of one hole (Figure 3). The average weight of tin expressed as a percentage of the total tin/lead weight was recorded. All four testers reported data for this method. This was not a wetting test, but rather used the change in composition to estimate the solder coverage at the "weak knee".

The Solder Float test used a 40 PTH (Figure 3) coupon. The solder float test consisted of fluxing the coupon with

type R flux and floating it on a 473 °F solder bath for 5 seconds. Each coupon was evaluated for fraction of holes filled, and wetted more than 95% of the surface. Optionally, some testers weighed the specimens before testing, and after flux removal and air drying.

The Wave Solder test consisted of running the MWTV through a wave solder machine using type R flux. Results were recorded from the two diagonally opposite corners which contained a total of 2,400 holes per board. Three testers reported data from this test on the percentage of holes filled, and two also reported on Class 3 compliance. The equipment and set-up of this test varied with the tester, except for the flux which was type R in all cases.

The Simulated Assembly test was identical to the Wave Solder test except for the type of flux that was used. Testers 1 and 2 used "No Clean" Low Solids Flux (LSF). Testers 3 and 4 used Rosin-Mildly Activated type

RMA flux. As was the case for the Wave Solder method, this test's set-up varied between testers.

PHASE I RESULTS

The following table (Table 6) summarizes the results of the Phase I testing. It is based on the combined data from all of the testers that ran the tests. The table shows the flux type used, the number of testers (N), and the rank (Rnk) and variability (Rng) of each finish for each test method. The variability is expressed as the range (Rng) of data from each tester, expressed as a percentage of the average of all testers, for each test method. The very broad range recorded with the OSP/Cu was attributed to the use of non-activated, type R flux. With the exception of tester 1, the results of the OSP and Solder finishes were equivalent when RMA and LSF fluxes were used on the Simulated Assembly process. Some other conclusions from the testing that was done are as follows:

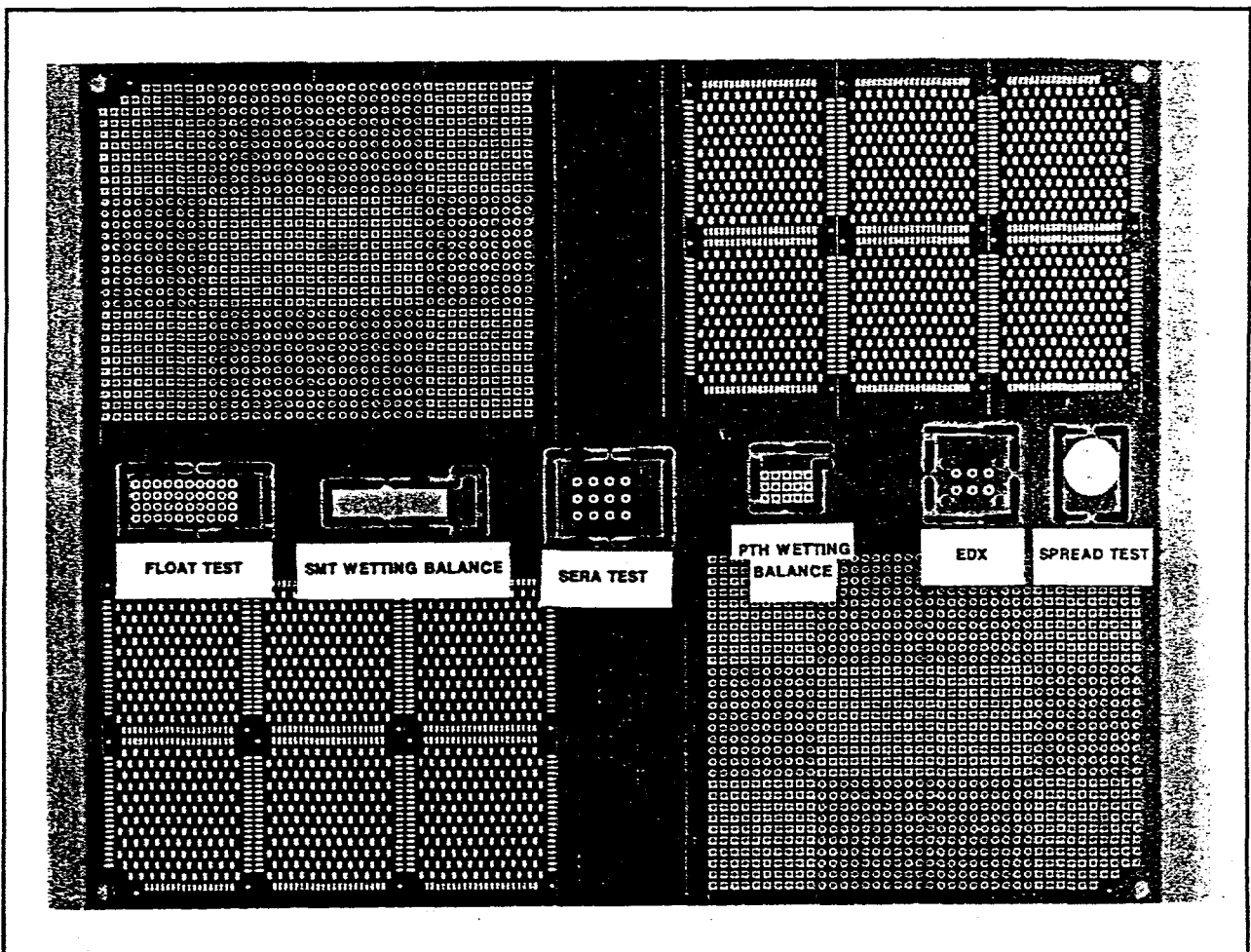


Figure 3 - Metal Wettability Test Vehicle (MWTV)

- The filled hole criteria generally gave the least tester to tester variation.
- Overall, the EDX test had the greatest degree of tester variability.
- The best correlations to simulated assembly results came from the Solder Float and Wave Solder tests.
- Use of the Spread test on solder coated samples may result in significant errors due to problems in identifying the limits of the spread.
- Neither of the wetting balance methods (PTH or Surface) provided any more information on solderability than the standard "Dip and Look" solderability tests.
- Only the Wave Solder and Solder Float methods were able to detect the relatively high defect rates experienced by all testers on the Simulated Assembly process of the RSP 1 parts. It was found that the problem with these parts was the thickness of the soldermask, and had nothing to do with the innate wettability of the metal of these parts. The ability of these tests to detect not only the wettability change in the OSP/Cu parts, but also the soldering problem in the RSP 1 parts indicate a more sensitive detection capability.

Based on the conclusions that were drawn from the test data, the team adapted the Solder Float and Simulated Assembly tests using the filled hole criteria as the two tests to use for evaluation and screening of alternative surface finishes.

PHASE II TEST METHOD DESCRIPTIONS

In this phase, three new tests were evaluated, Drag test, Capillary Flow test, and Sequential Electrochemical Reduction Analysis (SERA). The following is a brief description of the process and the results of each test.

Drag Test

The Drag Test evaluations were performed by AT&T. The purpose was to reduce the variability inherent in the solder float test and significantly increase the number of PTHs evaluated. The test was conducted using an RDT-1000 Solderability Tester from Robotic Process Systems. The RDT-1000 is an in-line machine with a self-contained conveyor system to transport a solderability coupon. The coupon is mounted on a trolley which follows a cam track that controls the orientation of the coupon to the fluxer and the solder pot, causing a simulated rotary motion as the coupon passes through these operations. As delivered, this equipment is considered a direct replacement for the apparatus specified in the "rotary dip" test method in ANSI-J/STD-003 "Solderability Testing of Printed Wiring Boards".

Three identical groups of 20 coupons (2600 holes per group) were tested. After soldering, the number of "unfilled" PTHs was recorded and compared to the other test groups. For comparison, the "drag soldering" and "solder dip" tests were conducted manually and evaluated for "unfilled" PTHs as well. The results are given in Table 7.

Flux Type	Test Method	Testers (N)	RSP2	HASL 1	HASL 2	RSP 1	OSP/Cu
			Rnk (Rng)	Rnk (Rng)	Rnk (Rng)	Rnk (Rng)	Rnk (Rng)
R	Sol Flt (fill)	2	1 (0.0%)	1 (0.0%)	1 (0.0%)	3 (1.3%)	8 (167.3%)
R	Sol Flt (wet)	2	2 (0.0%)	10 (34.4%)	4 (5.8%)	11 (160.0%)	10 (200.0%)
R	WB - PTH	1	3 (0.0%)	2 (0.0%)	2 (0.0%)	1 (0.0%)	1 (0.0%)
R	WB - SMT	2	4 (0.0%)	7 (9.3%)	9 (27.3%)	4 (11.6%)	3 (5.9%)
R	EDX	4	11 (22.6%)	9 (20.2%)	10 (33.0%)	8 (29.1%)	N/A
R	WS (fill)	3	5 (0.4%)	5 (6.4%)	6 (11.4%)	6 (18.9%)	4 (26.0%)
RMA/LSF	SIM (Cls 1)	4	6 (0.5%)	4 (1.2%)	5 (6.7%)	9 (56.0%)	9 (165.9%)
R	WS (wet)	2	7 (1.0%)	6 (7.6%)	8 (22.7%)	10 (78.3%)	7 (121.1%)
R	Spread	4	8 (3.3%)	11 (65.4%)	11 (33.9%)	7 (26.4%)	5 (28.8%)
RMA/LSF	SIM (Cls 3)	2	9 (4.8%)	3 (0.2%)	3 (5.6%)	5 (16.5%)	2 (0.9%)
R	Sol Flt (Wght)	2	10 (10.5%)	8 (16.3%)	7 (18.7%)	2 (0.3%)	6 (68.5%)

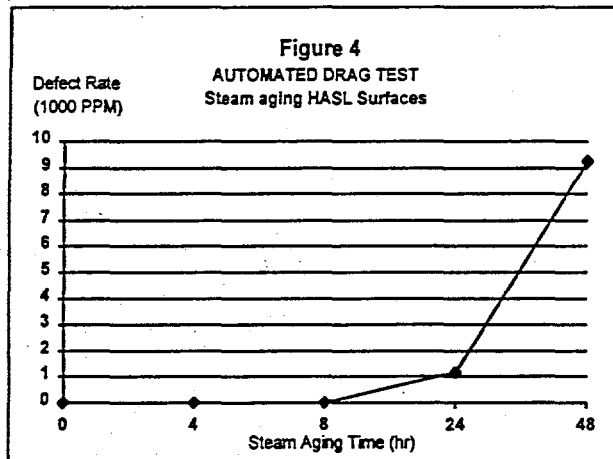
Table 6 - Phase I Solderability Test Variability By Process

TABLE 7 MEASUREMENT REPEATABILITY ANALYSIS			
Test Cell	Number of Defects *		
	Automated Drag Test	Manual Drag Test	Dip Test
1	0	9	0
2	0	100	0
3	0	0	86

* NUMBER OF OPPORTUNITIES: 2600

Steam aging

The drag soldering procedure was validated by subjecting four (4) groups of 20 HASL'ed coupons to different steam aging times. Three (3) steam aging times were used (4, 8, and 24 hours). The results of the earlier repeatability study are also plotted as a "baseline" (no steam aging = 0 hours). As can be seen from Figure 4, the defect rate (unfilled PTH's) steadily increased as the steam aging time was increased. It was also noted that no defects were reported for the HASL parts through eight hours of steam stressing.



OSP/Cu Coated Copper

The work also showed that the "drag soldering" method in conjunction with a mild stress (95% Relative Humidity and 95° F), can be used to determine if the specimens were

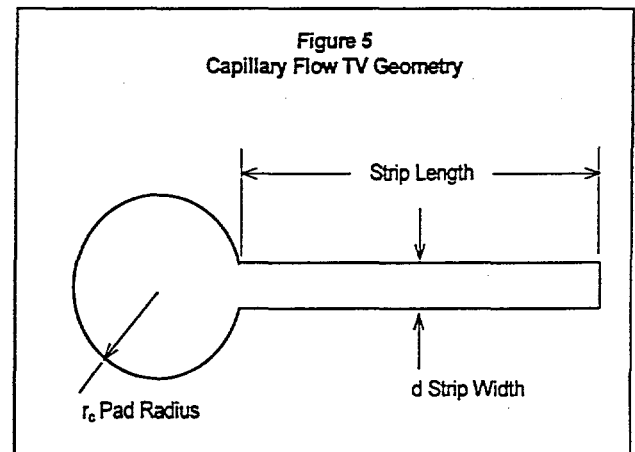
coated with an OSP/Cu coating, in this case Imidazole. It was shown that as little as 24 hours exposure to the above conditions could differentiate OSP/Cu coated and "uncoated" copper.

Currently AT&T is using this method to evaluate the solderability of PWBs being distributed to world wide assembly sites.

Capillary Flow Test

The "Capillary Flow" test method was evaluated at the Sandia National Laboratories in Albuquerque, NM. The evaluation was intended to 1) develop a method which would test the solder wetting capabilities of the surface mount attachment areas from the PWB as opposed to the PTHs used for the "solder float" and "drag soldering" methods and to 2) provide quantitative information about the wetting properties of the surface finish under evaluation.

A unique Capillary Flow Test Vehicle (CFTV) was developed as part of the evaluation. One element of the CFTV is shown in Figure 5. Four (4) sets of two (2) of these elements were placed on each CFTV as shown in Figure 6. The strip widths were either 0.026, 0.051, 0.077, or 0.102 cm for each set. Since the Pad Radius was constant at 0.102 cm for all elements, the resulting d/r_c ratios were 0.25, 0.50, 0.75, and 1.0 respectively.



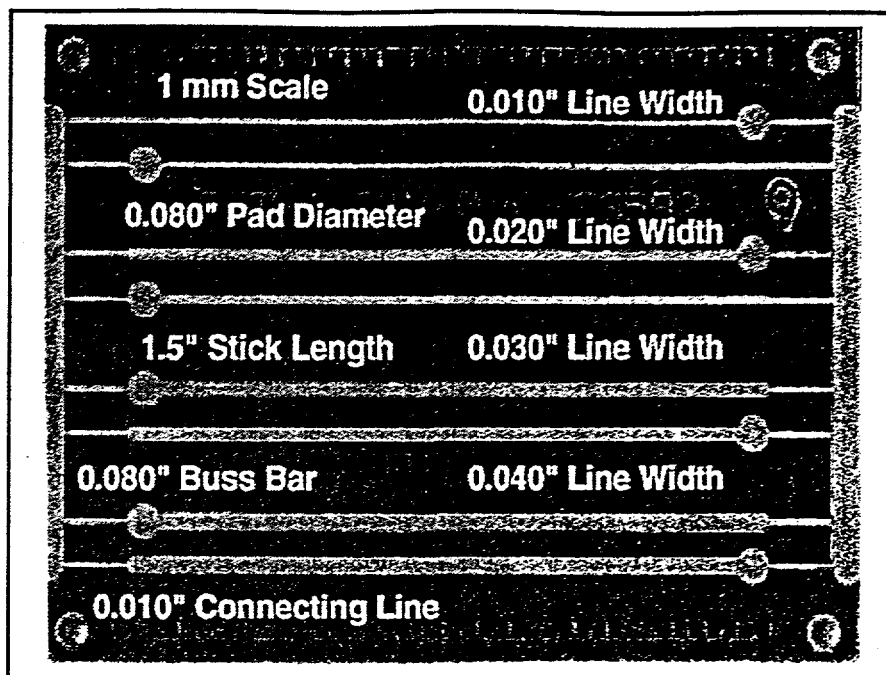


Figure 6 Capillary Flow Test Vehicle

The test consisted of coating the test board with a commercially available RMA flux. A solder pellet was dipped in the same RMA flux and placed approximately in the center of each of the CFTV pads. Each solder pellet weighed 10.1 ± 0.1 mg. The flux on the CFTV with solder pellets in place, was allowed to air dry for 15-30 minutes. Reflow was performed by floating each CFTV (one at a time) on a thermostatically controlled solder pot. The test temperature was 245 ± 2 °C. The CFTVs were floated 90-120 seconds, until the molten solder stopped moving up all strips. After removal from the solder pot the CFTVs were maintained horizontal until the solder solidified, thereby maintaining the final wetting results as they occurred during the test. Capillary flow data were analyzed from recorded video images. A camera was mounted perpendicular to the surface of the floated CFTV. The images of solder flow captured on video tape were digitally analyzed to derive the kinetic data. The flow "start time" was defined to be when the molten solder began to flow onto the strip. The distance was measured from the pad and strip intersection to the furthest distance traveled by the molten solder.

Only the 0.076 cm strips gave meaningful results. The narrower strips constricted the solder flow from the pad to the extent that only negligible wetting onto the strip was observed. For the 0.102 wide strip there was insufficient solder to consistently wet a significant length of the strips. In order for this procedure to work properly the d/r_s ratio must be near 0.75. Above this value there is insufficient solder volume available to allow a measurable flow onto the strip. Below it, the flow is so constricted that the resistance cannot be overcome by capillary force, no matter how much solder is available. The data points for the .076 cm strip

were plotted for Time/Wetting Length, and compared very well to a theoretical model.

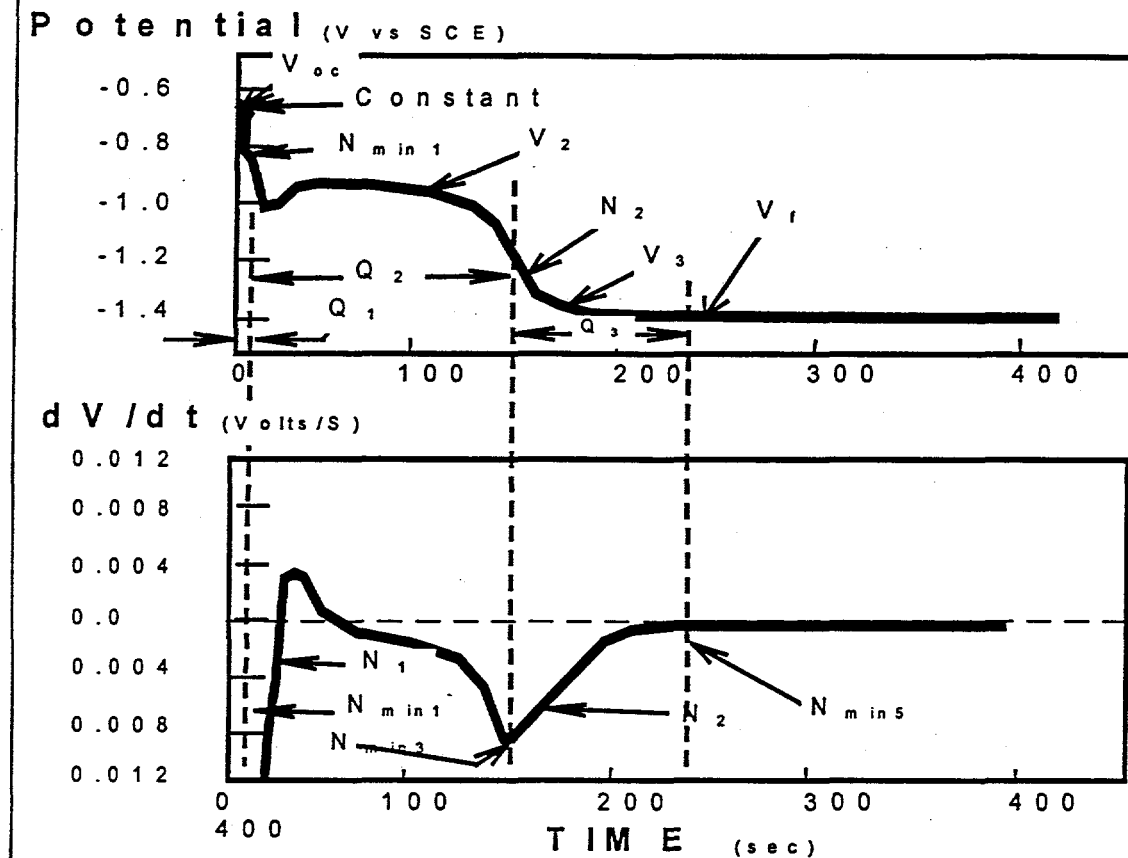
While the capillary flow method has been shown to measure capillary flow on PWB surfaces, it is not acceptable for fusible metal finishes like HASL. Since these finishes are all pre-wetted and will melt during the test, the flow properties are meaningless. On the other hand, it can be used to measure the effects of organic anti-tarnishing agents and all non-fusible metal finishes. This procedure is currently being used to investigate the effects of surface treatments and roughness on wetting rates. Sandia has applied for a patent for this procedure of measuring the solder flow properties on the surface of PWBs.

Sequential Electrochemical Reduction Analysis (SERA)

The evaluation of this technology was undertaken by Texas Instruments, Inc., Lewisville, TX, in cooperation with the Army Research Laboratories. The intent was to 1) verify prior experimental results and 2) measure the relationship between the SERA test results and solder joint rejects in a manufacturing environment.

SERA is an electrochemical procedure for measuring the thickness and type of oxides present on metallic surfaces. A small direct current ($20-40 \mu\text{A}/\text{cm}^2$) is passed through a PTH (or surface feature) using a boric acid buffer as the electrolyte. The PTH is maintained cathodic relative to an inert anode. As the current is maintained, the oxides are reduced sequentially at the cathode. As the oxides are reduced to metals, or to more electropositive oxidation states, the voltage will change. This change in voltage is

Figure 7
Typical SERA Curve



characteristic of one oxidation state, and the derivative of the voltage versus time curve (dV/dt) defines the critical inflection points. The change in voltage is plotted with time, and the results are interpreted by a computer program for voltages and times at these inflection points. A typical SERA curve is shown in Figure 7 with inflection points indicated.

The test is conducted by clamping a PWB in the test head. The PTH under test is isolated by O-rings and a buffer solution is drawn up through the hole. A small current ($30 \mu A/cm^2$) is applied and the cathode voltage versus a reference electrode is measured versus time. Three PTHs were evaluated from each board tested. In all, 479 Multi-Layer Boards, from four part numbers were evaluated.

Based on Rockwell's prior work ^[1], the V_2 parameter was used to evaluate solderability in the TI test. Any data more electronegative than -1.07 Vdc (relative to a Standard Calomel Electrode) were considered to indicate marginal solderability. If SERA was in-fact predicting soldering results, the test should show a direct correlation between V_2

and solder joint defects. In this experiment, 192 boards (40%) would have been rejected based on the V_2 values, resulting in the avoidance of 547 solder joint defects (approximately 80%). However, when the cost of scraping the boards was compared with the cost of reworking the solder joint, it was found that it was 10:1 in favor of rework. When the V_2 reject value was decreased to -1.17 Vdc the ratio would have been much worse (16:1). It was clear that using SERA to reject boards at assembly was not going to be cost effective.

It was discovered that most of the solder joint defects ($\approx 80\%$) were observed from only one of the four part numbers evaluated in the experiment. For this part number (891897-1), 88% of all of the SERA V_2 values were more negative than the -1.07 Vdc limit (see Table 8). For 893661-1 only 5% of the SERA results were below -1.07 Vdc.

Figure 8 shows graphically the impact of part number on defects from this study. All defects are normalized to maintain a standard ordinate axis scale. Note that not all

low V_2 values result in high soldering defect levels particularly for part number 891897-1 (Figure 7a) and not all high V_2 values resulted in the best soldering performance. Thus explaining the poor correlation between V_2 results and soldering defects.

Part Number	Average V_2 Vdc	Standard Deviation V_2 Vdc	Defects DPU
891897-1	-1.107	0.079	1.49
893661-1	-0.959	0.046	0.27

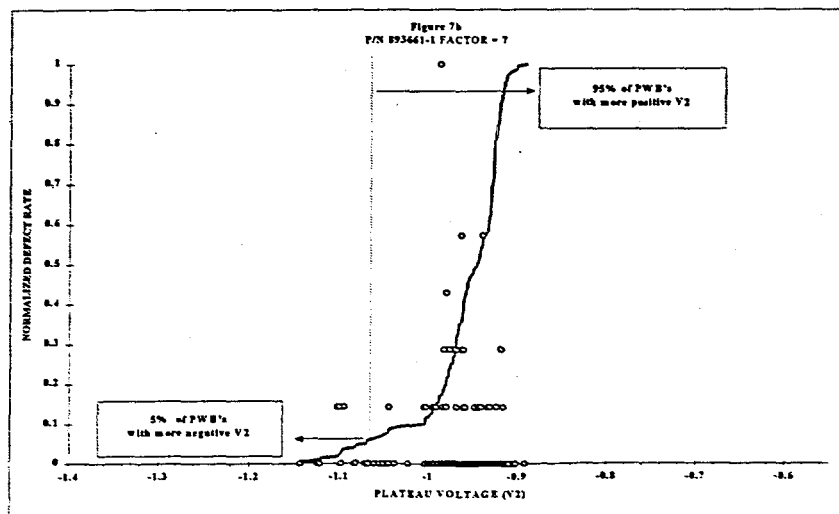
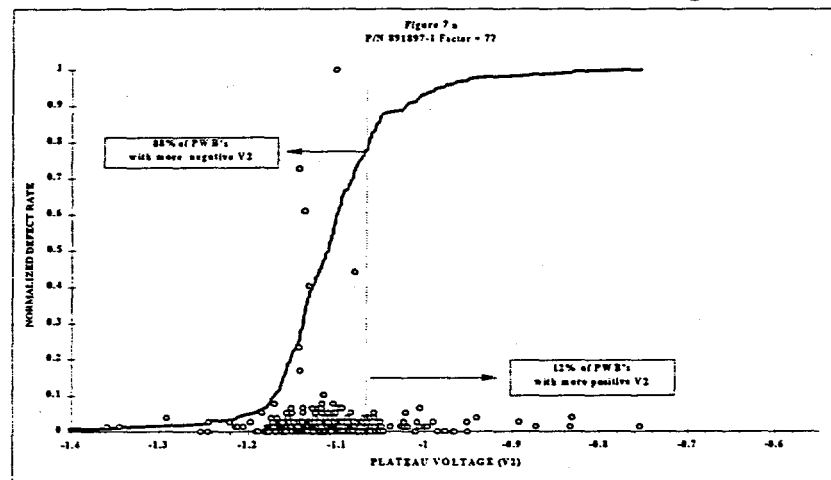
Table 8 - SERA V_2 vs. Defect Rate

The difference between these part numbers was found to be

a design which required a fabrication process change. The part with the worst soldering performance--and the most negative V_2 values--had a thermal plane bonded on the component side of the board before delivery to Lewisville.

The wave soldering experience from the Lewisville production indicates that parts with thermal planes consistently give more solder joint defects than similar boards but without thermal planes. It has been generally agreed that these degraded results were due to the changes in the board temperature during the wave soldering operation and was not associated with the fabrication process. This data clearly showed that it was likely that the fabrication process did have a significant (if unavoidable) degrading effect on soldering performance.

Figure 8
Normalized Defect Rate vs. Plateau Voltage



PHASE II RESULTS/CONCLUSIONS

- The TI fabrication shop in Austin, TX. is using SERA as a process troubleshooting tool and has verified the damage done to soldering performance as a result of the post reflow thermal plane bonding process first identified during the Lewisville study.
- The AT&T fabrication shop in Richmond, Va., is using SERA as a process control tool for the organic solderability preservative coating process. More data need to be collected and results published about the relationships between SERA results and soldering defects. SERA should be used in conjunction with other solderability tests, i.e. drag soldering, solder float, wave solder, etc., for lot acceptance until the solderability correlations are established with certainty.
- The drag soldering test is a superior wettability test. Whenever possible, this automated procedure should be used to take advantage of the consistency and larger sample size.
- Although the capillary flow test shows good potential for OSP coated copper and other non-fusible finishes, use of this test should be limited to engineering studies, until there is general agreement on coupon configuration, sample sizes, and acceptance criteria for production implementation.

V. THE DEVELOPMENT OF OSP COATINGS WITHIN AT&T

INTRODUCTION

Prior to the start of the NCMS PWB consortium, AT&T had developed and patented an Organic Solderability Preservative (OSP) referred to as imidazole. Unlike prior preservatives which simply coated the surface with an organic film, this coating chemically complexed with the copper features forming an oxidation barrier. A second important property was that the board could be electrically tested after the coating was applied, most other OSP coatings interfered with electrical testing.

At the time this coating was developed, the preferred solderability coating for PWBs was lead base solder. Generally, the solder coating was applied to the features of the PWB by either a plating-reflow or HASL process. In either case, a lead base process was used which produced lead waste that is both undesirable and expensive to treat. The imidazole process does not have this disadvantage. Also, the complexity and labor content of the imidazole process is appreciably less than HASL. As a result, the cost of the coating is substantially less than solder. For quite some time, cost was the principal advantage of an OSP coating over a solder coating.

Later, a second advantage began to emerge, the planarity of the coated surface. This advantage became important as the industry began to migrate to surface mounted components. Generally, fused solder forms a meniscus over the parent metal. As surface mounted features have become smaller, the planarity of the surface mount footprint has become a serious issue. It is generally accepted that twenty mil pitch features are unsuitable for fused solder coatings; in some instances, difficulties have been reported with twenty-five mil pitch features.

At the beginning of our consortium, fifty mil pitch features were the norm, but it was obvious that smaller surface mount features would soon be prevalent, and there was not a suitable surface finish. It was also the opinion of many, that OSP coatings were not robust enough for boards that required multiple soldering operations, which is the case for most surface mount boards. At the same time, the industry was beginning to migrate to no clean assembly processes using Low Solids Fluxes (LSF) and later Volatile Organic Component (VOC) free fluxes. Here again, there were serious concerns about the compatibility of OSP coatings and these newly emerging assembly processes. Consequently, one of the first activities identified for the Surface Finishes Team was to address these issues. Several laboratory studies carried out by Wenger^[2] suggested that most of these concerns could be resolved. Based on this foundation, a series of assembly studies were carried out to verify the laboratory results and to introduce OSP coatings for surface mount boards to the industry. The assembly studies that were conducted to investigate these issues are reported below.

INITIAL ASSEMBLY STUDIES

Based on Wenger's results, an initiative was put in place to evaluate the assembly performance of imidazole coated boards that required multiple soldering operations. The first trials were carried out at the AT&T assembly plant in Denver, Colorado. These results were documented in several papers presented at SMI^[3].

The first trials were carried out on a line which used a water soluble flux at wave solder. The early results were very encouraging, although the trial consisted of only twenty boards that were wave soldered immediately after reflow. The defect rates were essentially the same as observed on HASL boards. It was then decided to include some of the second order perturbations in our next set of evaluations. Boards were reflowed and then wave soldered after delays of two, four, and six days. The results were essentially the same as observed on the boards assembled immediately after reflow.

At this point, it was decided to convert several codes to the OSP coating and closely monitor the results. Table 9 compares the results for the first few weeks after the conversion to a similar time period prior to conversion when this code used a HASL coating. As seen, the results are indistinguishable. We also converted other codes which used bottom side surface mount discretes that are wave soldered. For chip resistors and capacitors, the defect rate was well below 100 ppm. However, the defect rate for SOTs was on the order of 500 ppm, which is not unusual for HASLed boards as well.

The successful introduction of imidazole coated boards to an assembly process using a water soluble flux (WSF) was the first milestone in the OSP initiative. The next objective was to evaluate the compatibility of the imidazole coating with a no clean assembly operation. These evaluations were first performed at the AT&T facility in Denver. At this time in Denver, the reflow process was operated in a standard atmosphere and followed by a wave solder process which applied the no clean flux with a wave fluxer. Here again, the results were found to be indistinguishable to those using HASLed boards. These results were reported at SMI^[4].

Based on these successes, we decided to explore the use of this OSP coating on less aggressive assembly processes. In particular, no clean processes which apply only a limited amount of flux at wave solder. Within AT&T, no clean processes that spray a metered amount of flux onto the board are very popular. This is particularly true with switching and transmission equipment, where ionic contamination issues are a major concern. These processes are however, carried out in nitrogen atmospheres. The AT&T facility at Oklahoma City was selected as the evaluation site.

Once again, the initial trials involved only a few boards, in this case twenty. Wave solder was carried out immediately after reflow. We found the performance of these boards to be at par with HASL boards. The next evaluation involved one hundred boards that were held for seven days between reflow and wave solder. Here again, we found that delays of one week do not result in any noticeable change in assembly performance. We then converted several large running codes to imidazole and monitored the results. The change was transparent. Presently, 50% of the boards assembled at Oklahoma City are coated with imidazole. Additional codes are presently being converted. These results were also reported at SMI^[4].

OEM ASSEMBLY EXPERIENCES

OSP coated boards have been used by a large number of AT&T OEM customers. One particular area of application has been PCMCIA cards^[5]. These cards

normally use very fine pitch components and require at least two and often three soldering operations. Customers have reported their experiences in several papers. Ochoa^[6] found a substantial first pass yield improvement by migrating from a HASL coating to imidazole. This of course is the result of a more planar surface. Tesch^[7] compared the imidazole and other OSP coatings to immersion gold and HASL. Once again, the best assembly yields were obtained by using an OSP coating.

In still another case, an OEM customer migrated from a LSF to a VOC free flux. The defect rate at wave solder on imidazole coated boards was 50 PPM. By all appearances, OSP coatings are compatible with most well managed assembly operations.

SUMMARY

OSP coatings are compatible with a wide variety of assembly processes. They are advantageous from several viewpoints. In most cases, they are cost effective. Also, as the industry migrates to finer pitch components, OSP coatings will become even more important because of their excellent planarity. As the regulatory pressures for lead elimination are increased, the circuit board fabricator will also benefit from OSP coatings; not to mention the simplicity of the OSP coating process as compared to HASL.

REFERENCES

- Desantis, C.V., Kokas, J.W., Fey, E., Parker, J.L., Wenger, G.W., Reed, J.R. "NCMS PWB Interconnect Project Alternative Surface Finish Evaluation" Technical paper presented at IPC Spring Meeting, May 1995
- Reed, J.R., "Solderability Test Method Evaluations - Phase I" Technical paper presented at IPC Fall Meeting, October 1992
- Reed, J.R., "Phase II Solderability Test Methods a NCMS Surface Finishes Team Report" Technical paper presented at Surface Mount International Conference, August 1995
1. Tench, D.M., Anderson, D.P., and Kim, P. "Solderability Assessment Via Sequential Electrochemical Reduction Analysis", *Journal of Applied Electrochemistry*, Vol. 24, p. 18, (1994)
 2. Wenger, G. et al "Application Model for Organic Solderability Preservation" IPC EXPO, April 1995
 3. Parker, J.L., Horton, J.S. "Assembly Performance of Printed Wiring Boards Coated with an Organic Solderability Preservative" SMI, August 1992

CCC4 SOLDER YIELDS FOR HASL PWBS				
Week of	Number Of CCC4 Built	Total MDA Test Yield (%)	Total # of Solder Defects	Solder Defect Rate (PPM)
2/3	255	96.9	0	0
2/10	500	96.8	9	11.2
2/17	477	96.2	13	17
2/24	210	96.7	0	0
3/2	237	95.8	2	5.2
3/9	212	87.3	0	0
3/16	270	94.8	0	0
3/23	216	97.7	1	2.9
3/30	258	95.7	0	0
4/6	269	91.8	0	0
4/13	90	97.8	0	0
4/20	415	94.5	4	6
4/27	239	95.4	1	2.6
Totals	3648	avg = 95.2	29	5

CCC4 SOLDER YIELDS FOR COPPER IMIDAZOLE PWBS				
Week of	Number Of CCC4 Built	Total MDA Test Yield (%)	Total # of Solder Defects	Solder Defect Rate (PPM)
8/3	119	100	0	0
8/10	291	90	1	2.1
8/17	145	97.2	4	17.2
8/24	238	97.9	1	2.6
8/31	150	98	1	4.2
9/7	120	96.7	1	5.2
9/14	259	98.8	0	0
9/21	277	96.8	2	4.5
9/28	347	98.3	5	9
10/5	384	98.2	2	3.3
10/12	400	96.8	1	1.6
10/19	559	96.2	14	15.6
10/26	338	97.9	2	3.7
Totals	3627	avg = 97.1	34	5.3

Table 9 - Comparison of Copper Imidazole vs. HASL Solder Yields

4. Parker, J.L. et al, "Performance of Printed Wiring Boards Coated with Imidazole and Assembled in No Clean Processes" SMI, August 1993
5. Parker, J.L. et al "Solderability Preservatives for PCMCIA Cards" NEPCON, February 1995
6. Ochoa, E. et al "Assembly of OSP Coated PC Cards Using a Tailored Process and Solder Paste" SMI, August 1995
7. Tesch, B., Lane D. "PCMCIA: The Realities of High Volume Manufacturing" NEPCON, February 1995

APPENDIX 1 - SF TEAM TECHNICAL PAPERS

"A Model of the Solder Flux Reaction; Reactions at the Metal/Metal Oxide/Electrolyte Solution Interface", M. Nasta, and H. C. Peebles, Proceedings of the International Conference on Solder Fluxes and Pastes, June 1-3, 1994, Atlanta GA.

"Effects of Surface Oxidation on the Wetting of Tin on Copper", H. C. Peebles, D. E. Peebles, F. G. Yost, and J. A. Ohlhausen, presented at the 40th National Vacuum Symposium and Topical Conference of the American Vacuum Society (Orlando, FL, Nov. 15-19, 1993).

"Extensive Wetting due to Roughness", F. G. Yost, J. R. Michael, and E. T. Eisenmann, submitted for publication in Acta Metall. et Mater; presented at the Spring meeting of The Metals Society, 1994; invited presentation at Rockwell International Science Center.

"Solderability Test Method Evaluations - Phase I", J. R. Reed, Fall IPC Meeting, October 1992

"Soldering Evaluations of Organic Solderability Preservatives", G. Wenger, D. Machusak, NEPCON West, February 1993

"Performance of Printed Wiring Boards Coated with Imidazole and Assembled in No-Clean Processes", J.L. Parker, Surface Mount International (SMI), August 1993

"Solderable Finishes Baseline", C. DeSantis, J. Kokas, J. Reed, G. Wenger, IPC Fall Meeting Oct. 1993

"The Effect Of Organic Inhibitors On The Aging And Solderability Of Copper", N. R. Sorensen, F. M. Hosking, TMS Spring Meeting Feb 28-March 3, 1994.

"Capillary Flow on Narrow Strips and V-Shaped Grooves", F. Yost, E. Holm, IPC Fall Meeting 1995 and Journal of Electronic Packaging, Spring 1995

"Solderability Enhancement of Copper Through Chemical Etching", J. Stevenson, R. Sorensen, 6th Annual Joint Meeting of the New Mexico Sections of the American Ceramic Society & Materials Research Society, October 1994

"SERA Application on Process Characterization and Troubleshooting for Printed Circuit Board Fabrication", J. Reed, J. Cheng, IPC Spring Meeting 1995

"NCMS PWB Interconnect Project Alternative Surface Finish Evaluation", C. DeSantis IPC Spring Meeting 1995

"Solderability Preservation Through the Use of Organic Inhibitors", R. Sorensen, Interpak '95, March 1995

"Assessing Capillary Flow on Printed Wiring Board Surfaces", F.M. Hosking, F.G. Yost, C.L. Hernandez, S.J. Sackinger, Interpak '95, March 1995

"Dynamic Studies of the Spreading of Tin on Copper as a Function of Oxide Coverage", D. Peebles, H. Peebles, J. Ohlhausen, Gordon Research Conference, Ventura CA, January 1995

"Dynamic Measurements of the Spreading of Liquid Metals in Controlled Atmospheres With In Situ Surface Preparation and Analysis", D. Peebles, H. Peebles, J. Ohlhausen, Publication - Review of Scientific Instruments, November 1994

"SERA Unit Characterization and Capability Studies", J. Cheng, J.Reed, San Antonio Chinese Professionals Association, January 1995

"Solderability Preservatives for PCMCIA Cards", J.L. Parker, G.M. Wenger, D.A. Machusak, NEPCON West, February 1995

"Dynamic Studies of the Spreading of Tin and Sn/Pb 60/40 on Sputter Cleaned Copper and Copper-Tin Intermetallic Alloys", J. Ohlhausen, D. Peebles, H. Peebles, 31st Annual Symposium of the New Mexico Chapter of the American Vacuum Society, April 1995
Solderability Enhancement of Copper Through Chemical Etching" J. Stevenson, M. Hosking, IPC Spring Meeting, May 1995

"Double Reflow: The Stress Fracture Reliability Problem of the 90's", G. Wenger, D. Machusak, Surface Mount International (SMI), August 1995

"Effects of Prestressing and Flux on the Flow of Solder on PWB Copper Surfaces", C. Hernandez, M. Hosking, NEPCON East, June 1995

"Phase II Solderability Test Methods - A NCMS Surface Finishes Team Report" J. Reed, SMI, Aug. 1995

"Characterization of Solder Flow on PWB Surfaces", M. Hosking, SMI, August 1995

"Shelf Life and Durability Testing of OSP Coated PCB's", J.L. Parker, SMI, August 1995

"Energetics and Kinetics of Solder Droplet Flow", F. Yost, H. Peebles, J. Ohlhausen, D. Peebles, Advanced Materials and Technology for the 21st Century Conference, December 1995

"Relationship Between Spreading, Intermetallic Alloy Formation and Solid Solubility for Tin", D. Peebles, J. Ohlhausen, H. Peebles, Advanced Materials & Technology for the 21st Century, Dec. 1995

"The Kinetics of Solder Spreading on Tailored Copper Surfaces", D. Peebles, H. Peebles, J. Ohlhausen, F. Yost, Advanced Materials and Technology for the 21st Century, December 1995

"Inspection of Chemically Roughened Copper Using Optical Interferometry and Electron Microscopy: Establishing a Correlation Between Surface Morphology and Solderability", J. Stevenson, M. Hosking, T. Guilinger, F. Yost, R. Sorensen, 28th Annual International Metallographic Society Convention, July 1995

"Capillary Solder Flow on Chemically Roughened PWB Surfaces", M. Hosking, J. Stevenson, IPC Expo, March 1996

"PWB Solder Wettability After Simulated Storage", C. Hernandez, M. Hosking, 46th Electronic Components & Technology Conference, May 1996

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