

Integrating Amplifiers for PHENIX Lead-Glass and Lead-Scintillator Calorimeters*

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Abstract

Two types of integrating amplifier systems have been developed for use with lead-glass and lead-scintillator calorimeters with photomultiplier tube readout. Requirements for the amplifier system include termination of the line from the photomultiplier, compact size and low power dissipation to allow multiple channels per chip, dual range outputs producing 10-bit accuracy over a 14-bit dynamic range, rms noise levels of one LSB or less, and compatibility with timing filter amplifiers, tower sum circuits for triggering and calibration circuits to be built on the same integrated circuit (IC). Advantages and disadvantages of an active integrator system are compared and contrasted to those of a passive integrator-based system. In addition, details of the designs and results from prototype devices including an 8-channel active integrator IC fabricated in 1.2 μm Orbit CMOS are presented.*

I. INTRODUCTION

Two large electromagnetic calorimeter detectors are planned for PHENIX. The lead-glass (PbGl) electromagnetic calorimeter (EM Cal) will contain 10,000 channels read out with FEU-84 photomultipliers while the lead-scintillator (PbSc) will contain about 15,000 channels and be read out with FEU-115M photomultipliers (PMTs). The electronics requirements for the two detectors are very similar, but not identical. Energy measurements from these detectors will be made by integrating the signal from the photomultipliers (approximately 500 picocoulombs maximum for PbSc and approximately the same or slightly more for PbGl), sampling the integrator output at the beam clock frequency using an analog memory and double correlated sampling of the appropriate samples following digitization.

The lead glass blocks, or "towers," photomultipliers and PMT bases planned to be used in PHENIX are presently in use in CERN experiment WA98 [1,2]. The FEU-84 photomultipliers are not particularly fast, and when coupled with the lead glass produce the pulse shown in Fig. 1 in response to incident particles. The output current pulse is

actually negative, and there is a low amplitude tail that extends out to nearly 300 ns.

The lead scintillator calorimeter is constructed from alternating layers of lead and scintillator tiles with interspersed wavelength shifting fibers. The light produced in the scintillator is routed to the FEU-115M photomultipliers via fiber optics. A typical output pulser is shown in Fig. 1. It is important to note that the lead scintillator output has a considerably faster risetime than does the lead glass. This means for equal output charge, the pulse delivered by the PMT coupled to the lead scintillator has approximately twice the peak current of the lead glass PMT. For an output of 500 pC, that current is 50 mA.

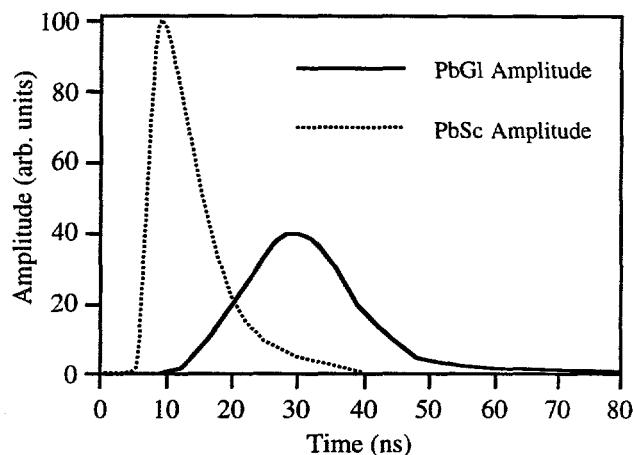


Fig. 1. PbGl and PbSc PMT output pulse shapes.

A number of requirements and constraints must be met in order to make the integrating amplifiers practical for these applications. To meet the physics goals of the calorimeters, a deadtimeless, 10-bit accurate energy measurement system with a dynamic range of 14-bits is needed. Due to the expected approximately 12-bit maximum accuracy of analog memories and ADCs under development for use in PHENIX, it appears that a multi-gain range system will be needed for the charge integrating amplifiers. As more ranges imply more hardware and calibration constants, a dual range system of 10+4 bits (two 10-bit ADCs preceded by signal processing gains separated by a factor of $2^4 = 16$) is the preferred arrangement to achieve 14 bits of dynamic range. This dual range system has a desired noise floor of less than 1 part in

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16000 or 0.5 MeV out of 8 GeV maximum for the lead scintillator detector. To allow for small variations in signal ranges, the system might be implemented as a 11+3, 11+4 or 12+3 bits.

The integrating amplifier outputs will be sampled at the bunch crossing frequency (about 8.9 MHz), and stored in an analog memory for digitization upon receipt of a level-1 trigger. To keep pile-up effects to a minimum, the amplifier must rise and settle on the order of 200 ns, and the samples to be correlated will be only a few bunch crossing times apart. Thus closed-loop amplifier bandwidths on the order of 5-10 MHz are needed.

To reduce the cost of the overall system, integrated circuits with multiple channels per chip and minimal external components should be used. Given multiple channels per chip, it is necessary that the per channel power dissipation be modest to preclude special packaging or heat sinking, and that the area occupied by each channel be limited to allow a reasonable sized die. Furthermore, the integrating amplifiers need to be compatible with other needed, on-chip circuits, including timing circuits (timing filter amplifier plus constant fraction discriminator or leading edge discriminator), calibration circuits, and tower analog sum circuits for trigger generation. Formation of analog sums of 4 and 16 channels also makes multiple channels per IC extremely desirable to reduce wiring between ICs. The variety of analog and digital circuits required to implement these functions implies that a CMOS implementation would be most suitable. Multiple channels per chip, and in the case of the lead glass, pre-existing PMT bases, mean that the amplifiers will be located apart from the PMTs, and therefore the amplifier input impedance must properly terminate a cable.

The zero deadtime requirement lead toward architectures different from the classic charge integrating ADC that is widely used for stop and read out applications [3]. A pipelined approach to photomultiplier readout including digitization has been implemented, but requires one IC per photomultiplier [4]. Both of these approaches also require bipolar transistors for handling the large peak output currents (>50 mA) of the PMT.

II. INTEGRATING AMPLIFIER ARCHITECTURES

Two approaches to the design have been investigated. The first (Fig. 2) uses an active integrator plus two voltage gain stages, while the second (Fig. 3) uses a passive integrator plus two voltage gain stages. The advantages of the active integrator are that the same input pin can be used for the timing filter amplifier and that the input impedance is very nearly 50 ohms for all frequencies. The main disadvantages of the active integrator is the loss of much of the signal due to current splitting between the integrator and the terminating resistor. This loss is necessary due to the impracticality of fabricating multiple large (>200 pF) capacitors on a reasonable sized IC die and, similarly, driving substantial currents (50 mA) with low-power amplifiers. Another

drawback to this implementation is the large gain at low-frequencies for the integrating amplifier equivalent input noise voltage. This makes it difficult to meet the noise specifications while keeping the integrating amplifier size and power dissipation to a minimum.

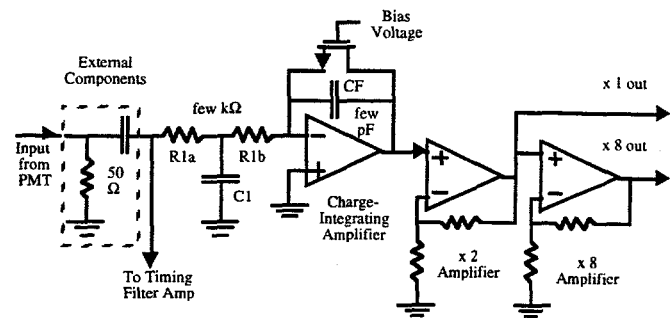


Fig. 2. Active integrator amplifier system.

The passive integrator has the advantage of locating the large capacitor and large PMT current off-chip with no loss of signal, but the termination is not suitable for long cables (greater than a few meters). Another advantage is the gain and decay time may easily be adjusted by changing external passive components. Also, since the integration is performed outside the IC, an additional input pin is required per channel if the performance of the timing channel is not to be degraded. The main advantage of the passive integrator may be that it can achieve much lower noise with similar amplifiers. This issue is considered in Section V.

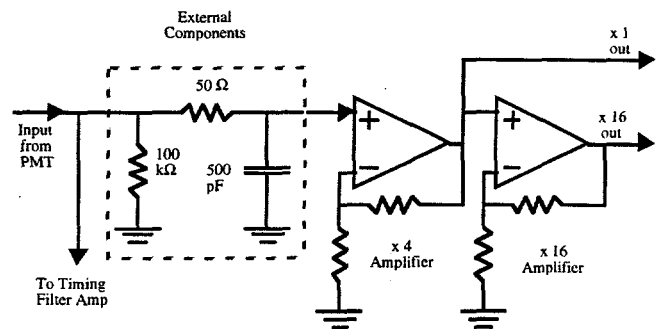


Fig. 3. Passive integrator amplifier system.

III. ACTIVE INTEGRATOR CIRCUITS

An implementation of the active integrator with features much like those needed for PHENIX electromagnetic calorimetry was developed for and used in WA98 [1]. This IC achieved better than 3 channels rms noise in a 10+3 bit lead glass calorimeter and satisfies most other functional PHENIX requirements. To support beam tests for prototype arrays of the lead scintillator modules, the design of the WA98 integrator IC was modified to provide improved noise performance and higher charge gain, while retaining compatibility with the WA98 144-channel circuit board. A schematic of the integrating amplifier is shown in Fig. 4. The

integrator actually collects only a small fraction of the charge delivered by the PMT, with most being shunted to ground by the 50- Ω termination resistor. The R1a, R1b and Ccomp network performs some preintegration of the signal and provide feedback compensation for the op amp. The feedback FET is biased to give a nominal 2 μ s decay time. A reference voltage of 1.25 V was originally chosen to prevent even the maximum input for the WA98 lead glass PMT (30 mA into 50- Ω resistor) from activating the clamping diodes on the integrator IC input, and this was retained for the lead scintillator tests. The 1.25V reference also allows the gain stages to easily have a 3-V dynamic range using a single 5-V supply.

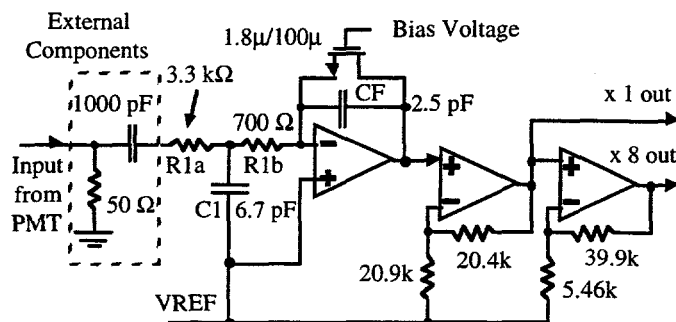


Fig. 4. Integrating amplifier for PbSc prototype.

The operational amplifier used in the integrator (Fig. 5) is an ordinary two-stage configuration. PMOS devices are used in the differential pair to allow biasing the input near the negative supply voltage (ground.) The PMOS (M7) common-source output stage with NMOS current sink (M6) provides the large positive slew rate (>100 V/ μ s) needed to maintain integrator linearity. The nominal bias current is 160 μ A, which results in a power dissipation of 6 mW for the amplifier. Only one amplifier in the IC has the complete bias network, and the others are mirrored from that master circuit. The op amp occupies an area of 143 μ m by 192 μ m. It and the other op amps used here are arranged with power busses running horizontally for ease of series connections.

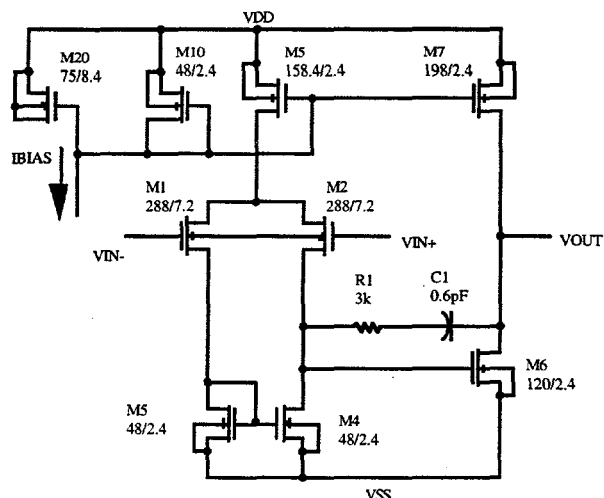


Fig. 5. Operational amplifier for PbSc prototype integrator.

Similar two-stage operational amplifiers are used for the x2 and x8 amplifier sections. The slew rate requirements are somewhat less as what is actually needed is for the amplifier to slew at least 3 V in 100 ns. As these amplifier outputs are outputs from the IC, the output stages were biased with approximately 1.5 mA to provide reasonable drive capability for up to a 20 pF load. The total supply current needed for the three amplifiers was measured to be 4.75 mA which results in a power dissipation of 24 mW per channel.

A calibration circuit is an essential part of the integrator IC. It allows calibration of the relative gains of the two outputs, checking to verify proper operation of the amplifiers and portions of the circuits following, and a means to monitor the gain of each channel in any pattern desired. The calibration circuit consists of a 6-bit voltage output DAC shared by all channels plus individual capacitors that may be connected via CMOS switches to either the DAC or to the inverting input of the integrator op amp. As the size of the calibration capacitor is not known accurately, this provides only a relative calibration, but one advantage of this method is that the control signal simply must be a logic pulse of sufficient duration to allow the integrator to fully drain the charge from the calibration capacitor.

As implemented in 1.2 μ m Orbit CMOS, one channel of on-chip calibration circuit, integrator and two voltage amplifiers occupied an area 180 μ m by 1200 μ m.

IV. ACTIVE INTEGRATOR RESULTS

The output of the PbSc prototype integrator IC was measured using a 10 ns input pulse which was approximately triangular due to the 6 ns risetime of the generator. A fit of this data (Fig. 6) reveals that the x1 charge gain was 4.76 mV/pC. The linear dynamic range exceeded 550 pC.

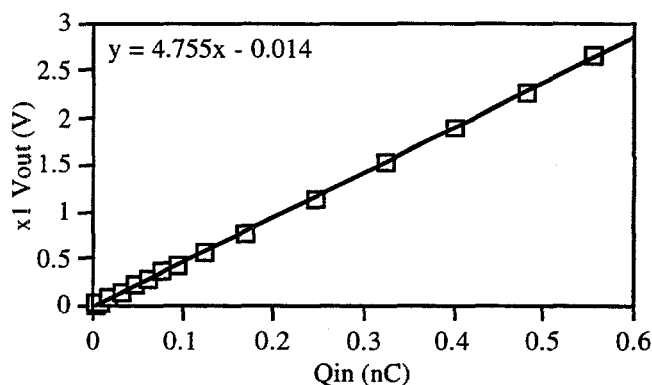


Fig. 6. PbSc prototype x1 output as a function of Q_{in}.

Using the linear fit obtained in Fig. 6, the integral non-linearity (INL) of the x1 output for the PbSc prototype was calculated on the basis of a 3 V full scale output. Fig. 7 shows

that the INL for the charge gain is less than $\pm 0.8\%$ over a 10 mV to 2.7 V range.

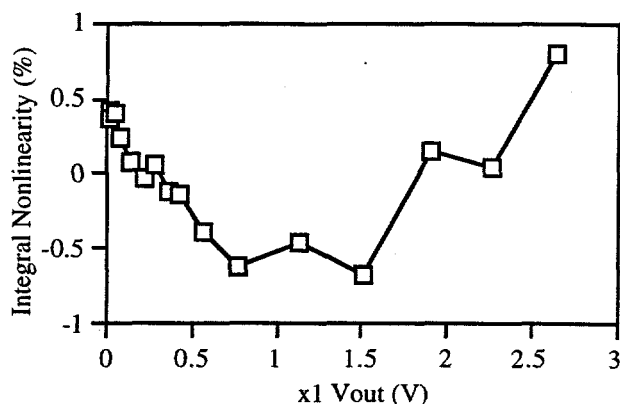


Fig. 7. INL of PbSc integrator x1 output.

Fig. 8 shows the x8 output of the WA98 integrator IC plotted against the x1 output. The gain ratio obtained from the best-fit line is 8.36, which is very close to the value of 8.31 determined by the feedback resistor network used in the x8 amplifier. For the x8 output of the PbSc integrator IC, the best-fit line slope was 8.28.

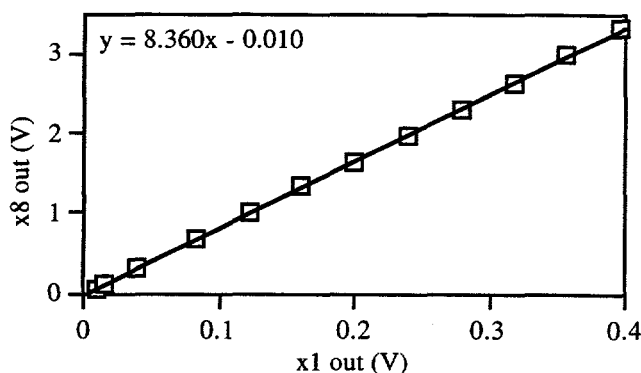


Fig. 8. PbGl integrator IC x8 and x1 relative gain.

The charge gain for the WA98 and the prototype PbSc integrator were measured as a function of pulse width using a pulser with a nominal risetime of 6 ns. The 20 ns setting corresponds to a FWHM of 18 ns and was considered a reasonable approximation to the output of the FEU-84 photomultipliers used for PbGl. As shown in Fig. 9, the charge gain for both changed only slightly with the pulse width. For a 10 ns input, the gain dropped 10% compared to the 20 ns case, while for a 40 ns input, the gain increased by about 6%. From a practical standpoint, this means that modest variations in photomultiplier response time among a single type would produce gain variations small enough to not affect dynamic range.

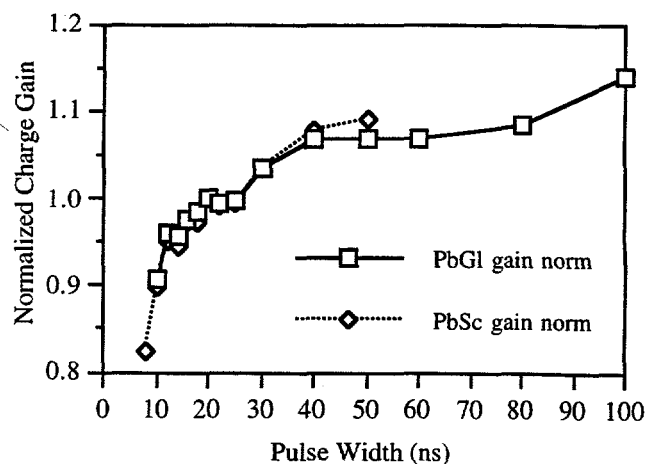


Fig. 9. Normalized charge gain for PbGl and PbSc active integrators as a function of pulse width.

A group of ten WA98 integrator ICs from one wafer was tested extensively. The x1 output was measured for each channel of each IC using a fixed input amplitude (which was selected to give approximately 1 V out.) The voltages were measured using a Tektronix TDS 420 oscilloscope set to average 1000 waveforms. The limit of resolution is ± 2 mV using this arrangement. The output voltages are plotted in Fig. 10. Since the same input was used in each case, the voltages are proportional to the charge gain.

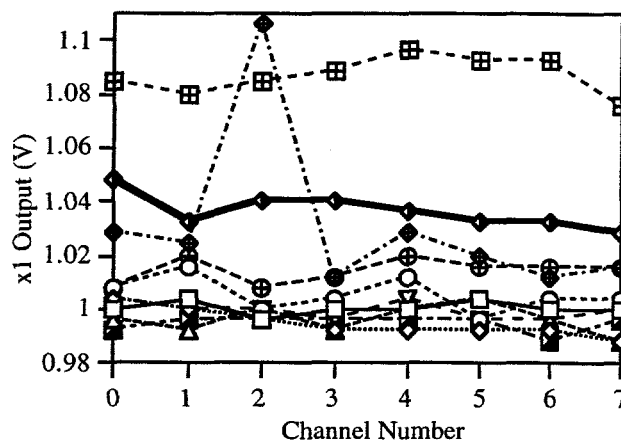


Fig. 10. x1 output as a function of channel number.

Examination of the data represented in Fig. 10 reveals that the gains of all channels on all the tested ICs are very similar. For all but one of the ten chips tested, the maximum deviation of the gain of any channel in a given IC from the average gain (for that IC) was less than 1%. Variations between ICs are somewhat greater, but the standard deviation of the x1 gain was less than 3% of the average gain of all 80 tested channels. Averaging on a channel number basis instead of on a per IC

basis revealed no systematic gain variations that might be due to a layout asymmetry.

A similar output test was conducted using the calibration pulser. A DAC setting was chosen to produce an x1 output of approximately 1 V. In this case, the maximum channel-to-channel gain variation in a given IC was $\pm 4\%$ with a standard deviation of less than 2% compared to the IC average. Variations between ICs were only somewhat greater with a maximum gain variation of $\pm 5\%$ and a standard deviation of 2% compared to the aggregate average gain. Fig. 11 shows a typical x1 channel response to the PbSc calibration pulser.

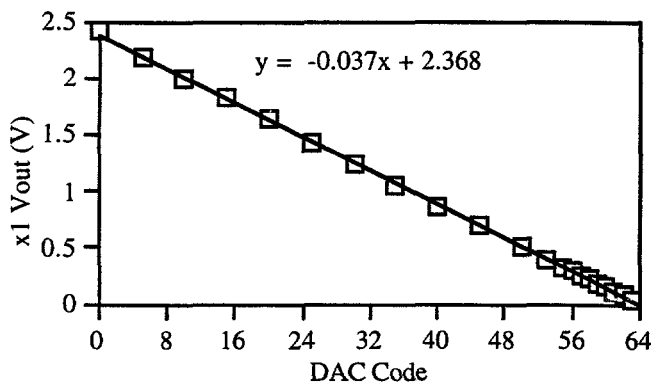


Fig. 11. x1 output as a function of the calibration DAC code.

V. COMPARISON OF PERFORMANCE

Simulations using nearly ideal amplifiers indicate that a considerably better signal-to-noise ratio is possible using the passive integrator than using an active integrator. An ideal correlator was added to the x16 output of the circuit shown in Fig. 3, and the output noise was simulated for a sampling time difference of 300 ns for two different cases. In the first, the amplifiers had an 8-MHz bandwidth and were noiseless, and the x16 output noise was found to be 82 μ Vrms or 0.64 fC. (This circuit has a charge gain of 128 mV/pC.) Clearly the passive integrating circuit itself produces very little noise. In the second case, the amplifiers were given an equivalent input noise voltage source of 10 nV/Hz^{1/2} and the output noise was 2.37 mVrms or 0.019 pC. Assuming a 4 V full scale output, the dynamic range of the x16 amplifier would be 1687:1, and this is greater than the needed 10 bit range.

Similar simulations were carried out for the active integrator circuit shown in Fig. 2. In this case, it was decided that the maximum practical integrating capacitor was 10 pF and that the circuit should have the same charge gain, decay time and bandwidth as the passive integrator circuit previously simulated. Thus, the feedback resistance was set equal to 5 M Ω , the coupling capacitor was 0.1 μ F, R1 was 1250 Ω , C1 was zeroed, the second amplifier gain was set to 16 and CF was 10 pF. Three cases were examined. In the first case, all three amplifiers were assumed to be noiseless. The x16 output noise was 4.18 mVrms in this case. When 10 nV/Hz^{1/2} was assumed for the x2 and x16 amplifiers, the noise rose only

slightly to 4.40 mVrms. For the last case, all three amplifiers were assumed to have 10 nV/Hz^{1/2} equivalent input noise voltages and the x16 output noise was 10.0 mVrms. For a 4 V full scale output, the dynamic range would be only 400:1, which is less than a 9-bit dynamic range.

The active integrator for the prototype PbSc had a charge gain of 39.5 mV/pC, a 3-V dynamic range and an rms noise of approximately 10 mV after double correlated sampling. Considerable improvement would be required to get to the desired levels for PHENIX: triple the gain and reduce the noise by more than a factor of two.

VI. CONCLUSIONS

Two types of integrating amplifiers have been investigated for use with lead glass and lead scintillator calorimeters using photomultiplier tube readout. The active integrator architecture has been proven in the WA98 lead glass calorimeter, but the existing implementations do not have sufficiently low noise for PHENIX. Reducing the noise to the levels desired for the PHENIX electromagnetic calorimeters may be possible, but may require much greater IC areas and power dissipation. The passive integrator architecture has several advantages that make it more suited for further development. Although it requires an additional pin and one additional external resistor per channel, the passive integrator should achieve lower noise levels with comparable amplifiers than the active integrator. Another advantage is that the charge gain can be set by an external capacitor, making possible that the same IC could be used by systems requiring different full scale charge levels.

VII. REFERENCES

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October, 1995

PHENIX Electromagnetic Calorimeters

Lead Glass:

10,000 channels

4 cm x 4 cm x 40 cm TF-1 glass

FEU-84 photomultipliers

Lead Scintillator:

15,000 channels

lead, scintillator, wavelength shifting fibers

FEU-115M photomultipliers

Instrumentation and Controls Division

lead glass photo

1995 IEEE Nuclear Science Symposium

ornl

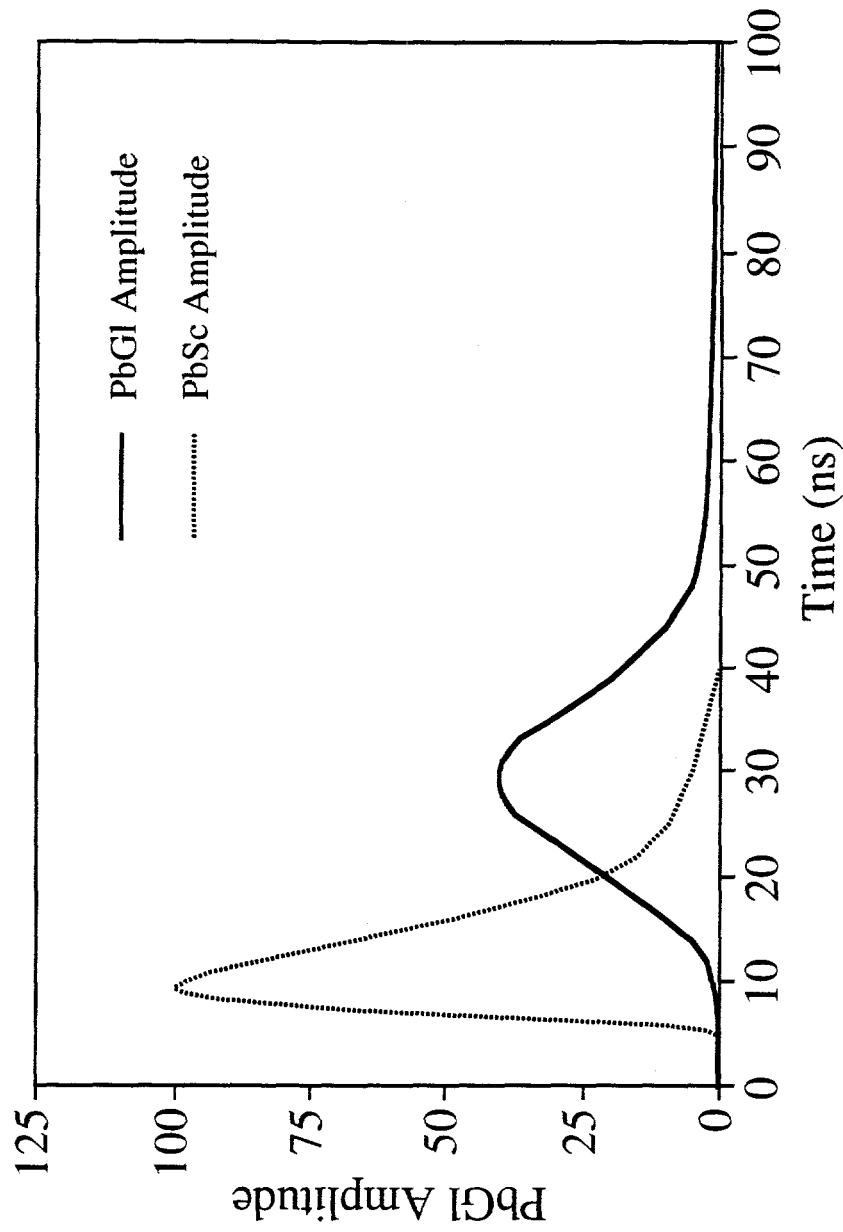
Instrumentation and Controls Division

lead scintillator photo

1995 IEEE Nuclear Science Symposium

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Photomultiplier Pulse Shapes



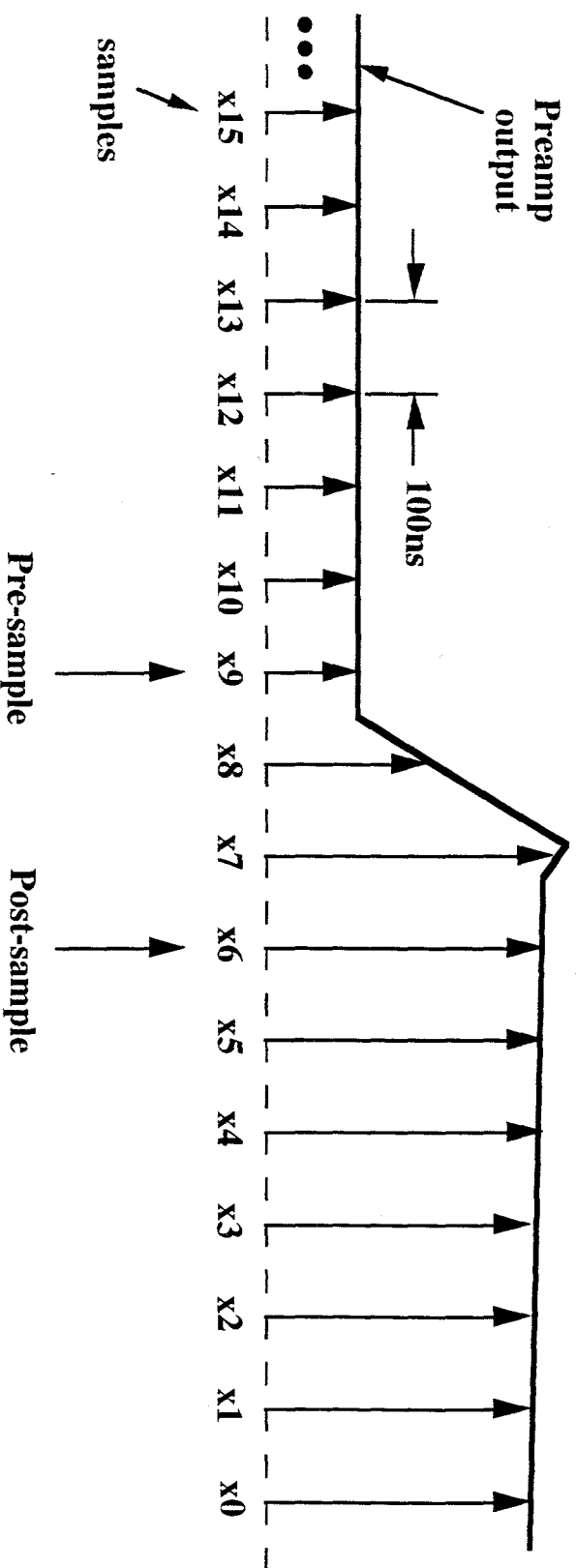
Energy Measurement Requirements

- Energy measurement with nominal 10-bit resolution with 14-bit dynamic range (cover 0.5 MeV to 10 GeV range)
- Deadtimeless
- Built-in calibration / diagnostic circuits
- Compatible with timing circuits and tower-cluster trigger

Likely Implementation Constraints

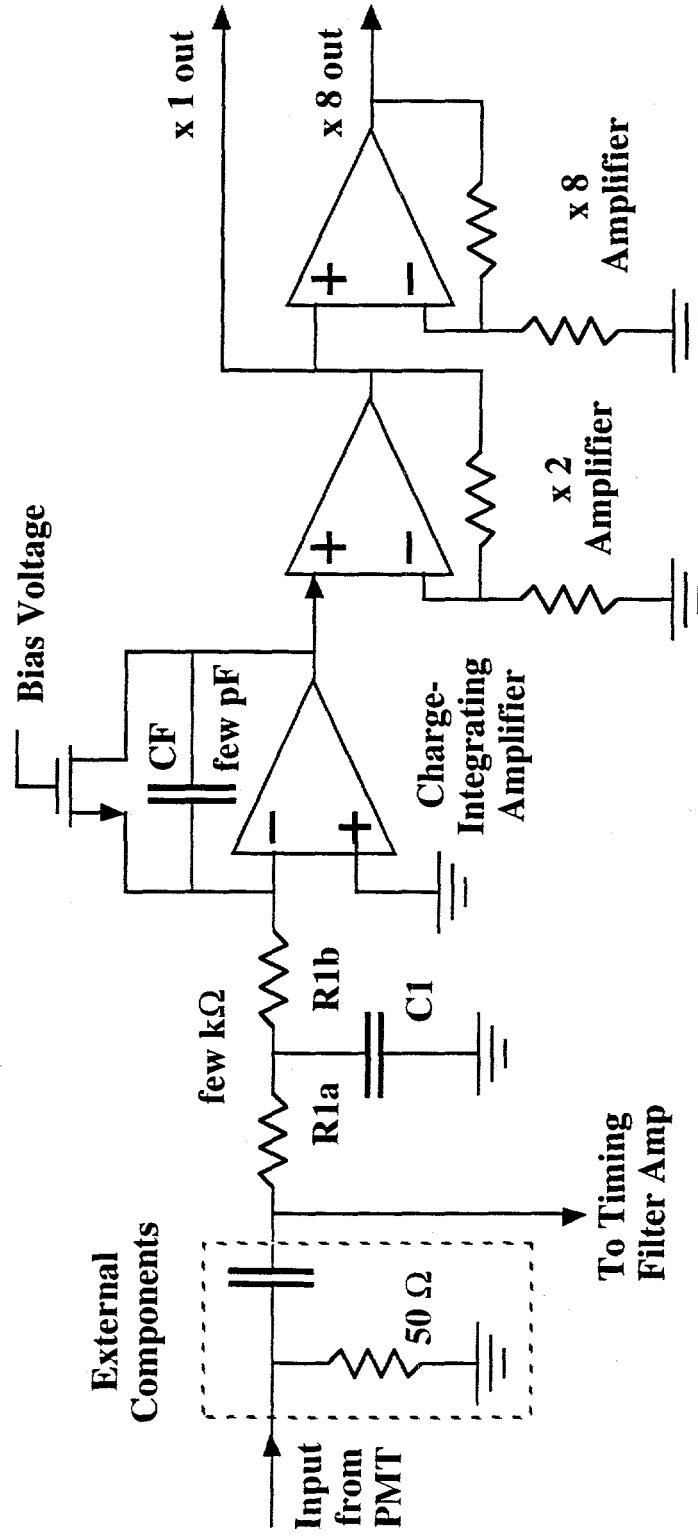
- Low cost (of system) and trigger sum wiring
====> need multiple channels per IC
- Many functional blocks - both analog and digital
====> CMOS IC
- Multiple channels /chip, pre-existing PMT bases
====> IC's located remotely ==> termination

Measurement Technique

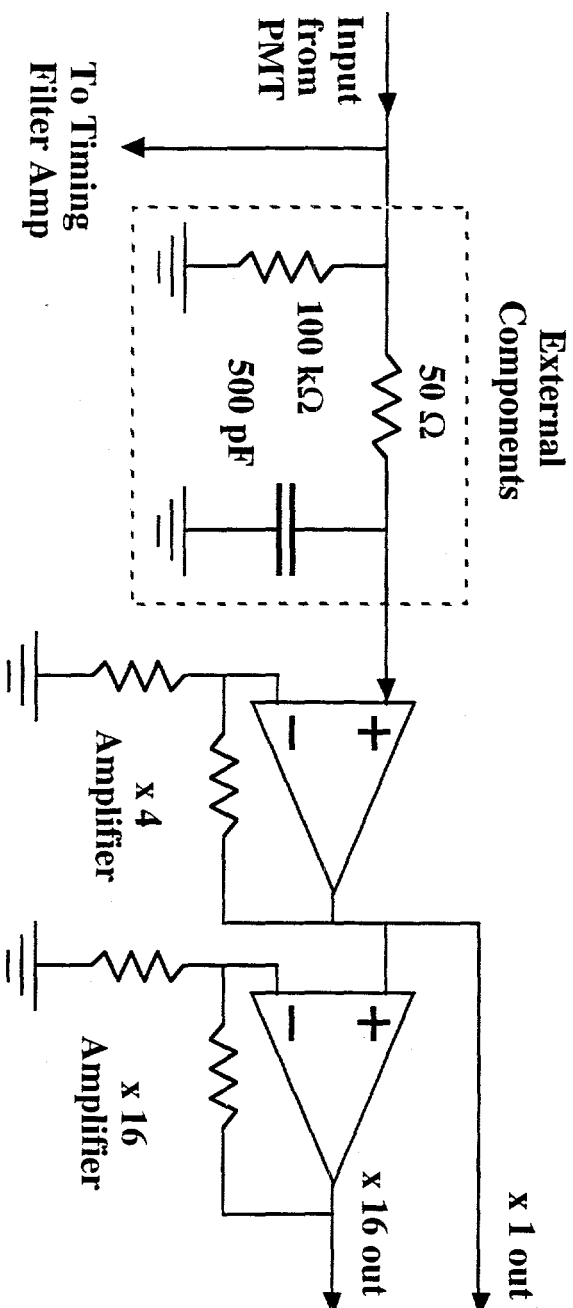


Double correlated output is post-sample minus pre-sample

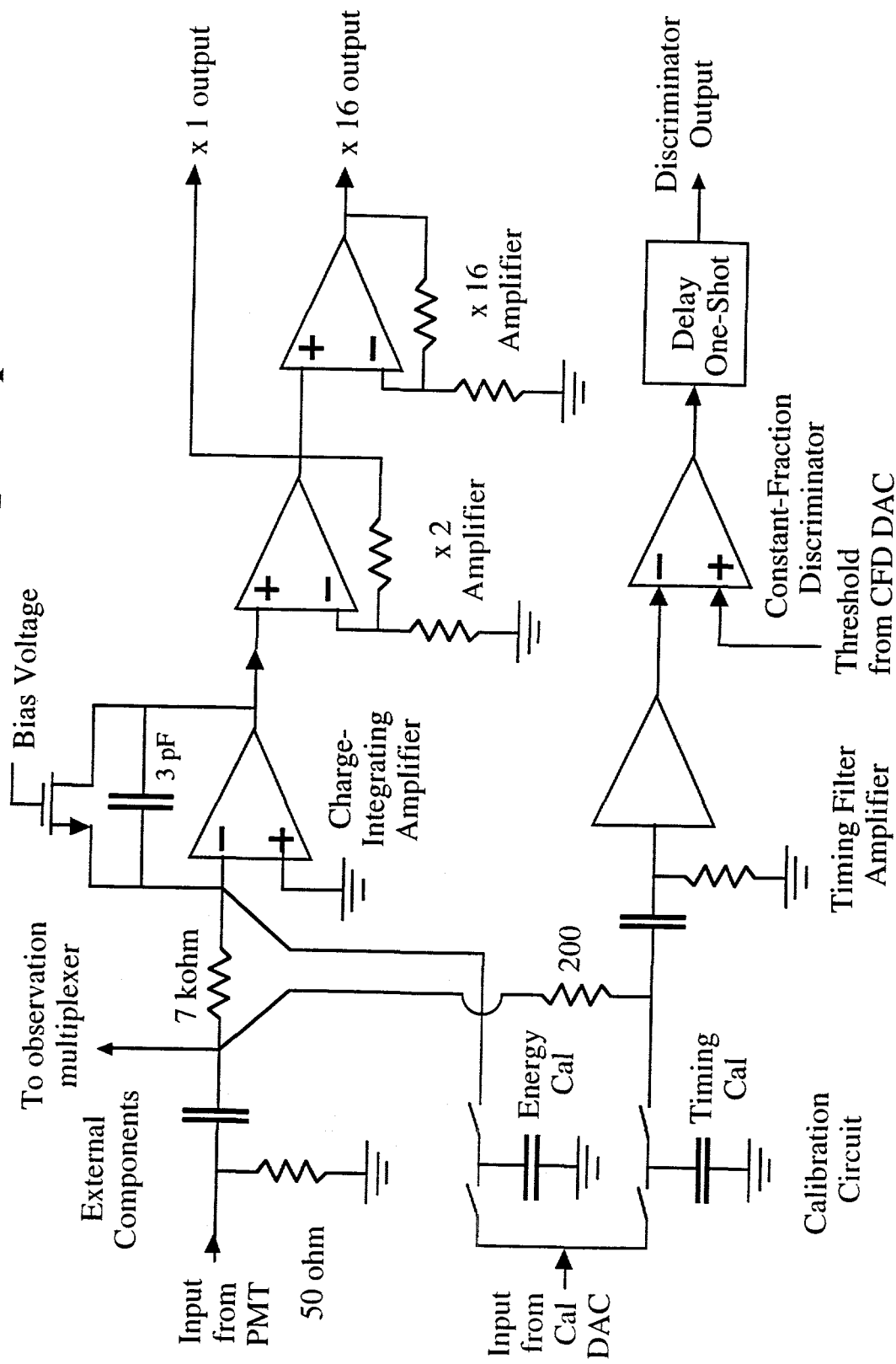
Active Integrator



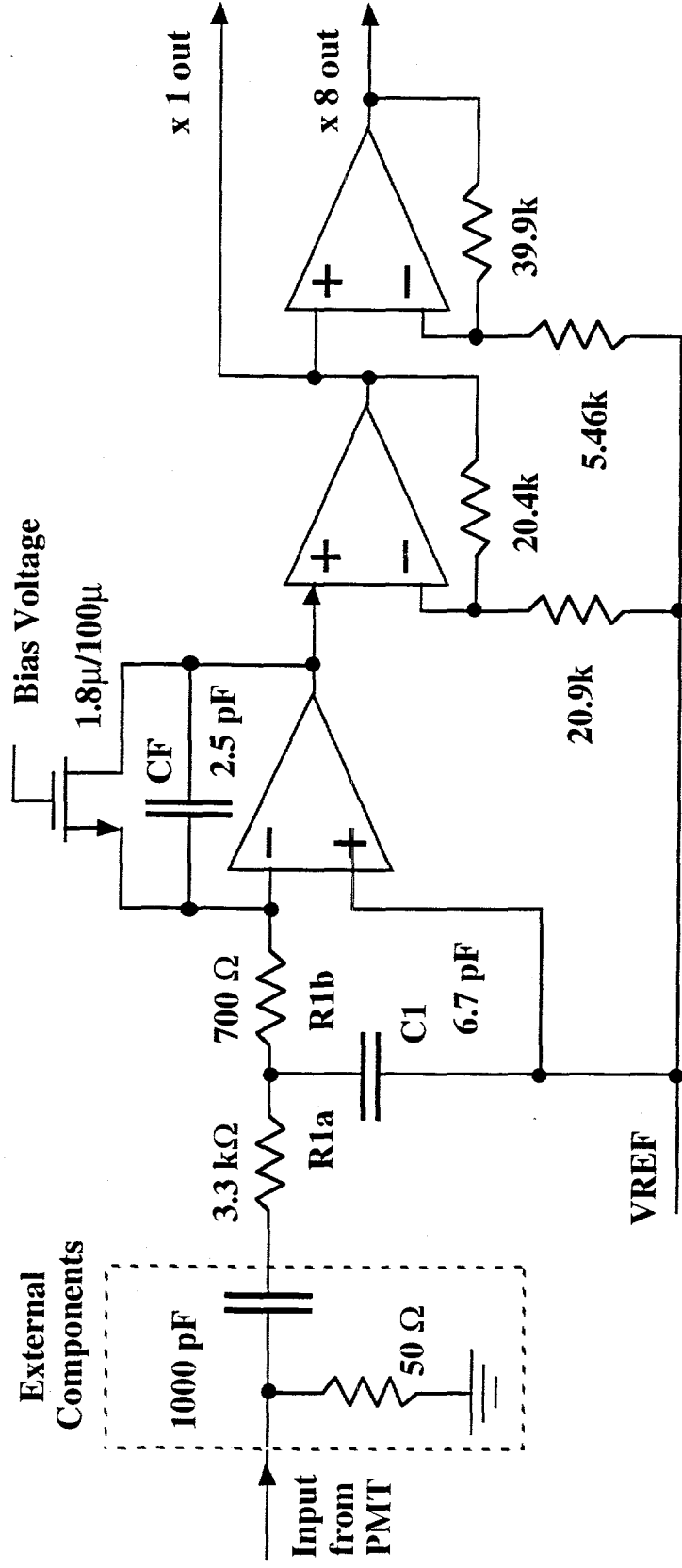
Passive Integrator



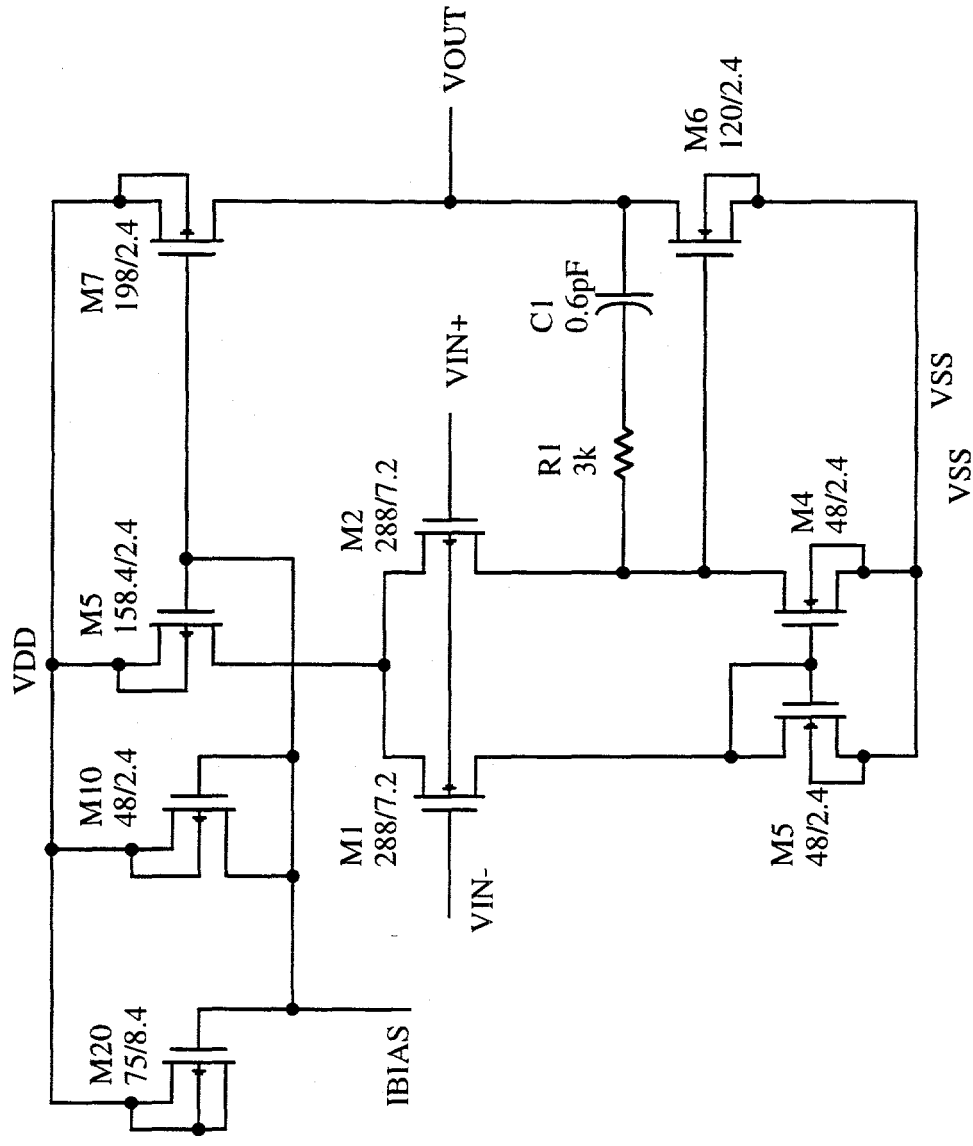
One channel of Preamp Chip



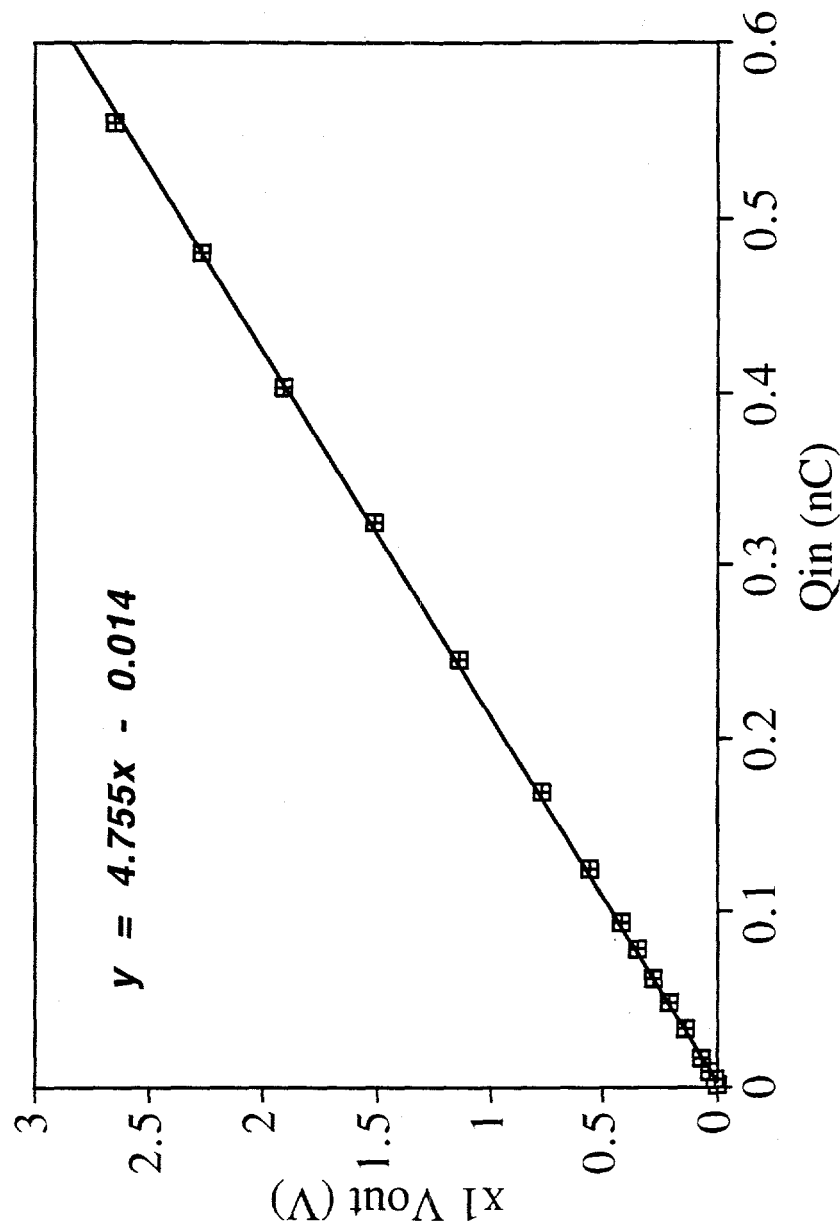
Active Integrator for Lead Scintillator Tests



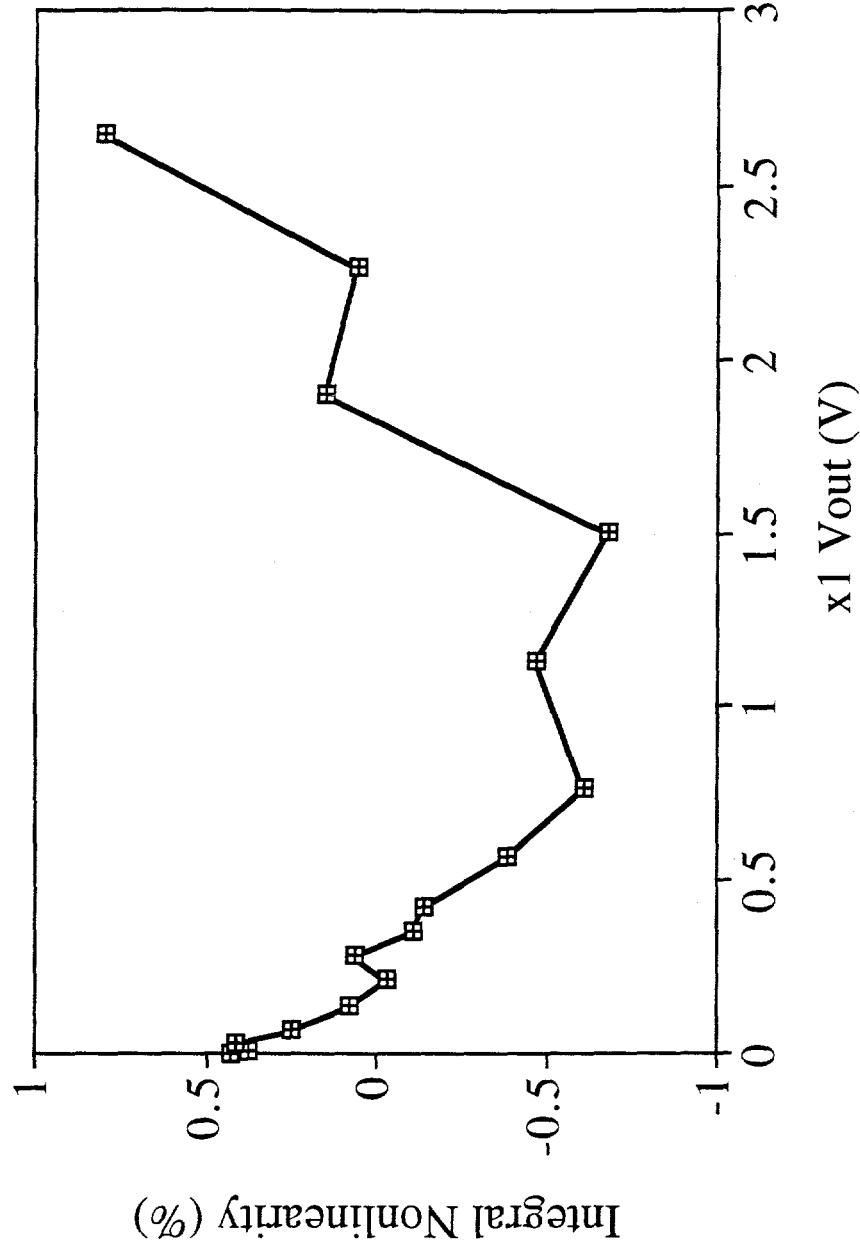
Op Amp for Integrator



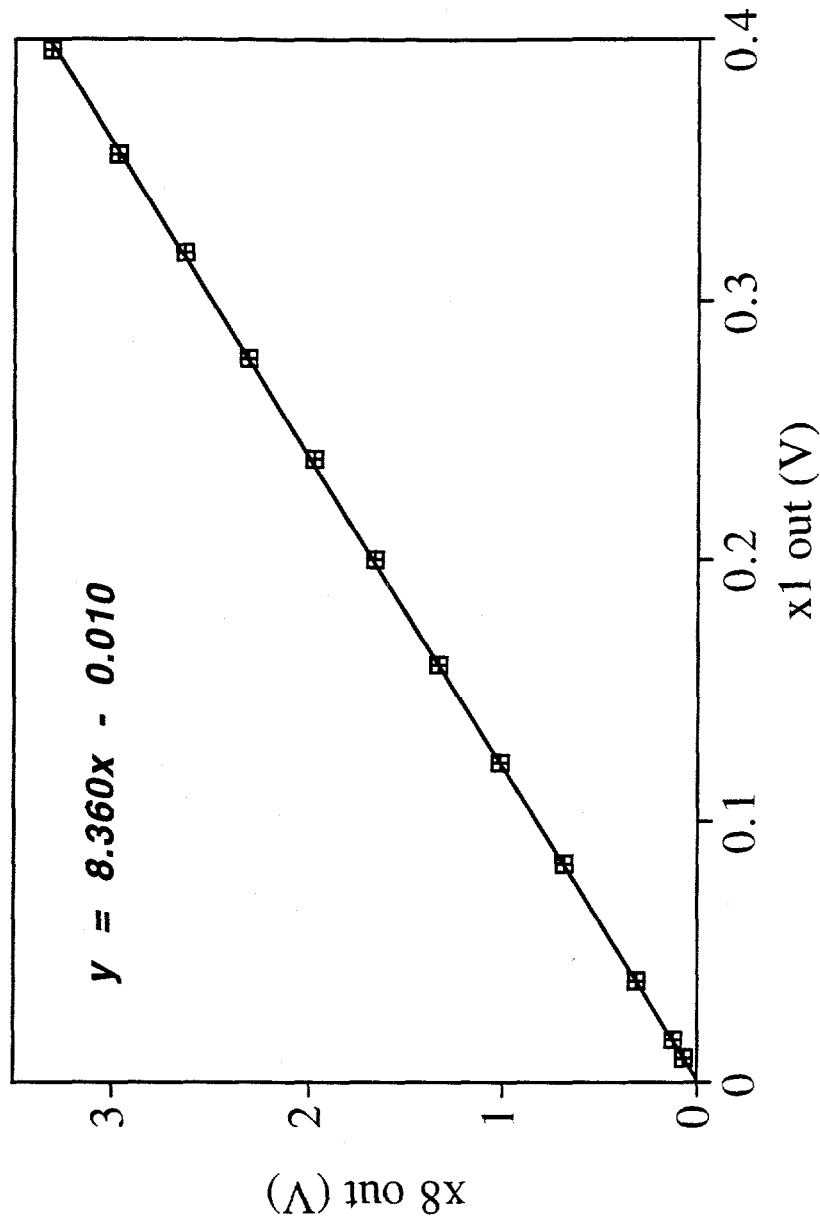
PbSc Prototype x1 Output



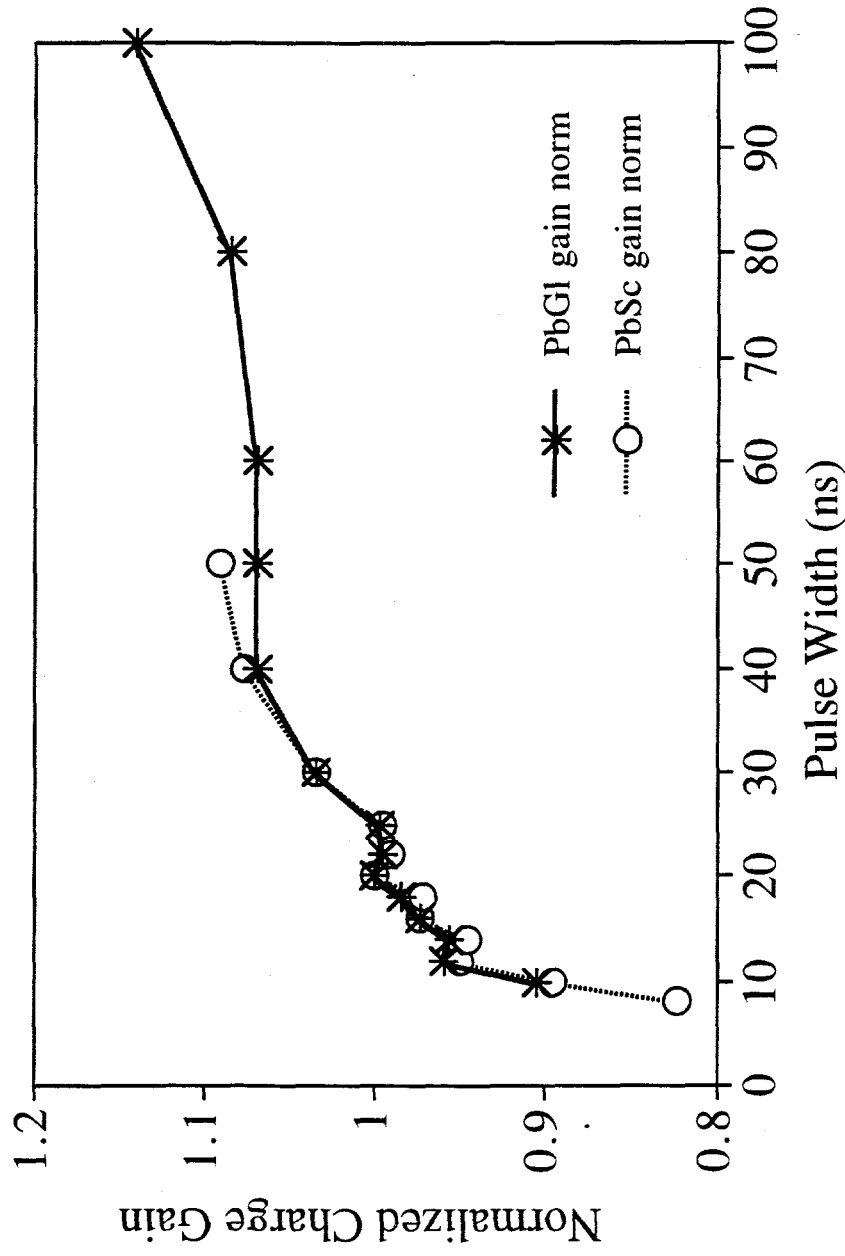
PbSc Integrator x1 INL



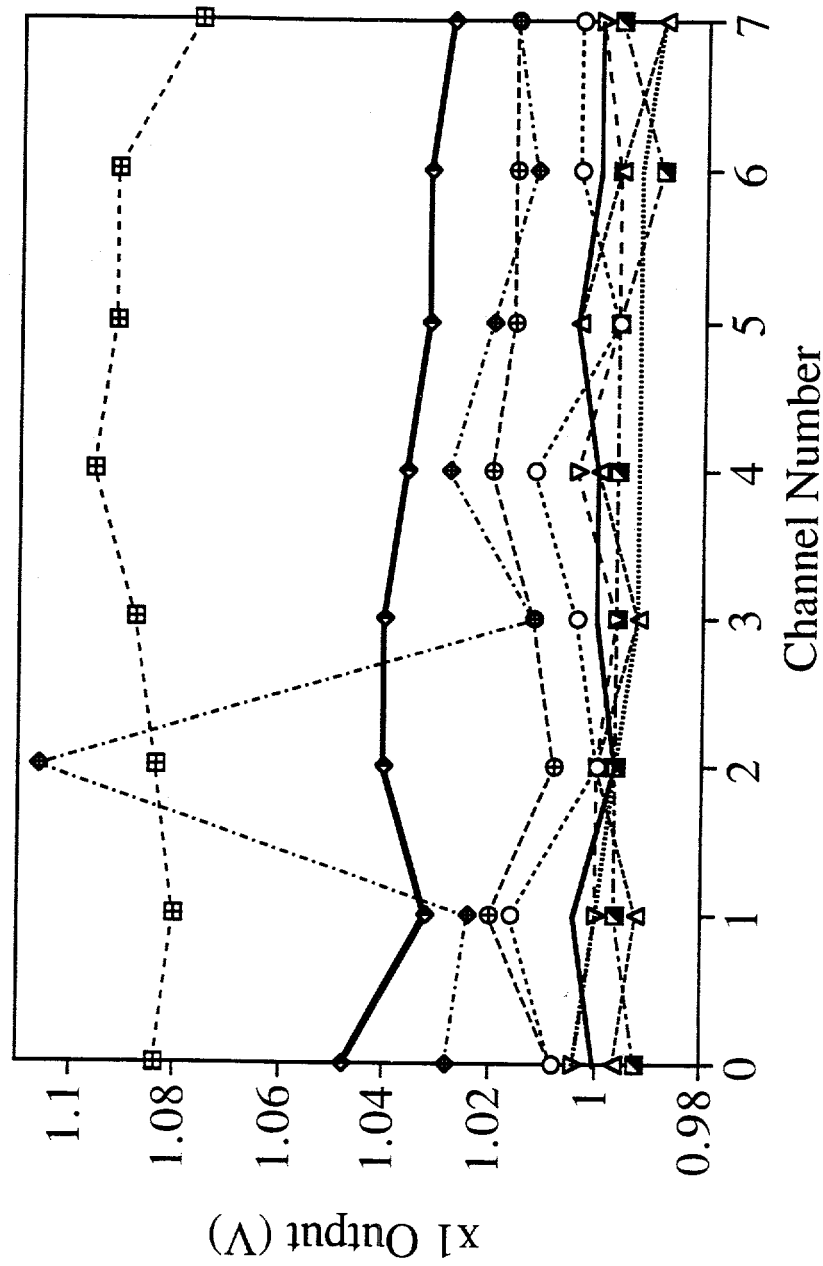
WA98 Integrator x8 vs. x1 Gain



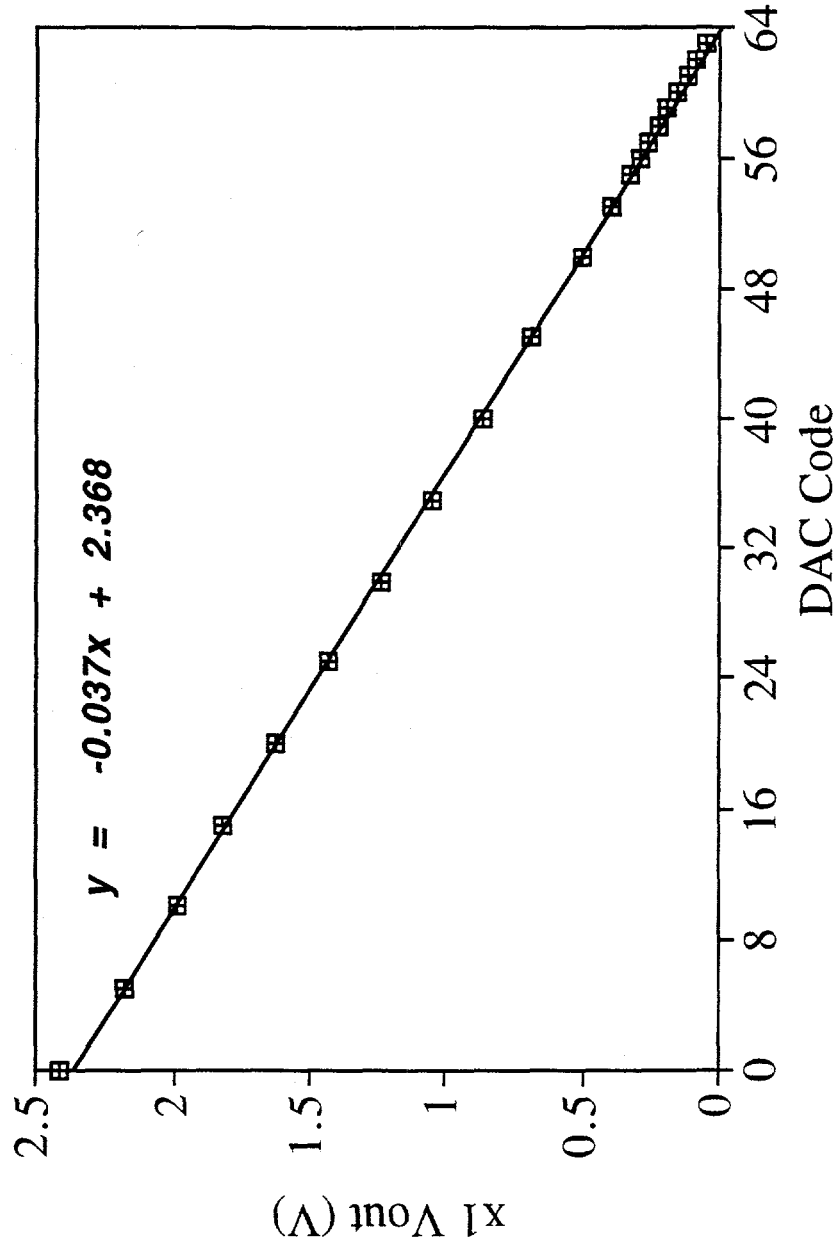
Charge Gain vs. Input Pulse Width



x1 Output vs. Channel Number



Calibration DAC and x1 Output



Passive Integrator

Case 1: No amplifier noise

Output x16 = $82\mu\text{Vrms}$

**Case 2: 10 nV/rt Hz amplifier noise,
8-MHz bandwidth per amplifier**

Output x16 = 2.37 mVrms

> 10-bit dynamic range

Active Integrator

Case 1: No amplifier noise, 8-MHz bandwidth per amplifier

Output x16 = 4.18 mVrms, 10-bit dynamic range

Case 2: 10 nV/rt Hz amplifier noise x2 and x16 amplifiers only, 8-MHz bandwidth per amplifier

Output x16 = 4.40 mVrms 10-bit dynamic range

Case 3: 10 nV/rt Hz amplifier noise all amplifiers, 8-MHz bandwidth per amplifier

Output x16 = 10 mVrms < 9-bit dynamic range

Conclusions

- Active integrator might meet requirements with more power, more area to get lower noise
- Passive integrator should meet requirements with only modestly low noise amplifiers.
- Passive integrator may also allow integrator IC to be used by different systems needing different charge gains