

EMI Filter Design

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Goals for EMI Filter

- Reduce noise reflected into the power supply circuit by the load to meet specifications set for root-mean-squared voltage (Vrms) and peak-peak voltage (Vpp).
- Main specifications for the power supply circuit are: Vrms < 75 mV and Vpp < 600 mV.
- Node where voltage is to be controlled is probed by the red probe in Figure 1.

Topology Selection and Simulation Results

- Figure 2 shows various topologies that were considered and simulated. Waveforms at the probes are not shown here.
- Series-damped filter in parallel with a larger capacitor (70 μ F) produced most desirable results for Vrms and Vpp. Model used for simulation incorporates commercial-off-the-shelf (COTS) parts and parasitic impedances.
- Additional methods we can use to reduce noise is to (1) delay operation of one of the flybacks by few msec, and (2) reduce peak-current regulated at one of the flybacks by a few hundred mA.
- Simulation results for Vpp and Vrms are shown in Figures 3. Note that for the circuit with the EMI filter, Vrms meets requirements, but Vpp exceeds requirements. Potential solutions for this may include relaxing Vpp specifications and/or modifying the filter to meet requirements.
- Monte Carlo analysis was used to understand range of Vpp observable with all device tolerances specified.
- Future work: Lab-test the assembled EMI filter

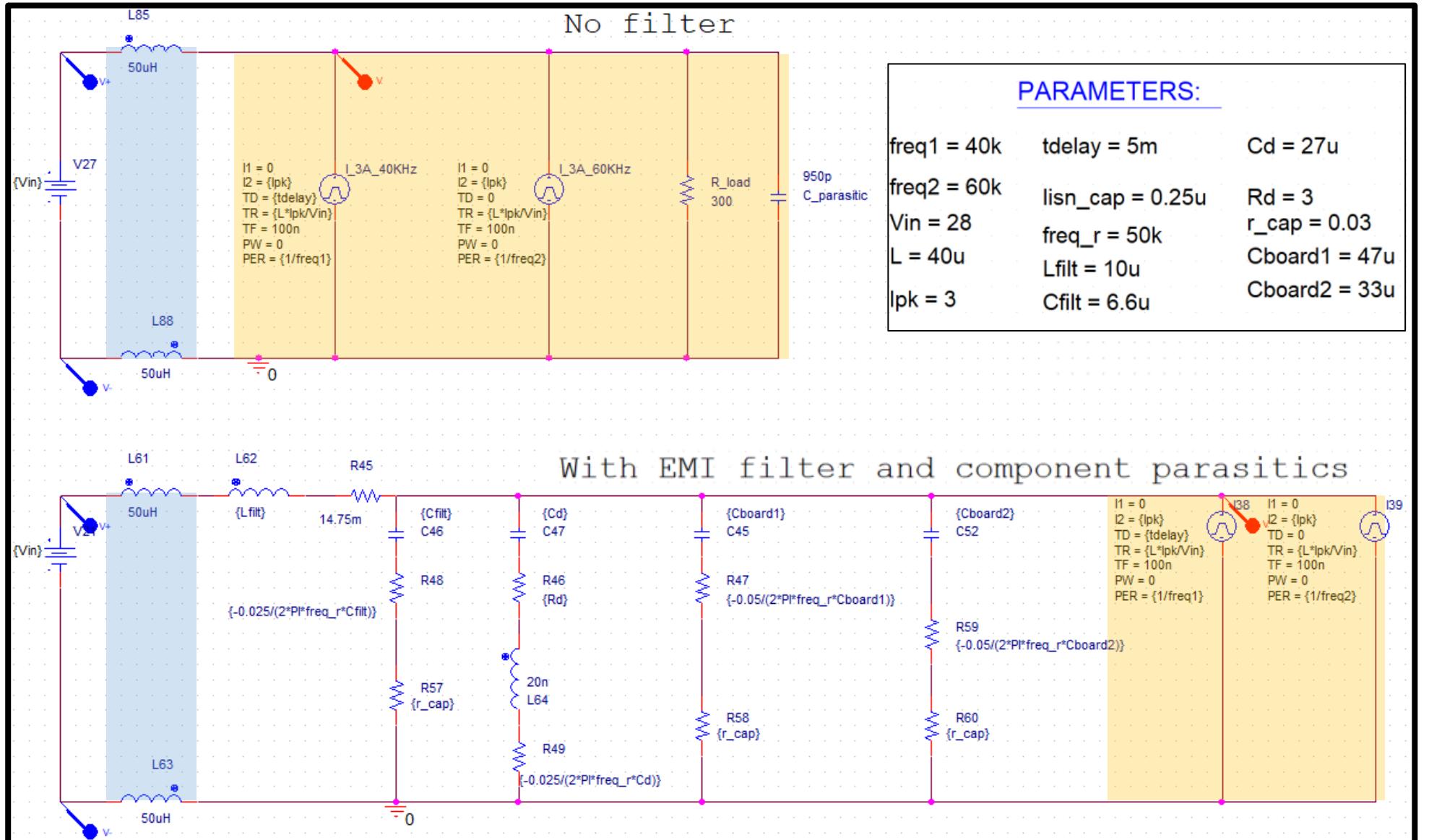


Figure 1. Reference circuit without EMI filter and circuit with EMI filter. Portions highlighted in blue are the line impedance stabilization networks (LISN). Portion highlighted in yellow represents the load that is reflecting noise into the power supply circuit. Load includes the current observed by the primary-winding of two flybacks. Operation of the 40 kHz current load is delayed by 5 ms to help reduce Vpp. Node to be monitored is probed in red.

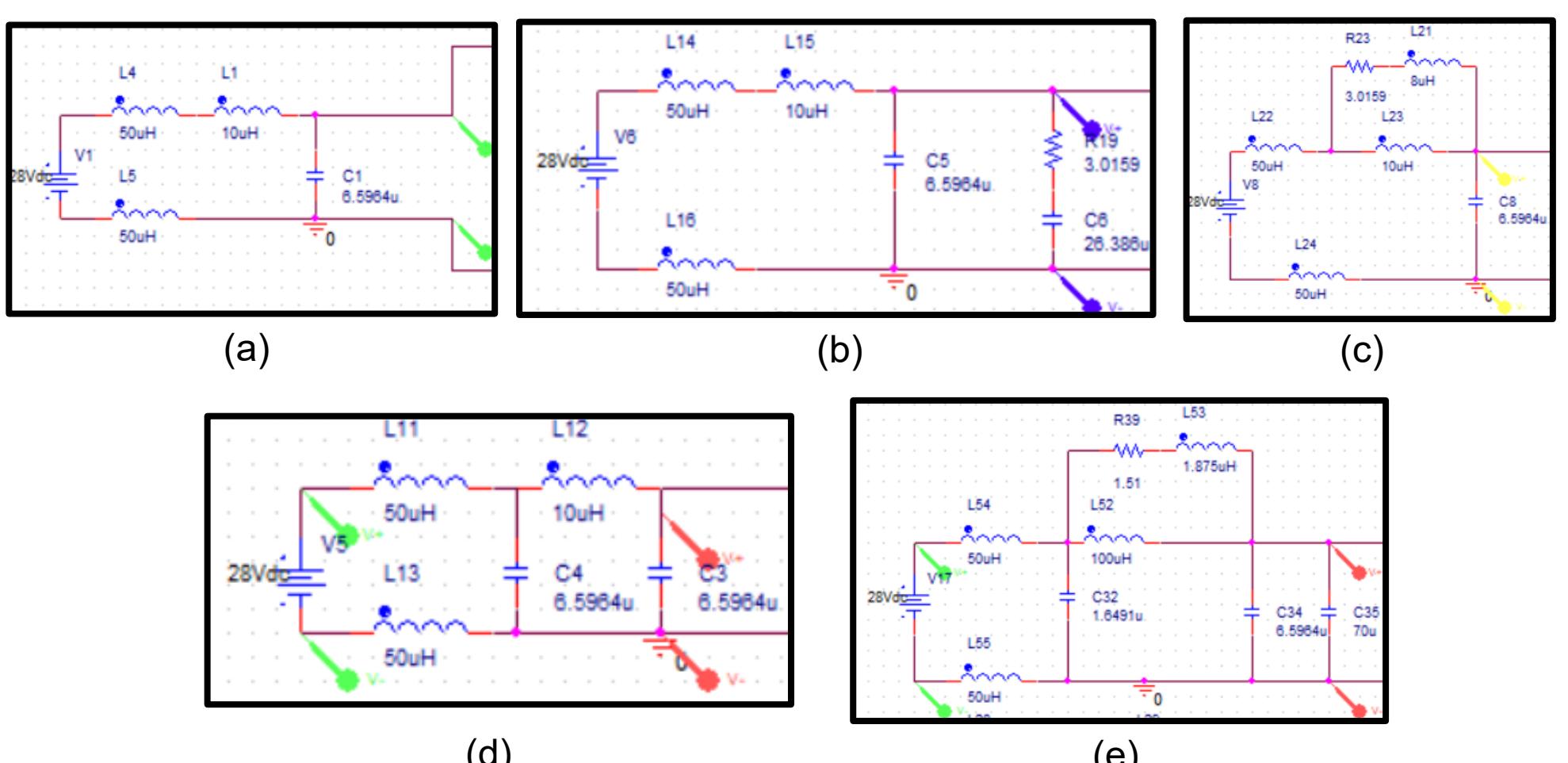
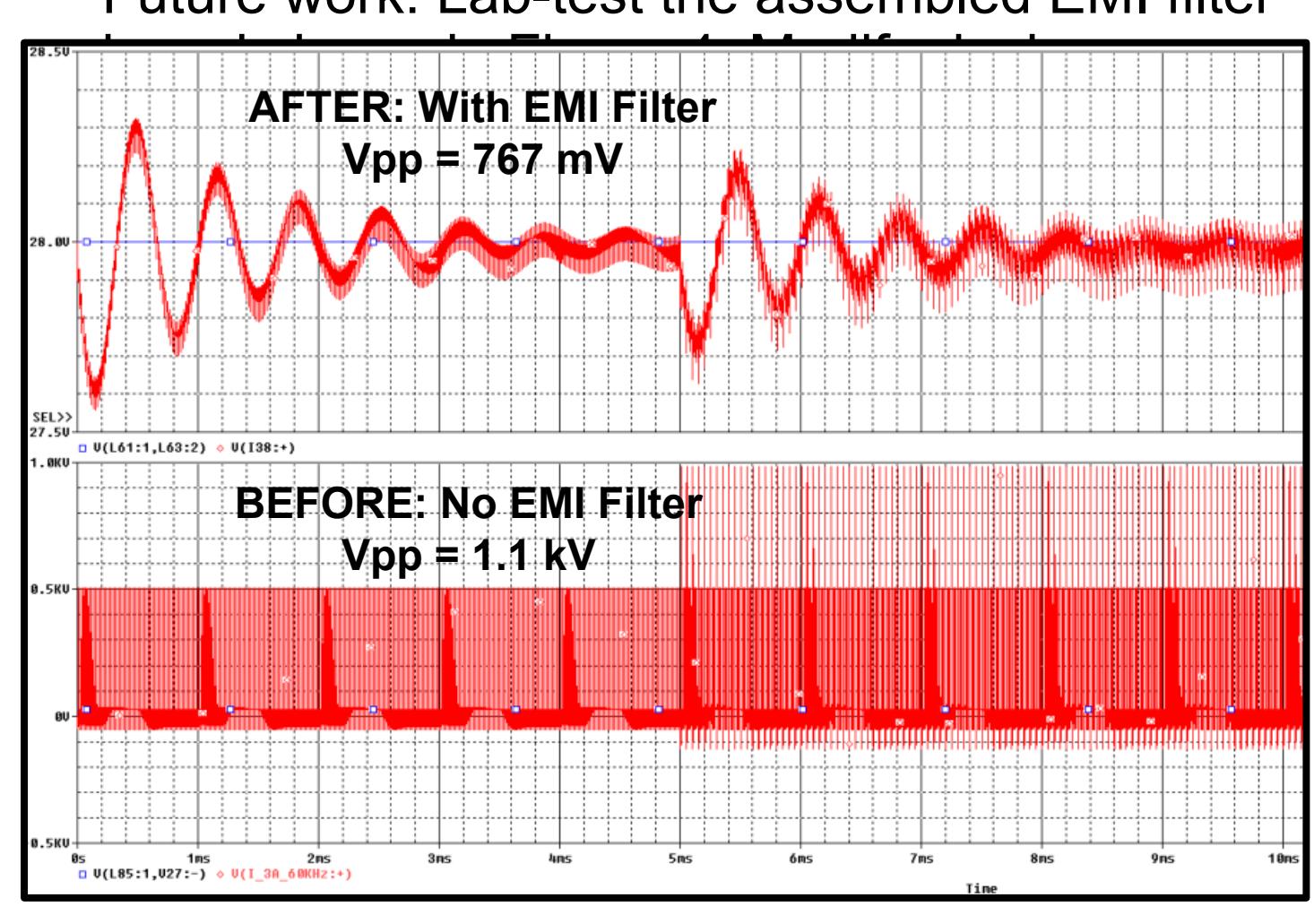
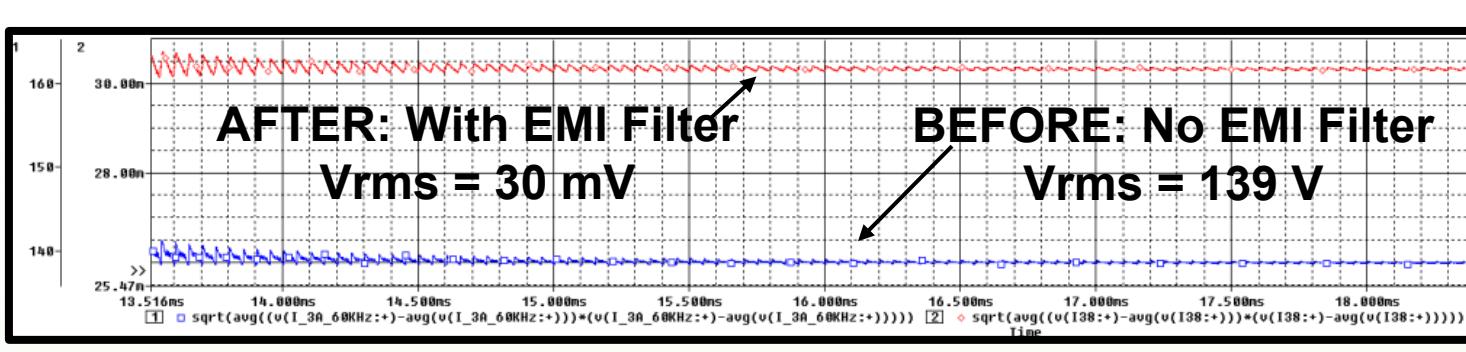


Figure 2. Various topologies simulated: (a) Undamped LC; (b) Series-damped; (c) Parallel-damped; (d) CLC; (e) Multiple-stage. Circuits were simulated via PSPICE.



(a)



(b)

Figure 3. (a) PSPICE simulation of Vpp for circuit with and without EMI filter referenced in Figure 1. Notice that the EMI filter has reduced the Vpp from 1 kV to 767 mV. Vpp is still slightly higher than requirements, but this is work in progress; (b) Vrms evaluation for circuit with and without the EMI filter. EMI filter reduces Vrms from 139 V down to 30 mV, meeting the Vrms specifications of 75 mV or less.

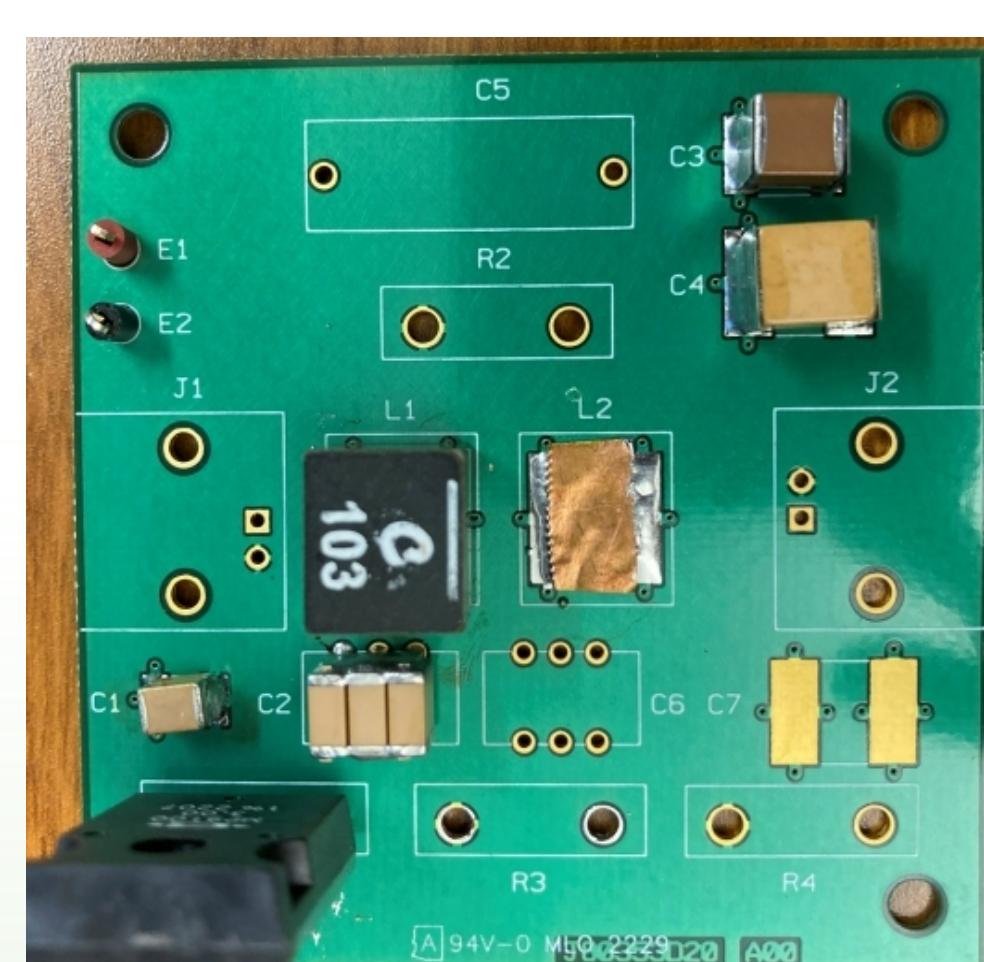


Figure 4. Printed circuit board (PCB) for EMI filter referenced in Figure 1. EMI filter does not include the LISN and the load. The PCB design includes some unoccupied spaces for additional capacitors, inductors, and resistors if needed.