SAND2022-16898C

Ballistic Asynchronous Reversible Computing in Superconducting Circuits

Michael P. Frank
Sandia National Laboratories
Albuquerque, NM USA
mpfrank@sandia.gov

Rupert M. Lewis
Sandia National Laboratories
Albuquerque, NM USA
rmlewi@sandia.gov

***Abstract*—In recent years we have been exploring a novel asynchronous, ballistic physical model of reversible computing, variously termed ABRC (Asynchronous Ballistic Reversible Computing) or BARC (Ballistic Asynchronous Reversible Computing). In this model, localized information-bearing pulses propagate bidirectionally along nonbranching interconnects between I/O ports of stateful circuit elements, which carry out reversible transformations of the local digital state. The model appears suitable for implementation in superconducting circuits, using the naturally quantized configuration of magnetic flux in the circuit to encode digital information. One of the early research thrusts in this effort involves the enumeration and classification, at an abstract theoretical level, of the distinct possible reversible digital functional behaviors that primitive BARC circuit elements may exhibit, given the applicable conservation and symmetry constraints in superconducting implementations. In this paper, we describe the motivations for this work, outline our research methodology, and summarize some of the noteworthy preliminary results to date from our theoretical study of BARC elements for bipolarized pulses, and having up to three I/O ports and two internal digital states.**

Keywords— theoretical models of reversible computation, asynchronous ballistic reversible computing, reversible superconducting circuits, superconducting flux quanta

I. Introduction

A longstanding motivation for the exploration of reversible computation in a classical computing context has been to improve the energy efficiency of general digital computing hardware, with the goal of circumventing the Landauer limit and approaching true physical (*i.e.*, thermodynamic) reversibility [1]. Most design schemes for hardware implementation of classical reversible computation that could potentially approach physical reversibility rely on synchronous, adiabatic transformations of the machine's digital state under control of externally supplied power-clock waveforms (*e.g.*, see [2][3]). Approaching physical reversibility requires these waveforms to be provided using high-quality resonant circuit elements to recover and reuse signal energy. But designing high-quality resonant circuits presents significant engineering challenges [4].

A potential alternative to this *adiabatic* approach to reversible computing is represented by *ballistic* schemes for reversible computing, the archetypal example of which is Fredkin's billiard ball model [5]. In ballistic approaches, the energy required to carry out logical state transitions is carried along with the digital information in a compact, ballistically-propagating entity (*e.g.*, an ideal billiard ball), and interactions (*e.g.*, elastic collisions) between these entities carry out reversible logical operations, while locally conserving signal energy. However, classic setups for ballistic reversible computing required precise synchronization between independent ballistic signals, which is not physically realistic. Realistic implementations would incur chaotic instability that degrades signal trajectories, requiring dissipation to restore the degraded signal.

These well-known difficulties with synchronous ballistic models of reversible computing motivated development of the novel reversible computing paradigm known as *asynchronous ballistic reversible computing* [6] (abbreviated ABRC or henceforth BARC). In BARC, the ballistically-propagating energy- and information-bearing entities (which we call "pulses") follow one-dimensional, non-branching interconnects, interacting *one at a time* with stationary circuit elements or "devices" bearing an internal digital state. Due to the temporal separation of pulse arrivals, the physical dynamics of this class of systems is much less prone to dynamical instability, needing only relatively occasional signal restoration to keep pulses' kinetic energies and arrival times within specified tolerances.

The BARC model was first introduced in 2017 along with a proof of its computation universality [6], and in 2018 [7] and 2019 [8] we described early results from a present effort at Sandia to develop a physical implementation of this new scheme in superconducting circuits. In this effort (called BARCS, for BARC with Superconductors), pulses are physically embodied by solitons of quantized magnetic flux, *i.e.*, *fluxons*, propagating along long Josephson junction (LJJ) transmission lines, and the devices are also implemented as JJ circuits. In BARCS circuits, a natural digital representation of information utilizes the polarization and location of magnetic flux quanta in the circuit; superconductor physics naturally stabilizes digital information encoded in this way.

A central goal of the BARCS effort is to demonstrate working implementations of a computation-universal subset of the

Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration (NNSA) under contract DE-NA0003525. This work is supported by a grant awarded under the U.S. Department of Defense Advanced Computing Initiative, BAA #W911NF-19-S-0007. This document describes objective technical results and analysis. Any subjective views or opinions that might be expressed in this document do not necessarily represent the views of the U.S. Department of Energy or the United States Government. Approved for public release.

possible asynchronous reversible devices. The engineering work on this is still in progress, but an important theoretical step on the way to this goal is to thoroughly characterize the possible digital functional behaviors of such devices. Thoroughly understanding the full space of design possibilities facilitates our search for workable physical implementations of useful devices, and for simplified schemes for constructing arbitrary reversible computations out of potentially implementable primitive circuit elements.

In this paper, we summarize the major results to date that have emerged from the theory side of this effort, which include the classification of the possible asynchronous reversible behaviors for devices having up to three bidirectional I/O ports and two internal states, in the context of applicable conservation and symmetry constraints. To facilitate this effort, we developed a simple Python program called `barc` to assist in classifying BARCS devices.

The organization of this paper is as follows: §2 briefly reviews the BARCS model; §3 introduces notations for transition functions and symmetries; §4 summarizes some results to date from the function classification effort; §5 gives a brief overview of the custom `barc` software tool facilitating this effort; and §6 concludes. Note that the present paper comprises a somewhat high-level overview of our work in progress; a more detailed report of results along these lines will be published at a later time.

II. Review of BARCS Model

The Ballistic Asynchronous Reversible Computing (BARC/ABRC) model was previously detailed in [6]. In lieu of repeating the full definition here, we briefly review a few key features. A BARC circuit is a network of primitive *devices* a.k.a. *elements*, each of which has a fixed set of named or numbered I/O *ports*. Each port connects to one end of a (non-branching) interconnect. Localized information-bearing *pulses* (which are conserved, as in [5]) propagate *ballistically* (*i.e.*, with low loss) along the interconnects. In general, all ports and interconnects are assumed to be *bidirectional*; that is, pulses may propagate in either direction, although a given circuit may have been designed for use with a specific (*e.g.*, feed-forward) directionality.

The key difference between BARC vs. *synchronous* ballistic models (compare Figs. 1(b) and 1(a)) is that, in BARC, we specify that pulses must arrive at a given device at different times from each other, that is, far enough apart so the device dynamics is insensitive to the relative pulse arrival times. Doing logic in BARC therefore requires devices with a persistent internal state variable (circled *S* in Fig. 1(b)) so that data inputs can be meaningfully combined.

In general, pulses may come in multiple distinct types; however, universal reversible logic can be built even with just one pulse type; Figs. 1(c,d) illustrate part of a construction for this from [6]. The control pulse C (if present) arrives first (@1), sets the state of the toggle barrier, and then (@2) the data pulse D (if present) passes through the barrier if C had arrived (output CD), or reflects off the barrier and is routed around to the other output $C\bar{D}$. This circuit is designed for feedforward operation within a larger circuit that reversibly resets the state of the toggle barrier (which can be done easily using two additional devices termed *toggling rotaries*, TR; *e.g.* see Fig. 2). Inverting logic operations

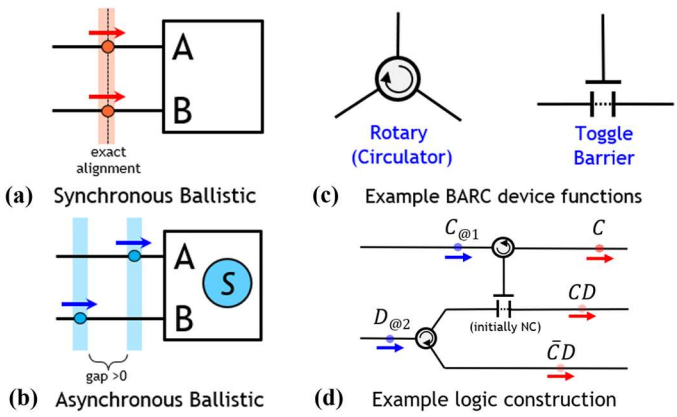

Fig. 1. Illustration of BARC model. Inputs to (a) traditional, synchronous ballistic devices, contrasted with (b) asynchronous ballistic devices, which may have internal state. (c) Two example devices: (Left) a stateless *Rotary* R which routes pulses clockwise between adjacent ports, and (Right) a *Toggling Controlled Barrier* (TCB) a.k.a. "Toggle Barrier", which has conducting (C) and nonconducting (NC) states. Pulses reflecting off the control terminal toggle the state; pulses on other terminals reflect in state NC and pass through in state C. (d) Part of the universal circuit construction from [6], illustrating how R and TCB devices can be set up to implement a reversible AND-like function, given an unpolarized pulse-type alphabet (*i.e.*, where only one type of pulse is used).

can be implemented using a dual-rail encoding, and superfluous ("garbage") outputs can be later *decomputed* using a similar circuit, as is typical within reversible logic architectures.

Although the above construction is sufficient to demonstrate universality, the superconducting circuit domain naturally supports not one but *two* pulse types, consisting of opposite polarities of magnetic flux quanta [7]. One aspiration of the BARCS effort is to identify a simple set of BARC primitives in general utilizing such *bipolarized* pulses that are readily implementable as reactive (*i.e.*, undamped) superconducting circuits and are sufficient for universal reversible computation. To facilitate this effort, we would like to understand the full set of all possible bipolarized BARCS elements having up to three I/O ports and up to two internal states. The remainder of this paper summarizes our work in progress on this task.

III. Definitions and Notations

In general, we may assume some fixed but arbitrary set of labels (*e.g.*, $\uparrow, \downarrow$) for the two distinct moving flux (*fluxon*) polarities m. For each specific type of device having n I/O ports and k internal states, we may also assume that there is an associated, arbitrary set of labels (*e.g.*, $\{1, \ldots, n\}$) for its ports p, and similarly a set of labels (*e.g.*, $\{S_1, \ldots, S_k\}$) for its available internal states s.

For a given device, an *input syndrome* $i = m\rangle p(s)$ denotes a (moving) fluxon with polarity m arriving at port p when the device is in state s, and an *output syndrome* $o = (s)p\rangle m$ denotes a fluxon with polarity m emerging from port p of an element that is now in state s. The *transition function* f of a given BARCS element is simply a map $f: I \to O$ from the set $I = \{i\}$ of possible input syndromes to the set $O = \{o\}$ of possible output syndromes; any given transition $f(i) \in O$ may also be written out more explicitly as

$$m_i\rangle p_i(s_i) \to (s_o)p_o\rangle m_o, \tag{1}$$

where the i, o subscripts denote the values associated with input and output syndromes, respectively. In this paper, we assume that each transition function f comprises an injective map over its entire domain I, so that we say it is *fully logically reversible*. In future work, we will also explore transition functions F that are only injective over an *assumed set* $A \subset I$; such functions are termed *conditionally logically reversible*, and their appropriate use can be adequate for achieving energy-efficient computation, as discussed in the earlier work on generalized reversible computing theory [9].

When studying the implementability and distinctness of BARCS elements, it's useful to consider the applicable symmetries that they could respect. Any given (self-)symmetry $\mathcal{X}$ is associated with some invertible *symmetry transformation* X that operates on transition functions f, and a *symmetry group* $\mathfrak{X}$ consisting of distinct powers of X (with $X^0 = \mathrm{I}$ being the identity). The symmetries considered in our studies include:

- *Direction-reversal symmetry* $\mathcal{D}$ – This refers to symmetry of f under an exchange of roles between input and output syndromes (ignoring their notational differences). Note that $D(f)$ corresponds to f^{-1}.
- *State-exchange symmetry* $\mathcal{S}$ – Defined only for two-state devices, this refers to symmetry of f under an exchange of the two state labels S_1, S_2.
- *Flux-negation symmetry* $\mathcal{F}$ – This refers to symmetry of the device's transition function under a polarity reversal of both internal and I/O fluxes (and associated currents). Properly defining this symmetry's relations to others requires that the encoding of internal states in terms of flux configurations in the circuit element has been defined. However, to simplify implementations, we initially assume that the state encoding is such that a flux negation transformation includes performing a state exchange S. Note that $\mathcal{F}$negation also includes exchanging I/O fluxon polarities. For physical reasons, it appears that implementable BARCS devices must obey $\mathcal{F}$ symmetry unless the symmetry is explicitly broken, *e.g.*, by introducing permanently trapped fluxes into the device's structure.
- *Port-relabeling symmetries* $\mathcal{R}_P$ – These refer to symmetries under permutations P of the port labels. Special cases include $\mathcal{R}_\mathbf{r}$ = rotational symmetry, and $\mathcal{R}_{\{p\}}$ = reflection of port labels across the port p "axis" (note that defining both of these requires specifying the port order). $\mathcal{R}(n)$ refers to symmetry under *all* possible port rearrangements for an n-port device.

In addition to the $\mathcal{F}$ symmetry constraint, planar circuit elements with continuous superconducting boundaries must obey a *flux conservation* constraint; however, characterizing the detailed implications of this constraint requires specifying how internal states are encoded—specifically, what is the net internal flux of the device in each of its states. In this work, we considered cases in which the net internal fluxes of the two states were $\{1, -1\}$ or $\{0,0\}$ in units of the magnetic flux quantum Φ_0.

IV. Summary of Results

At this time, we have essentially completed the classification of BARCS functional element behaviors for devices with up to three I/O ports and up to two internal states. Below is a summary of some of the key results to date for various device types:

- ***One port, one state.*** – As was mentioned in [7], the only reversible elements of this type are the *reflector* and the *inverting reflector*; these have trivial superconducting implementations as closed-circuit and open-circuit line terminations.
- ***One port, two states.*** – Modulo basic symmetries, the only nontrivial element is the *reversible memory* (RM) cell, described [7] and implemented [8] in 2019. A test chip for it was fabricated in 2020, and a U.S. patent on the implementation concept was issued in 2022 [10].
- ***Two ports, one state.*** – There are four I/O syndromes, so $4! = 24$ reversible functions. The nontrivial function with maximal symmetry is a bidirectional NOT gate; this is trivially implementable as a *non*-planar circuit via a half-twist of the conductor pair in the interconnect; a planar implementation (with open boundary) was described in [11]. One interesting albeit less-symmetrical element is the *reversible polarity filter* (RPF); it lacks $\mathcal{F}$ symmetry, and so its implementation would require permanent trapped flux or external flux biasing.
- ***Two ports, two states.*** – In this case, there are $2^3 = 8$ possible I/O syndromes and thus $8! = 40{,}320$ reversible functions, so full enumeration and classification requires software assistance. However, restricting attention to flux-conserving planar circuits simplifies the situation considerably. If the internal states are both flux-neutral, the I/O fluxon polarity is unaffected by the operation; and if $\mathcal{F}$ symmetry is also respected, the function count reduces to $2^2! = 24$, of which 14 are atomic and nontrivial. Alternatively, if internal states are flux-polarized, the only possible effect on the fluxes is an exchange, like in the RM cell. There are 7 primitive functions of this type (modulo symmetries), and the most self-symmetrical of these include the Ballistic Shift Register (BSR) [12], and a dual-port version of the RM cell (differing from the BSR in that the fluxon emerges from the same port that it entered). We recently implemented the 2-port RM cell at the schematic level and verified its functionality in WRspice.
- ***Three ports, one state.*** – If we ignore conservation and symmetry constraints, there are $(2 \times 3)! = 720$ possible functions in this case, requiring software enumeration. But if we assume flux conservation and $\mathcal{F}$ symmetry, the only nontrivial behavior is a polarity-independent rotary. It is not yet clear whether this function is implementable as an unbiased, reactive BARCS circuit.
- ***Three ports, two states.*** – Without constraints, there are $12! = 479{,}001{,}600$ possible fully reversible functions. Restricting attention to flux-conserving, $\mathcal{F}$-symmetric functions lowers this to 252 functions for flux-polarized

states, and 720 for flux-neutral states. These cases are described in more detail below. We have verified a 3-port version of the RM cell in WRspice.

The most complex category of devices studied in detail in this effort so far was the last one mentioned above, consisting of all three-port flux-conserving elements with two flux-neutral internal states and respecting $\mathcal{F}$ symmetry. The `barc` program generated a complete enumeration of all 600 non-trivial, primitive transition functions in this category and grouped them into 45 distinct symmetry-equivalence groups (Table II), such that the members of each such class transform to each other via some subset of the natural mutually commuting symmetry transformations that function descriptions in this family may support. The 11 largest equivalence classes represent the most "irregular" reversible device behaviors of this type, each of which exhibits only the minimal self-symmetry ($\mathcal{F}$) that is assumed to be required. Each such behavior can be described via 24 essentially equivalent transition functions, corresponding to the largest composite symmetry group $\mathfrak{D} \cdot \mathfrak{S} \cdot \mathfrak{R}(3)$ consisting of all $2 \cdot 2 \cdot 6 = 24$ possible combinations of the various optional symmetry transformations (D, S, and the various port rearrangements R_P).

Similarly, in the flux-polarized case, 219 of the 252 functions are non-trivial primitives, and classify into 39 equivalence groups (Table III). Since applying S transforms would cause flux conservation violations in this case, the overall composite symmetry group becomes just the 12-element group $\mathfrak{D} \cdot \mathfrak{R}(3)$.

Space constraints preclude inclusion, in the present paper, of a detailed description of each of the many qualitatively distinct device types (*i.e.*, equivalence groups) that we identified in this study; the full details will be published in a subsequent article. For now, we illustrate the flavor of the results with a few example function descriptions.

V. Example Functional Element Behaviors

The following example behaviors (Figs. 2–5) are all taken from the set of 3-port, 2-state flux-conserving $\mathcal{F}$-symmetric elements with flux-neutral internal states. (Such states might be implemented by, for example, an internal exchange between two

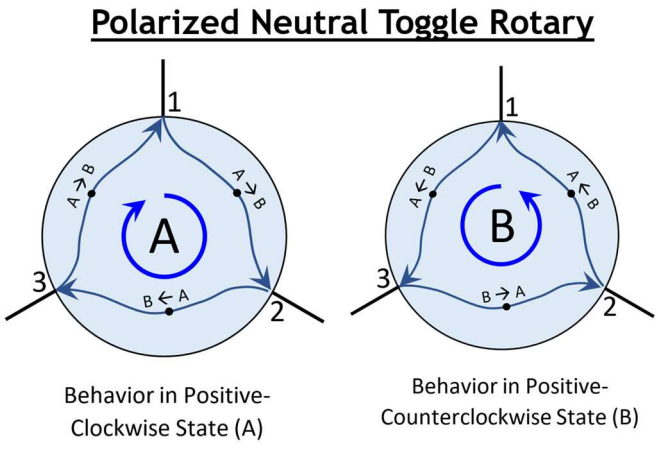

Fig. 2. The Polarized Neutral Toggle Rotary (PNTR) leaves the polarity of the moving fluxon unchanged, routes it in a polarization-dependent direction, and alternates its direction with each fluxon that passes through. The arrows in the figure illustrate behavior for positive input fluxons. The dots denote that the state is toggled when the arrows are followed.

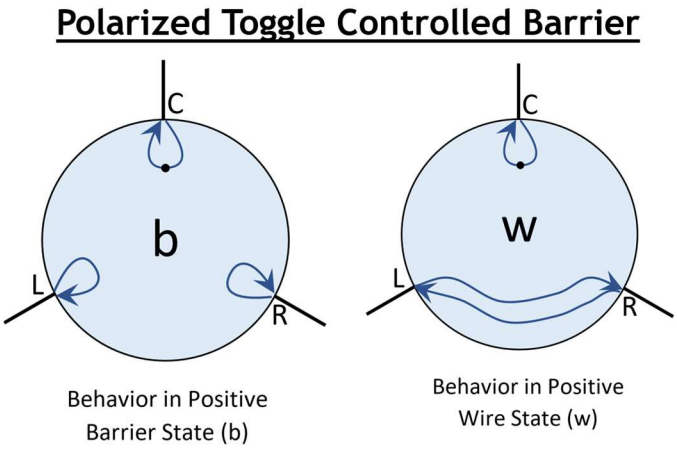

Fig. 3. The Polarized Toggle Controlled Barrier (PTCB) extends the ordinary unipolar Toggle Control Barrier (TCB) described in [6] and Fig. 1 by taking on opposite state behaviors for oppositely-polarized fluxons that hit the L/R channel ports.

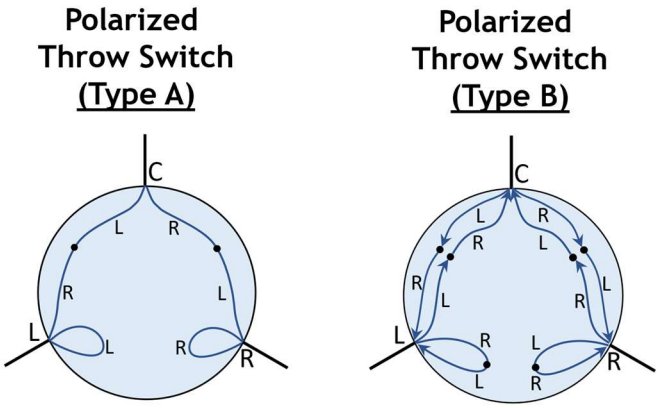

Fig. 4. Two variations of a behavior called Polarized Throw Switch (PTS) which routes fluxons from the central port C to either the L or R arm port depending on the device's state (also called L or R). The "Type A" behavior (left) does not change its state when a fluxon bounces off one of the L/R arm ports, whereas the "Type B" behavior (right) does. Labels on the arrows illustrate the state (L/R) during the given transition. Arrow-less lines denote that transitions are allowed in both directions.

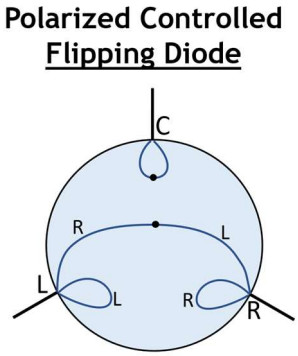

Fig. 5. A Flipping Diode (FD) is a 2-port device that passes fluxons between its L/R channel ports in one direction, and reflects them in the other direction, and toggles its state when they pass through. A Controlled Flipping diode (CFD) adds a 3rd port C that also toggles the state when a fluxon reflects off of it. A Polarized Controlled Flipping Diode (PCFD) differs from regular unpolarized CFD behavior just in that the role of the two states is interchanged for negatively-polarized fluxons hitting the L/R channel ports.

oppositely polarized storage cells.) Due to flux conservation, the I/O fluxon's polarity remains unchanged by an interaction with such a device. All of the diagrams illustrate functional behaviors for the case of a positively polarized ($+1\Phi_0$) fluxon only. Due to $\mathcal{F}$-symmetry, the behavior for a negatively polarized ($-1\Phi_0$) fluxon is the same as that shown except that the roles of the two states are interchanged.

Proper BARCS-style (reactive) circuits implementing these functions have not yet been found, but the search continues.

VI. Classification Tool

The task of enumerating and classifying possible BARCS functions of different types is being facilitated by a simple custom software tool called `barc`, written in Python for this purpose. This tool simply (1) enumerates all reversible transition functions of a given type, (2) groups them into symmetry/equivalence classes, where the members of each such class transform to each other via combinations of D, S, R_P transforms, and (3) prints out a listing of the equivalence classes and a representative function in each class. Table I summarizes the overall structure of the program, with modules grouped into layers reflecting dependencies. Table II summarizes results for the largest category of devices studied to date, mentioned above, *i.e.*, the 600 nontrivial functions for 3-port, 2-state, flux-conserving, flux-neutral elements. Fig. 6 shows sample output from `barc` describing one of the 45 equivalence classes (here describing its behavior for positive fluxons) in this category. Table III summarizes results for the 3-port, 2-state, flux-conserving, flux-polarized elements.

Other cases that had been previously analyzed by hand were also verified by the `barc` program, including those for 1- and 2-port devices with two flux-polarized or flux-neutral states. In the 2-port flux-polarized case, there are 4 equivalence groups of size 1 (fully self-symmetric) and 3 equivalence groups of size 2 (elements having dual representations). In the 2-port flux-neutral case, there are 3 equivalence groups of size 2 and 1 equivalence group of size 8—this one is an element that we call the *asymmetric polarized flipping diode* APFD or *selectable barrier* SB which has minimal self-symmetry; the APFD and SB behaviors are $\mathcal{D}$-duals to each other.

VII. Conclusion

Some next steps planned for this particular line of work are to more fully document the results of the classification effort, as well as to continue our investigations regarding implementability of the elements, with assistance from the circuit-discovery tool discussed in [8], which is still in development. Components suitable for consideration include inductors, mutual inductances, capacitors, unshunted Josephson junctions (both regular and π junctions), and other types of reactive superconducting devices that have been proposed. In the process of searching for element implementations, we might discover that implementable behaviors must obey additional symmetries, reducing the number of behavioral elements that we need to consider. Finally, we hope to discover a new universal circuit construction utilizing implemented elements, which can then serve as a basis for exploring architectural implementations for more complex reversible functional behaviors.

```
Symmetry group #38 has 6 functions:
    Function #155.
    Function #340.
    Function #481.
    Function #285.
    Function #365.
    Function #185.

Example: Function #155 = [1]*3(L,R):
    1(L) -> (R)2
    1(R) -> (L)3
    2(L) -> (R)1
    2(R) -> (R)3
    3(L) -> (L)2
    3(R) -> (L)1

Function #155 has the following symmetry properties:
    It is D-dual to function #481
    It is S-dual to function #481
    It is E(1,2)-dual to function #340
    It is E(1,3)-dual to function #185
    It is E(2,3)-dual to function #481
    It R(-1)-transforms to function #365
    It R(1)-transforms to function #285
```

Fig. 6. Example description of an equivalence class as output by `barc`.

TABLE I. Modules in the barc Tool

Layer	Module Names & Descriptions
4	**barc** (top-level program)
3	**deviceType** – Classification of devices with given dimensions.
2	**deviceFunction** – Device with a specific transition function.
1	**pulseAlphabet** – Sets of pulse types. **symmetryGroup** – Equivalence class of device functions. **transitionFunction** – Bijective map, input→output syndromes.
0	**characterClass** – Defines a type of signal characters. **deviceDimensions** – Defines size parameters of devices. **dictPermuter** – Used to enumerate transition functions. **pulseType** – Identifies a specific type of pulse. **signalCharacter** – Identifies I/O event type (pulse type & port). **state** – Identifies an internal state of a device. **stateSet** – Identifies a set of accessible device states. **symmetryTransform** – Invertibly transforms a device function. **syndrome** – An initial or final condition for a device transition. **utilities** – Defines some low-level utility functions.

TABLE II. Result Summary for 3-port Flux-Neutral Devices

Equivalence Class Size:	**2**	**4**	**6**	**12**	**24**	
Self-Symmetry Group Size:	**12**	**6**	**4**	**2**	**1**	**Tot.**
No. of Equivalence Classes:	1	1	9	23	11	**45**
Total number of Functions:	2	4	54	276	264	**600**

TABLE III. Result Summary for 3-port Flux-Polarized Devices

Equivalence Class Size:	**1**	**2**	**3**	**6**	**12**	
Self-Symmetry Group Size:	**12**	**6**	**4**	**2**	**1**	**Tot.**
No. of Equivalence Classes:	1	4	6	24	4	**39**
Total number of Functions:	1	8	18	144	48	**219**

Acknowledgment

The authors would like to thank Frank Allen, Rudro Biswas, Terence Bretz-Sullivan, Han Cai, Ryan Clarke, Oscar Corces, Erik DeBenedictis, Deepnarayan Gupta, James Hardy, Rishabh Khare, Fadi Matloob, Nancy Missert, Marshal Nachreiner, Kevin Osborn, Samuel Perlman, Donovan Sharp, Jesus Sosa, Karpur Shukla, Dewan Woods and Liuqi Yu for helpful collaborative efforts over the course of this line of work.

References

[1] M.P. Frank, "Physical Foundations of Landauer's Principle," in Reversible Computation 2018, LNCS vol. 11106, J. Kari and I. Ulidowski, Eds. Cham: Springer, 2018, pp. 3–33.

[2] M.P. Frank, R.W. Brocato, B.D. Tierney, N.A. Missert, and A.H. Hsia, "Reversible Computing with Fast, Fully Static, Fully Adiabatic CMOS," in Int'l. Conf. on Rebooting Computing 2020, IEEE, 2020, pp. 1–8.

[3] N. Takeuchi, T. Yamae, C.L. Ayala, H. Suzuki, and N. Yoshikawa, "Adiabatic Quantum-Flux-Parametron: A Tutorial Review," IEICE Trans. Elec., art. 2021SEP0003, 2022.

[4] M.P. Frank, R.W. Brocato, T.M. Conte, A.H. Hsia, A. Jain, N.A. Missert, K. Shukla, and B.D. Tierney, "Special Session: Exploring the Ultimate Limits of Adiabatic Circuits," in 38th Int'l. Conf. on Computer Design 2020, IEEE, 2020, pp. 21–24.

[5] E. Fredkin and T. Toffoli, "Conservative logic." Int. J. Theor. Phys., vol. 21, no. 3, pp. 219–253, 1982.

[6] M.P. Frank, "Asynchronous ballistic reversible computing," in Int'l. Conf. on Rebooting Computing 2017, IEEE, 2017, pp. 1–8.

[7] M.P. Frank, R.M. Lewis, N.A. Missert, M.A. Wolak, and M.D. Henry, "Asynchronous Ballistic Reversible Fluxon Logic." IEEE Trans. Appl. Supercond., vol. 29, no. 5, pp. 1–7, 2019.

[8] M.P. Frank, R.M. Lewis, N.A. Missert, M.D. Henry, M.A. Wolak, and E.P. DeBenedictis, "Semi-Automated Design of Functional Elements for a New Approach to Digital Superconducting Electronics: Methodology and Preliminary Results," in Int'l. Supercond. Elec. Conf. 2019, IEEE, 2019, pp. 1–6.

[9] M.P. Frank, "Foundations of Generalized Reversible Computing," in Reversible Computation 2017, LNCS vol. 10301, I Phillips and H. Rahaman, Eds., Cham: Springer, 2017, pp. 19–34.

[10] M.P. Frank, and E. DeBenedictis, "Ballistic Reversible Superconducting Memory Element." U.S. Patent no. 11,289,156 B2, 2022.

[11] K.D. Osborn and W. Wustmann, "Ballistic Reversible Gates Matched to Bit Storage: Plans for an Efficient CNOT Gate Using Fluxons." Reversible Computation 2018, LNCS vol. 11106, J. Kari and I. Ulidowski, Eds. Cham: Springer, 2018, pp. 189–204.

[12] K.D. Osborn and W. Wustmann, "Asynchronous Reversible Computing Unveiled Using Ballistic Shift Registers." Preprint arXiv:2201.12999 [cond-mat.supr-con], 2022.