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Systematic Investigation of SIR Testing Phenomena with Constant Capacitance Interdigitated Comb Patterns

Matthew A. Kottwitz,† Bobby G. Glidwell III,‡ Samuel Z. Grosso,† Mark T. McMeen,‡ Mike Bixenman,‡ J. Elliot Fowler†

†Sandia National Laboratories, Albuquerque, New Mexico 87185, United States

‡Magnalytix, Nashville, Tennessee 37211, United States

Abstract Surface insulation resistance (SIR) testing serves as the standard method for quantitative determination of cleanliness and prediction of service life or failure mechanisms of printed boards or assemblies, commonly through a pass/fail threshold paradigm. To move beyond a binary system of evaluation towards greater insight into the underlying phenomena manifested in the observed SIR response, we demonstrate an approach that utilizes interdigitated comb (IDC) patterns spanning a range of design specifications while maintaining a constant capacitance value. Twelve different 10 pF IDC patterns were purchased from an external board vendor and measured via SIR. The average response of each IDC pattern design maximally varied by approximately 2 pA over 22 hours of SIR testing under 25 °C and 40% relative humidity. The consistency is observed values, as well as the trends in the data, suggest that this platform is a good approach for future work that seeks to induce failure and correlate modes to unique SIR features.

Introduction

Surface insulation resistance (SIR) testing serves as the standard method for quantitative determination of the deleterious effects of fabrication and processing, quality conformation, and the prediction of service life and failure mechanisms of printed boards or assemblies.[1] Industrial usage of this technique commonly relies upon a pass/fail threshold value of resistance for a board or assembly. One common mode of failure involves leakage current and is typically caused by electrochemical migration, itself a multistep process consisting of path formation, electrodissolution, ion transport, electrodeposition, and filament growth.[2-4] This process is influenced by a multivariate space consisting of test pattern design, materials choices, and testing environment.[5] This work demonstrates the exploration of the test pattern design space, while holding materials choices and testing environment constant, as a path towards an understanding of how the underlying physical phenomena of an SIR test manifest in the observed data.

Broadly, test patterns for SIR consist of either interdigitated comb (IDC) patterns or representative samples of a printed circuit assembly.[1,6] IDC patterns serve as the more straightforward starting approach for modeling considerations, especially given their utilization in MEMS devices and sensors arising from the fact that they are functionally capacitors.[7] From the macroscopic perspective, capacitors of a given capacitance value are largely interchangeable regardless of their design details. For the purposes of SIR, however, these design considerations become increasingly relevant as the electric field generated during testing and the distance between electrodes combine to influence the rate of electrochemical migration.[8] To investigate this relationship and others and the impact on the measured SIR response, this work investigates a set of IDC patterns with a range of design specifications with constant capacitance.

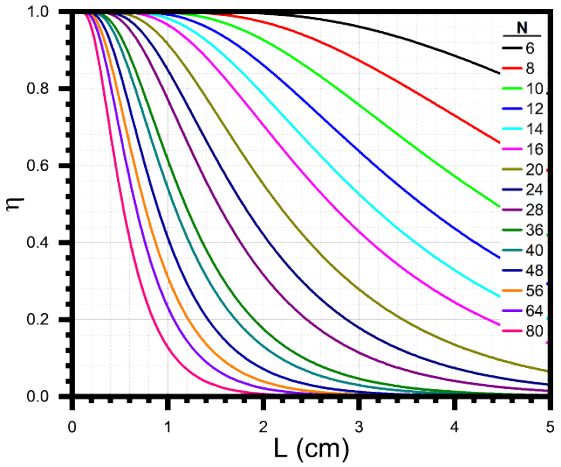

Figure 1. Relationship between the number of fingers (N), overlap length (L), and metallization ratio (η) required for a 10 pF IDC pattern.

Results and Discussion

Figure 1 displays the computed relationship between N, L, and η for an IDC pattern with a capacitance of 10 pF given the assumptions

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detailed above. From this parameter space we selected twelve patterns split between three test card designs as summarized in Table 1. The computed capacitance of each pattern deviates slightly from the targeted 10 pF as a result of self-imposed rounding of the design specifications.

Table 1. Selected IDC pattern design specifications

ID	N	L (cm)	η	W (μm)	G (μm)	C (pF)
1-U1	20	2.15	0.5	200	200	9.99
1-U2	40	1.06	0.5	200	200	9.99
1-U3	60	0.70	0.5	200	200	9.95
1-U4	80	0.53	0.5	200	200	10.07
2-U1	34	1.00	0.67	200	100	10.21
2-U2	42	1.00	0.5	200	200	9.91
2-U3	54	1.00	0.33	200	400	10.00
2-U4	68	1.00	0.2	200	800	10.00
3-U1	40	1.06	0.5	100	100	9.99
3-U2	40	1.06	0.5	200	200	9.99
3-U3	40	1.06	0.5	400	400	9.99
3-U4	40	1.06	0.5	800	800	9.99

Analysis of the test cards as received reveals the deviation between the design specification and the results of the external vendor's fabrication process as shown in Figure 2. Average per pattern finger widths (W) and gap widths (G) respectively ranging 14-36 μm narrower and 3-21 μm wider suggest that an over-etching of the copper laminate occurred. The increased range of the width and gap measurements for 2-U4, as well as 2-U3 and 3-U4 to a lesser degree, are likely attributable to errors in edge detection within the software used to capture the measurements. While the error in overlap length (L) is much larger in absolute terms (ranging 88-166 μm longer on average with 1-U1 an outlier at 288 μm longer), these deviations are smaller in relative terms and would therefore be expected to have less of an impact on the capacitance of the IDC patterns. Alternative fabrication methods could more accurately produce the given design specifications,[9] but this approach serves to capture the variability and limitations present in current industrial production.

Measurement of the capacitance of the twelve patterns revealed a significant deviation from the expected value of 10 pF as summarized in Figure 3. The computed capacitance values

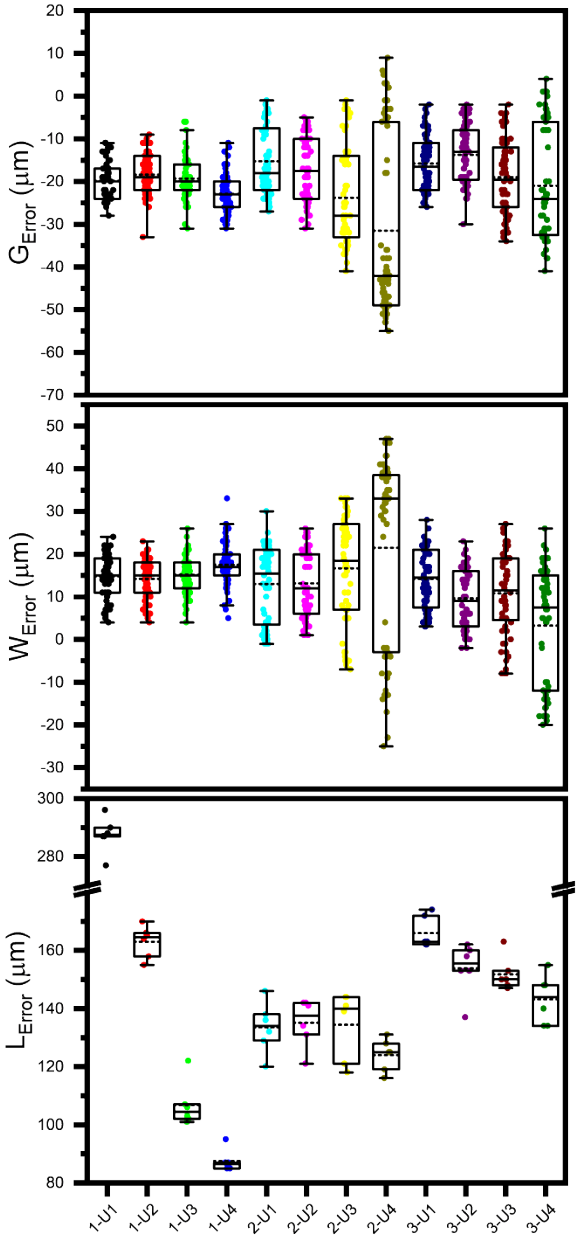

Figure 2. Measured deviation from the design specifications for finger width (W), gap width (G), and overlap length (L).

rely upon the assumption that the copper fingers are sufficiently thin relative to the in-plane dimensions. Finger thickness for the received test cards, however, was measured at roughly 40 μm on average or 5% of the largest width and gap design specifications. Determination of pattern capacitance at a single frequency (1 kHz) contributes to the uncertainty in the measurement and future work will include a more rigorous approach.[10] Environmental conditions and possible variation in the FR-4 substrate relative

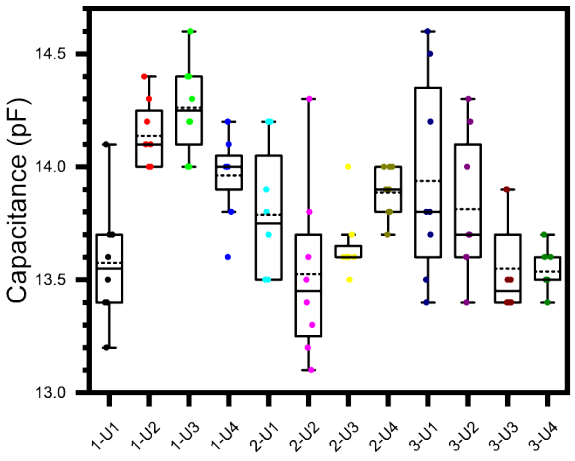

Figure 3. Measured capacitance values for the boards prior to SIR test testing.

permittivity as a result of the exact fiberglass to epoxy ratio may also play a role in the observed deviation.

The results of SIR testing, under nonstandard, relatively benign conditions of 25 °C and 40% relative humidity, are shown in Figure 4 for each of the patterns. Measured current values for all test patterns spread across three chambers and two separate days of testing lie within an 18 pA range. Each individual pattern follows a similar trend of decreasing current during the first 4 hours of testing followed by a steady-state period lasting for roughly 12 hours. Most of the channels display a peak in the 16-20 hour time window, though there is some variation in the exact time of occurrence that has not been correlated to a particular chamber or day of testing. Averaging the data in 2 minute windows for each of the twelve patterns, as shown in Figure 5, further illustrates the consistent SIR response across the variation in design parameters with total spread at roughly 2 pA for any given time. The initial decrease within the first 6 minutes likely corresponds to the tail end of the transient response typical of RC circuits. Pending further investigation, we predict that the steady decrease over the next 4 hours may correspond to the movement of surface ionic species under the electric field between neighboring fingers. It would then follow that the subsequent steady-state period corresponds to an equilibrium between ionic species moving under the electric field and those diffusing in the opposite direction due to the formation of a concentration gradient. We do not yet have proposals as to phenomena that may correspond to the peak that occurs during the steady decreasing period at the 1 hour mark or the peak(s) that occur during the 16-20 hour period. It appears that there may be a return to a steady-state, albeit at a higher current, during the last 2 hours, but further investigation is needed.

Conclusion

This work has demonstrated that capacitance largely determines the SIR response under benign conditions of IDC patterns across the design space explored. Subsequent work will expose these patterns to the traditional SIR environmental conditions to promote electrochemical migration and induce failure. We expect failure mechanisms to differ with the design parameters in a systematic fashion.

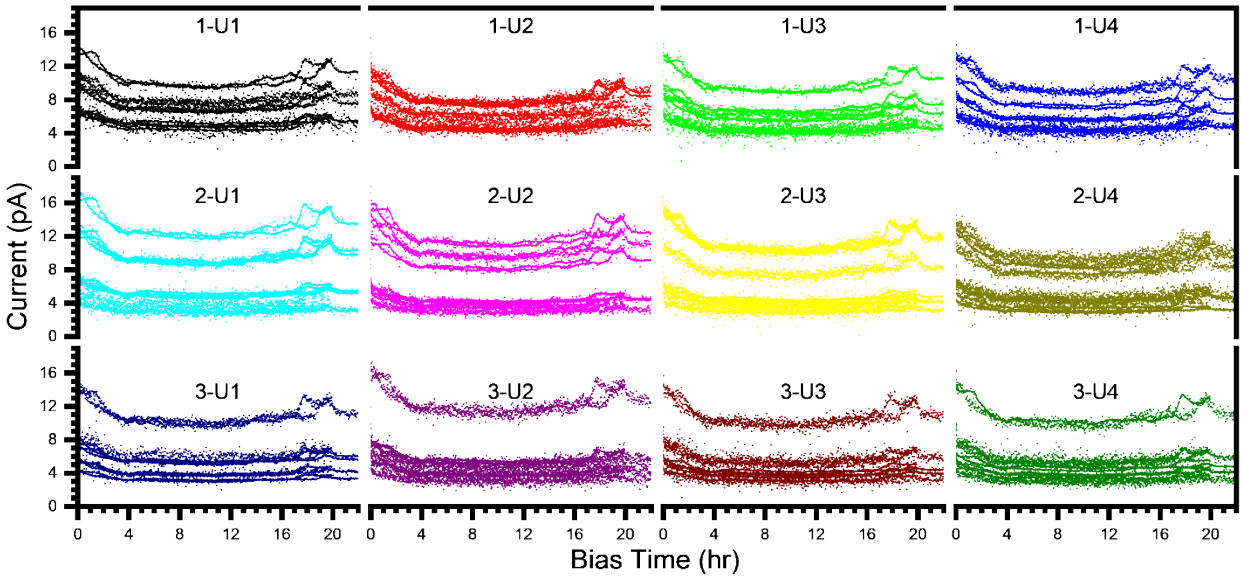

Figure 4. Measured current values during SIR testing for the twelve IDC patterns.

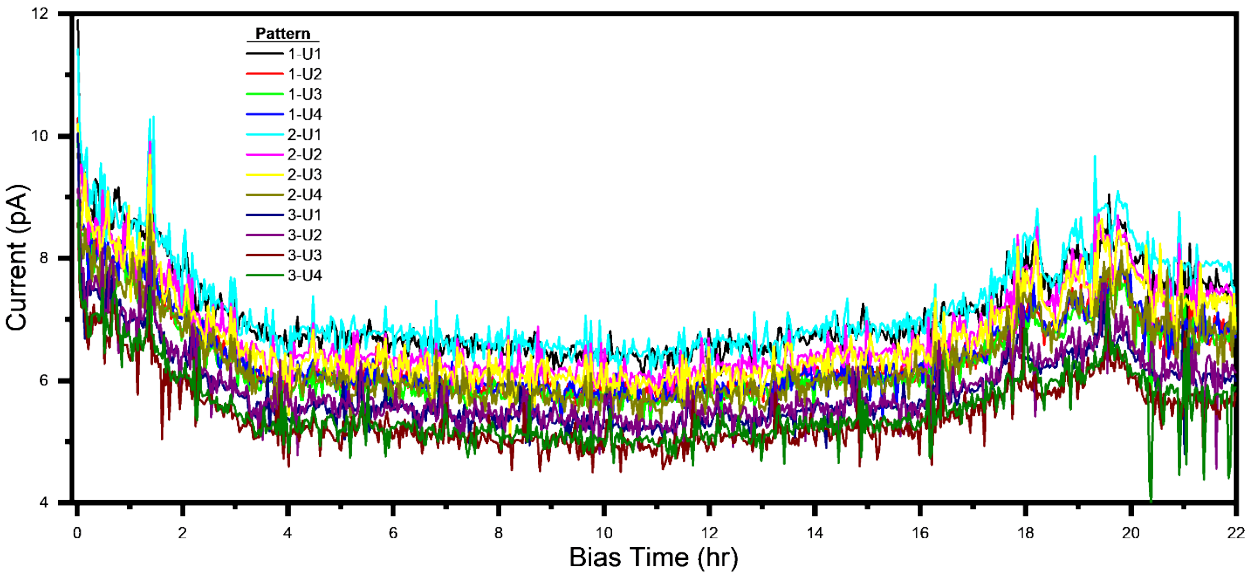

Figure 5. Measured current values during SIR testing for the twelve IDC patterns averaged in 2 minute windows.

Correlation of these failure mechanisms with features in SIR response will elucidate the corresponding phenomena and move SIR towards a technique applicable to materials and process characterization.

Methods

Design and Fabrication

As demonstrated by Igreja and Dias,[7] conformal mapping and partial capacitance techniques generate relatively simple expressions for the computation of the capacitance of planar IDCs. With the assumption that (a) the IDC pattern is sufficiently planar, (b) the FR-4 substrate has a relative permittivity of 4.4 and may be approximated as infinitely thick, and (c) the top layer consists of an infinitely thick layer of air, we constructed plots relating the number of fingers (N), the overlap length (L), and the metallization ratio (η) for capacitance values of 1, 10, and 100 pF. The parameter space for IDCs with capacitance of 10 pF was found to be the most conducive to arranging multiple (4) IDCs on a single test card given the size constraint imposed by the standard test card dimensions and the finger width (W) and gap (G) constraint imposed by chemical etching of copper laminate at reasonable cost. From this parameter space we chose twelve IDC patterns split between three test card designs that either (a) held η constant while varying N and L, (b) held L constant while varying N and η, or (c) held N, L, and η constant while varying W and G together.

An external vendor fabricated forty test cards of each of the three designs by chemically etching half-ounce copper laminated FR-4 boards followed by electroless nickel immersion gold (ENIG) plating of the contact pads and spraying of the copper traces with organic solderability preservative (OSP).

Validation

A sampling of the test cards (six per design) as received was imaged on a Keyence VHX-7000 optical microscope. For each IDC pattern ten measurements of W and G and one measurement of L were made with edge detection enabled in the accompanying software.

Profiles of the IDC patterns on the same sampling of boards were taken on a Keyence VK-X150 confocal microscope. A least squares plane was subtracted from the raw height maps and the height data binned to obtain height distribution plots.

Following sonication in isopropyl alcohol to remove the OSP and drying with air, each of the IDC patterns on the test cards to be tested with SIR was measured with an Agilent E4980A Precision LCR Meter operated at 1 kHz to obtain the capacitance.

SIR

For each of the three designs, sixteen test cards were systematically distributed across three Magnalytix OE-300 test systems and two days of testing. Environmental conditions in the chambers were set to 25 °C and 40% relative humidity with the test cards given one hour to equilibrate prior to testing. Once the testing began, all four channels on the eight test cards in a given chamber were placed under a 5 V forward DC bias. Every two minutes a testing cycle was

initiated wherein the 32 channels were sequentially removed from the forward bias and placed under a 5 V reverse DC bias to measure the current. The testing ran for 20 and 22 hours on the two days of testing.

Following SIR testing, the elapsed time associated with each two-minute testing cycle was converted to a time under forward bias for each channel with an estimated individual measurement time of 2.5 seconds. Data from the second day of one of the chambers was excluded from analysis due to a technical issue. Additionally, data from two test cards from the first day of the same chamber was excluded due to abnormal readings likely attributable to a cabling issue.

This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government

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