SAND2022-15812C

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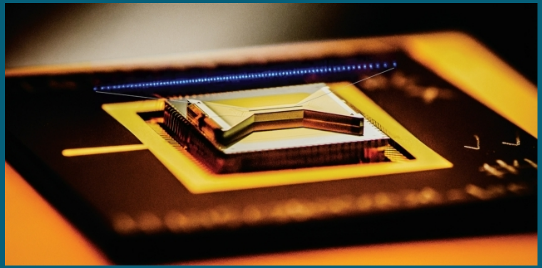
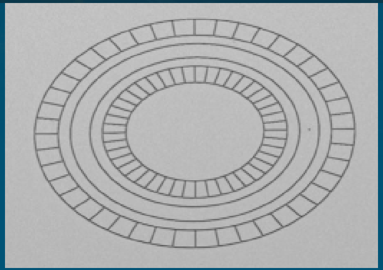
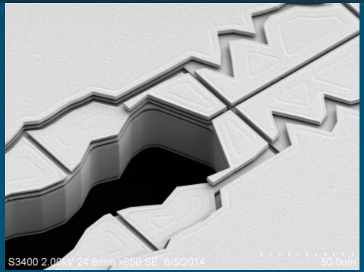
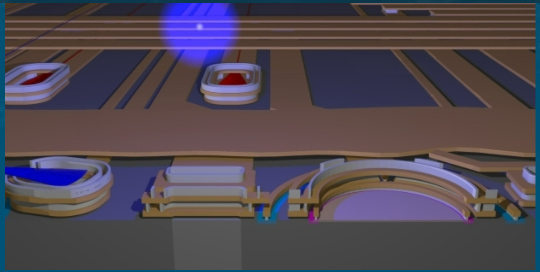
Junction transport for trapped-ion quantum systems









For Dr. Thomas Monz

November 2022

Dan Stick

U.S. DEPARTMENT OF ENERGY NNSA National Nuclear Security Administration

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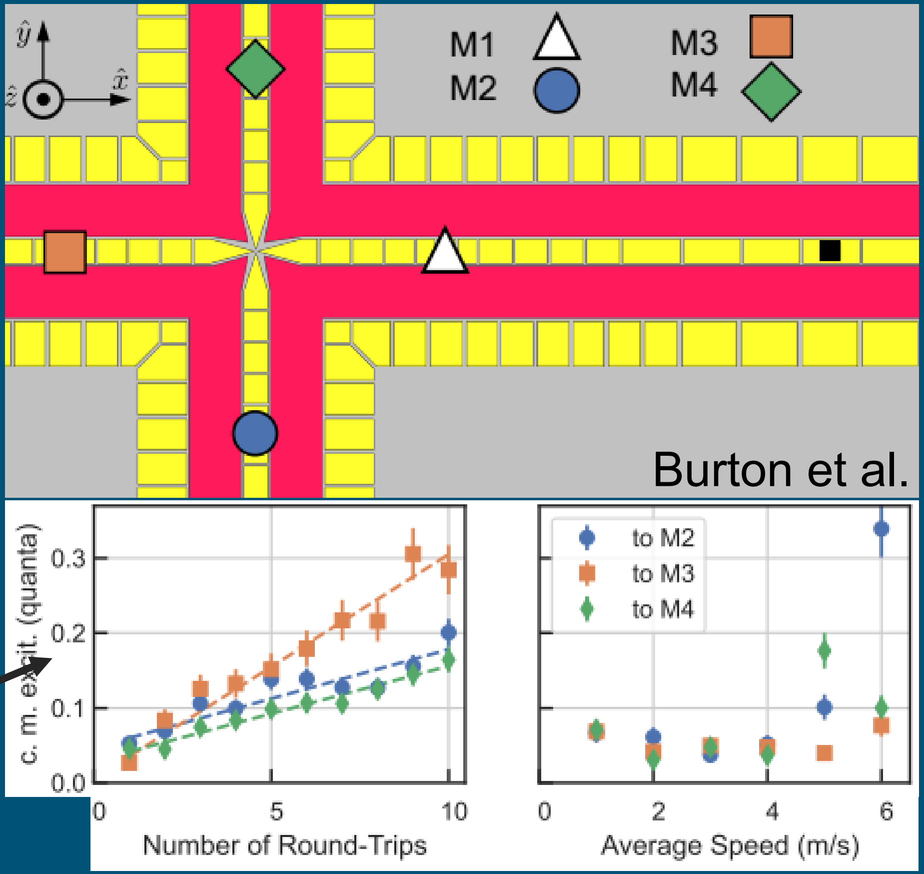
Junction transport– Motivation, Challenges, Results

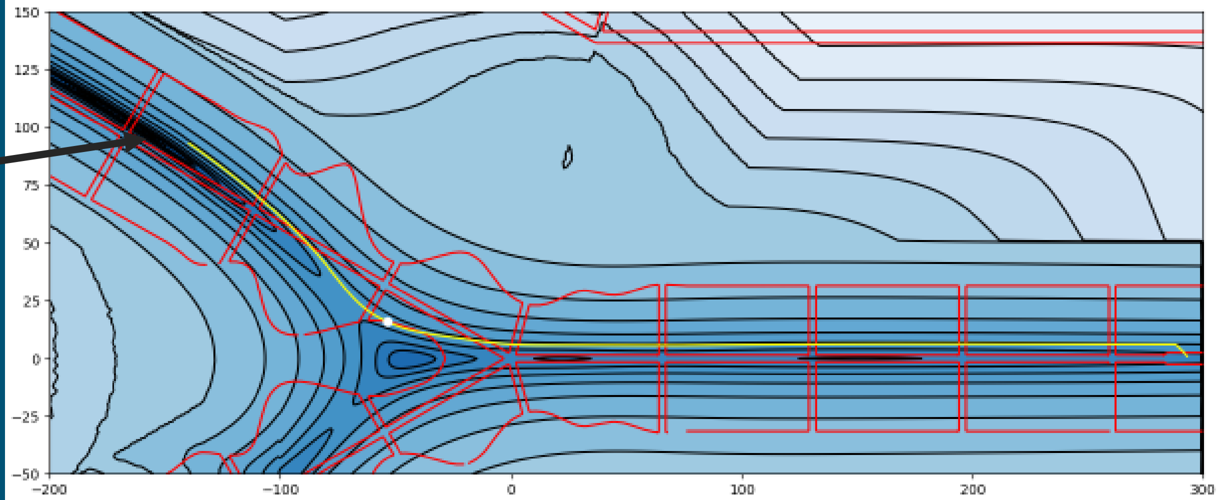
- A 2D array of ions is a promising geometry for a trapped-ion quantum computing architecture
  - often called the quantum charge coupled device[1] (QCCD)
  - it maps naturally to the connectivity needs for quantum error correction
  - junctions are fundamental building blocks for this architecture as they connect different linear sections
- What are the challenges and state-of-the-art results?
  - junctions inevitably create pseudopotential bumps and pits that the ion must go over or around at high speeds with low excitation
  - recent research[2] has demonstrated impressive low excitation transport by pushing ions off the RF null in an X junction



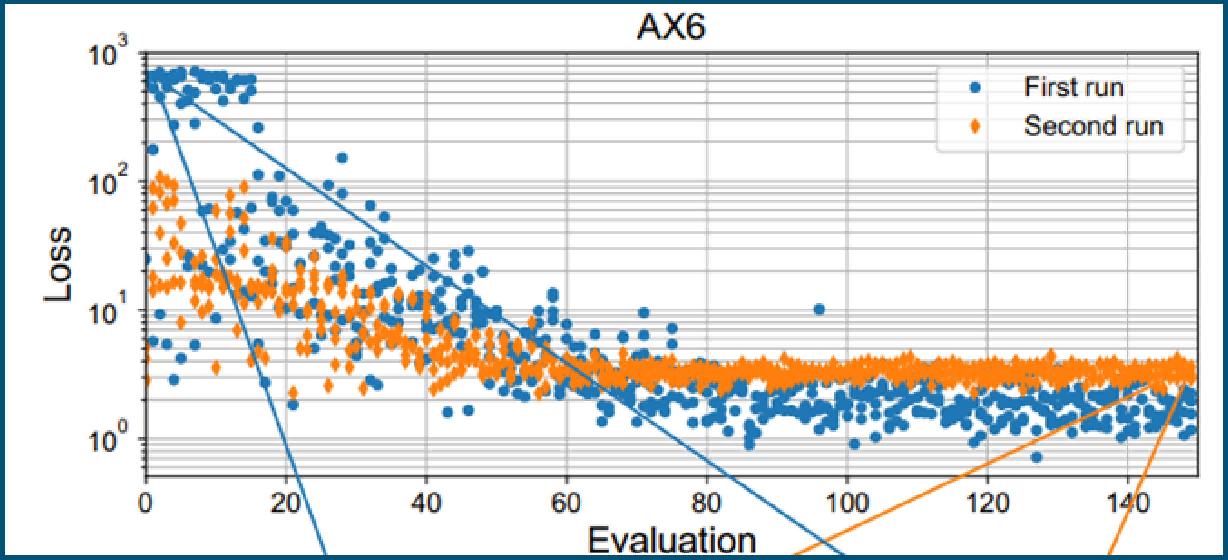
1. Kielpinski, et al. "Architecture for a large-scale ion-trap quantum computer". Nature 417, 709–711 (2002)
2. Burton, et al. "Transport of multispecies ion crystals through a junction in an RF Paul trap".

Challenges with junction performance

- Sandia is using a Y junction to enable a hexagonal array architecture
  - same pseudo-potential bumps and pits
  - We employ a comparable strategy of pushing the ion off the RF null to limit pseudopotential variation (yellow line).



- Demonstrated shuttling back and forth in the "Roadrunner" trap (QSCOUT) at 5 m/s and one way at 50 m/s. Working on reducing motional excitation.

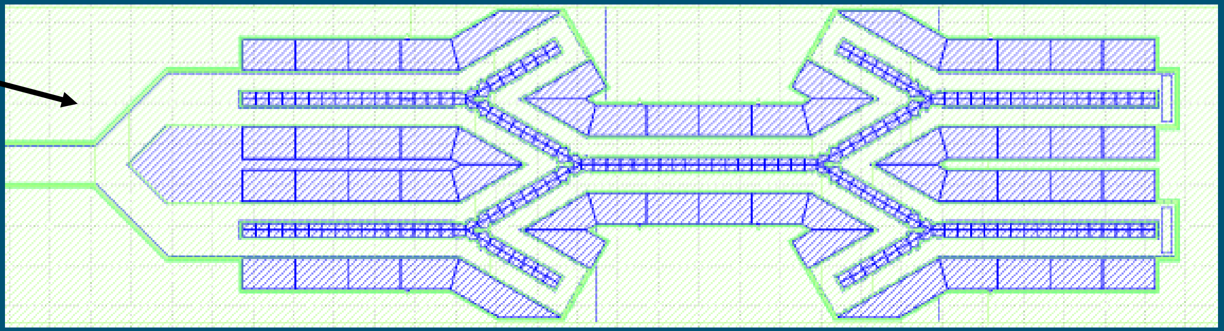


- Will use closed-loop optimization (demonstrated on linear trap[1]) to tune out experimental imperfections (e.g.

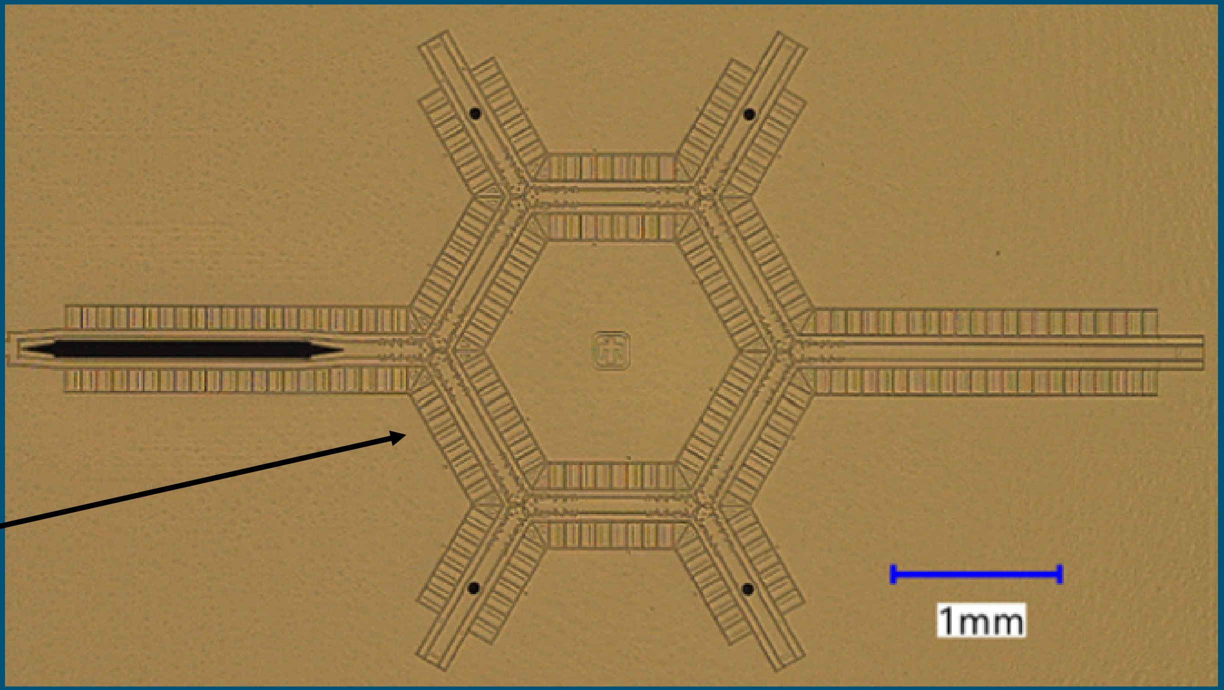
1. Sterk, *et al.* "Closed-loop optimization of fast trapped-ion shuttling with sub-quanta excitation." npj Quantum Information 8

Challenges and approaches to junction scaling

- Full version of trap is currently in fabrication
  - 6 junctions to support storing up to 200 ions (ion chains in outer zones + central interaction zone)



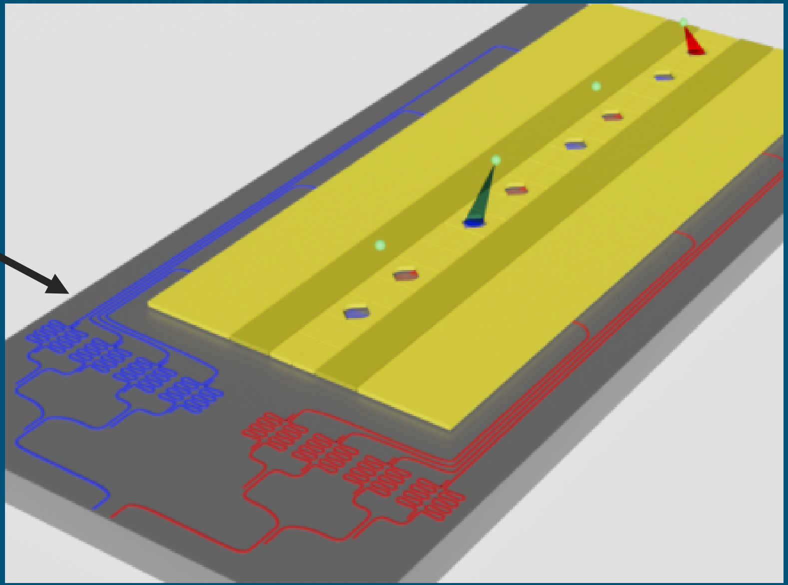
- Challenge 1: RF capacitance and power dissipation
  - Reduced the RF capacitance by 4× by raising the RF electrodes above the control electrode layer and perforating the dielectric.
- Challenge 2: I/O and routing density
  - 316 control electrodes, can be independent or tied together
  - Multiple metal levels needed to connect islanded electrodes.
  - Geometric consistency inherent with lithographic fabrication allows tied junction electrodes to operate with the same voltages (showed that ions can be shuttled around hexagon with same voltages)[1]

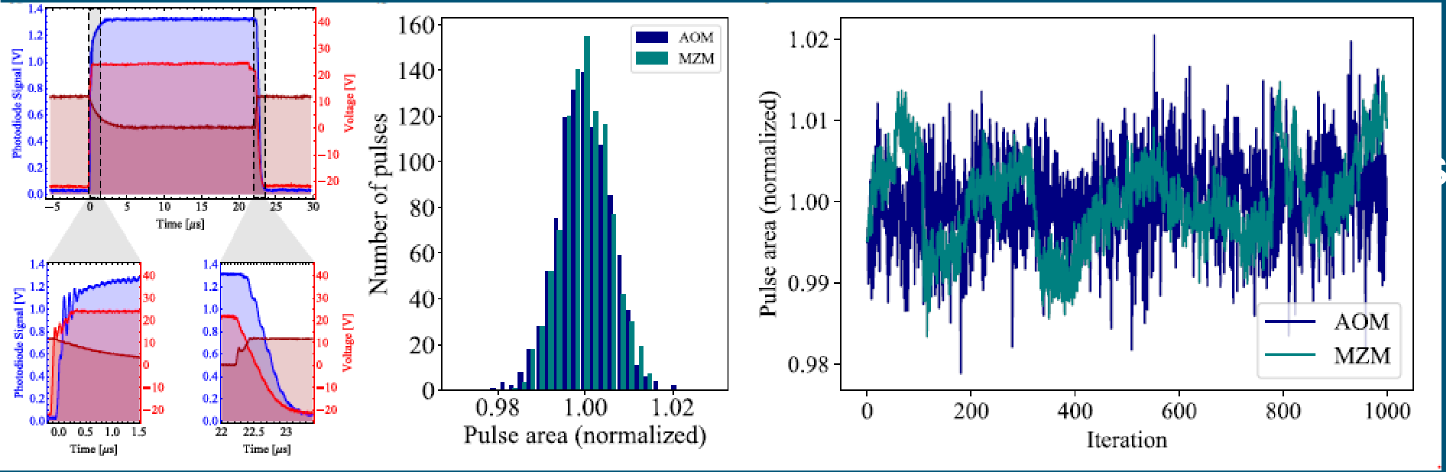


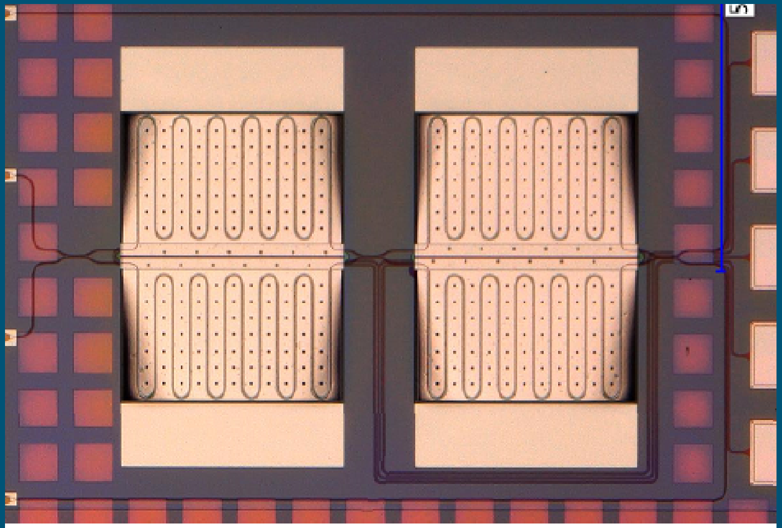
1. Blain, *et al.* "Hybrid MEMS-CMOS ion traps for NISQ computing." QST 6, 034011 (2021)

Optical I/O challenges and modulators

- I/O density is a challenge in traps for both electrical and optical signals
- On-chip modulators can mitigate the optical challenge through fanout
- Sandia fabricated and tested[1] CMOS (and ion trap) compatible piezo-activated MZI optical modulators (but not yet integrated with trap)
  - tested amplitude modulation, in future will test phase modulation
- <0.5 μs turn on/off time, ~1.5 dB loss per MZI, 38.7 dB extinction rat
- Si
  (al







1. Hogle, *et al.* “High-fidelity trapped-ion qubit operations with scalable photonic modulators.” arXiv:2210.14368v1 (2022)