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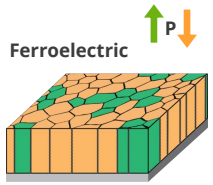
Sandia National Laboratories

Emerging Ferroelectric Materials for Microelectronic Technologies



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U.S. DEPARTMENT OF ENERGY | National Nuclear Security Administration

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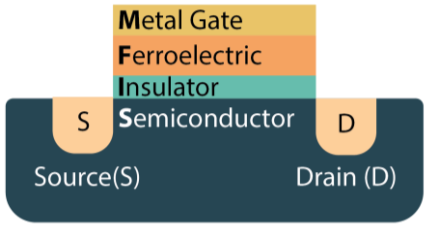
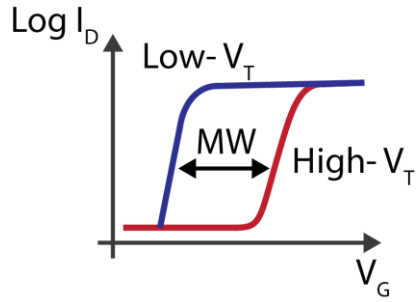
Ferroelectric Materials Revolution & Device Opportunities

Robust ferroelectricity recently demonstrated with CMOS compatible materials at previously unobtainable length scales (i.e., 10s of nm)

Ferroelectric Field Effect Transistor

- Fully integrated ferroelectric memory on transistor



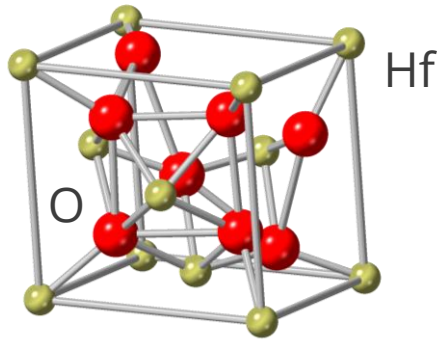


MW: Memory window
V_T: Threshold voltage
I_D: Drain current
V_G: Gate voltage

Ferroelectric Tunnel Junction

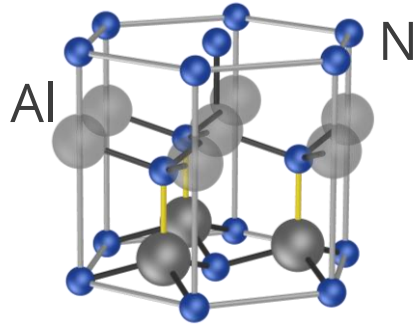
- Multi-resistance state device with 3D integration capability

Hafnia-Based



HfO_2, $Hf_{x-1}Zr_xO_2$, $Hf_{x-1}Si_xO_2$

AlN-Based

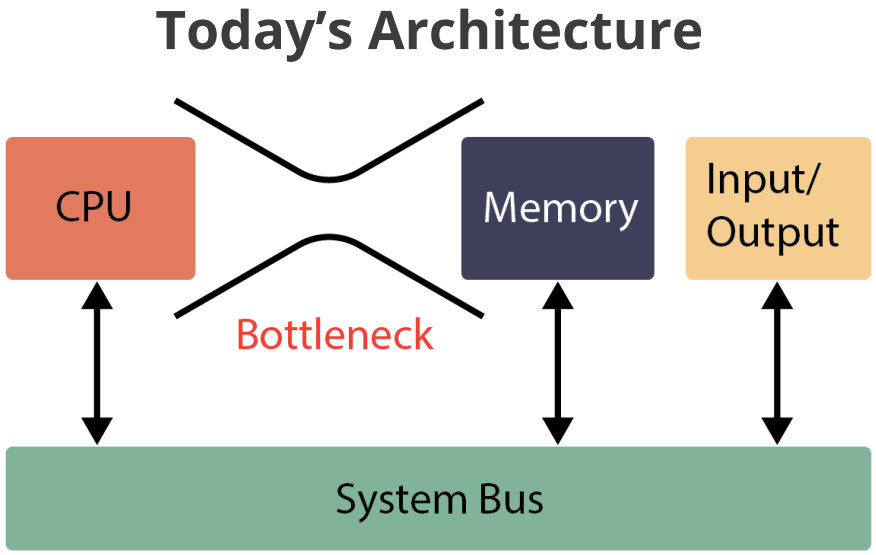


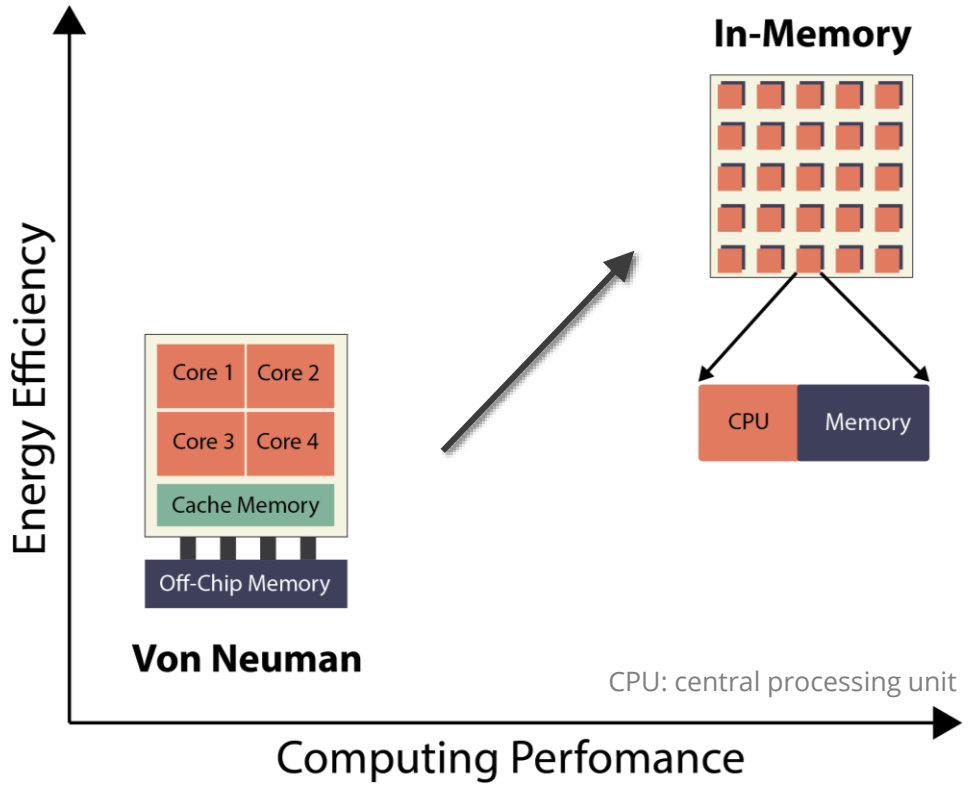
AlN, $Al_{1-x}Sc_xN$, $Al_{1-x}B_xN$

CMOS: complimentary metal oxide semiconductor

Ever-Increasing Computational Demand

- Demand for higher processing efficiency grows as data becomes the new ‘oil’
- Data communication between chips dominates speed and energy consumption
- In-memory computing architectures project to overcome today’s limitations





Enabling In-Memory Compute

- Non-volatile memory integration with CMOS enables higher processing efficiency
- Today's memory devices options are limited to MRAM, PCM, and ReRAM
- All options suffer from high write energy
- Emerging ferroelectrics enable potential efficient integrable memory devices

ReRAM: resistive random access memory, MRAM: magnetic random access memory, PCM: phase change memory

Metric	ReRAM	PCM	MRAM	Ferroelectric FTJ	Ferroelectric FeFET
Energy (fJ)	>10^4	10^5	>10^4	0.5	10
Cell Size (F^2) *F* is feature size	12	30	50	< 4	20
Speed (ns)	<10	50	<10	10	10
Endurance (cycles)	10^8	>10^9	>10^{15}	10^{11}	10^{11}
			BEOL		FEOL

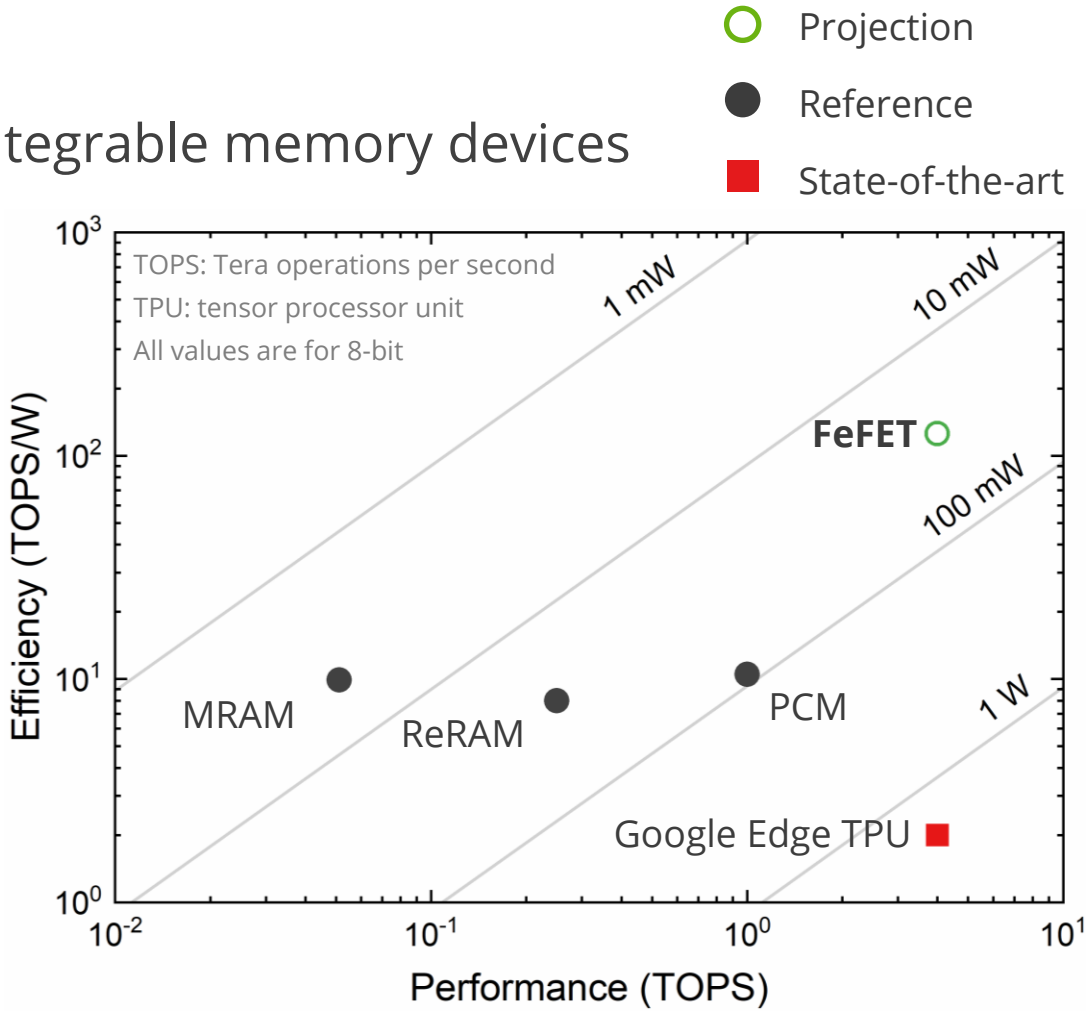


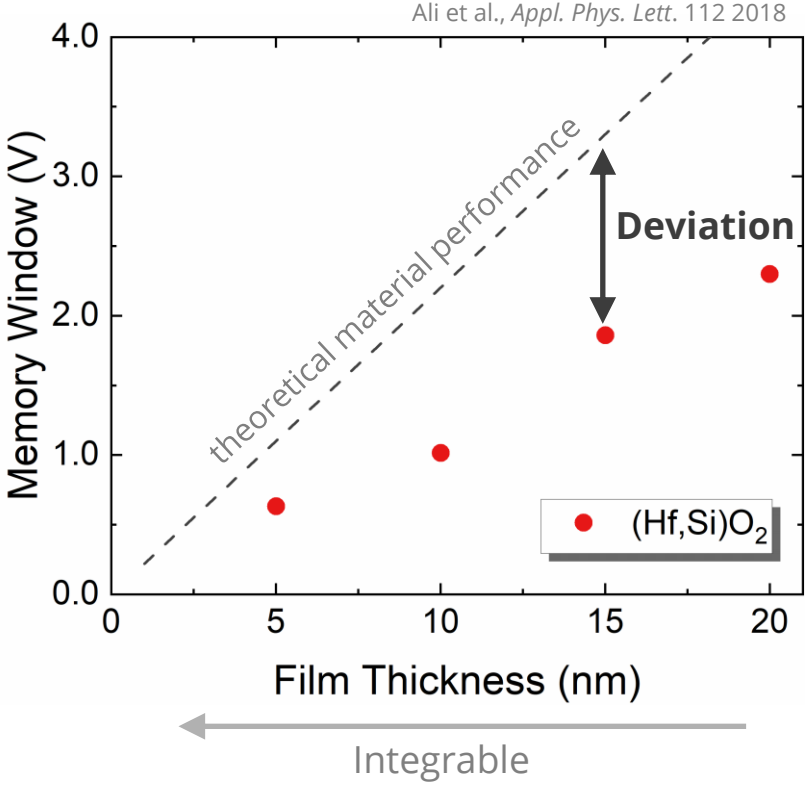
Table: Khan et al., *Nat. Electron.*, 3, 2020 Khosla & Sharma *Appl. Electron. Mater*. 3, 2021 Mikolajick et al., *Adv. Mater*. 2022

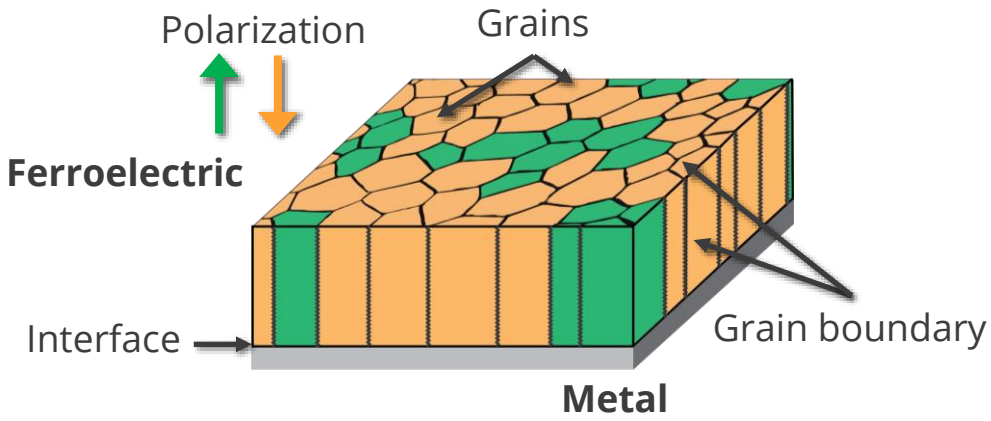
Figure: Wang et al., *IEEE TCAS-I*, 69, 11, 2022, Wan et al., *Nature*, 608, 2022, Khaddam-Aljameh et al., *IEEE J. Solid-State Circuits*, 57, 4, 2022, Xiao et al., *IEEE TCAS-I*, 69, 4, 2022

Ferroelectric Device Integration Challenges

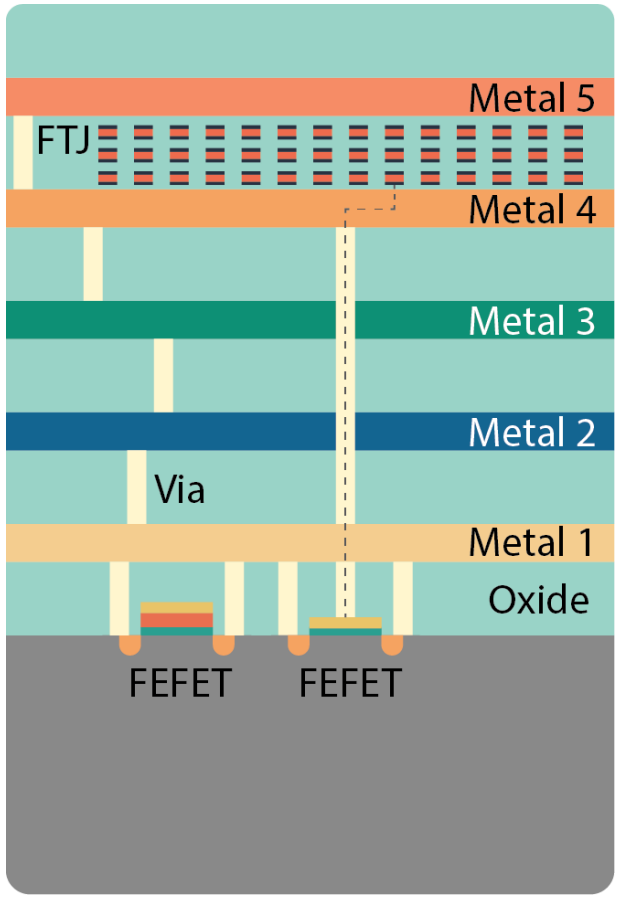
- Ferroelectrics material quality is affected by integration
- Defects introduced can alter polarization, fatigue, breakdown, and operating voltage
- Processing, temperature, interfaces, etc. introduce material defects

Ali et al., *Appl. Phys. Lett*. 112 2018





Integration with CMOS

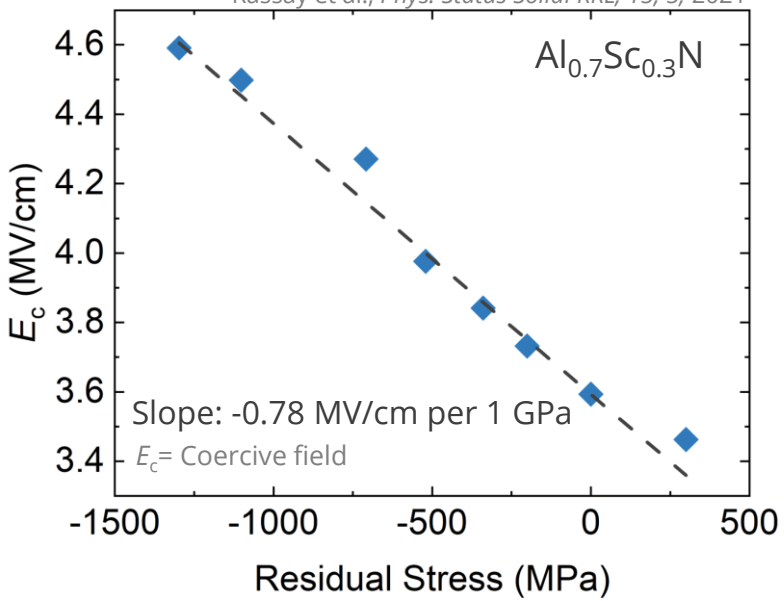


FeFET: ferroelectric field effect transistor
FTJ: ferroelectric tunnel junction

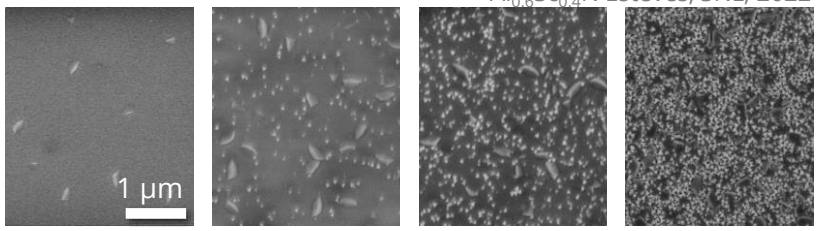
Fabrication Challenges

- Fabrication processing can introduce undesirable results
- Controlling material behavior often comes with tradeoffs

Rassay et al., *Phys. Status Solidi RRL, 15, 5,* 2021

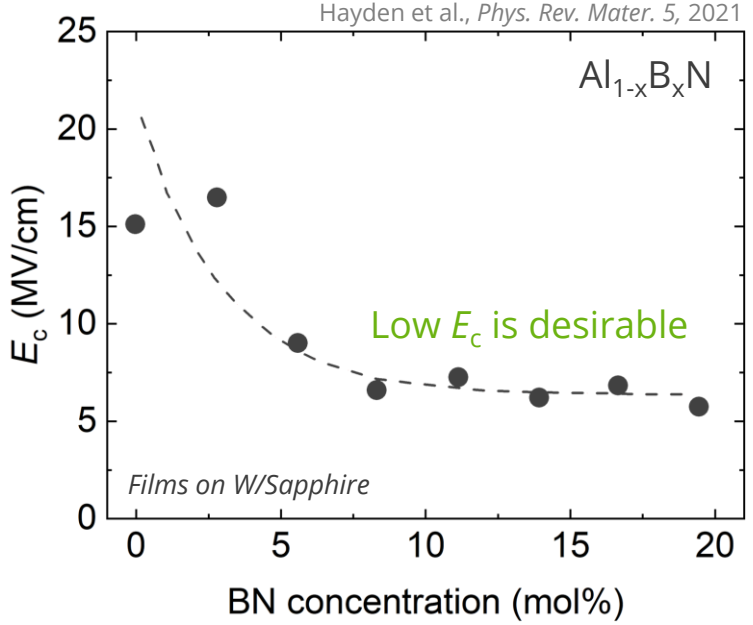


$Al_{0.6}Sc_{0.4}N$ Esteves, SNL, 2022



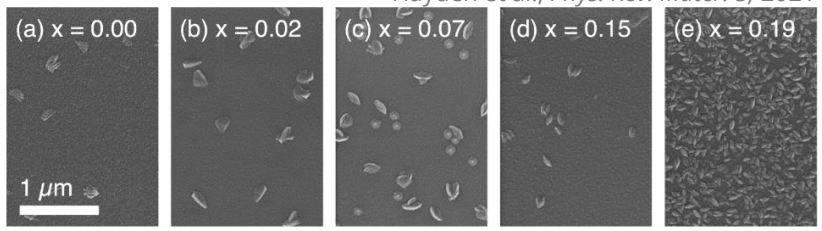
Tensile stress increases abnormal grain density

Hayden et al., *Phys. Rev. Mater. 5,* 2021



BN: boron nitride

Hayden et al., *Phys. Rev. Mater. 5,* 2021



Abnormal grains increase with boron