This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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Summary of Recent Total Ionizing Dose Testing on GF 12LP CMOS Technology

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Reliable Microsystems

November 7, 2022

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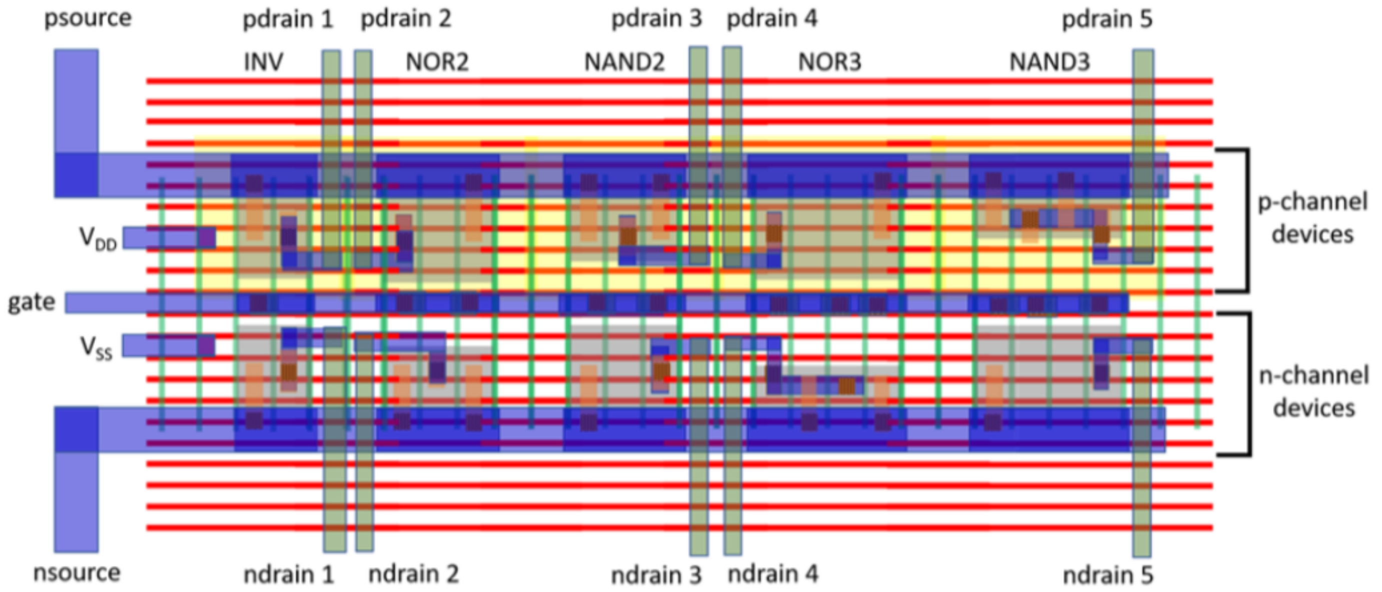
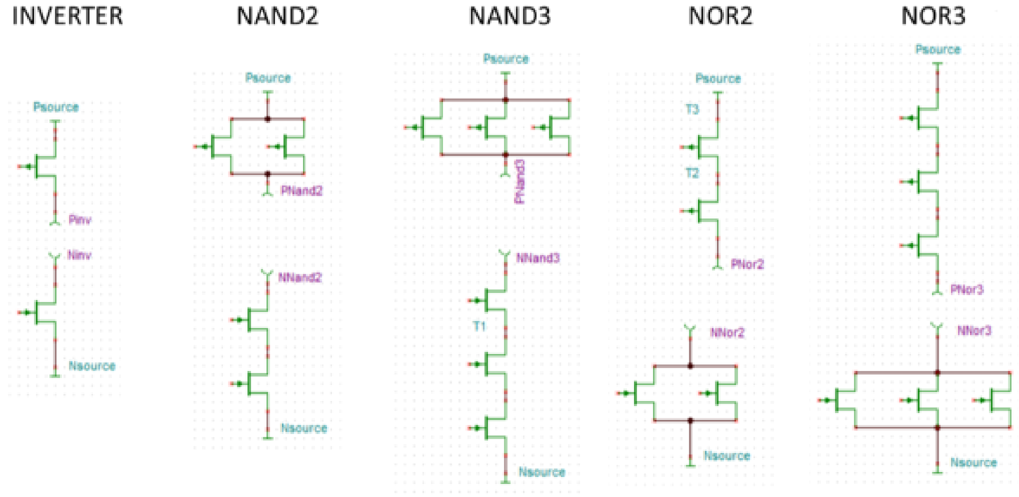
Outline

- ASU TID Test Structure Description
- ASU/AFRL X-ray Irradiation Details
- ASU TID Test Results
  - Id vs. Vgs curves
  - Off-state current response, configuration and layout dependence
- RMS TID Test Structure Description
- RMS/Vanderbilt X-ray Irradiation Details
- RMS TID Test Results
  - Id vs. Vgs curves
- Summary

ASU TID Test Structures



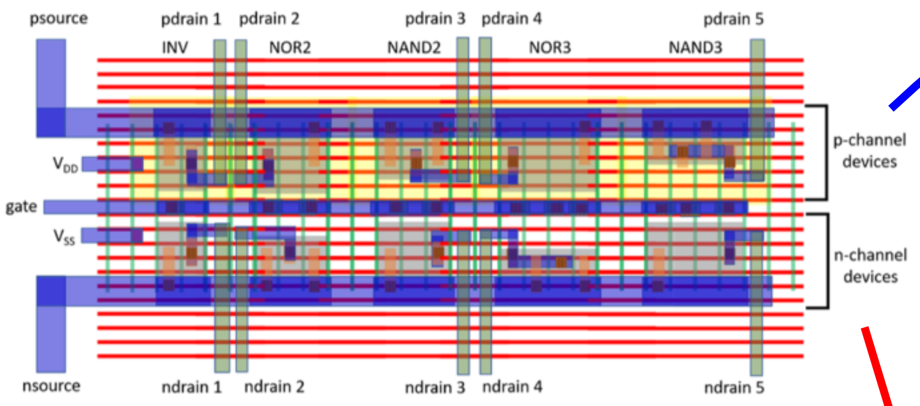


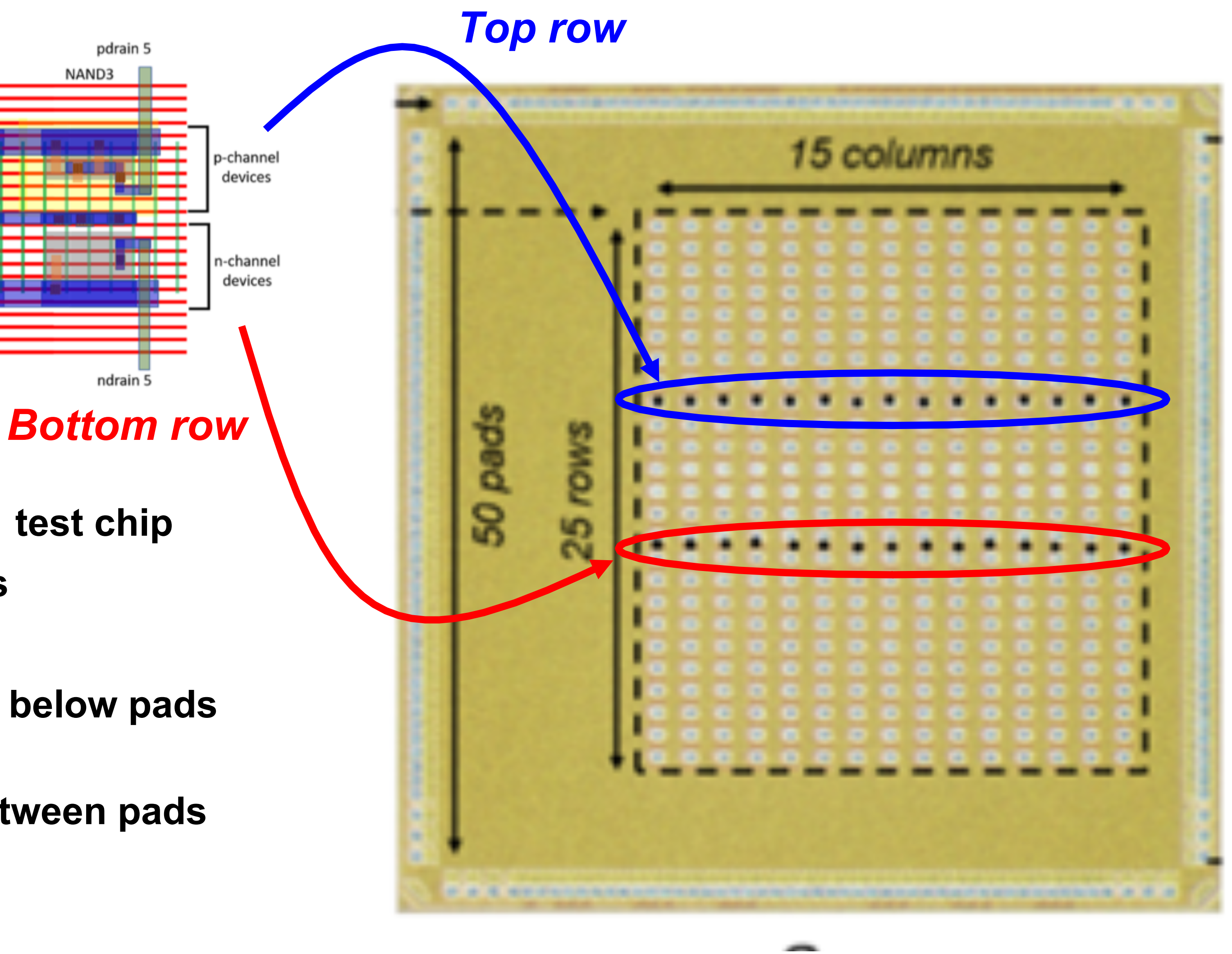
- **Structures modified forms of standard digital library cells: inverter, nor(2, 3), and nand(2, 3)**
- **Both nFET (PDN) and pFET (PUN) RVT variants**
- **Minimum gate length, with varying W based on number of parallel fins**
- **Terminals: gate, nsource, psource, body, nwell, independent drains (10)**

TABLE 1
NORMALIZED W/L FOR NFET CONFIGURATIONS

Config.	# Fins	# Parallel	# Series	W/L (equiv.)
INV	4	1	1	4
NOR2	3	2	1	6
NAND2	4	1	2	2
NOR3	2	3	1	6
NAND3	4	1	3	4/3

Pad Arrays



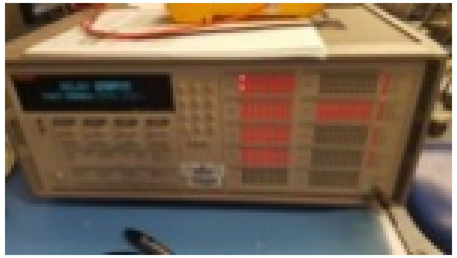


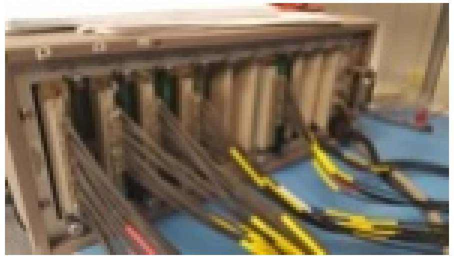
- Structures integrated on SEEEC TC1 test chip
- Pad matrix: 25 rows and 15 columns
- Two structures per column
- 15 top row structure laid out directly below pads (row 9)
- 15 bottom row structures laid out between pads (rows 15 and 16)

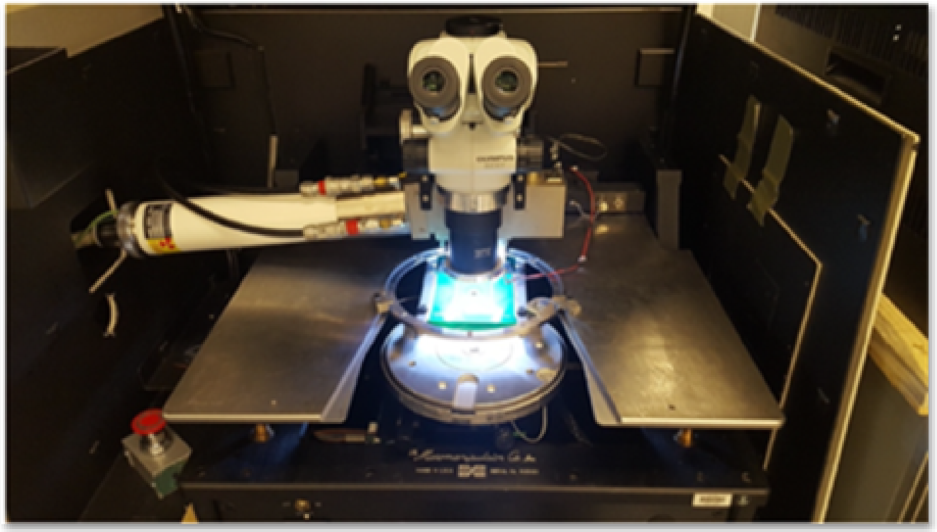
ASU X-ray Testing

- 10 keV X-ray) testing (ARACOR) perform at the AFRL space electronics facility (KAFB)
- Probe card attached to ARACOR system enables 20 nFET configurations across two adjacent columns
- Chips irradiated with ON-state bias,
  - NMOS - gate = 0.8V, nsource, body, drain = 0V
  - PMOS – gate = 0.8V, psource, nwell, drain = 1.6V
- NMOS and PMOS configurations measured with KeySight B1500A Parameter Analyzer through S/M prior to and after TID exposure using a step stress approach
- TID steps: 10, 20, 50, 100, 200, 500 krad(Si), and 1 Mrad (Si)

Note: dose level reported in rad(Si) and assumes ~50% attenuation caused by probe shielding

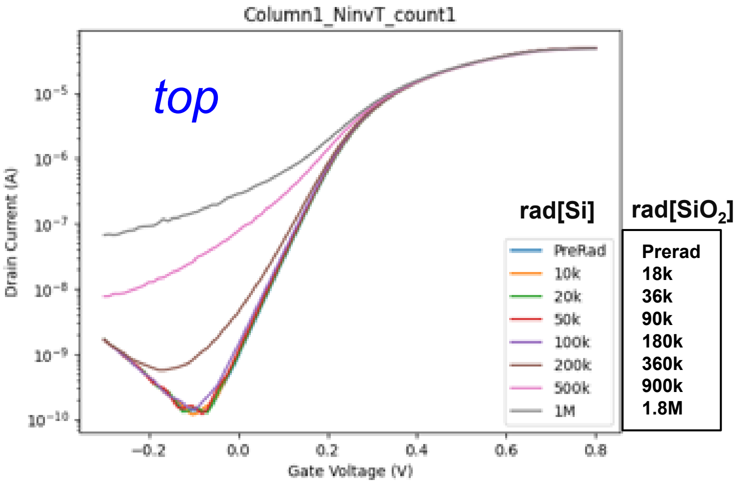


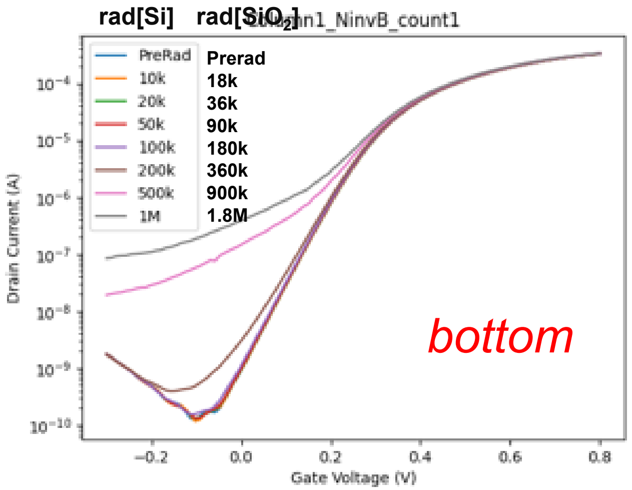




ASU Structure TID Response

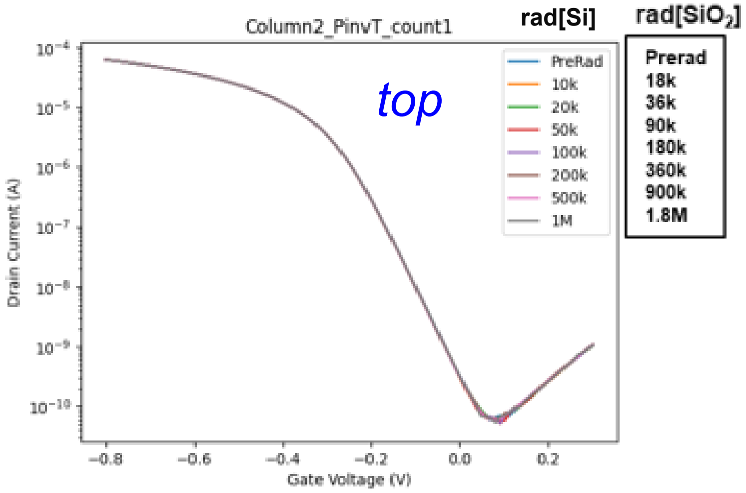
NMOS

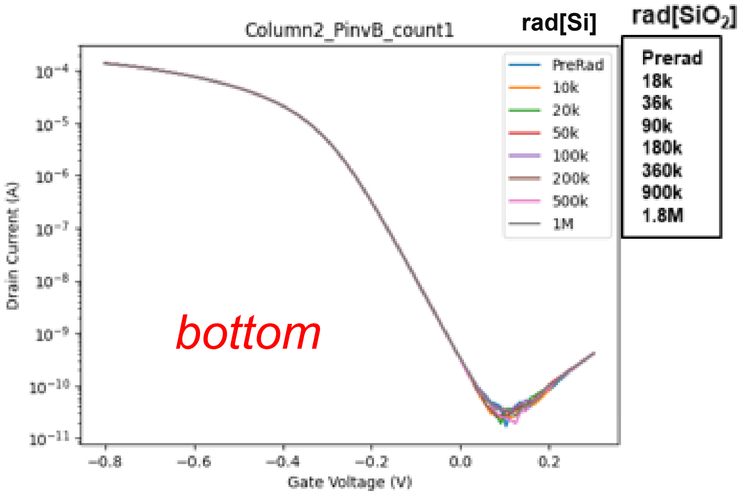




NMOS devices show increase in subthreshold current consistent with drain-source edge leakage

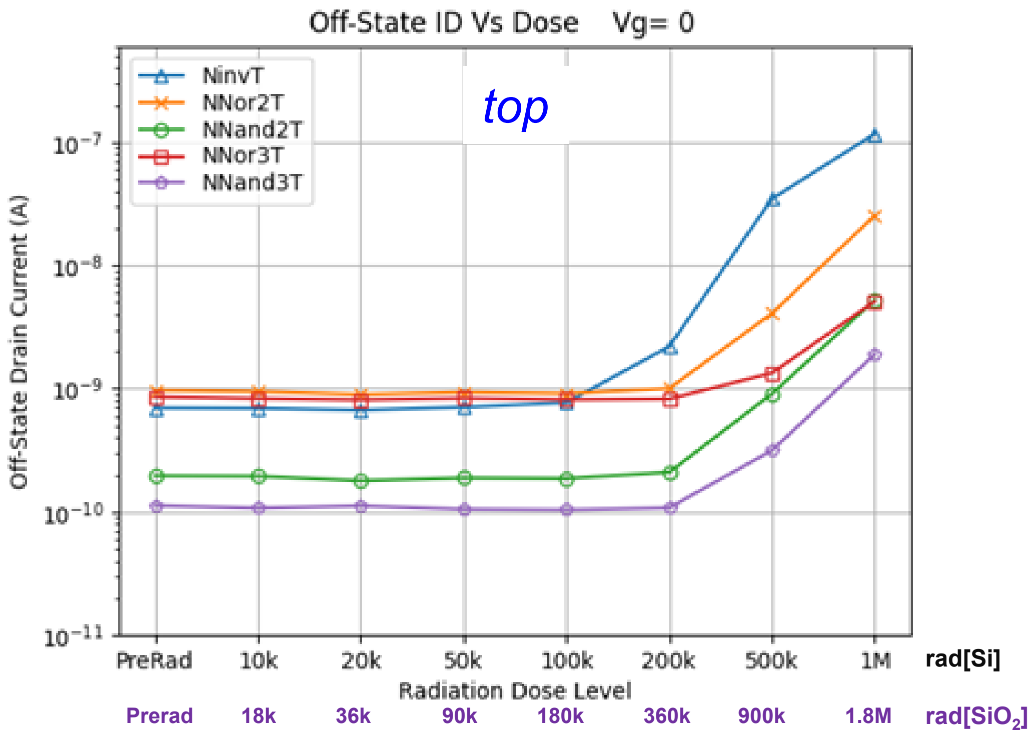
PMOS

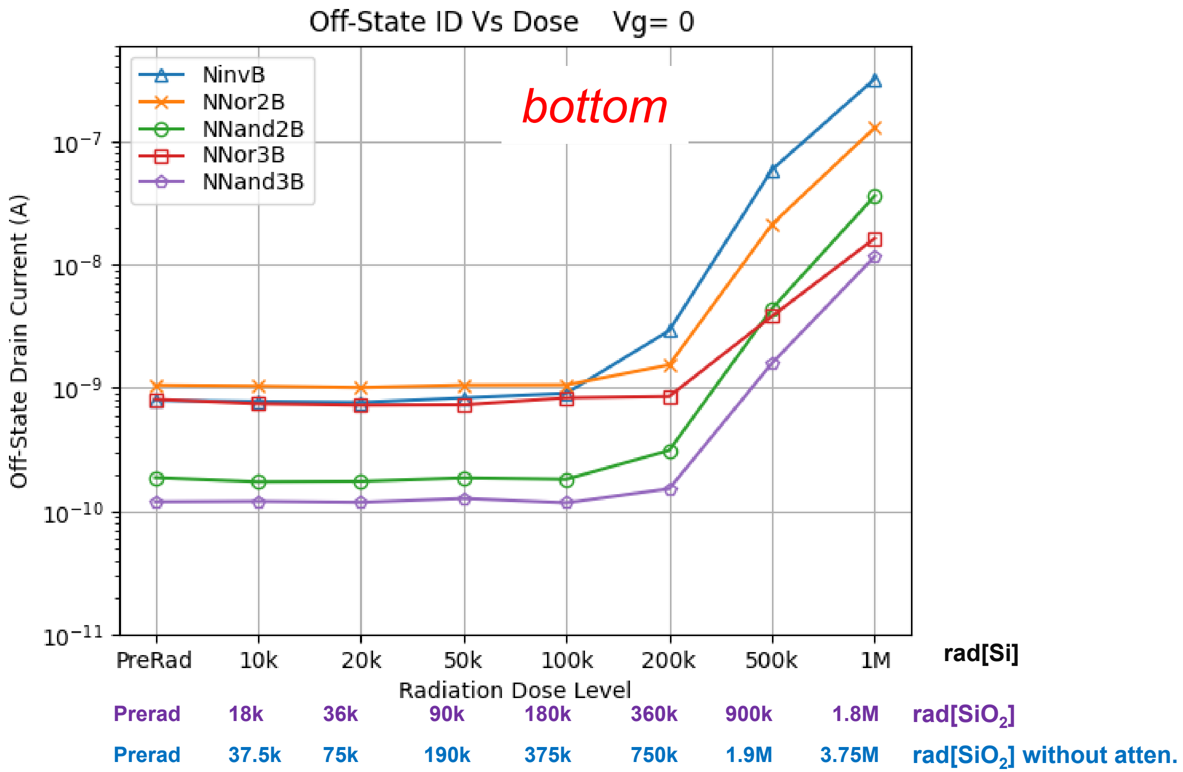




PMOS devices show no measurable change with radiation X-ray exposure

NMOS Response Dependence on Row Placement

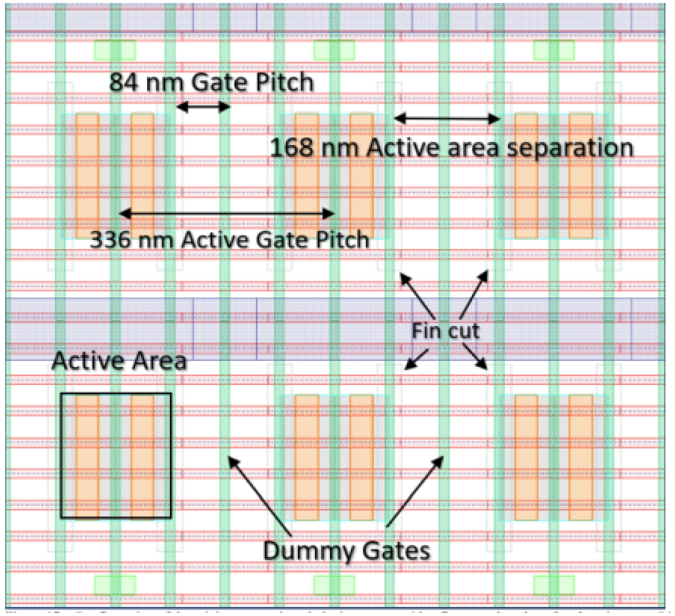


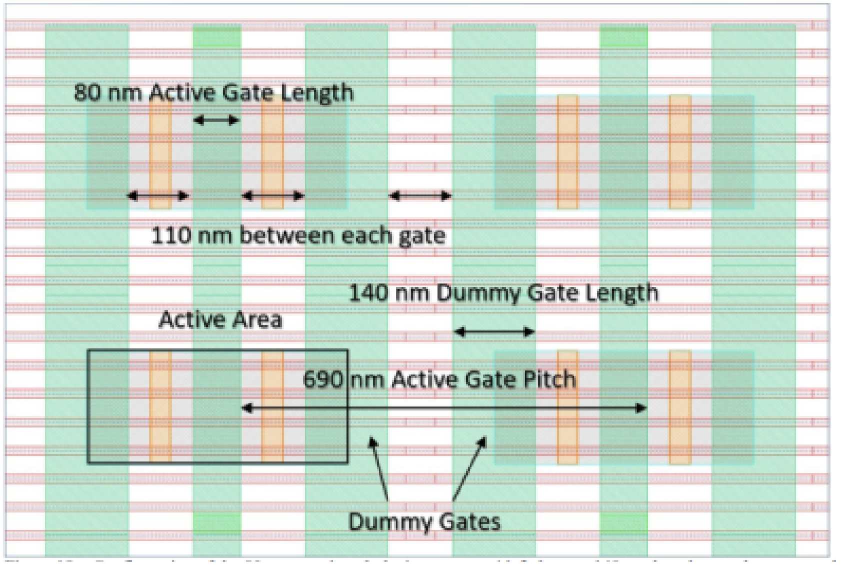


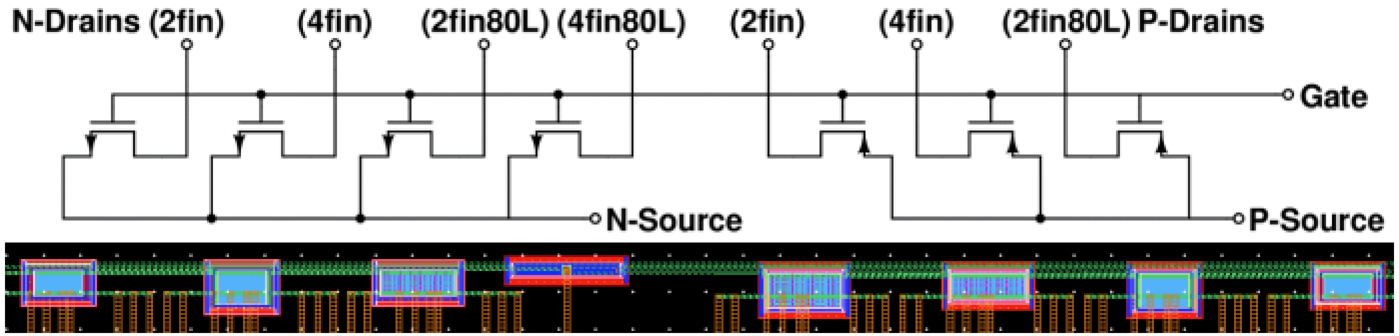
- **Off-state current in bottom row devices is between 1.5X and 3X degradation in top row devices (Average of 10 devices tested for both top and bottom)**
- **Source of discrepancy may be caused by probed shielding (i.e., bottom row should not we attenuated)**
- **Also, layout position, not # of fins, becomes dominant factor in response at high doses**

Wallace et al, 2022 NSREC

RMS TID Test Structures





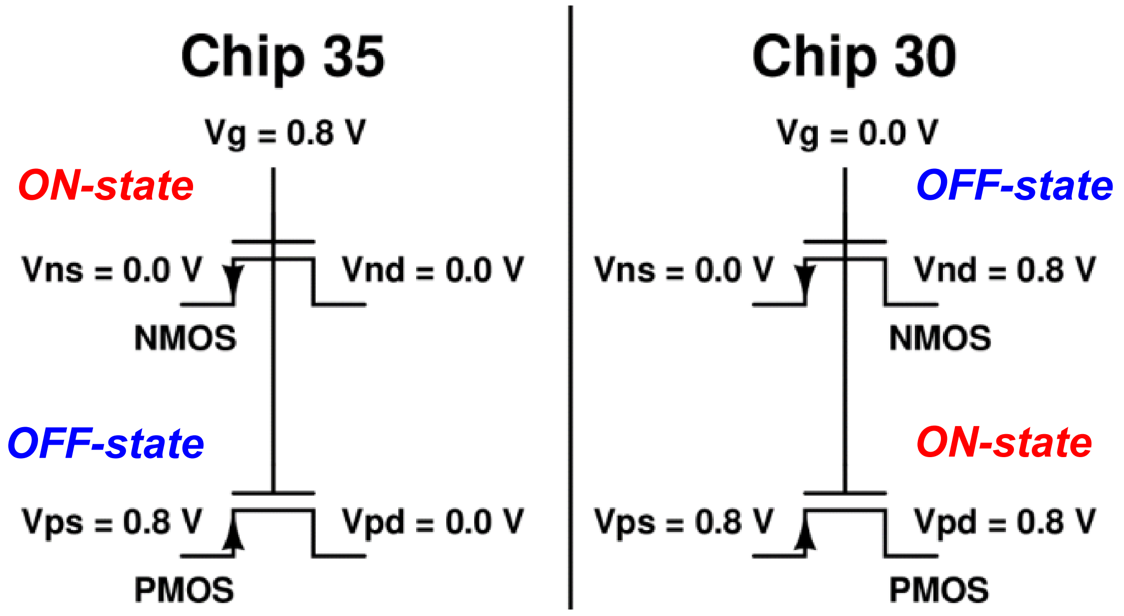


- All RMS devices are RVT types
- RMS devices are independent
  - not derived from standard digital library cells
  - not as densely packed as ASU cells
- RMS devices (both nFET and pFET) include minimum L and 80nm gate lengths
- Shared gate pins include ESD protection

RMS X-ray Testing

- Vanderbilt's 10keV ARACOR 4100 at a dose rate of 30.3 krad(SiO_2)/min
- Vanderbilt's HP4156B Parameter Analyzer, 2 Keysight E36313A PSUs
- During irradiation, the NFET drains were tied together and PFET drains were tied together
- During I/V sweeps of NFET devices, the source and drain terminals of the PFET devices were grounded, and vice versa
- During measurement of a given NFET/PFET array, remainder of NFET/PFET arrays drain terminals were tied common and left floating.
- Current compliance levels were set to 5 mA for both the PA and PSU outputs

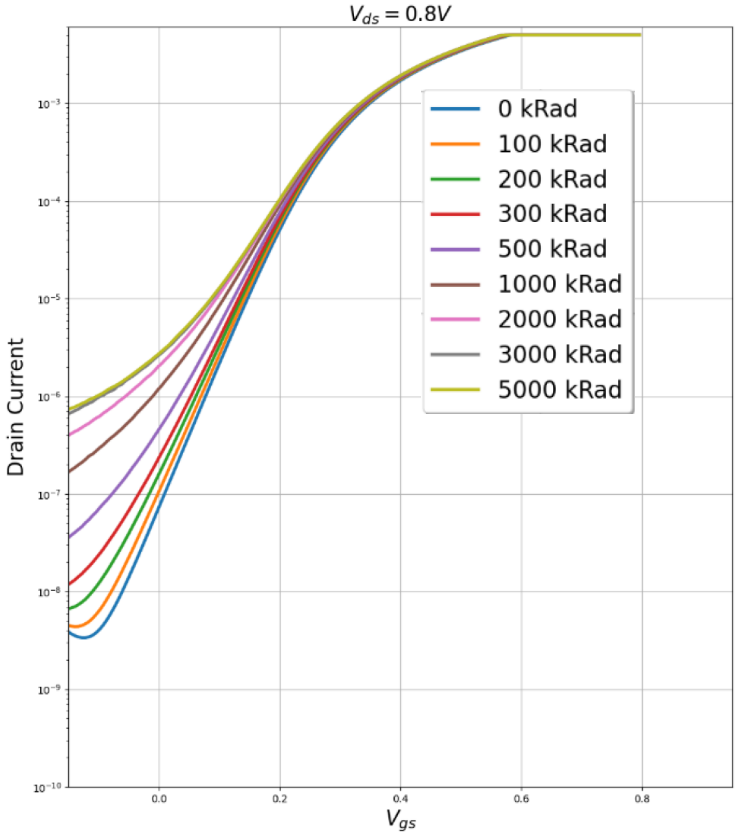
Radiation Bias Configurations



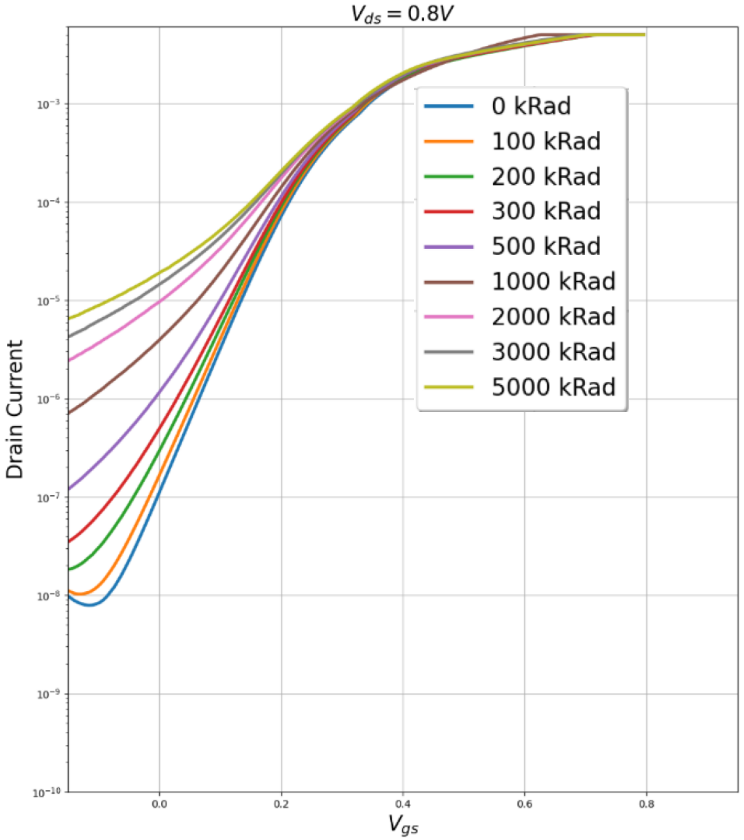
Note: dose level reported in rad(SiO_2) and assumes no attenuation

RMS Structure TID Response

Minimum L, 2-fin RVT NFET devices (Irradiated in ON-state)



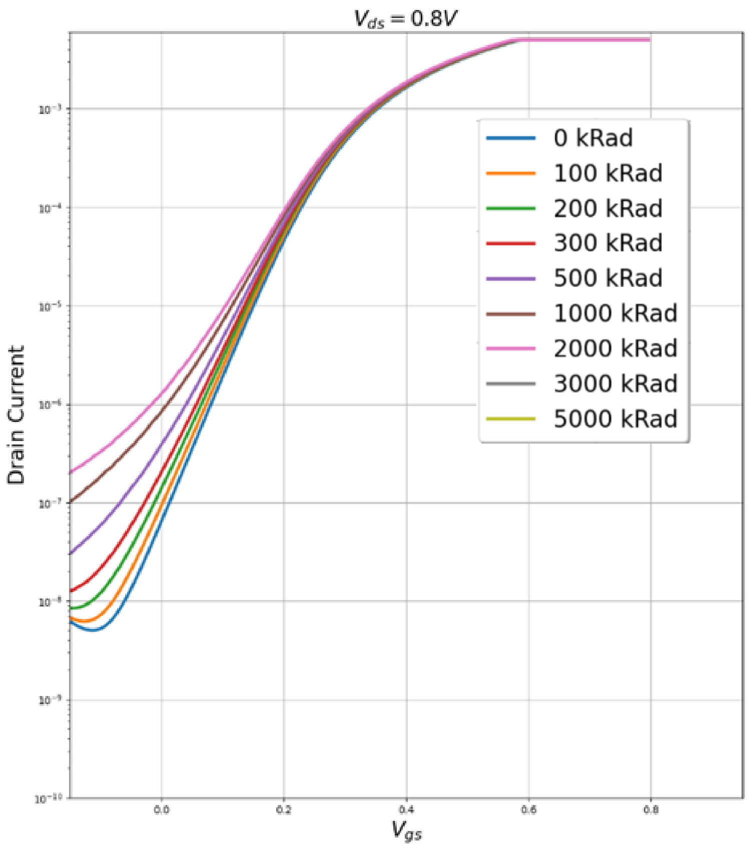
Minimum L, 4-fin RVT NFET devices (Irradiated in ON-state)



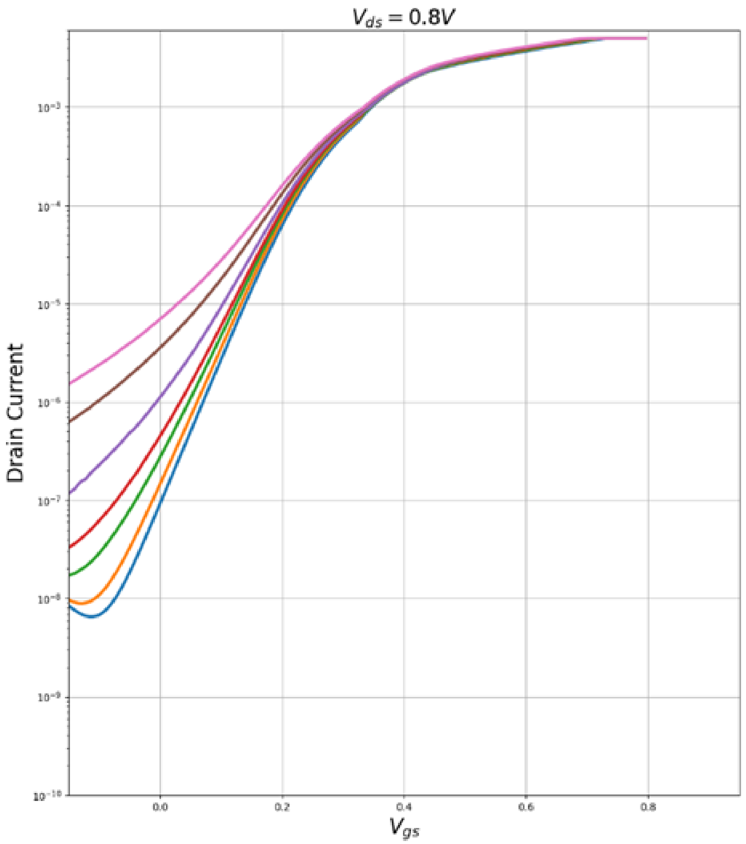
Results indicate more TID sensitivity in minimum L, 4-fin nFET devices vs. 2-fin for ON-state rad bias

RMS Structure TID Response

Minimum L, 2-fin RVT NFET devices
(Irradiated in OFF-state)



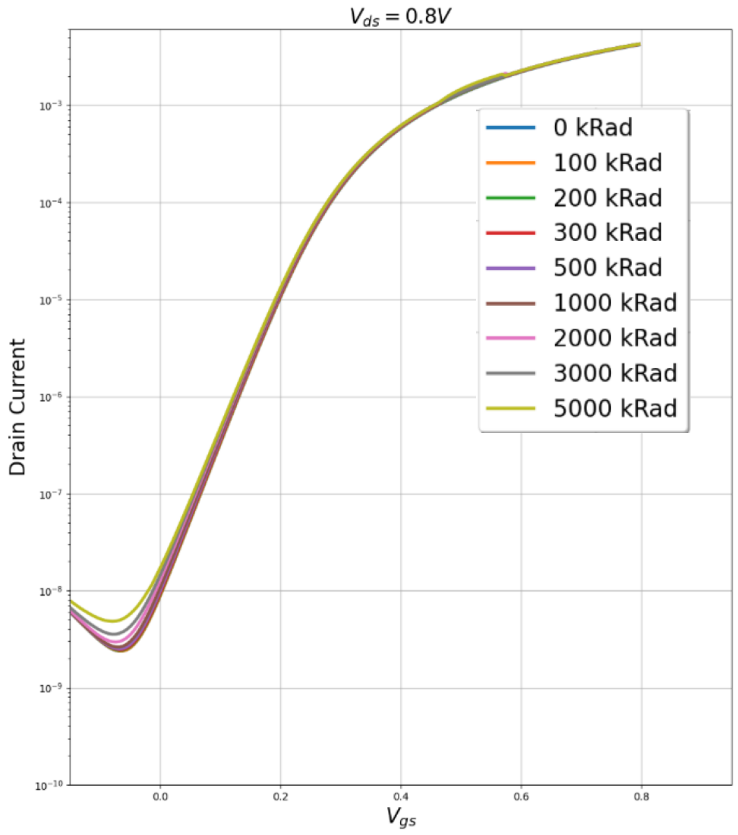
Minimum L, 4-fin RVT NFET devices
(Irradiated in OFF-state)



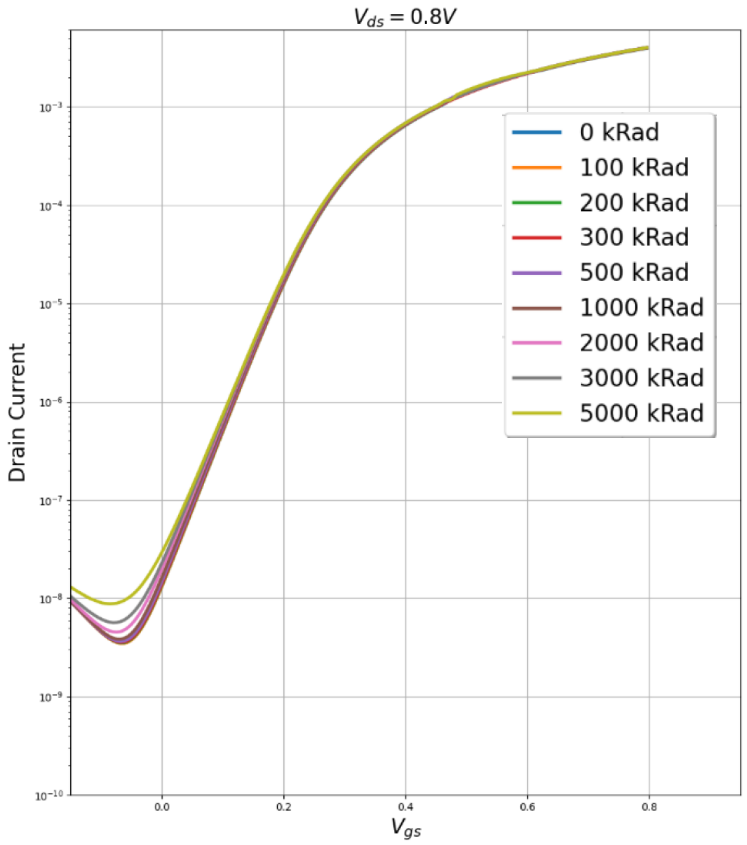
Results indicate more TID sensitivity in minimum L, 4-fin nFET devices vs. 2-fin, but less degradation in OFF-state vs. ON-state

RMS Structure TID Response

80nm, 2-fin RVT NFET devices
(Irradiated in ON-state)



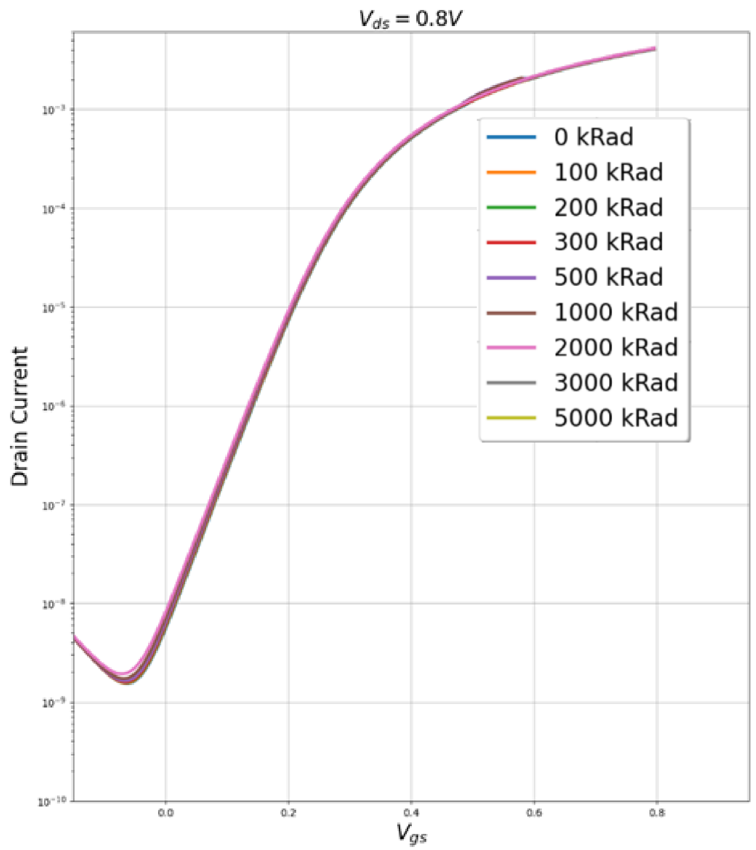
80nm, 4-fin RVT NFET devices
(Irradiated in ON-state)



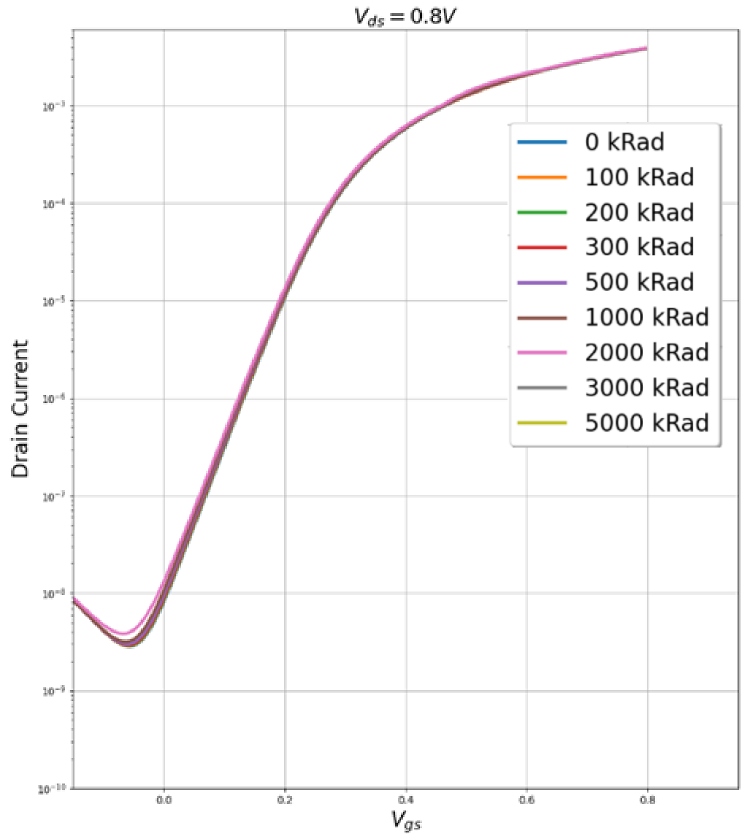
Results indicate low TID sensitivity in 80nm gate length nFET devices, in ON-state

RMS Structure TID Response

80nm, 2-fin RVT NFET devices
(Irradiated in OFF-state)



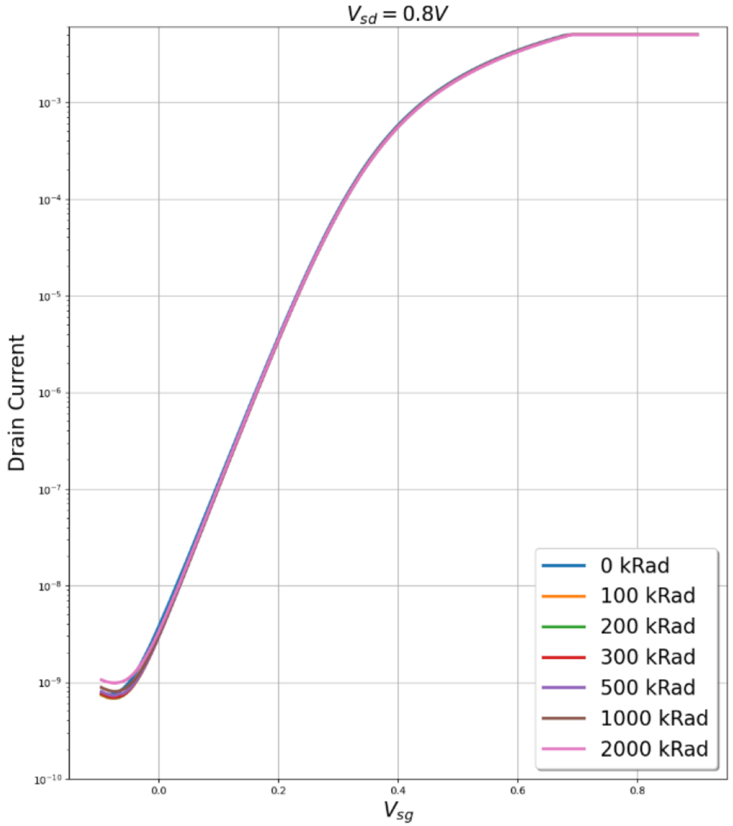
80nm, 4-fin RVT NFET devices
(Irradiated in OFF-state)



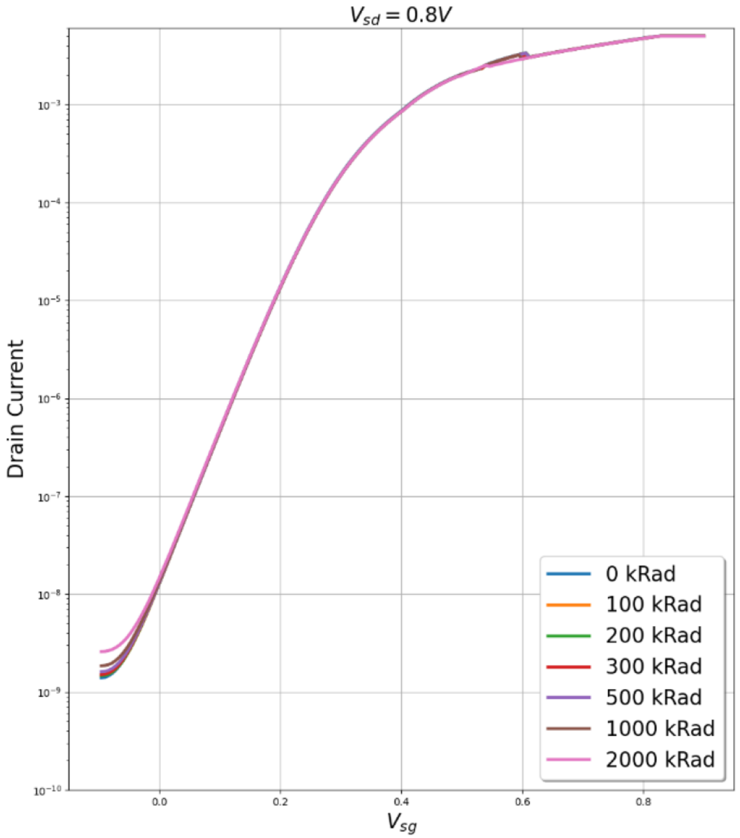
Results indicate negligible TID sensitivity in 80nm gate length nFET devices, in OFF-state

RMS Structure TID Response

Minimum L, 2-fin RVT PFET devices
(Irradiated in ON-state)



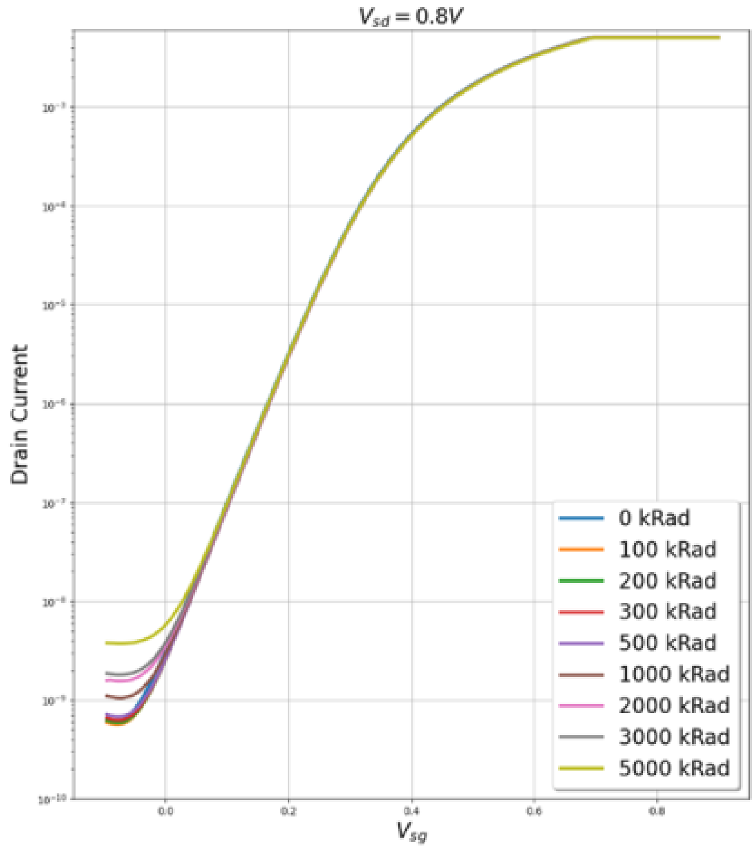
Minimum L, 4-fin RVT PFET devices
(Irradiated in ON-state)



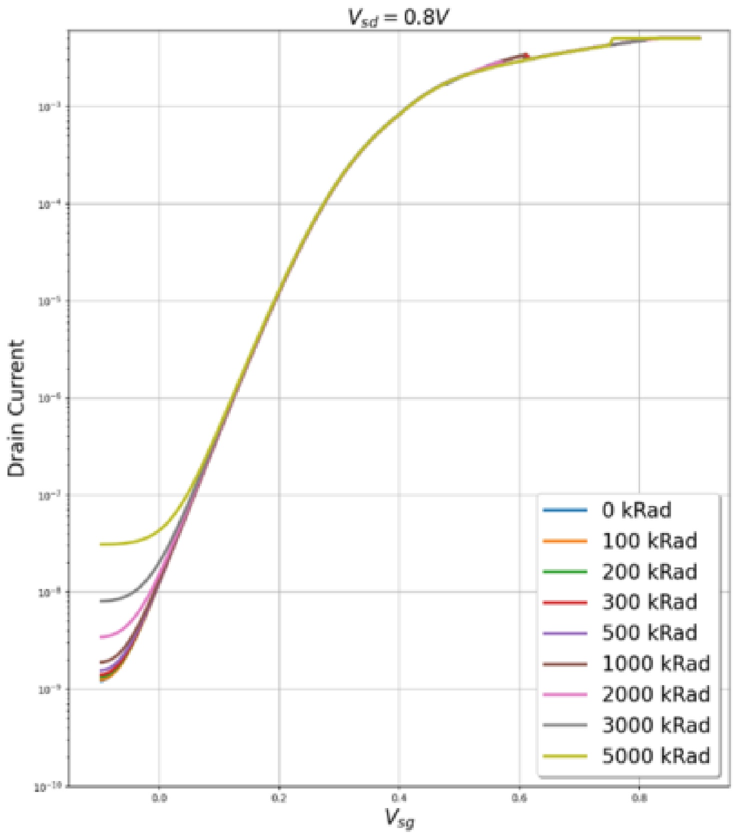
Results indicate negligible TID sensitivity minimum L pFET in ON-state rad bias

RMS Structure TID Response

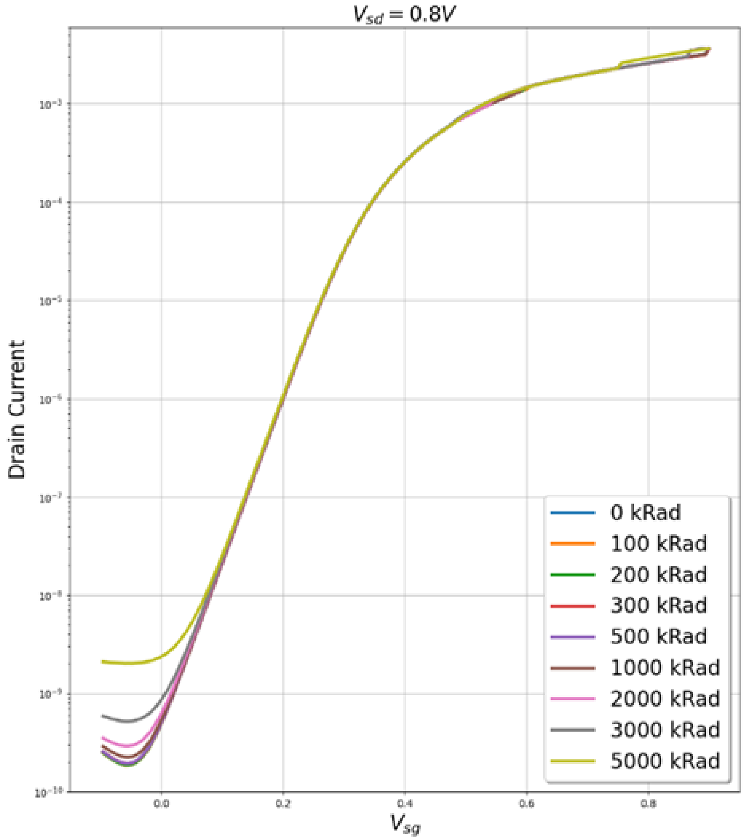
Minimum L, 2-fin RVT PFET devices
(Irradiated in OFF-state)



Minimum L, 4-fin RVT PFET devices
(Irradiated in OFF-state)



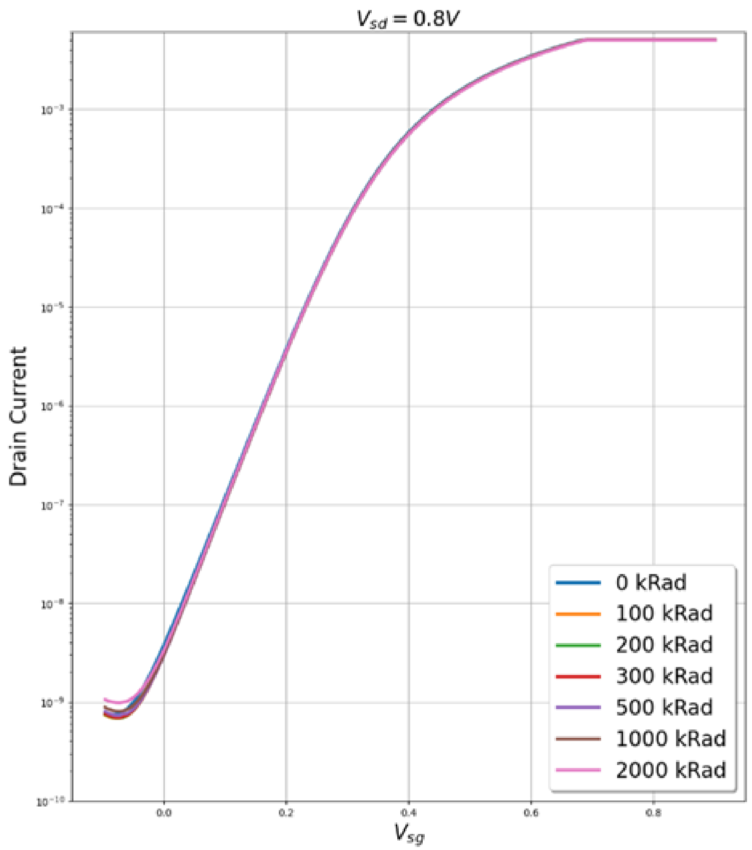
80nm, 2-fin RVT PFET devices
(Irradiated in OFF-state)



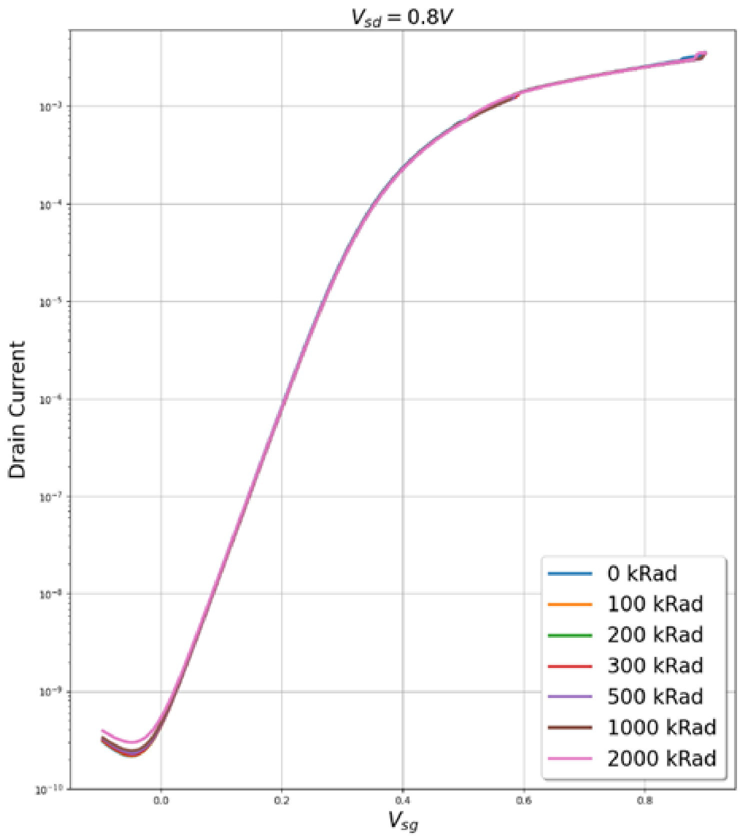
Results indicate TID sensitivity low in pFET OFF-state although slightly more leakage in minimum L, 4-fin nFET devices vs. 2-fin (similar degradation in 80nm)

RMS Structure TID Response

Minimum L, 2-fin RVT PFET devices
(Irradiated in ON-state)



80nm, 2-fin RVT PFET devices
(Irradiated in ON-state)



Results indicate negligible TID sensitivity pFET ON-state for both minimum L and 80nm

Summary

- ASU and RMS structures show similar TID sensitivity
- Both ASU and RMS show 4-fin nFET devices show greatest TID sensitivity (2 order of magnitude at 2Mrad(SiO_2)
- ASU structures off-state leakage current shows layout dependence (see Wallace, 2022 NSREC)
- RMS shows ON-state bias causes more degradation than OFF-state in nFET devices
- RMS shows longer nFET devices (80nm) are much harder to TID compared to minimum L
- Both ASU and RMS pFET devices show low to negligible TID sensitivity (slight degradation in OFF-state)