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Effect of Bias Voltage on Surface Insulation Resistance Measurements

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ABSTRACT

As electronics continue to decrease in size, dendrite growth is a growing concern for long term reliability of printed circuit boards (PCBs). Dendritic growth is a process that is caused by electrochemical migration (ECM). When the metal of the anode reacts with contaminants in the air or on the surface of the board, they form ions, which follow the path of the electric field. The metal from the anode begins to bridge the gap to the cathode, as the migrating ions follow the shortest path and deposit on the tip of the forming dendrite. If the dendrite structure reaches the cathode, a short occurs, and results in a temporary failure for the PCB. In past literature, the relationship between voltage bias and the tendency (propensity) of dendrites to form has been inverse; as the voltage bias increases, different failure mechanisms, such as dielectric breakdown, dominate and do not allow dendritic growth to occur. In this study, we analyzed the effect that voltage bias has on dendrite growth both in clean PCBs and PCBs that were contaminated. All boards were first cleaned thoroughly in-house, to set a baseline. The boards were contaminated with different concentrations of chloride-containing salts, then imaged at 30x magnification. The boards then were inserted into the SIR chamber, with environmental conditions set to 90% RH and 40C. The boards rested overnight to stabilize, and then a bias voltage was applied. The time between measurements was set to 5 minutes, for 168 hours of total test length. The surface insulation resistance graphs of these boards served as an indicator of any electrochemical processes that occurred during the test. The boards then were re-imaged at 30x magnification, and any areas of interest were looked at with the DSC for further evaluation.

Key words: Surface Insulation Resistance, Bias Voltage, Electrochemical Migration

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INTRODUCTION

Surface Insulation Resistance (SIR) is a tool that is used for process quality control in the industry[1]. Surface insulation resistance provides relevant data regarding the cleanliness and product reliability for a printed circuit board (PCB) by performing accelerated aging[2]. Accelerated aging is achieved in SIR by applying a constant bias voltage, along with heightened temperature and humidity[3-4]. It is difficult to make quantifiable statements using SIR data, but the data provides qualitative feedback that can be interpreted.

In previous literature, it has been determined that SIR experiments will be performed at a bias voltage of 5VDC[5]. However, the electronics industry has needs of printed circuit boards (PCBs) that continue to evolve as the electronics industry continues to develop. Furthermore, the effect of bias voltage may have an effect on the time to failure of a PCB when tested under SIR, an important consideration for real-world applications[6]. Thus, it may not be reasonable to assume that one bias voltage provides an accurate representation of real phenomena in applications.

As electronics continue to decrease in size, dendrite growth continues to emerge as a concern for long term reliability of printed circuit boards (PCBs)[7-8]. Dendritic growth is a process that is caused by electrochemical migration (ECM). The metals on the anode can react with contaminants in the air or on the surface to form ions. These ions can follow the

electric field and deposit on the cathode. Soon, bridges form between the anode and the cathode, as the ions that are migrating will tend to follow the shortest path and deposit on the tip of the dendrite that is forming. This process is accelerated by the presence of ionic contamination on the surface as well as the presence of water layers on the surface[9].

The finishes that were chosen to be studied were copper fingers on bare FR4, and electroless nickel/immersion gold (ENIG) plated copper with a solder mask between the electrodes. ENIG plating is commonly used on PCB designs, but it comes with drawbacks of its own[10]. The Au serves as a passivation layer that prevents oxidation of the Ni and Cu underneath, while the Ni prevents the movement of Au down the stack, due to its exceptional mobility. However, the Ni atoms that are between the Cu and Au layers have a much smaller atomic diameter than the thin Au layer that is deposited above it, and it is very possible that Ni atoms will diffuse through the thin passivation Au layer, which allows them to migrate [11-12]. The designs we are interested in are interdigitated comb (IDC) patterns, which have widespread use in surface insulation resistance, as well as other MEMS devices[13-14].

Using Surface Insulation Resistance (SIR), we can measure resistance between the anode and the cathode at consistent intervals. However, the graphs that this data produce can be tricky to interpret and are non-discriminatory. SIR is not a diagnostic tool; it simply measures the resistance. There are many variables that could affect these readings[15]. Thus, it can be difficult to pinpoint the cause of failures when they occur. Two failures that have very similar shapes in resistance can be caused be entirely different phenomena, as will be discussed.

The primary purpose of this experiment was to look at the effect that voltage bias has on Surface Insulation Resistance measurements, to determine whether it is appropriate for one bias voltage to be used for all experiments of this nature. The change in bias voltage could have many potential effects on the characteristic behavior of surface insulation resistance, due to the presence of ions that are present on the board. Another objective was to determine whether greater bias voltages had a larger propensity of dendrite growth. If the voltage bias exceeds the electrochemical potential of the metal, dendritic growth is possible[4].

EXPERIMENTAL

To examine the effect of bias voltage for reliability testing, clean and contaminated PCBs will be used. All PCBs were initially cleaned by submerging the coupons in an isopropyl alcohol bath and sonicating for 2 minutes. All coupons were then submerged into a separate isopropyl alcohol bath and sonicated for 2 minutes again. The PCBs that were classified "contaminated" were contaminated using common salt, NaCl. This was chosen because sodium and chlorine are two common contaminants in an industrial setting. They were contaminated according to an estimate of 10 years of contamination deposit in a common industrial setting[16]. The salts were dissolved into a solution of water, then deposited onto the surface of the board using a calibrated micropipette from Eppendorf.

After the PCBs are prepared, all boards will be imaged using a Keyence optical microscope, at 30x magnification. The 2D image stitching feature is used to get an image of the board before testing. This is intended to provide a good reference and an indicator of any defects that were present before the SIR began.

Once the PCBs were in the environmental chamber, the chamber was set to 30C/30%RH, and the PCBs rested for an hour. The temperature was then increased to 40C with no change in RH, and the PCBs were allowed to rest for an hour. Finally, the humidity was increased to 90%RH, and the PCBs rested in this environmental condition overnight before testing began. This process prevents the effects of localized condensation on the PCB and allows the PCBs plenty of time to achieve a relative steady-state condition before a bias voltage is applied. It is assumed that before this bias voltage is applied, no electrochemical changes occur on the surface of the PCB. The steady-state environment in the chamber was set to 40C/90% RH, according to the IPC guidelines for testing the PCB. This will accelerate the aging of the PCBs to evaluate the effect over time, which is what SIR aims to achieve. The applied bias voltages will be 5VDC, 10VDC, and 25VDC.

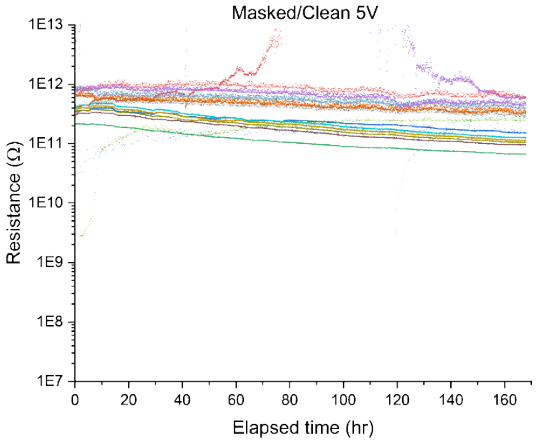
After the experiment is performed, the PCBs were once again imaged under the Keyence under the same 30x magnification. The resistance vs time graph was considered, and any quadrants that experienced failures were chosen to be looked at under SEM and EDS. A failure was defined as a change in resistance of two or more decades within an hour, significantly compromising the performance of the board during that period. These techniques allowed us to determine whether dendritic growth or electrochemical migration was the cause of the failure.

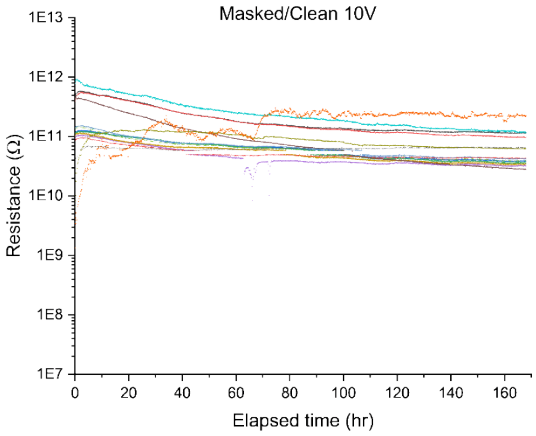
RESULTS AND CONCLUSIONS

The experimental design was performed with no incidents. The boards were given appropriate time to adjust to the new temperature before the humidity was increased, and there was no evidence of excessive condensation before the experiment began. Likewise, the roof of the chamber was examined after all experiments, and there was no evidence of water condensation that could have dripped onto the PCBs that were being tested. Results in Figures 1 and 2 were obtained, for both the masked/ENIG plated PCBs.

The SIR graphs for clean, masked, ENIG plated boards were consistent, despite the increase in voltage bias, as shown in Figures 1 and 2. All graphs demonstrated what appears to be an exponential decay in resistance over the period of the test, which levels out at similar resistance values which are well above the threshold for acceptable. One channel experienced

a failure about 120 hours in, however analysis under SEM and EDS determined that it was not due to electrochemical migration.





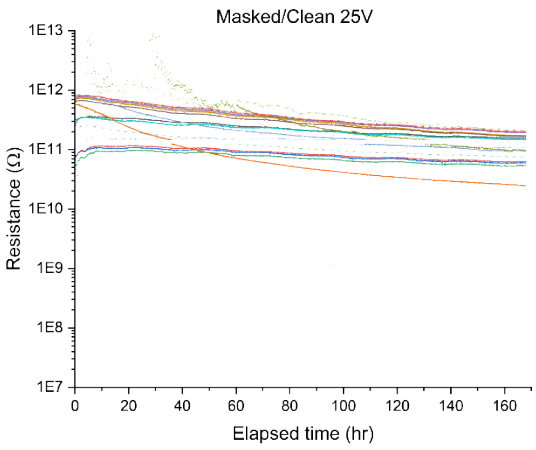
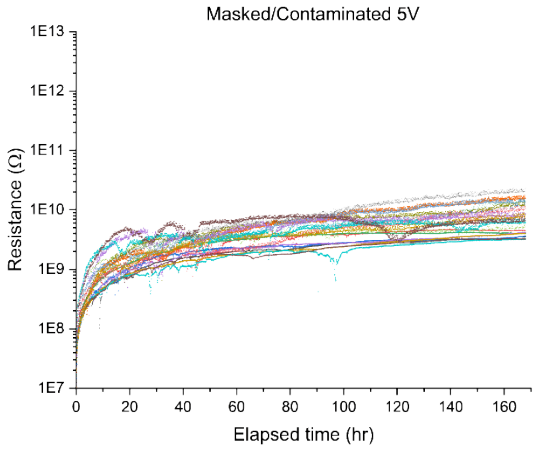
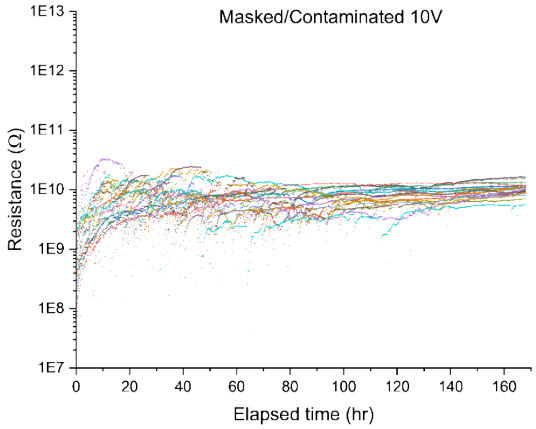


Figure 1. SIR of Clean Masked/ENIG plated PCBs tested under 40°C/90%RH and varying bias voltages.

The SIR for contaminated, ENIG plated PCBs with solder mask demonstrated differing characteristics with varying bias voltage. In all contaminated experiments, the SIR begins at a lower value, and resistance increases linearly with time (remember these are plotted on a log10 scale) for the transient portion of the graph. At the end of the transient period, the resistance stops increasing at its linear rate, and in some cases begins decreasing.





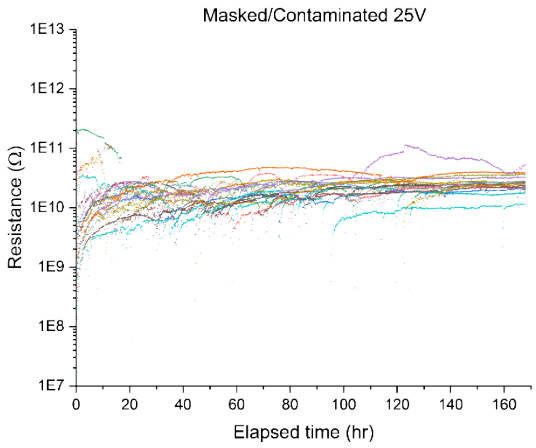


Figure 2. SIR of Contaminated Masked/ENIG plated PCBs tested under 40°C/90%RH and varying bias voltages.

The initial SIR reading of these PCBs increases as the voltage bias increases. At 5V, the initial resistance was 6.9E6 ohms; at 10V 9.4E7 ohms; and at 25V 1.6E10 ohms.

The time to reach the stable period also decreases as voltage bias increases. There are multiple failures of contaminated PCBs, and the occurrence of failures that were caused by ECM increased as the bias voltage increased as well. These results are shown in Table 1.

Table 1 - Instances of ECM occurrences for Masked/ENIG PCBs that occurred during SIR testing.

Instances of Electrochemical Migration (ECM) Occurrences for Masked/ENIG Plated PCBs Observed during SEM/EDS		
	Clean	Contaminated
5V	0	1
10V	0	1
25V	0	3

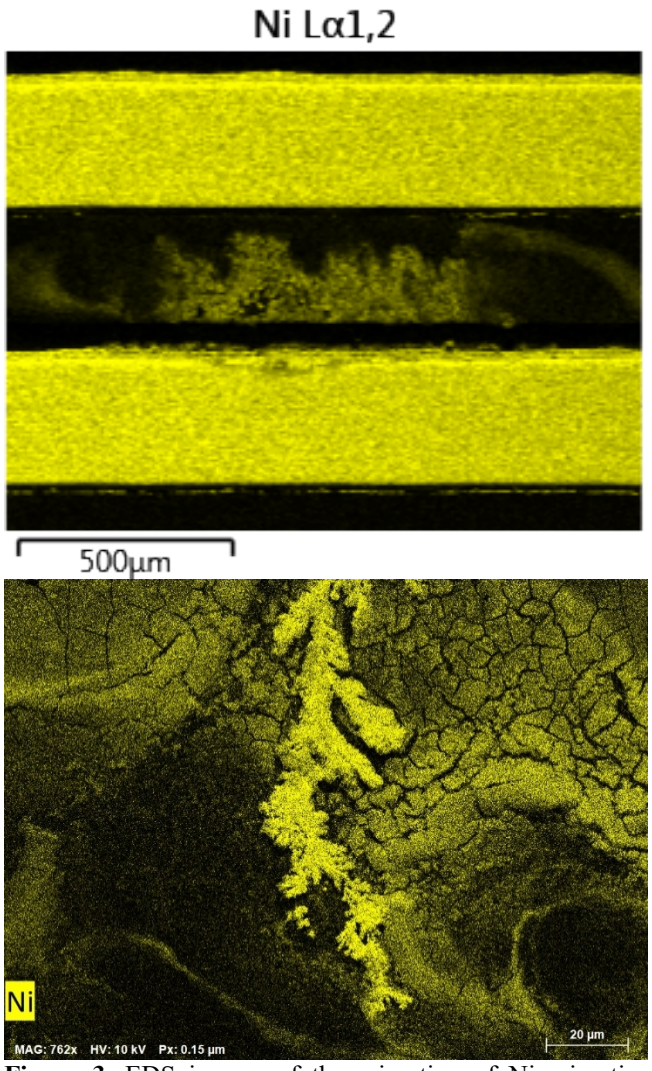


Figure 3. EDS images of the migration of Ni migrating between the cathode and anode. The bottom image is of a dendritic growth observed, while the top image is of ECM with no special shape.

It should be noted that ECM includes both dendritic growth and electrochemical migration without definite shape, and two examples are included in Figure 2. Both instances of ECM caused a failure in SIR, which was the cause of investigation under EDS, an example shown in Figure 3.

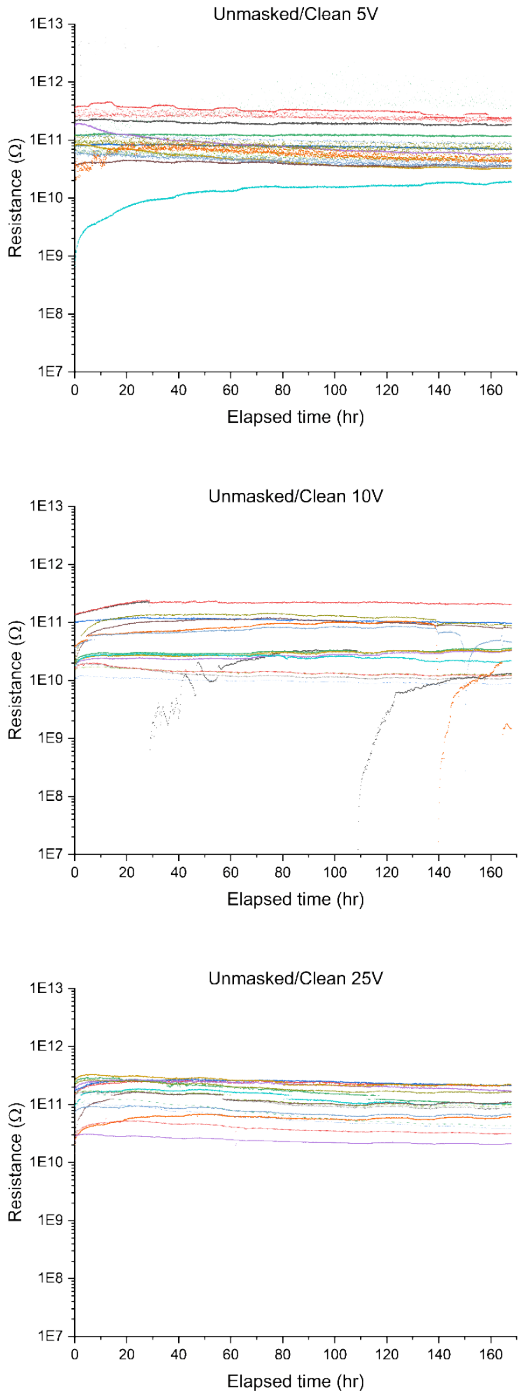


Figure 4. SIR of unmasked, clean copper PCBs under 40°C/90%RH and varying bias voltages.

The SIR results for bare copper on FR4 PCBs is presented in Figures 4 and 5.

The SIR behavior of cleaned copper/FR4 PCBs was relatively consistent, with minor differences. Some channels had the transient period of increasing SIR growth, but the stable resistance was within a decade of the initial value.

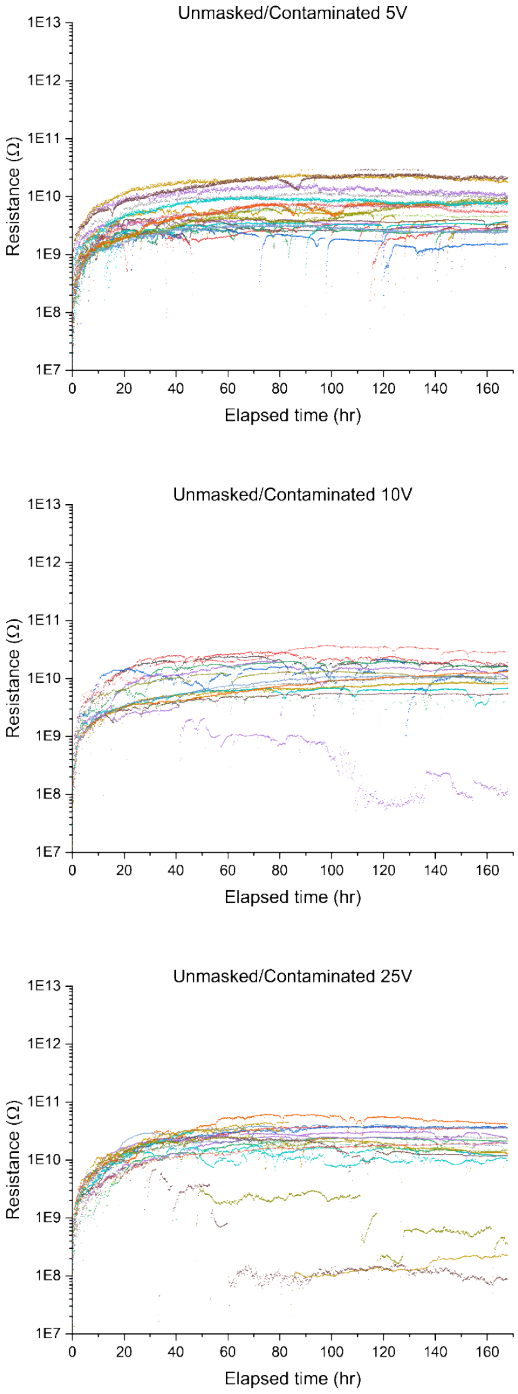


Figure 5. SIR of unmasked, clean copper PCBs under 40°C/90%RH and varying bias voltages.

The resistances, once reaching this stable value, tended to stay constant with a minor decrease over the period of the test. This, of course, contrasts with the exponential decay to a constant that was exhibited by the masked/ENIG plated PCBs. Three channels experienced failures under the 10V bias, and one channel was observed to have dendritic growth between the anode and cathode, shown in Figure 6. This kind of growth is unusual for bare copper with no ionic contamination, although the presence of oxygen under EDS may suggest there was a water deposit. The time of failure is also unusual for the dendrite, occurring after 100 hours into the test.

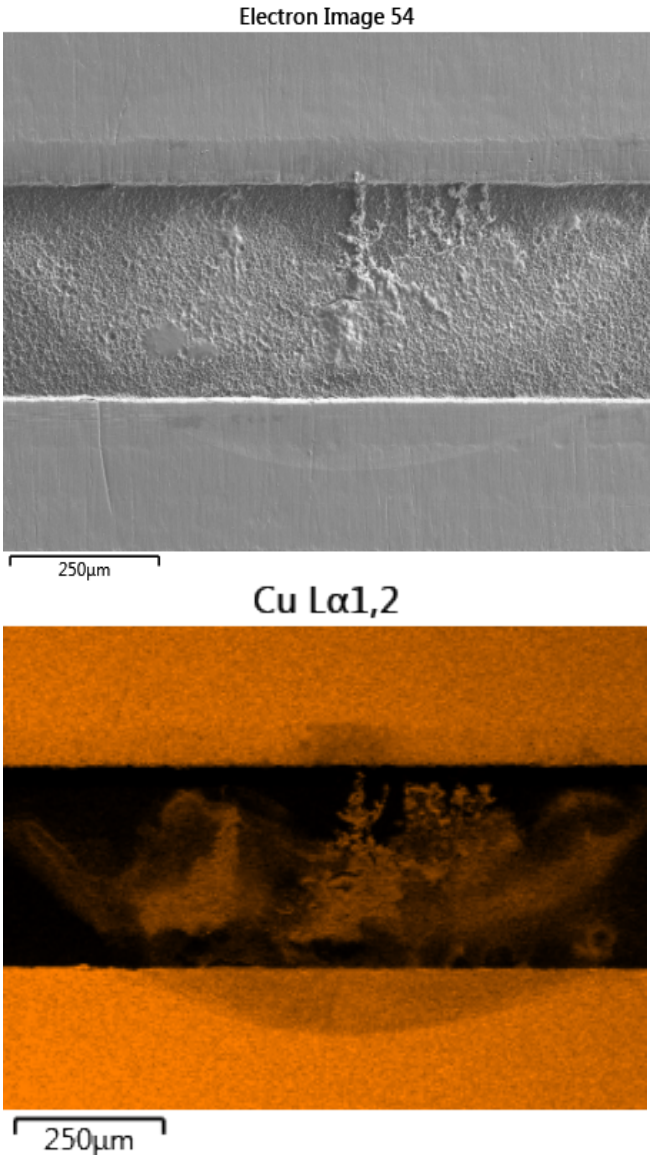


Figure 6. SEM (top) and Cu EDS map (bottom) of dendritic growth occurring on a cleaned copper/FR4 board under 10VDC bias.

The SIR of bare copper/FR4 PCBs exhibited similar behavior for the contaminated boards as the solder mask/ENIG plated PCBs, with the initial resistance beginning at a lower value

than the resistance in the stable period. Likewise, as the voltage bias increases, the time to reach this stable period is shorter, and the initial resistance reading is also larger. As voltage bias increases for contaminated Cu/FR4 PCBs, the number of channels experiencing failure exhibit no trend, but the failures that are caused by ECM do occur with a 25VDC bias, as shown in Table 2.

Table 2. Instances of ECM occurrences for Bare Copper PCBs that occurred during SIR testing.

Instances of Electrochemical Migration (ECM) Occurrences for Cu/FR4 PCBs Observed during SEM/EDS		
	Clean	Contaminated
5V	0	0
10V	1	0
25V	0	2

This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government

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