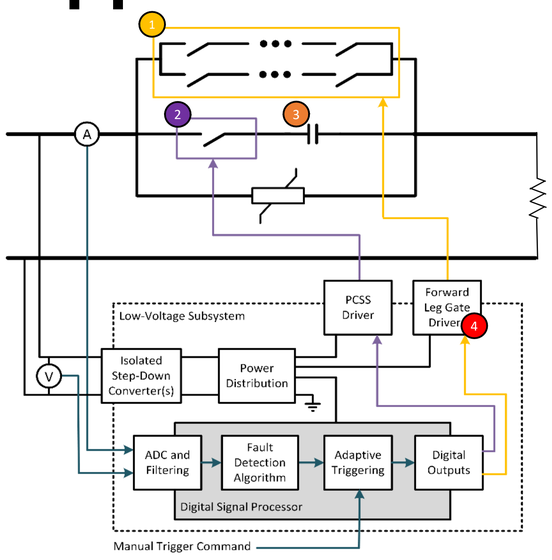
SAND2022-14425C

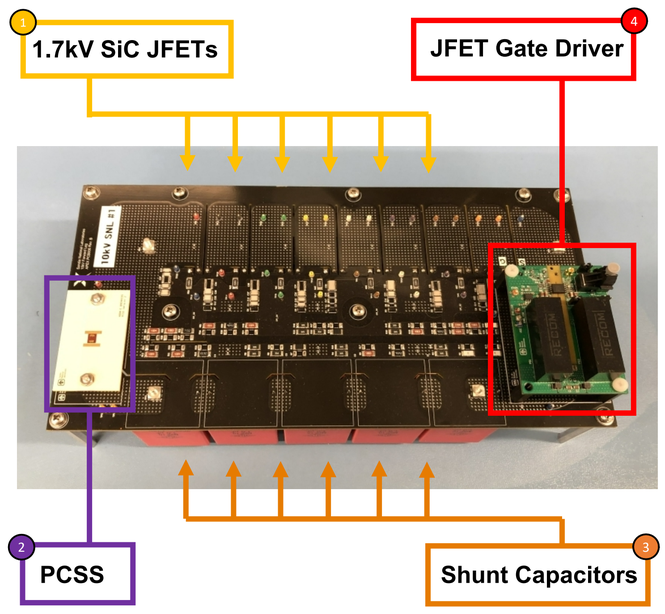
Sandia National Laboratories

ARC-SAFE: Accelerated Response Semiconducting Contactors and Surge Attenuation for DC Electrical Systems

6 kV/5 A DC Circuit Breaker Demonstration

Approach



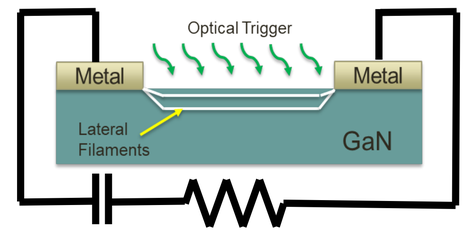


1. Normally-on Leg consists of cascaded SiC JFETs with passive balancing approach
2. Normally-off Leg uses GaN PCSS
3. Energy dissipating leg uses shunt capacitor to manage flyback current.
4. System control (sense and trigger) included in low-voltage subsystem
   - Instrumented to allow characterization of circuit breaker components
   - Shrinking design for 10 kV/100 A target

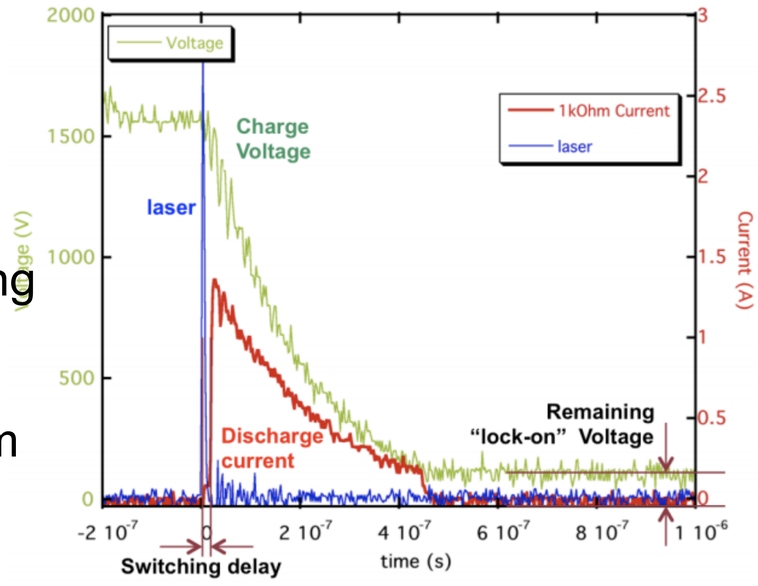
Benefits

- *Normally on, low loss JFETs improve CB efficiency*
- *Galvanic isolation from optically triggered GaN PCSS (fast acting)*
- *System control powered from HV side voltage tap*

GaN PCSS (Lateral Design)

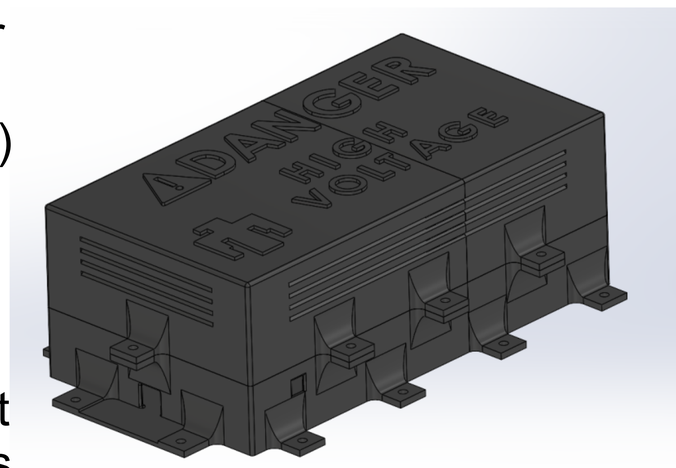


- < 2 kV switches using 0.6 mm gap
- Higher voltage switches using 2 mm gap
- Optically triggered using 532 nm (Nd:YAG laser)

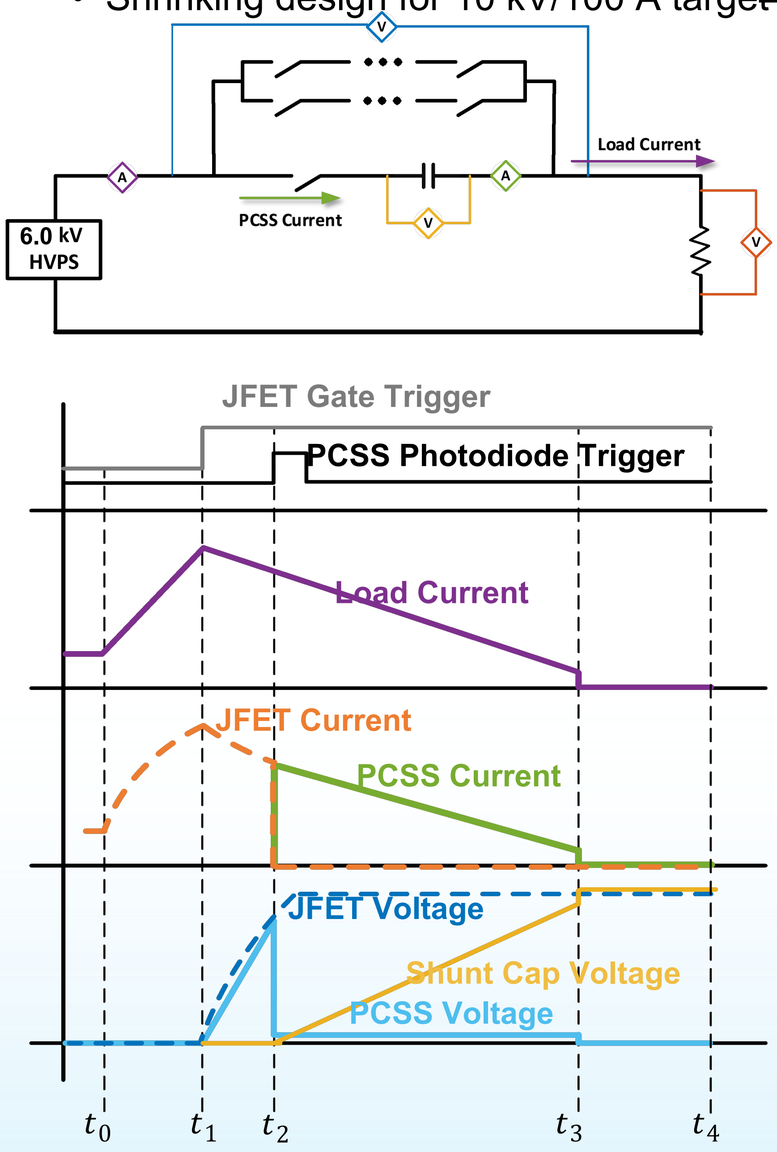


Circuit Breaker Packaging

- Prototype package for DC Circuit Breaker fabricated (3D printed)
- Estimated power density 1.98 kW/in^3
- Contains forward leg, control circuit, GaN PCSS submount, heat sinks, & feed-throughs



DC Circuit Breaker Operation



Interval I [$t_0 \rightarrow t_1$]

- Fault current rises at t_0 until t_1 when the fault current is detected, turning JFETs OFF

Interval II [$t_1 \rightarrow t_2$]

- JFET voltage starts to rise at t_1 and JFET/load current starts to decrease.

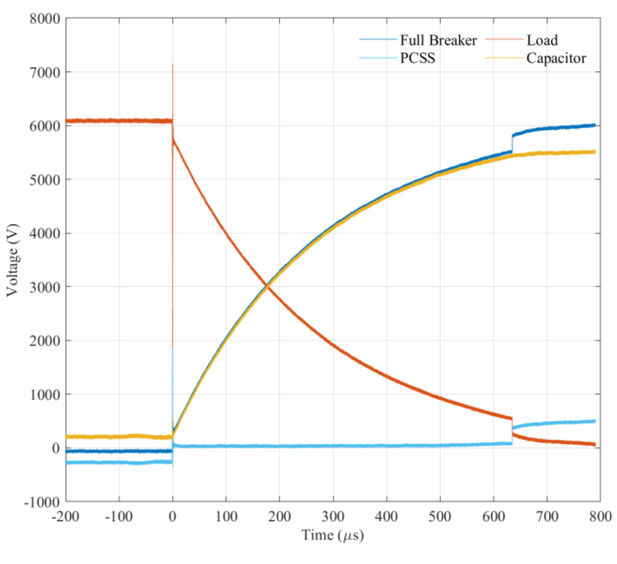
Interval III [$t_2 \rightarrow t_3$]

- PCSS is triggered at high-gain mode at t_2, diverting fault current from JFET leg to shunt cap.
- Shunt capacitor voltage rises based on RC value.

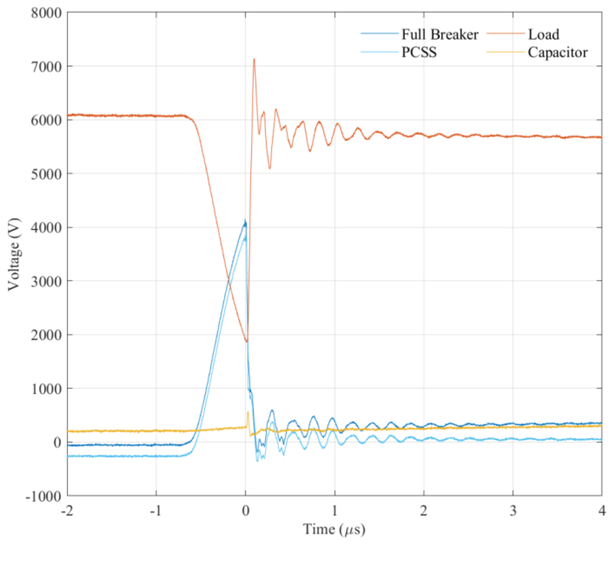
Interval IIV [$t_3 \rightarrow t_4$]

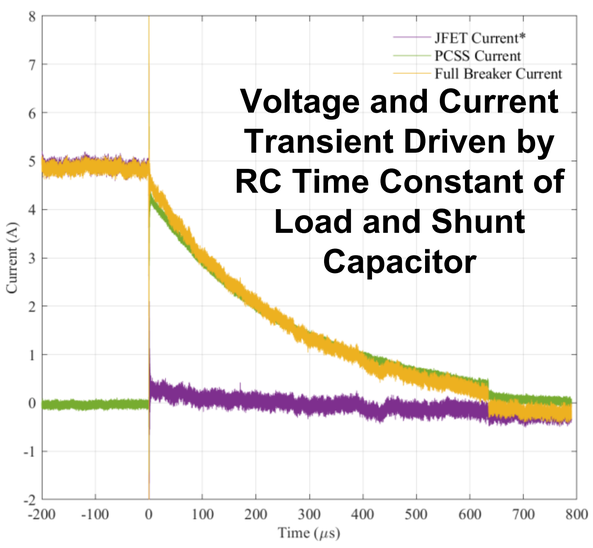
- PCSS voltage reaches OFF state and breaks remaining current.

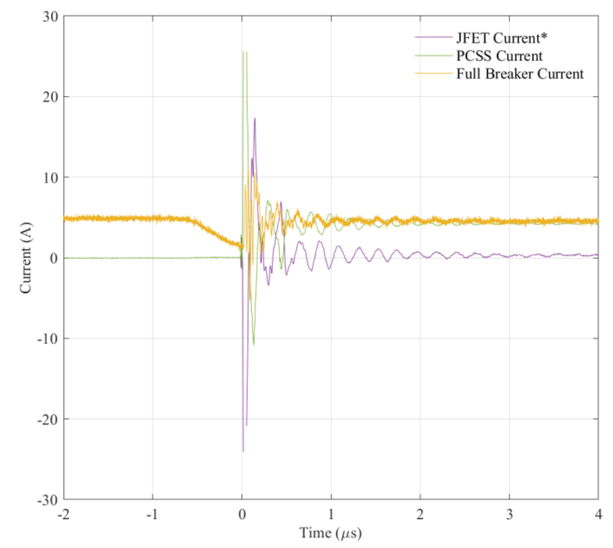
Nominal test shot capacitor charge



Nominal test shot transient







Current limited by testing setup and GaN PCSS

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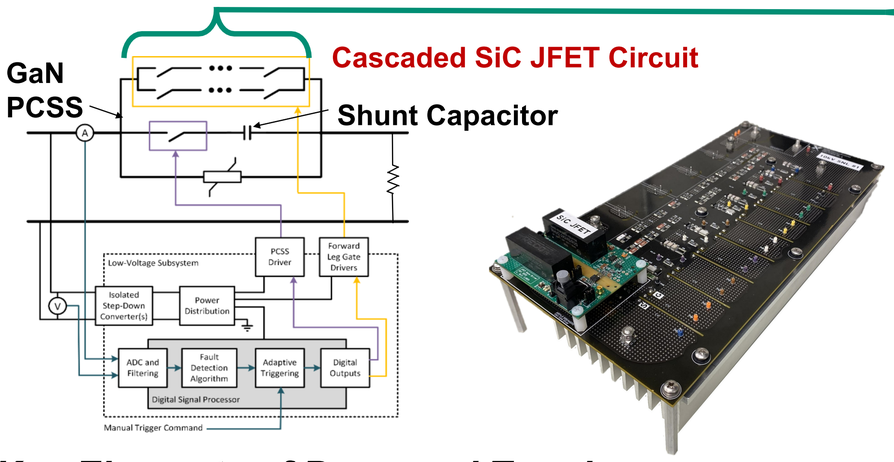
ARC-SAFE: Accelerated Response Semiconducting Contactors and Surge Attenuation for DC Electrical Systems

Cascaded JFET Circuit for DC Circuit Breaker Applications

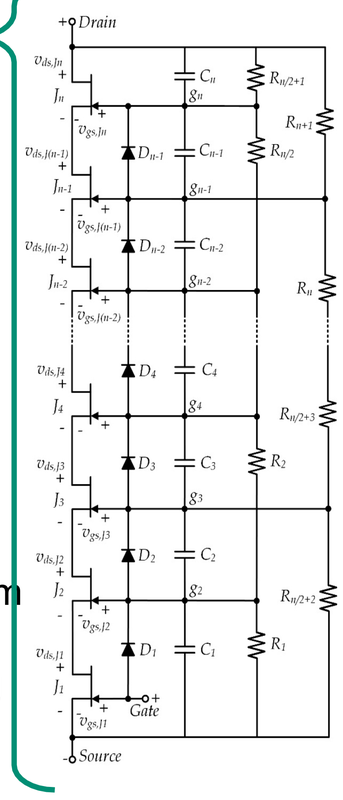
Approach

1. Cascaded SiC JFET circuit is used to implement main switch of a DC circuit breaker
2. Circuit must ensure DC line voltage is distributed evenly across multiple devices in both transient and steady-state conditions
3. On-state must provide low conduction losses, off-state must block full DC line voltage
4. Operation coordinated with fast acting GaN PCSS to manage the substantial stresses of DC current breaking events



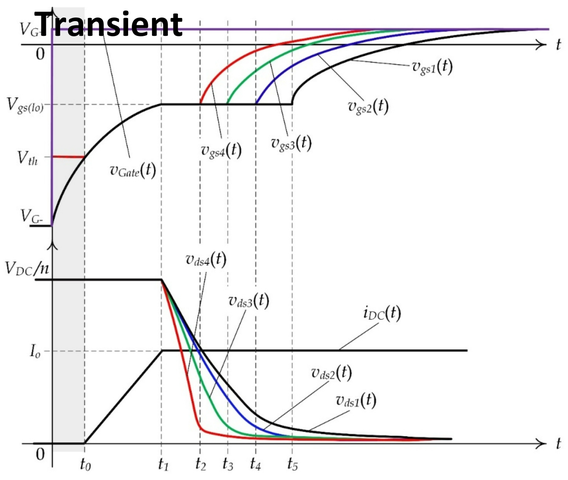
Key Elements of Proposed Topology:

- *n* SiC JFETs connected in series
- $D_1 – D_n$ avalanche diodes provide protection from potential over voltages across the devices
- $C_1 – C_n$ dynamically balance the voltage sharing of each transistor
- $R_1 – R_{n+1}$ achieve the static voltage sharing

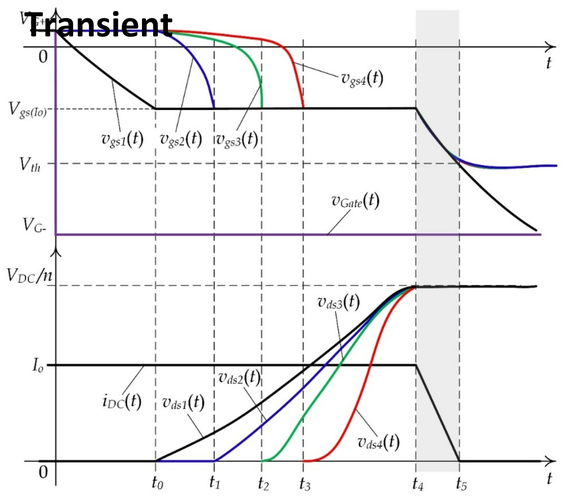


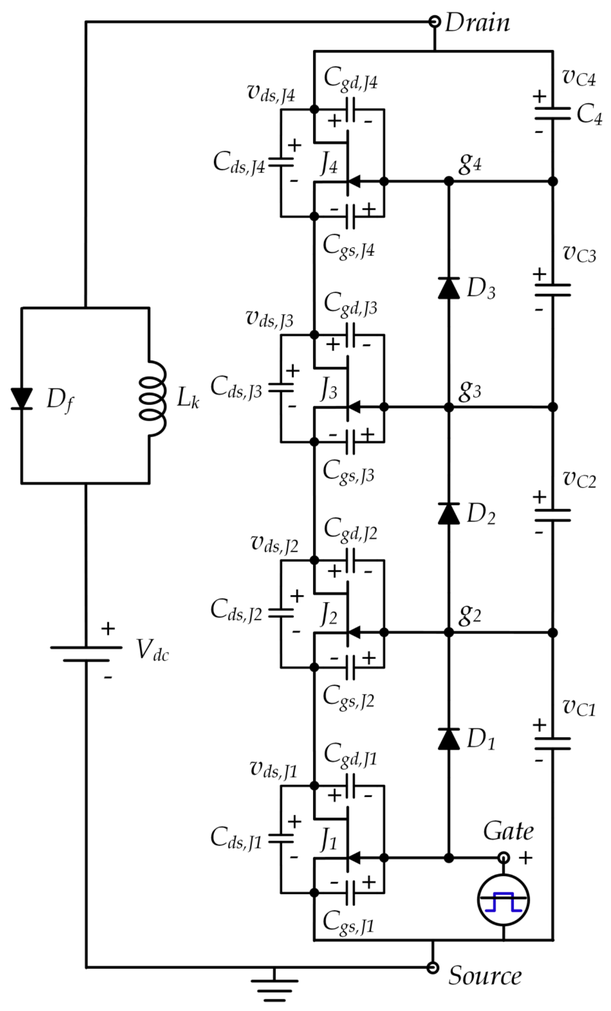
Voltage Balancing During Switching

Waveforms of Turn-On Transient



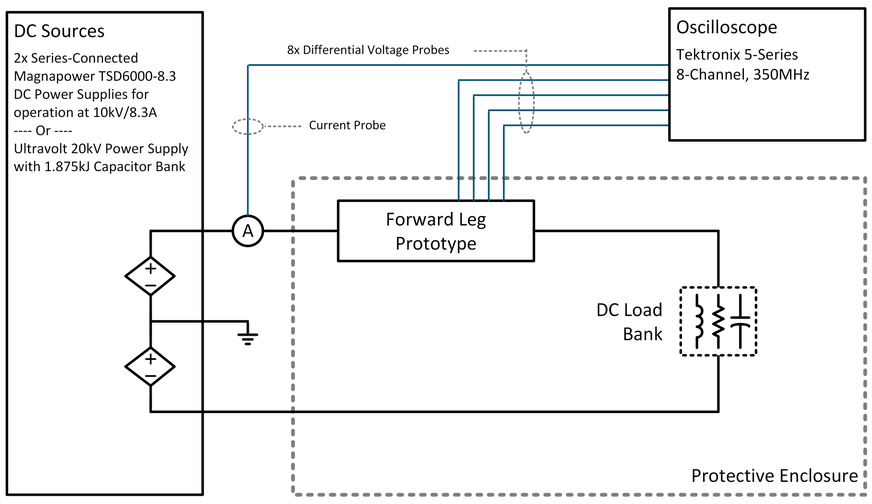
Waveforms of Turn-Off Transient



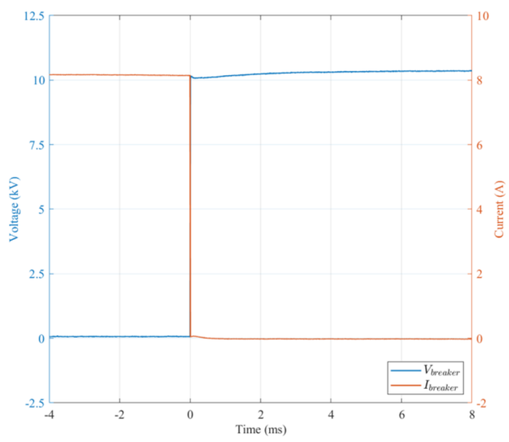


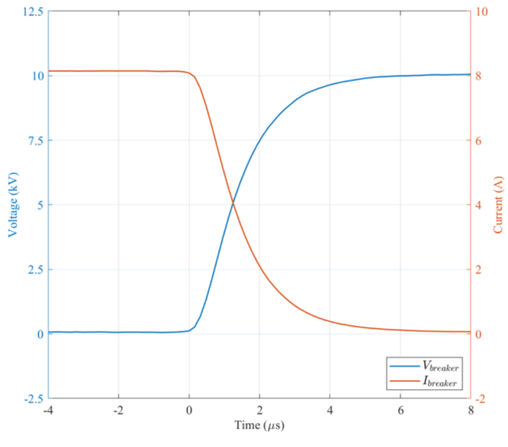
- Example using four cascaded JFETs
- Precise selection of *R* and *C* values is critical for proper management of leakage currents and effective voltage balancing performance

10 kV/8.3 A Demonstration Test

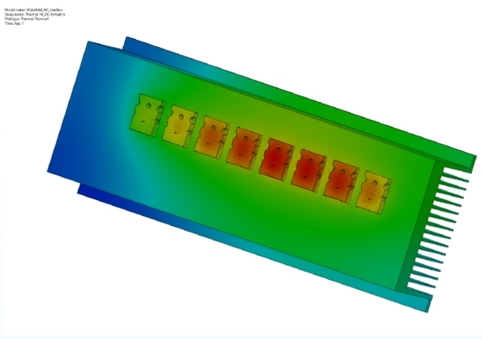


Line Voltage and Current at Millisecond (Left) and Microsecond (Right) Timescales

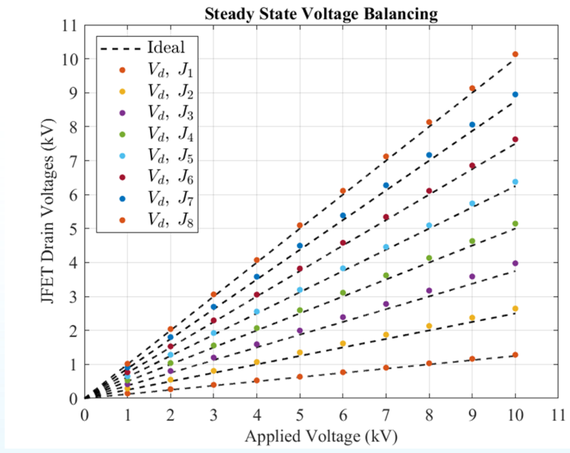


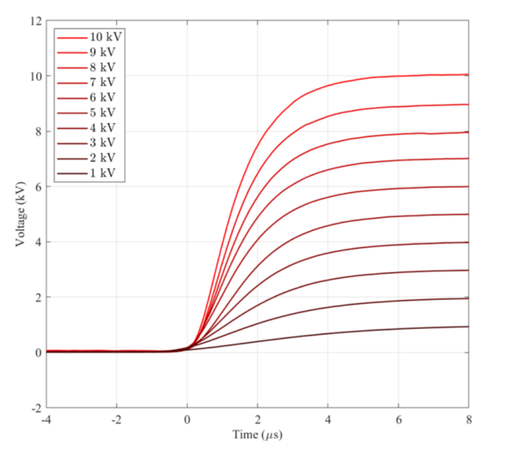


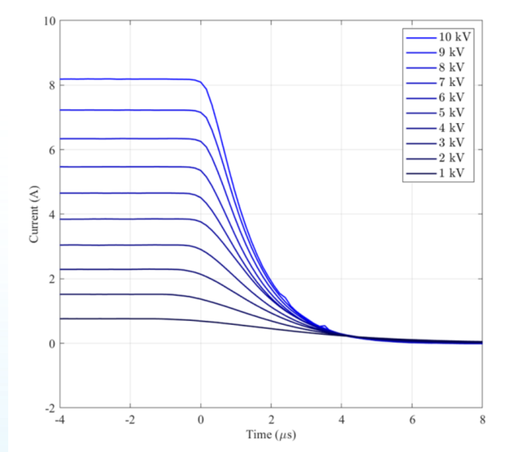
JFET Drain Voltages and Currents at 1 kV to 10 kV Voltages



Thermal Simulation at 50A with Passive Cooling







Results: Steady-State Behavior

- On-State shows high efficiency, even above rated current
- Off-State voltage balancing is accurate over a wide range of line voltages

Results: Transient Behavior

- Turn-off transient is fast (<10µs) limited by load RC values
- Passive voltage balancing is effective across large voltage ranges

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