PCB-on-DBC GaN Power Module Design with High-Density Integration and Double-Sided Cooling

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***Abstract*— Lateral gallium nitride (GaN) high-electron-mobility transistors (HEMTs) present better electrical characteristics compared to silicon or silicon carbide devices such as high switching speed and low gate charge, but also present additional challenges on the module design. This paper discusses a high-density GaN power module with double-sided cooling, low inductance, on-package decoupling capacitors, and integrated gate drivers. The GaN dies as well as the gate drive are sandwiched between the printed circuit board (PCB) and direct bonded copper (DBC) substrate to achieve compact loop and double-sided cooling effect. Design considerations and thermal performance are analyzed. A module assembly procedure is presented utilizing the layer-by-layer attachment process. Finally, a 2.7 cm × 1.8 cm half-bridge GaN power module is fabricated and tested, achieving a low power-loop inductance of 1.03 nH, and the overshoot voltage of the switching waveform is less than 5% under a 400-V/25-A double-pulse test. The thermal resistance is 0.32 K/W, verified by simulation and experimental results. The design and assembly process can be generalized and applied to high power applications to achieve high power density and high performance.**

***Index Terms*—Double-sided cooling, Hybrid PCB and DBC technology, GaN, integrated gate driver, parasitic inductance, power module.**

I. INTRODUCTION

Gallium nitride (GaN) semiconductors are being applied in many power electronics applications, especially in high-frequency, volume-constrained applications such as wall adapters, data centers, electric vehicles, and aircraft [1]–[3]. Compared to silicon (Si) and silicon carbide (SiC) devices, GaN devices can switch at a higher speed with lower on-state resistance thanks to the high electron mobility and high breakdown field, which allow GaN devices to switch a given current with a smaller size and lower switching loss [4].

Due to the high cost and low growth rate of vertical GaN devices [5], most GaN devices available today are lateral HEMTs. The GaN layer can deposit on the Si substrate, and several buffer layers should be inserted between the GaN layer and other material layers when GaN is grown on Si. There are several concerns regarding the design of GaN power modules. First, the lateral enhancement-mode (E-mode) GaN HEMTs have a minimal value of gate capacitance (C_{gs}), which enables faster switching speed. However, the fast switching speed requires more attention to the circuit design, especially the parasitic elements [6], [7]. Its lower gate threshold voltage makes the device more likely to be mis-triggered [8]. Second, ringing and overshoot at the gate signal during switching transients is another challenge for GaN devices because the margin of lateral GaN gate voltage is highly stringent. Thus, the gate loop inductance should be minimized when driving the GaN HEMTs. Third, large parasitic inductance in the power loop will cause more severe voltage overshoot and switching losses across the lateral GaN HEMTs, which decreases the reliability and shortens the lifetime of GaN HEMTs [9]. Last but not least, the heat dissipation of lateral GaN dies should be well designed because of the narrow conductive path of the lateral structure and high current density, which leads to a smaller size under a given current compared to Si and SiC. Overall, designing a reliable GaN power module requires balancing electrical performance and thermal performance.

Several literatures have discussed improved structures of power modules to maximize GaN device performance. As shown in Fig. 1(a), traditional wire bonding solutions for GaN HEMTs integration [10]–[13] are reliable and cost-effective. However, the power loop inductance is large due to the lateral power loop through the introduction of bonding wires. Implementation of through-holes in the ceramic substrate can achieve a vertical power loop to minimize power loop inductance (Fig. 1(b) [6]) but at the expense of increased cost and limited layers for design flexibility. A hybrid concept has been followed in [7], [14]–[17], as shown in Fig. 1(c). These modules use insulated metal substrate or direct bonded copper (DBC) as substrate and a regular printed circuit board (PCB) placed on the top of the substrate to integrate the decoupling capacitors and gate drive circuits. The gate loop inductance and power loop inductance are at levels of several nanohenries. With the advancement of PCB manufacturing technology, GaN HEMTs can be embedded inside the PCB, and peripheral components are integrated on the PCB surface layer, as shown in Fig. 1(d) [18]–[20]. However, the thermal performance is not attractive compared to the hybrid solution [21]. A recent effort

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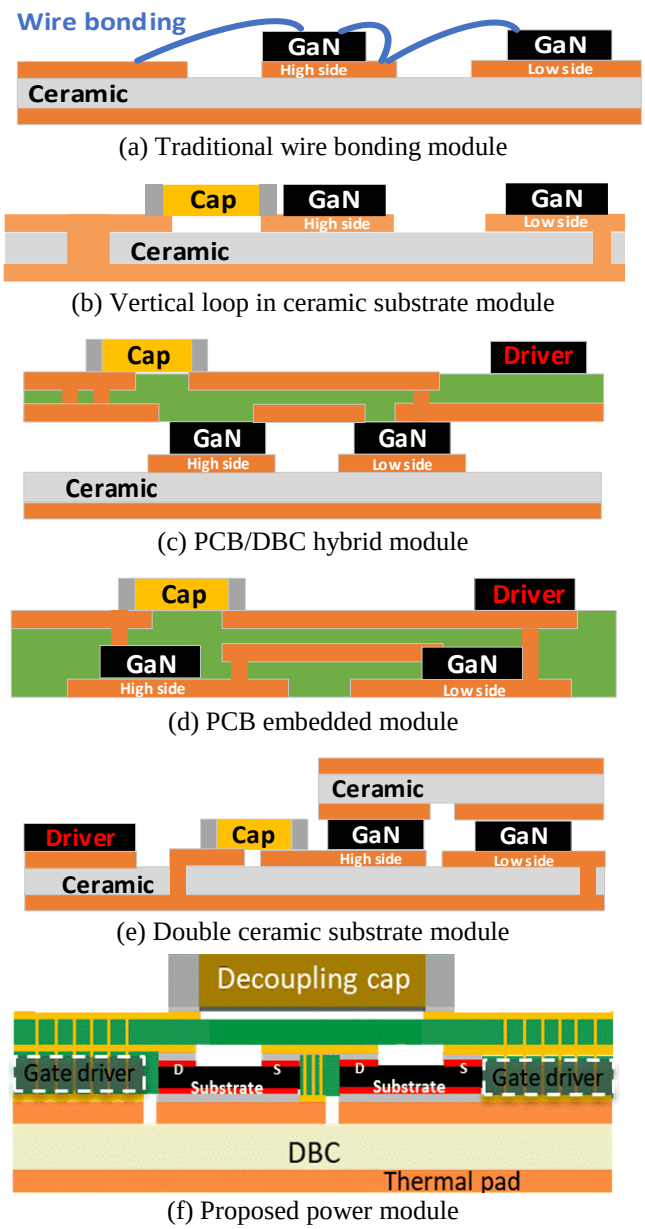


Fig. 1. Advancement of GaN power module packaging.

to improve the thermal performance of GaN hybrid power modules with integrated components is by implementing double-sided cooling (DSC). The GaN HEMTs and integrated components are sandwiched between two direct-plated copper, as shown in Fig. 1(e) [22]. However, the area of the top direct-plated copper is limited by the height mismatch between the GaN die and other components and there are limitations on the design flexibility using DBC for the power and gate loop layouts. The power module structure proposed herein employs the hybrid PCB-on-DBC structure, but with additional heat dissipation path that yields double-side cooling effect and lower thermal impedance compared to Fig. 1(c). To illustrate the design trade-off between electrical and thermal performance, Fig. 2 compares the proposed concept with the state-of-the-art packaging structures depicted in Fig. 1. Thanks to the multilayer design flexibilities in the PCB techniques, the design

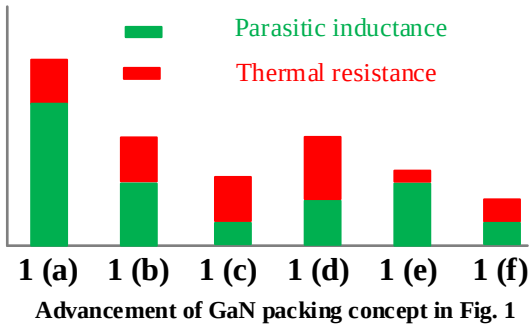


Fig. 2. Comparison of parasitic inductance and thermal resistance for 600-V and 650-V GaN power modules shown in Fig. 1.

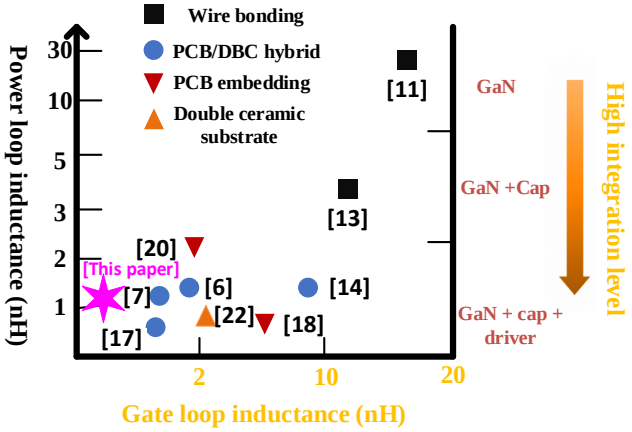


Fig. 3. Parasitic inductance and integration level of different 600-V and 650-V GaN power modules.

can be more compact and lower parasitic inductance is obtained compared to Fig. 1(e). Although the thermal resistance of the proposed module is not the lowest considering only one ceramic substrate is used, the overall performance is optimal, balancing modules the electrical and thermal performance. The comparison of these power modules' integration level regarding their power loop inductance and gate loop inductance is shown in Fig. 3. The closer to the lower left corner of Fig. 3, the lower the parasitic inductances (of both power and gate loop) and the higher the integration level of the power module.

The paper's primary contribution is the analysis, fabrication, and characterization of the hybrid PCB-on-DBC configuration that facilitates DSC and high-density integration with only one substrate for the GaN power module. The organization of the manuscript is as follows. The design considerations of the proposed module, optimization of parasitic parameters and thermal analysis are discussed in Section II in detail. The fabrication procedure to realize the PCB-on-DBC structure is described in Section III, and Section IV shows the electrical and thermal evaluations of the fabricated module. Conclusions are given in Section V. Such modules will find immediate applications in on-board chargers of electric vehicles and data centers with significantly increased power density and operating frequency.

Fig. 4. Thermal model of lateral GaN HEMT (GS-065-060). $R_{j\text{-}s}$ is the thermal resistance from junction to substrate. $R_{j\text{-}t}$ is the thermal resistance from junction to top.

TABLE I
STATIC CHARACTERIZATION OF GAN DIE

PARAMETERS	25°C	90°C	CONDITION
$R_{DS(ON)}$	20.2 mΩ	33.5 mΩ	V_{GS} = 6 V I_{DS} =20 A
$V_{GS(th)}$	1.2 V	1.5 V	V_{DS} = 10 V
C_{ISS}	500 pF	502 pF	V_{DS} = 400 V
C_{OSS}	123 pF	125 pF	V_{GS} = 0 V
C_{RSS}	1.5 pF	1.9 pF	f = 100 kHz

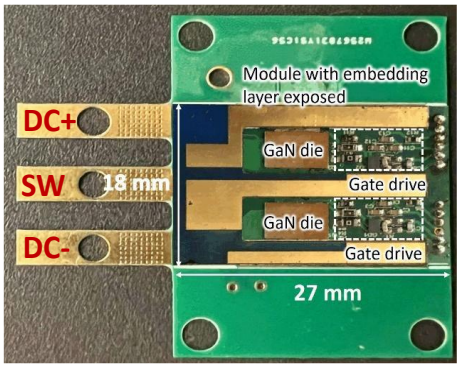


Fig. 5. Bottom view of the PCB showing gate drivers and GaN dies in the middle layer without DBC attached.

II. DESIGN OF PROPOSED PCB-ON-DBC POWER MODULE

A. Static Characterization of GaN HEMTs

Heat dissipation is a major challenge for GaN-based power modules because GaN HEMTs have smaller die areas than SiC at the same voltage and current level. Its two-dimensional (2D) electron gas layer is the conductive path where most of the heat is generated. While the substrate is the main path to dissipate the heat, a notable amount of the heat can still be dissipated through the top surface since the 2D electron gas is closer to the electrical pad. The thermal circuit of the selected GaN die (GS-065-060) is shown in Fig. 4. Considering the thermal model of the selected GaN die, adopting a DSC strategy can further improve the power module's thermal capability [23].

To gain an in-depth understanding of the performance of the selected GaN die, the curve tracer B1505A from Keysight was used to conduct a static characterization at different temperatures. Table I shows the impact of temperature on the on-state resistances ($R_{DS(ON)}$), gate-source threshold voltages ($V_{GS(th)}$), input capacitance (C_{ISS}), output capacitance (C_{OSS}), and reverse transfer capacitance (C_{RSS}). The $R_{DS(ON)}$ of the tested

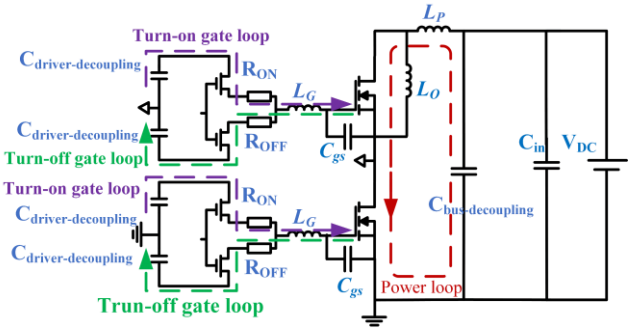


Fig. 6. Key parasitic inductances and components in half-bridge power module circuit

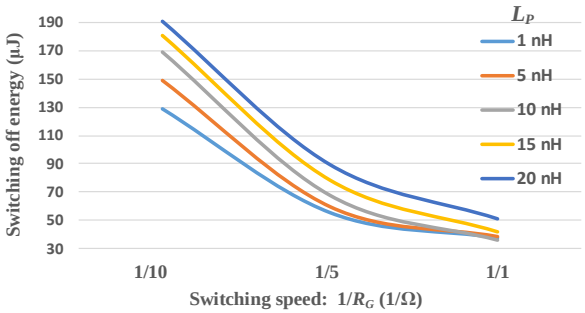
devices increases by more than 60% when the temperature is elevated from 25 °C to 90 °C. The $V_{GS(th)}$ increases slightly while capacitances (C_{ISS}, C_{OSS}, C_{RSS}) remain the same. Overall, the GaN die presents a temperature-sensitive resistance, low threshold gate voltage, and small capacitances compared to Si and SiC power devices. These characteristics enable fast-switching capability, but also add extra challenges on the gate loop design. Section II. D discusses the gate drive circuit design in detail to address these challenges.

B. Proposed PCB-on-DBC Structure

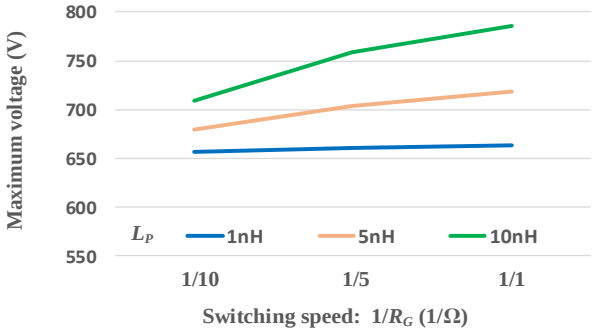
Fig. 1(f) shows the cross-section view of the power module, which has a multilayer PCB on the top and DBC at the bottom. The hybrid structure adopts the benefit of both low-cost PCB and highly thermally conductive DBC substrate. Two GaN dies are placed in the middle layer sandwiched between the PCB on the top and the DBC on the bottom, as shown in Fig. 5. The substrate and source of GaN dies are connected by thermal vias filled with copper to assist the heat dissipation. Therefore, two paths are formed to dissipate the heat: one through the substrate, where the die is attached to the DBC directly; and the other from the top side of the die through the PCB thermal vias to the DBC. The DBC substrate is leveraged for both sides' heat dissipation so that DSC is achieved. The decoupling capacitors and gate drivers are integrated into the multilayer PCB to reduce the parasitic inductance in both the power loop and the gate loop. An electromagnetic interference filter is also integrated with the module on the top of the PCB to improve the noise attenuation, which is elaborated in [24] and thus omitted herein. In the end, the highly integrated power module has a size of 2.7 cm × 1.8 cm targeting applications of <10 kW.

C. Power Loop Design and Optimization

The parasitic power loop inductance in a half-bridge power module induces the voltage overshoot and affects the switching loss [26], [27]. The influence of the power loop inductance becomes more severe for extremely fast-switching GaN devices. Fig. 6 shows the key parasitic parameters in the proposed half-bridge power module, including power loop inductance L_P and gate loop inductance L_G. The circuit components also include two GaN dies, bus decoupling capacitors, gate driver and drive decoupling capacitors. A 650-V/30-A double-pulse test (DPT) simulation is established shown in Fig. 6, in which an inductor is used as the output inductor to short the upper die and the lower die is the device



(a)



(b)

Fig. 7. Power loop inductance's impact on the (a) switching-off energy and (b) voltage overshoot.

under test. To illustrate this issue, GS66508T from GaN Systems is selected [28] and results are presented in Fig. 7. The switching speed represented by $1/R_G$ is changed by the gate resistor R_G within the range of 1–10 Ω. Higher switching speed (i.e., smaller R_G) reduces the switching transient period and results in significantly lower switching loss (see Fig. 7(a)), but increases the drain current slope di/dt and results in higher voltage overshoot (see Fig. 7(b)). The voltage overshoot occurring on top of the steady-state voltage V_{dc} in the switching transient is related to the di/dt and power loop inductance L_p by

$$V = L_P \frac{di}{dt} + V_{dc} \tag{1}$$

Large voltage overshoot poses high voltage stress (e.g., 800 V) across the device that goes beyond the maximum transient voltage (i.e., 750 V) of the GaN device, which will cause device failure and reduced lifetime. Therefore, the power loop inductance needs to be minimized to get both low voltage overshoot and low switching loss. In the example shown in Fig. 7(b), the power loop inductance needs to be less than 5 nH with 5-Ω gate resistance to keep the voltage below the 750-V limit.

To minimize the power loop parasitic inductance, a vertical power loop layout is desired, as lateral loop design still results in relatively large inductance [10]–[13]. The conceptual design of the proposed PCB-on-DBC power module is based on the concept of a vertical power loop. The parasitic inductance is reduced significantly due to the self-cancellation of magnetic flux. The GaN dies are placed into the cavity layer inside the multilayer PCB to minimize the vertical distance without sacrificing the design flexibility. The integration of decoupling

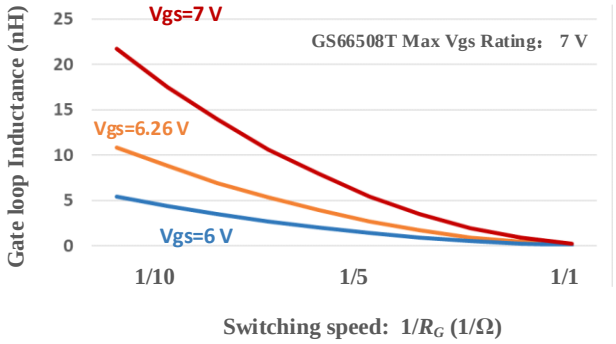


Fig. 8. Parasitic gate loop inductance's impact on the gate voltage overshoot.

capacitors on the top also helps to decouple the busbar inductance and leads to extremely low power loop inductance. The perpendicular distance, or the board thickness, is selected as 0.4 mm due to the PCB manufacturing limits. The PCB layout of the geometry shown in Fig. 5 is imported to ANSYS Q3D for parasitic inductance extraction, where the power loop inductance yields 1.27 nH.

D. Gate Loop Design and Optimization

The gate loop parasitic inductance is also important for GaN module designs. Lateral E-mode GaN HEMTs have a small gate capacitance (C_{gs}) and low threshold voltage, which make the device more likely to be mis-triggered. Moreover, its gate-voltage range is highly stringent (e.g., −10 V to 7 V), so the maximum tolerable voltage at gate for the selected GaN chip is only 1 V if using 6 V to turn on.

The gate loop parameters include the gate resistance R_G, the gate loop inductance L_G, and the gate-source capacitance of the device C_{gs} as shown in Fig. 6. Most practical gate designs adopt the Kelvin connection to avoid the common-source inductance-associated issues in the gate loop [29], [30]. Therefore, the common-source inductance L_{CS} is not considered in the circuit model. The dynamic response of the turn-on path is a form of a second-order system. The expressions for relative overshoot voltage ($\sigma\%$) and damping ratio (ξ) are as follows:

$$\sigma\% = e^{\frac{-\pi\xi}{\sqrt{1-\xi^2}}} \tag{2}$$

$$\xi = \frac{R_G}{2}\sqrt{\frac{C_{iss}}{L_G}} \tag{3}$$

From the equations above, either increasing the gate resistance or reducing the loop inductance L_G will decrease the gate voltage overshoot. However, large gate resistance will decrease the switching speed and increase the switching loss (Fig. 7(a)). Thus, small gate loop inductance is preferred to minimize the voltage overshoot without reducing the switching speed. Under a given maximum voltage limit at the gate, the maximum gate loop inductance allowed can be calculated by (2) and (3). Fig. 8 shows the relationship between gate loop inductance and gate resistance under different overshoot voltages when using 6 V to turn on. The C_{iss} value for the device

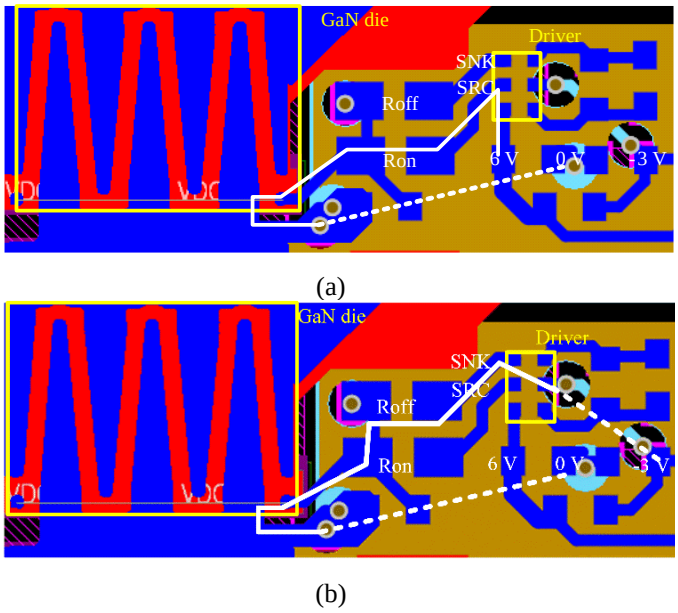


Fig. 9. PCB layout showing (a) turn-on gate loop and (b) turn-off gate loop.

selected is 242 pF [28]. Smaller gate loop inductance allows the use of smaller gate resistance (with high speed and low loss) without exceeding the maximum gate voltage of the selected GaN device.

Therefore, a compact GaN power module integrated with gate drivers is necessary. In the proposed power module, the gate drivers are integrated close to the GaN dies to reduce the gate loop area as shown in Fig. 9. In addition, a gate driver with small footprints (1EDN7550U) is selected to further reduce the gate loop area. The simulated turn-on and turn-off gate loop inductance of the upper die are 0.32 nH and 0.29 nH, respectively; and those of the lower die are 0.30 nH and 0.34 nH, respectively. According to (3) with a damping ratio of 0.5, the minimum gate resistance allowed at the pull-up path of the gate driver is found to be 1.6 Ω. In the end, a 5.1-Ω gate resistance is adopted in the turn-on loop for the margin of safety, while the internal gate resistance of the 1EDN7550U is 0.85 Ω.

During the turn-off transient, the turn-off gate resistance selection is based on the Miller effect. The high *dv/dt* is generated by the turn-on of the complementary switch, which creates a current through the Miller capacitance and then tries to sink in the gate driver. The current flowing through the turn-off gate resistor generates a gate-source voltage. If this voltage is higher than the threshold voltage, it may lead to a false turn-on. The calculation of the maximum turn-off gate resistance is calculated as [31] in (4).

$$R_{OFF} \le \frac{V_{thG}}{C_{gd} \times \frac{dv}{dt}} = \frac{1.7\ V}{1.8\ pF \times 200 \frac{V}{ns}} = 4.7\ ohm \qquad (4)$$

To increase the switching speed, the external turn-off resistance is chosen as zero, while the internal gate resistance is 0.35 Ω. This choice considers both the impact of the parasitics issue and the Miller effect.

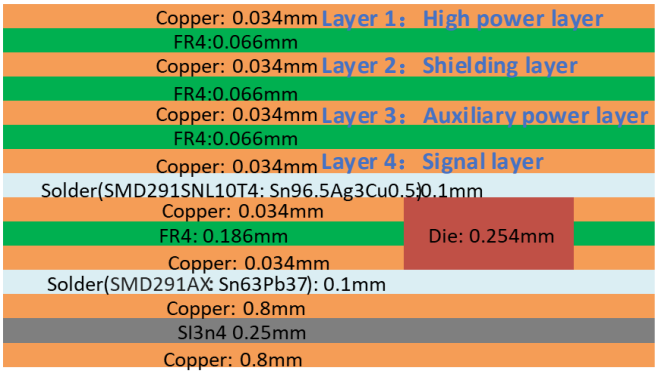


Fig. 10. Layer stack of proposed power module.

TABLE II
COUPLING CAPACITANCES BETWEEN POWER NODE (V_{DC}) AND HIGH-SIDE SIGNALS

	VDC+ TO PULSE-WIDTH MODULATION	VDC+ TO AUXILIARY POWER (−3 V)	VDC+ TO AUXILIARY POWER (6 V)
With shielding layer	0.00 pF	0.01 pF	0.00 pF
Without shielding layer	4.68 pF	7.5 pF	1.7 pF

E. Cross-Coupling Capacitance Minimization

Overlapping conductor layers induce coupling capacitances that provide noise traveling paths harmful to the switching condition. Take the half-bridge circuit as an example; an extremely high *dv/dt* is generated at the switch node since the voltage swings between the bus voltage (VDC+) and the ground (VDC−). The coupling capacitance between the power nodes (e.g., VDC+ and switch node) and the signal nodes (e.g., gate drive) could cause coupling noises that lead to falsely triggered switches. Therefore, it is critical to decouple the power layers and the signal layers by using shielding layers (see Fig. 10) for high-frequency GaN module designs. Take the high-side GaN HEMT as an example; all signals are referenced to the high-side ground by the shielding layer with the same potential as the high-side ground, so that the coupling capacitances between the VDC+ and the signal traces are minimized. The coupling capacitance on the high side with the shielding layer is simulated in Ansys Q3D and compared to those without the shielding layer, as listed in Table II. It shows a significant reduction in coupling capacitance with the shielding.

F. Thermal Performance Evaluation

Fig. 11 shows the traditional single-sided cooling hybrid GaN power module. The heat is dissipated through the DBC only. As discussed in the previous section, 70% of the heat of the GaN die is dissipated through the bottom, and 30% of heat is dissipated through the top. The equivalent DSC is applied to the proposed power module, and the steady-state thermal performance is compared to a counterpart with single-sided cooling using the same GaN die, outline dimensions, and thermal boundary. The power loss of each GaN die is set as 5 W, and the temperature at the module exterior is kept constant

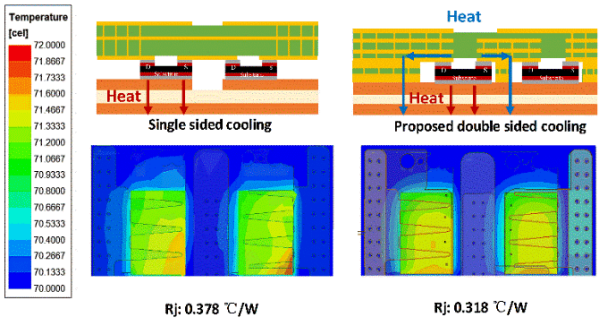


Fig. 11. Thermal simulation setup and results of single-sided cooling and double-sided cooling.

TABLE III
COMPONENTS IN POWER MODULE PROTOTYPE

COMPONENT	VALUE	PART
GAN DIE	650 V/ 60 A	GS-065-060
DRIVER		1EDN7550U
TURN-ON RESISTOR	5 Ω	RCS06035R10FKEA
TURN-OFF RESISTOR	0 Ω	HCJ0603ZT0R00
DRIVER DECOUPLING CAP	1 μF	CGB2A1X5R1E105K033BC
BUS DECOUPLING CAP	0.3 μF	C4532X7T2J304M250KA

at 70 °C. All the layer stack information used in the Ansys Icepak simulation are shown in Fig. 10. The thermal vias diameter is 0.2 mm based on the capabilities offered by the PCB manufacturer. According to the simulation results shown in Fig. 11, the proposed equivalent DSC further reduces the junction-to-case thermal resistance to 0.318 K/W due to the additional path dissipating heat from the top side of the die. Given that the geometry of these two configurations is identical, except for the absence of the cavity board, we can obtain from parallel relationship that the estimated value of the top thermal resistance is approximately 2.008 K/W. Employing larger thermal vias will further reduce the thermal resistance.

III. POWER MODULE FABRICATION

The components used to fabricate the power module are listed in Table III. The GaN die used in the module has a size of 6.0 mm × 4.0 mm × 0.27 mm. For the PCB-on-DBC power module, the gate driver selection is critical since the size and thickness should be comparable to those of the GaN dies. In this design, 1EDN7550U [32] is chosen due to the small PG-TSNP-6 package with a size of 1.5 mm × 1.1 mm × 0.375 mm. The 0.1-mm difference in the thickness between the gate driver and GaN die can be evened by screen printing the soldering layer. The decoupling capacitance should be higher than 100 times of the C_{oss} of the selected die [33] and is chosen as 1 μF to reduce the influence of inductance on the power loop. To realize the hybrid PCB and DBC structure, a layer-by-layer lamination process is adopted as shown in Fig. 12. The detailed process is described as follows:

1) The power module board and cavity board are fabricated. The power module PCB have 1-oz copper, and the thickness is 0.4 mm to ensure a low power loop inductance. The cavity PCB is selected to have a thickness of 0.254 mm to be aligned with the GaN die thickness. It has through-hole plated vias filled with copper to achieve better thermal performance.

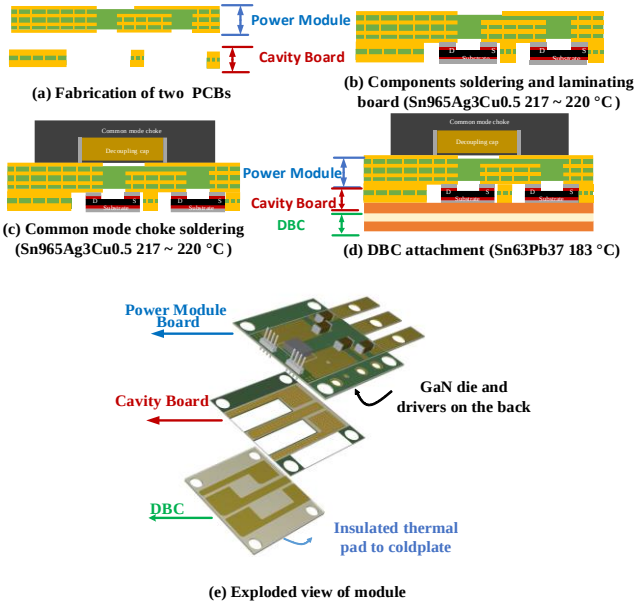


Fig. 12. Fabrication process of the proposed GaN power module.

2) A 100-μm-thick stencil board is used to screen print the solder paste Sn96.5Ag3.0Cu0.5 with a melting temperature of 217°C on the bottom layer of the power module PCB. The Sn96.5Ag3.0Cu0.5 is recommended by the GaN die manufacturer because of its good fluidity, which ensures an even solder layer to avoid voids. After the GaN dies, gate drivers and the cavity PCB are placed on the power module PCB, and the power module PCB is reflowed in the T-962A reflow oven under a suitable temperature profile [34] with the top layer facing down.

3) The bus decoupling capacitors and the common mode choke are hand-soldered onto the top layer of the power module with the Sn96.5Ag3.0Cu0.5 solder wire.

4) A second reflow profile is used to attach the DBC substrate to the power module board with the cavity board. This step requires careful handling to prevent the solder in the previous step from melting. The ceramic material of DBC in the proposed power module is AlN with high thermal conductivity compared to other ceramic materials, and the thickness of copper metallization on both sides is 0.2 mm. The Sn63Pb37 solder paste is selected in this step with a melting temperature of 183 °C, which is lower than that of the solder used in Step 2. First, the solder paste is applied to all the pads on the DBC, and the DBC is attached to the power module with the cavity PCB. Second, the whole power module with the DBC layer facing down is heated by a hot plate, and a thermocouple is used to closely monitor the temperature until it reaches 185°–195°C. The ramp rate is kept below 0.3°C/second to avoid damaging.

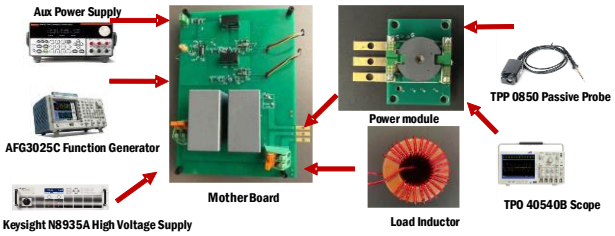


Fig. 13. Double-pulse test prototype setup.

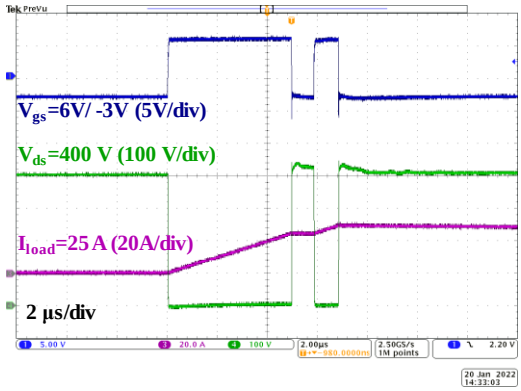


Fig. 14. Switching waveforms obtained from the double-pulse test under 400 V and 25 A.

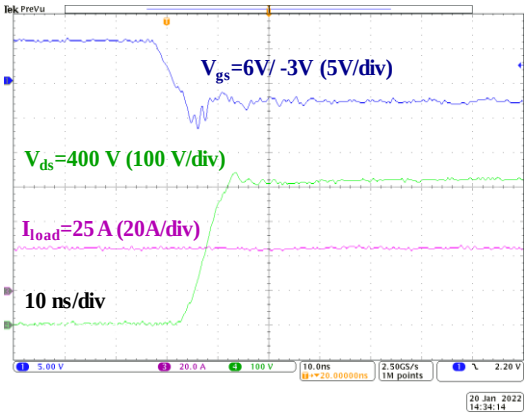


Fig. 15. Zoom-in view of switching waveforms at the turn-off transient showing low overshoot and fast *dv/dt*.

IV. Power Module Characterization

This section focuses on the electrical and thermal characterizations of the power module. The electromagnetic interference performance of the power module with integrated common mode choke is discussed in [24]-[25] and omitted herein.

A. Electrical Characterization of the Proposed Power Module

A double-pulse test circuit was built as shown in Fig. 13 to characterize the power module's electrical performance. A static -3 V was applied at the gate of the top GaN die, and the bottom die was the device under test. The power module was tested at 400-V DC-bus voltage and 25-A load current at room temperature (25 °C), and the characterization results of the hard-switching transition for the proposed power module are shown in Fig. 14. A 1,000-V passive probe (TPP0850) was used to capture the drain-to-source voltage. The bandwidth is up to 800 MHz, and the input capacitance is 1.8 pF to minimize the probe's loading effect on the circuit. The bandwidth of the probe should be high enough to capture the rise/fall time, as well as the high-frequency oscillation of the fast-switching transient of the GaN device.

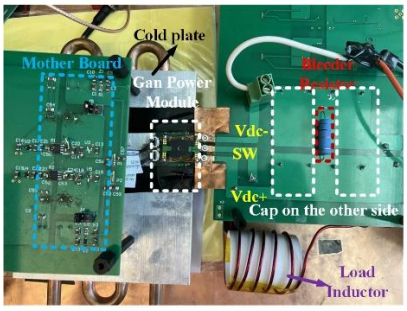


Fig. 16. Experiment setup of 500-W/600-kHz buck converter using the proposed power module.

The turn-off transient is shown in Fig. 15. The overshoot voltage across the die is less than 5% of the static voltage at 25 A, and no appreciable undershoot is observed in the gate loop, even with 0-ohm external gate resistor. Moreover, the loop inductance extracted from the ringing frequency yields 1.03 nH using the following equation:

$$L_{loop} = \frac{T^2}{4\pi^2\left(C_{oss} + C_{para} + C_{probe}\right)} = \frac{2.3\ ns^2}{4\pi^2(127 + 1.5 + 1.8\ )\ pF} = 1.03\ nH \quad (5)$$

where C_{oss} is the output capacitance of GaN die, C_{para} is the parasitic capacitance induced by the PCB layout, and C_{probe} is the capacitance induced by the passive probe. As shown in Fig. 3, both the power loop inductance and gate loop inductance are among the lowest of comparable designs. Moreover, the module has low thermal impedance thanks to DSC, and the fabrication does not involve any exotic process.

B. Continuous Switching Test of the Power Module

Based on the proposed hybrid power module with the DSC design, a buck converter is built for the power module with the integrated gate drivers to demonstrate the continuous switching performance. Fig. 16 shows the experimental setup, and the heat dissipation method is liquid cooling. The proposed power module is placed on the cold plate with a thin layer of thermal interface material in between. The input voltage is set to 120 V with a duty cycle of 0.5. The output power of the converter is kept at 500 W when the switching frequency is 600 kHz with zero-voltage switching to minimize switching loss and avoid any shoot-through. As shown in Fig. 17, the drain-source voltage is very clean, which indicates the proposed GaN power module works very well at 600 kHz. The module is actually designed to be capable of handling higher power and frequency. However, a higher power level was not tested due to the selected gate driver's operation limits [32]. Our future work involves modifying the module such that gate drivers for

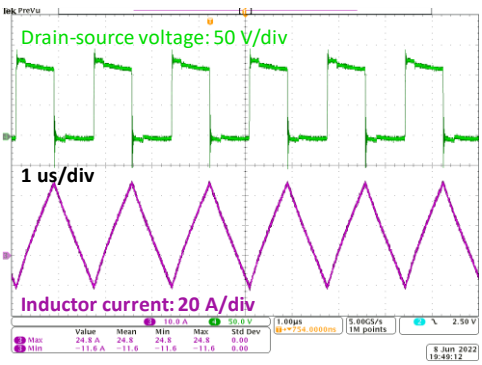


Fig. 17. Buck converter experiment waveforms of the proposed power module with 500-W output power and 600-kHz switching frequency.

higher-power operation can be accommodated into the sandwiched structure, which will be reported in subsequent publications.

C. Thermal Characterization of the Proposed Power Module

For thermal characterization of the GaN power module, the devices were first shorted and connected to a power supply. The heat generated within the devices by reverse conduction was controlled by the power supply's output voltage and current settings and was ramped from 1 W to 12 W. A thermoelectric generator was placed in the thermal path to confirm dominate pathway of GaN heat loss flow. Four thermocouples were also placed at key locations of interest to measure ambient, heat sink, bottom of the package, and top of the package temperatures. These thermocouple measurements were compared to a revised thermal model that replaced the liquid cold plate with a heat sink. Fig. 18 shows the experimental thermal setup and corresponding thermal model. The thermal model results and experimental measurements exhibited similar temperatures through the package, as shown in Fig. 19. More accurate measurements of all interface layers (solders and grease) would further improve the model correlation.

V. Conclusion

A compact PCB-on-DBC GaN half-bridge power module with DSC, low inductance, low thermal resistance, and integrated gate drivers has been proposed. Hybrid PCB and DBC technology is explored with multiple layer attachment as a cost-effective solution to achieve DSC and enhanced design flexibility. The experimental results validate the module performance under 400-V/25-A double-pulse test with 1.03-nH power loop inductance and less than 5% overshoot voltage. In the continuous switching test, a 500-W buck converter is built based on the presented GaN module with an operating frequency of 600 kHz. Furthermore, the proposed module is verified with thermal characterization results that show low junction-to-case thermal resistance of 0.32 K/W. In the future, the module will be tested under higher frequency and power level with updated gate driver integration and substrate selection for improved module reliability.

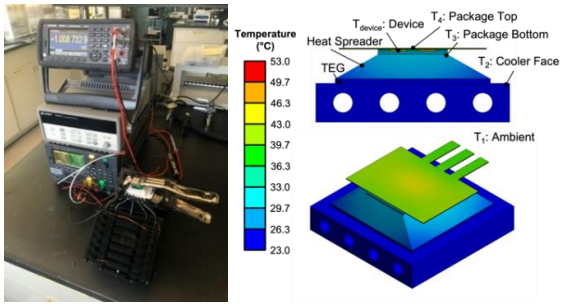


Fig. 18. Experiment thermal setup of the GaN power module, power supply, thermoelectric generator, and heat sink with corresponding thermal model.

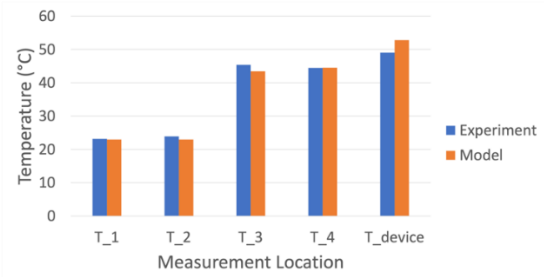


Fig. 19. Experimental thermocouple measurements compared to the thermal model with 10 W of module heat loss.

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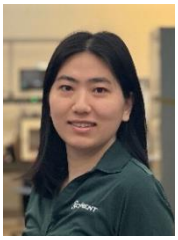

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