SAND2022-13367C

The Effects of Gamma Ray Integrated Dose on a Commercial 65nm SRAM Device

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Dose-Rate Testing

Conventional Single-Event Testing:

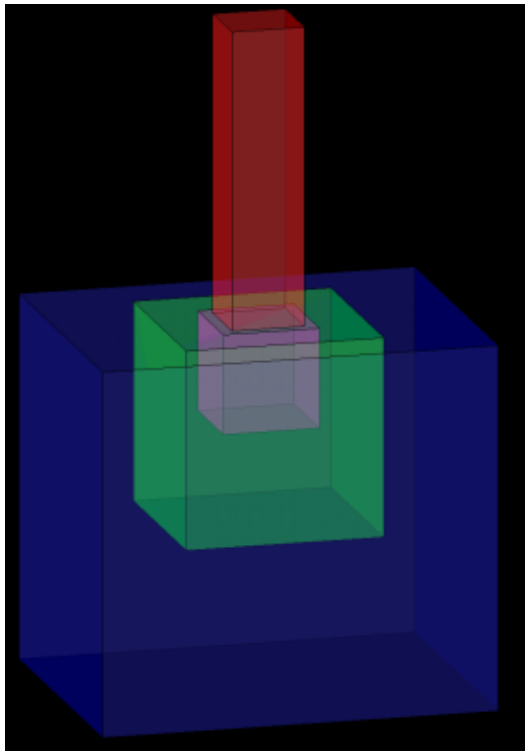
- Continuous particle beam
- Low rads(Si)/s
- Often long runtimes
- Capturing transients, upsets, latchups + measure cross-section of effect

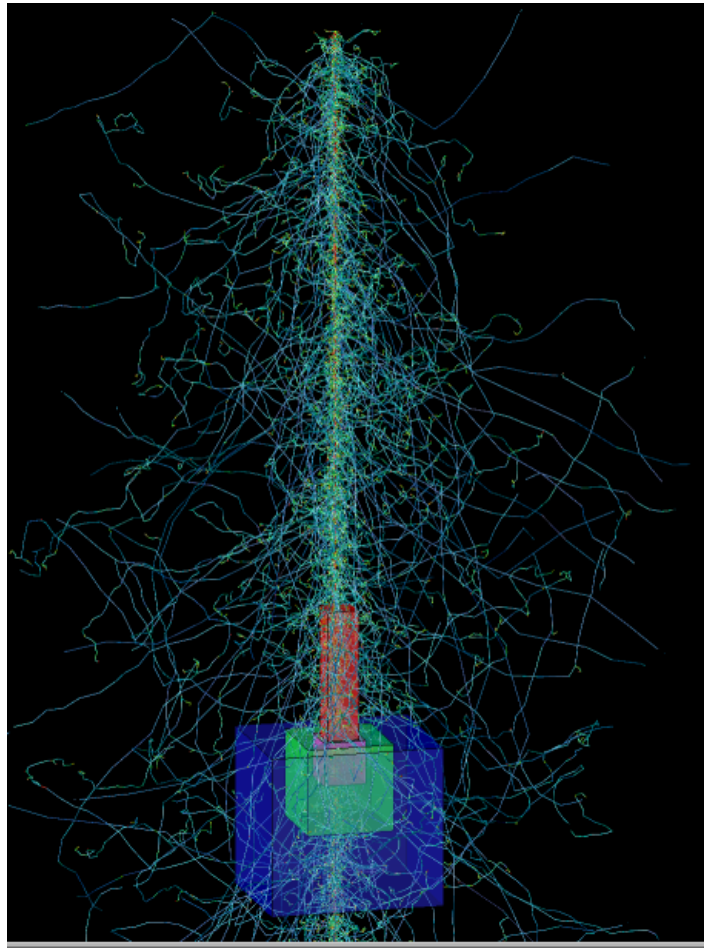
Dose-Rate Testing:

- High dose rate, for example 1e8 rads(Si)/s
- Short pulse width (50ns – 100μs)
- Focus on device response (upsets, damage)

Traditional dose-rate testing: effects at a given dose-rate

Our experiments: effect of dose-rate *and* dose



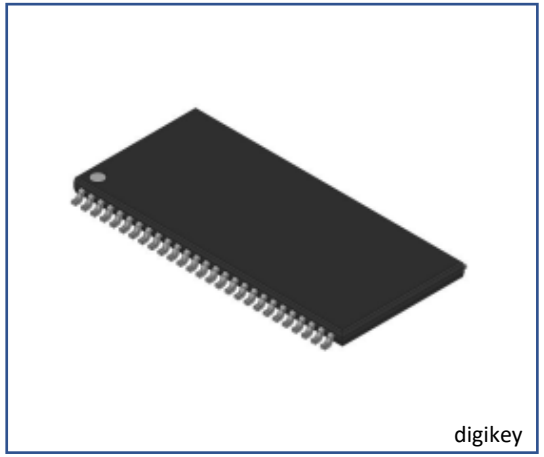


SRAM Dose Rate

- **Goal:** Explore behavior of commercial SRAM in dose-rate testing, varying several parameters.

- Why SRAM?
  - Simple, highspeed device – can collect lots of data fast
  - Commonly building block of more complex devices
  - Often one of the most “soft” components of a system

- Our DUT:
  - CY7C1069GN SRAM from Cypress (now Infineon)
  - 65nm CMOS
  - 8-bit transfers
  - 2 Chip Enables
- General Methodology:
  - Write values to SRAM → Provide dose → Read SRAM + count bit upsets
  - Repeat ***MANY*** times, varying dose-rate, and pulse width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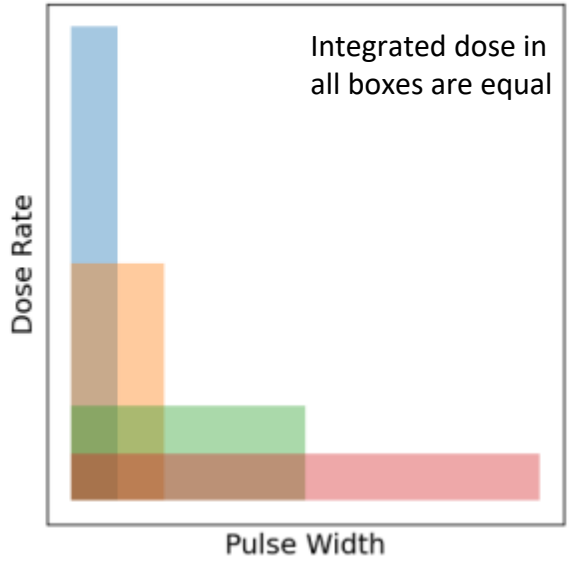

Little Mountain Test Facility (LMTF)

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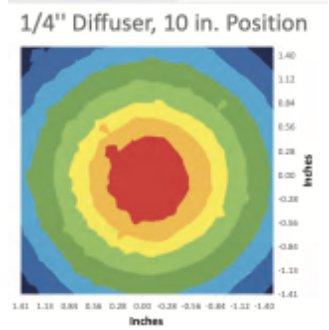
- Little Mountain Test Facility (LMTF)
  - Hill Air Force Base, Ogden Utah
  - LINAC (Dual Electron Gun)
  - Prompt Pulse & Long Pulse

- User control of dose rate, pulse width
  - Dose rate: table position
  - Pulse width: 50ns - 100µs

- Consistent and repeatable
- Rapid pulse rate

- The high configurability of this facility allows us to provide a large **exploration of the effects of dose rate and pulse width.**



Experiment Steps

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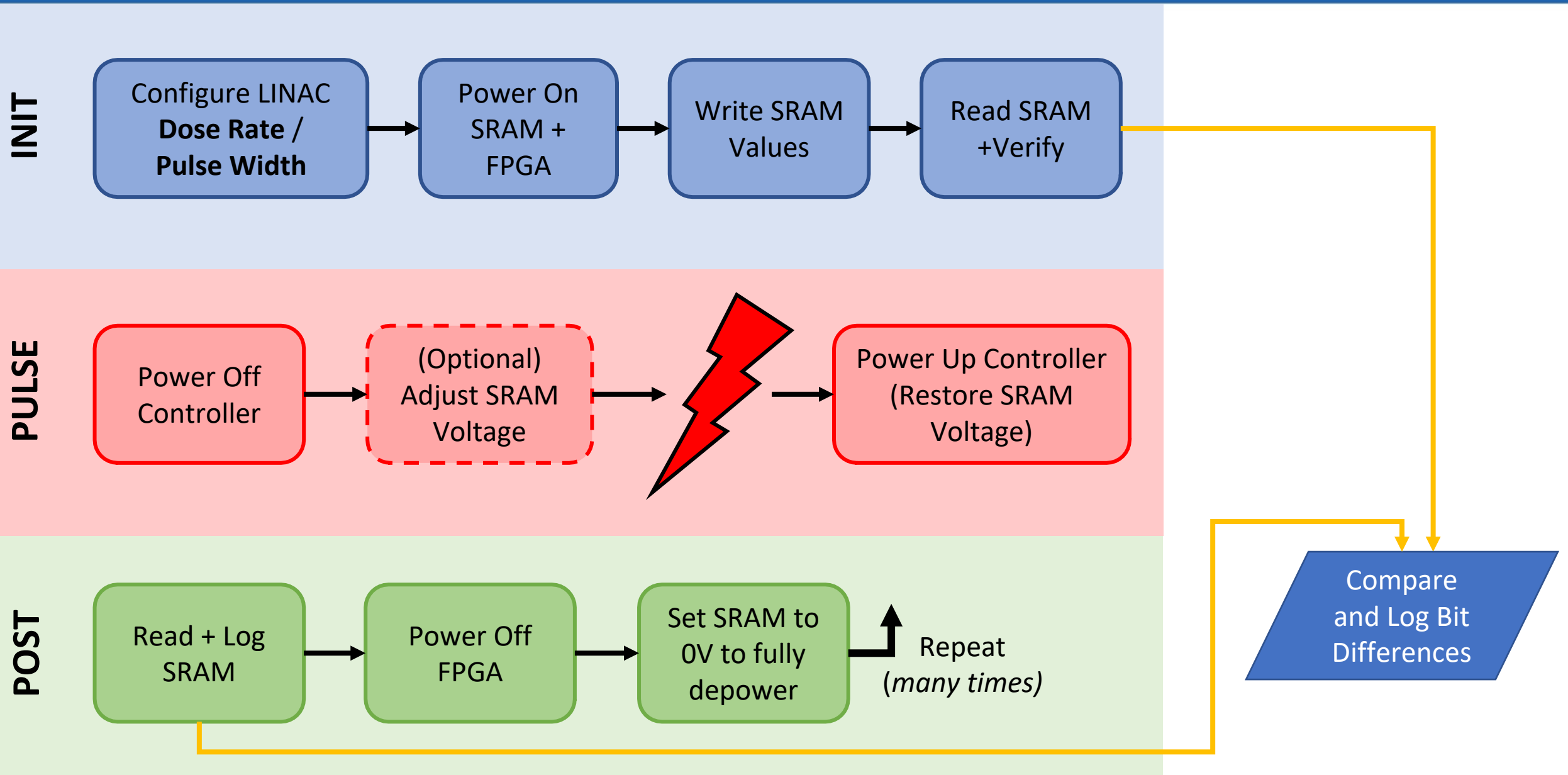
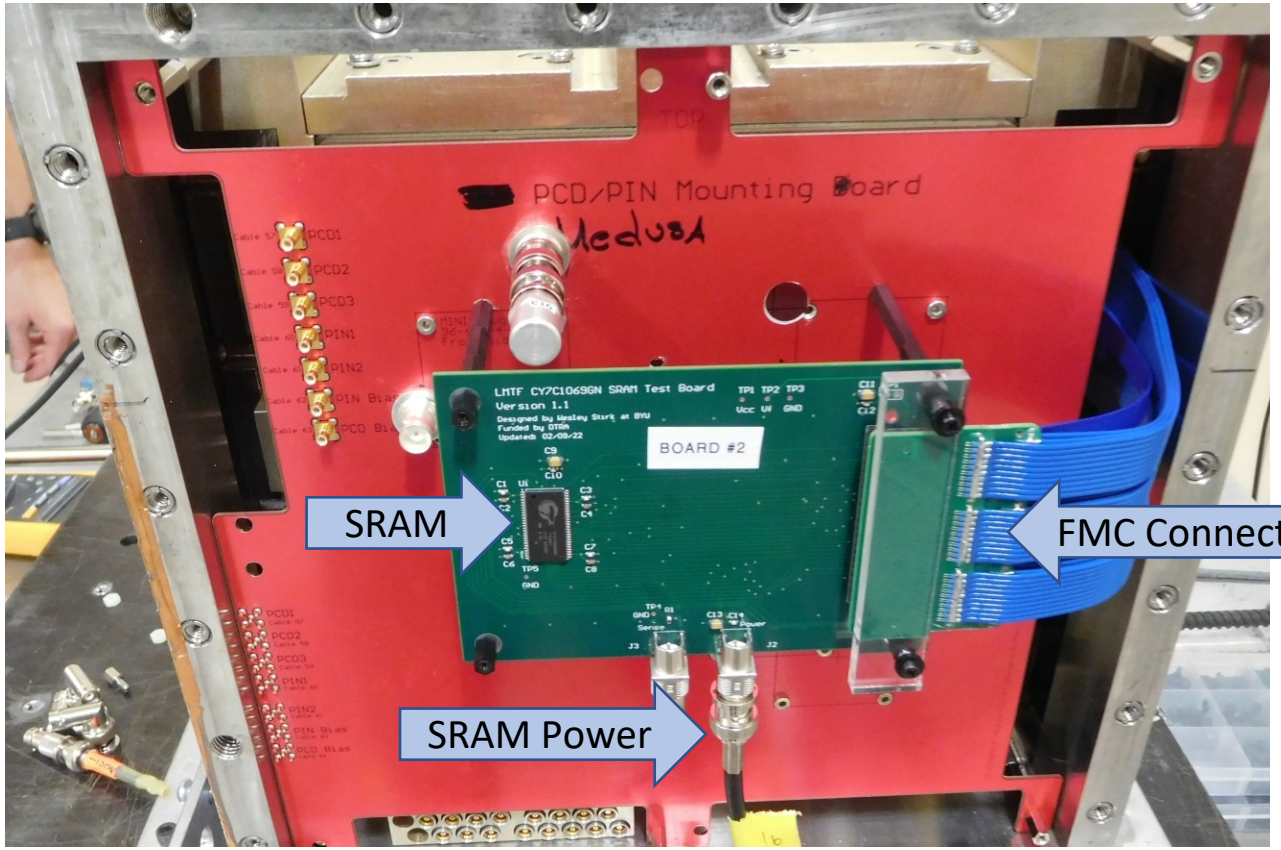
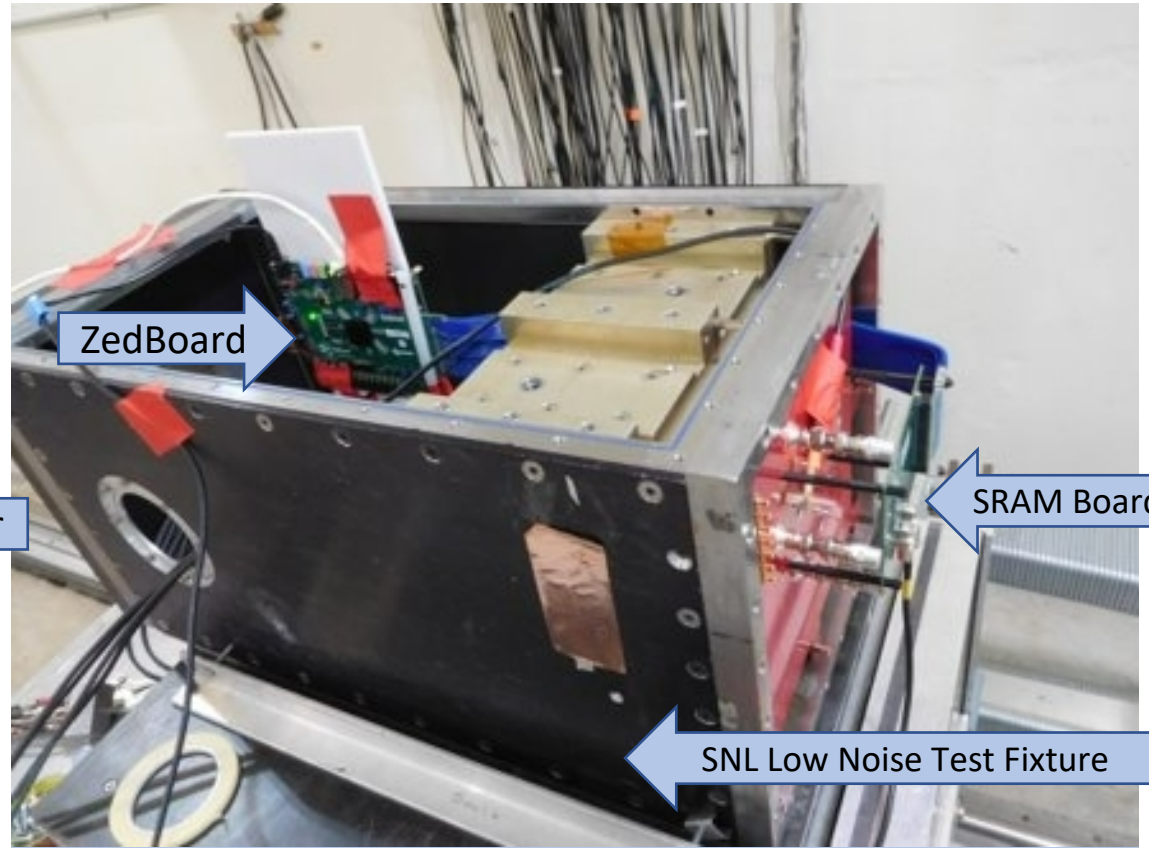
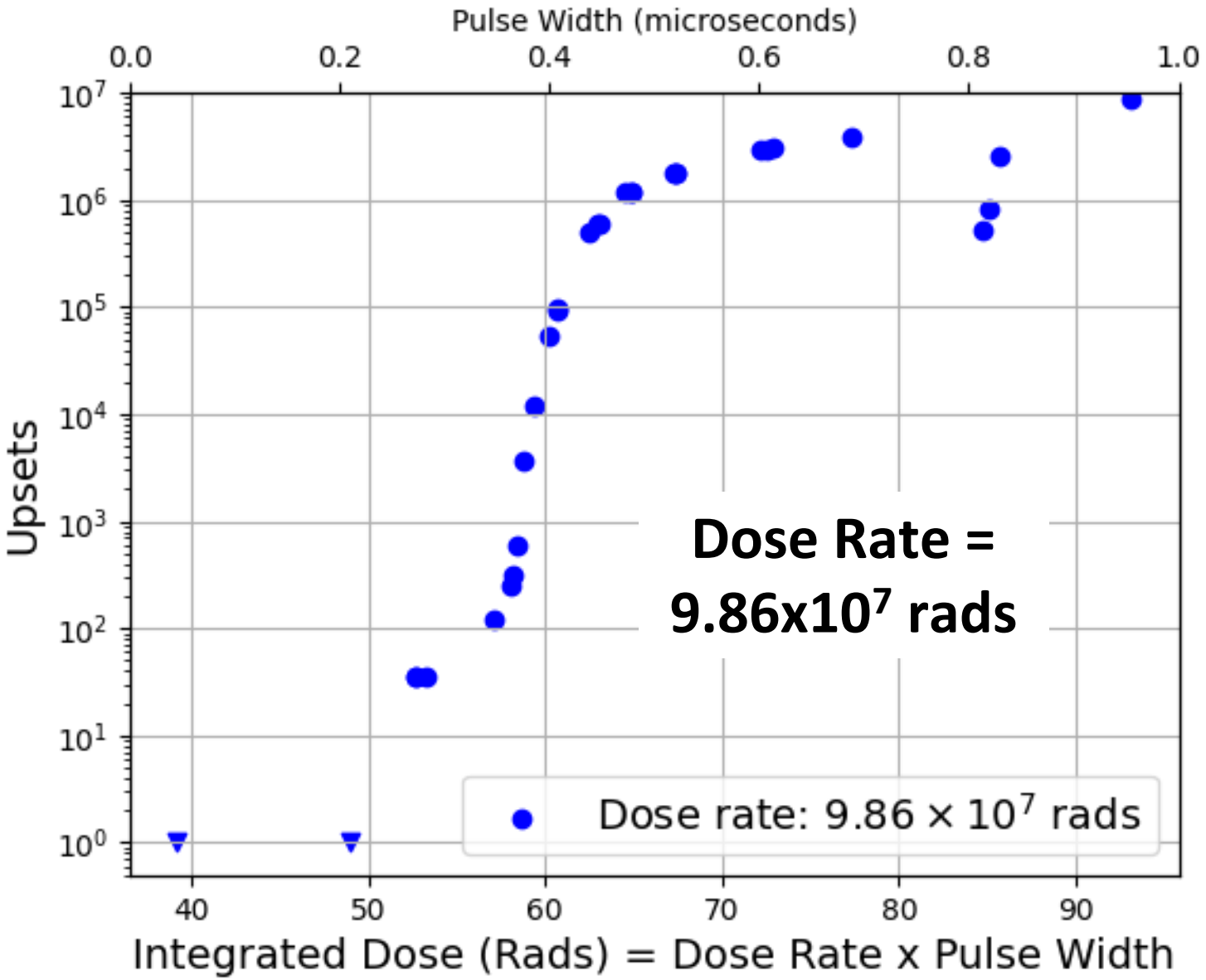


Equipment Setup





Varying Pulse Width at Fixed Dose Rate



31 total data points

Step function-like Behavior:

- No upsets detected < 50 rads(Si)
- Saturated Upsets > 75 rads(Si)

Saturation: ~Half of the bits are upset

Exploration of Dose Rates / Pulse Widths

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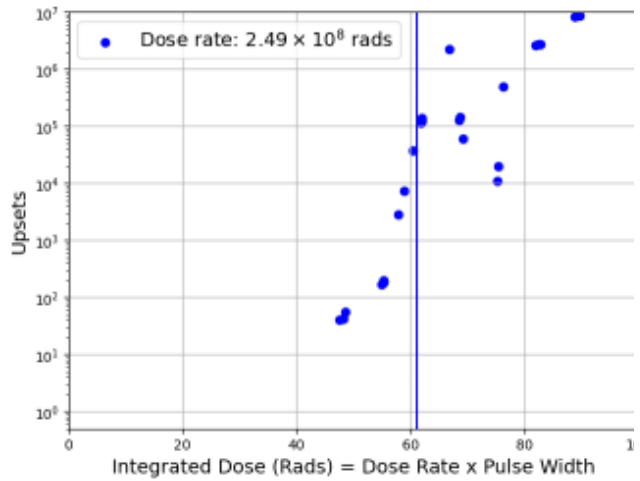
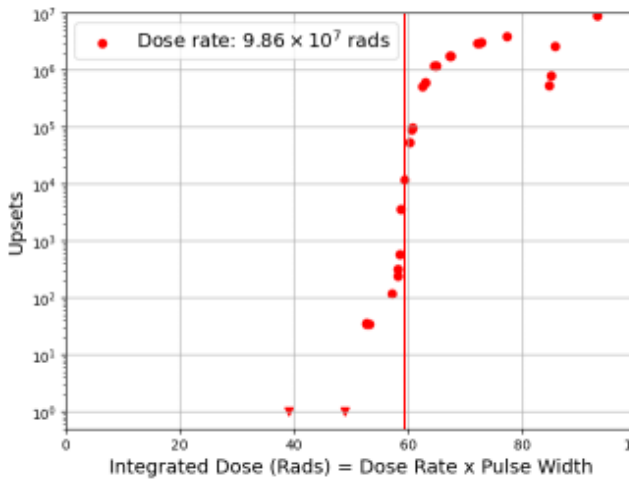
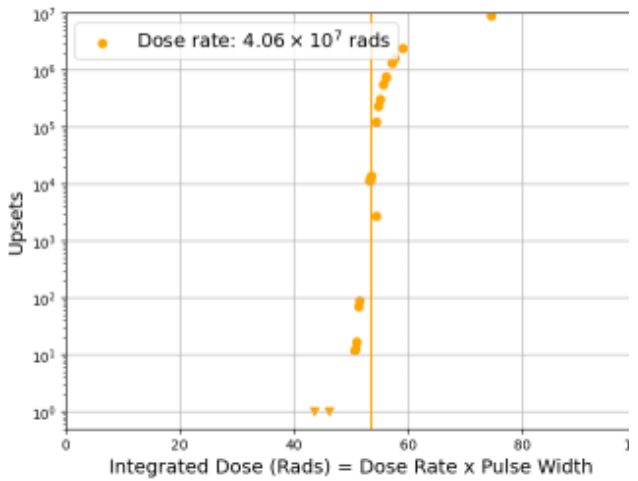
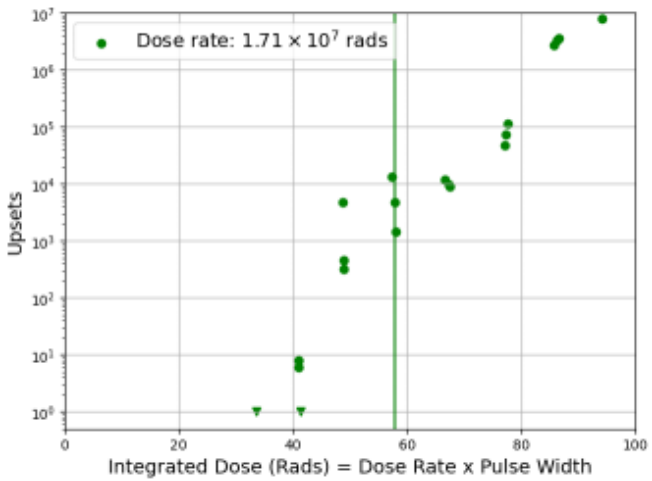
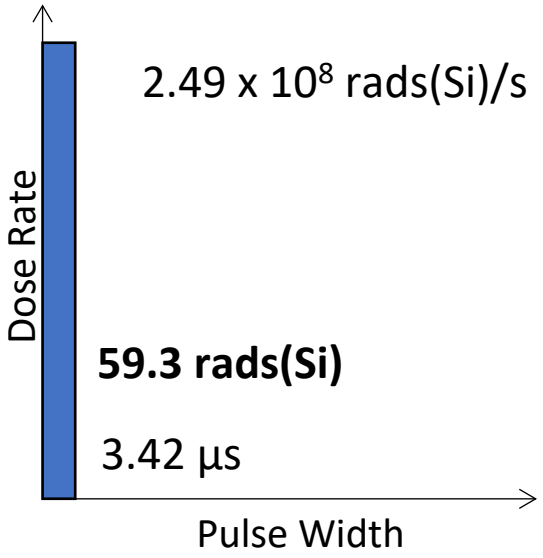
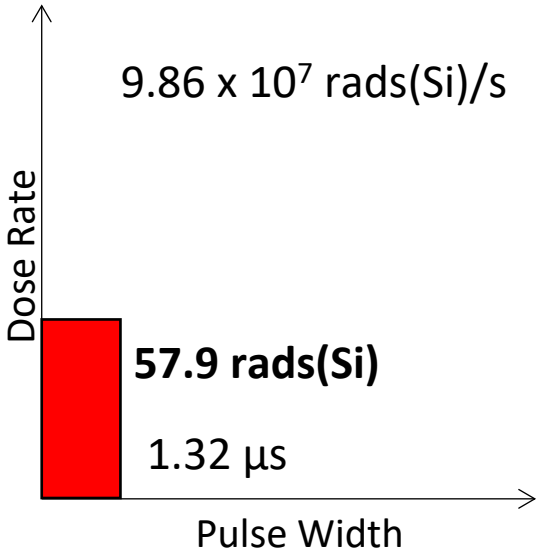


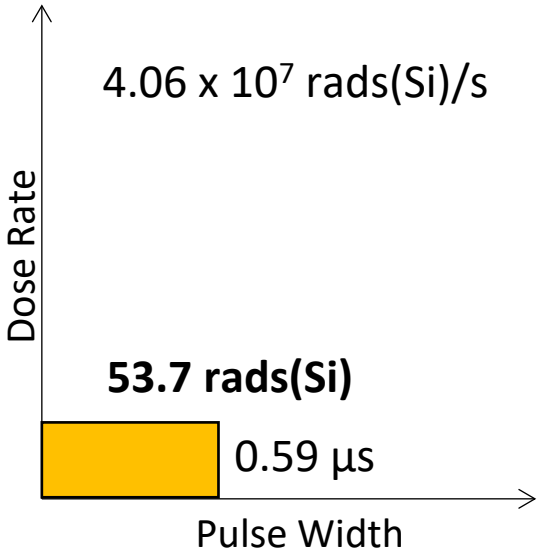


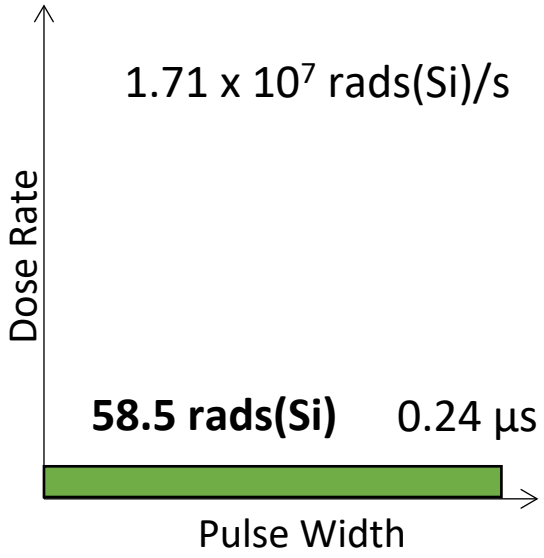






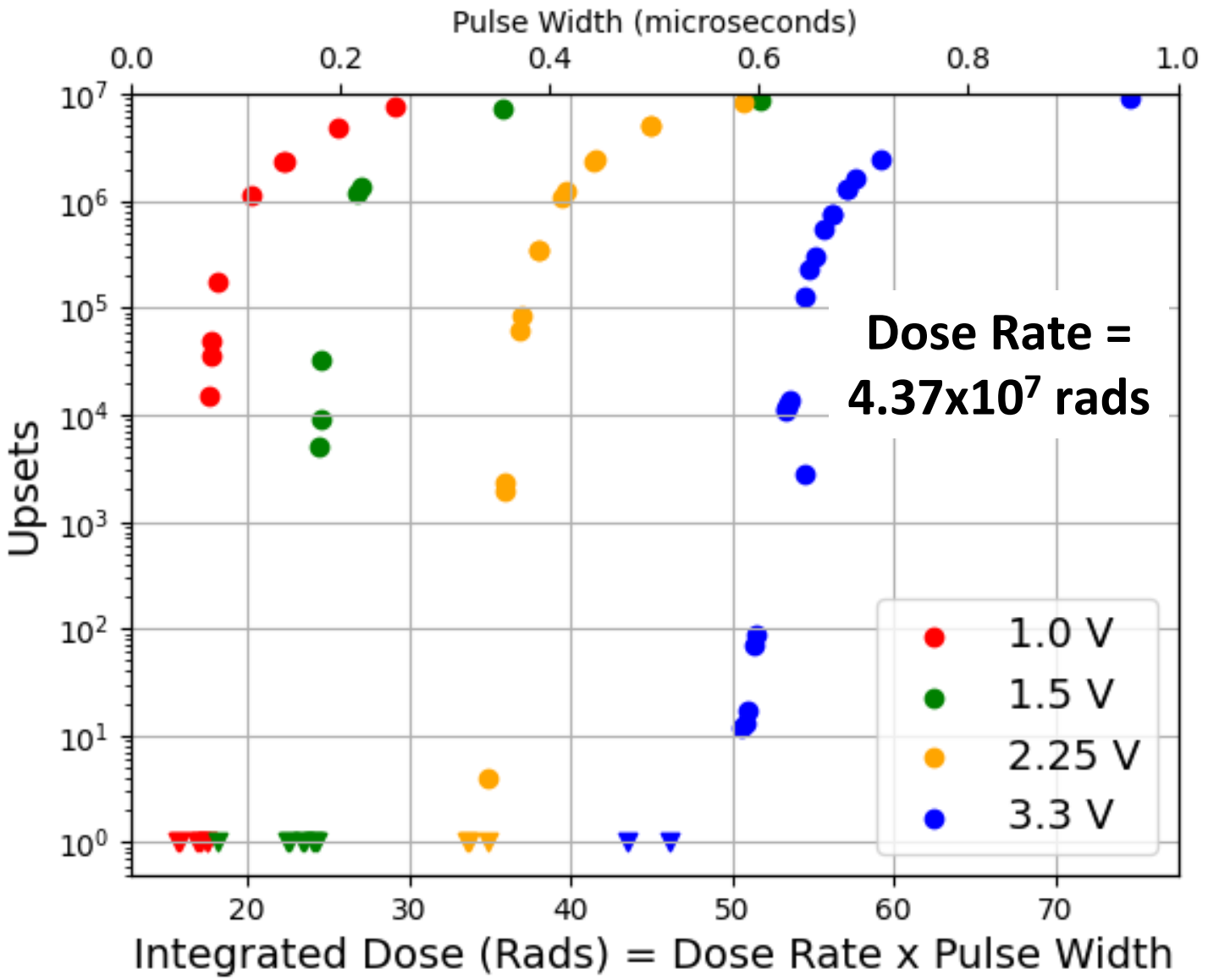






Key Takeaway: Upset rate is highly dependent on ***integrated dose*** (and much less so on *dose rate*)

Effect of SRAM Voltage on Upset Rate



As SRAM voltage decreases, less integrated dose is required to reach the step function.

Normal Operation – 3.3V

Data Retention – 1.0V

Effect of SRAM Fill Value

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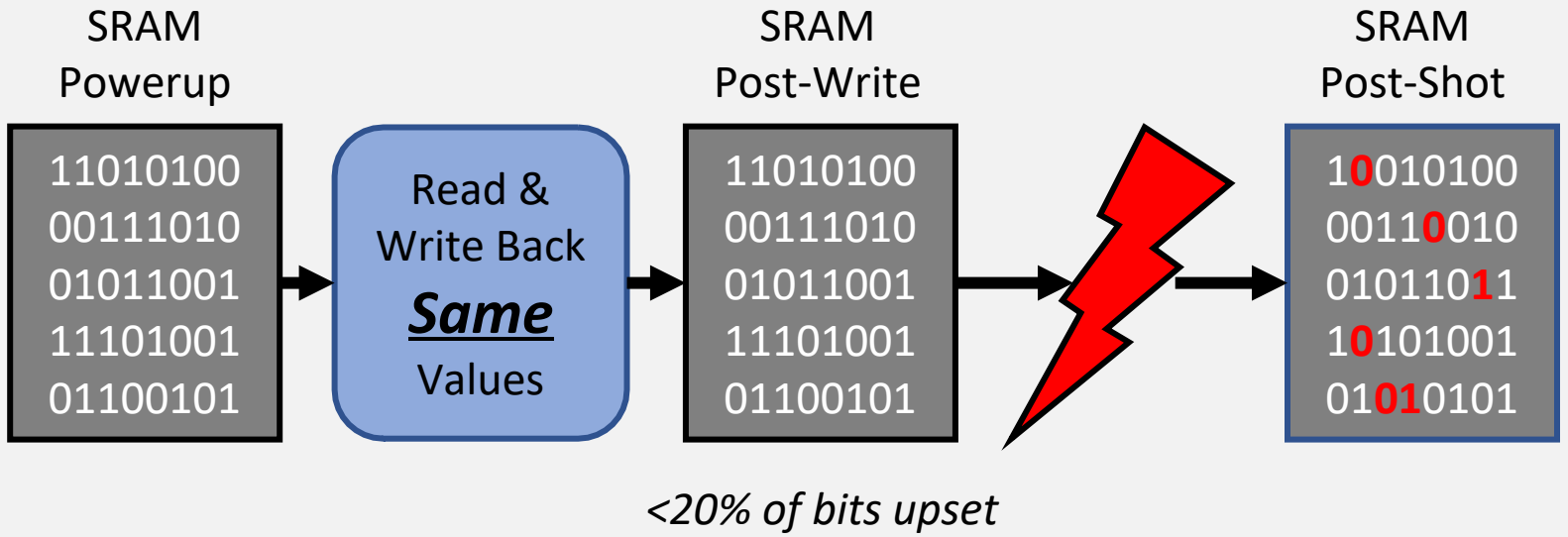
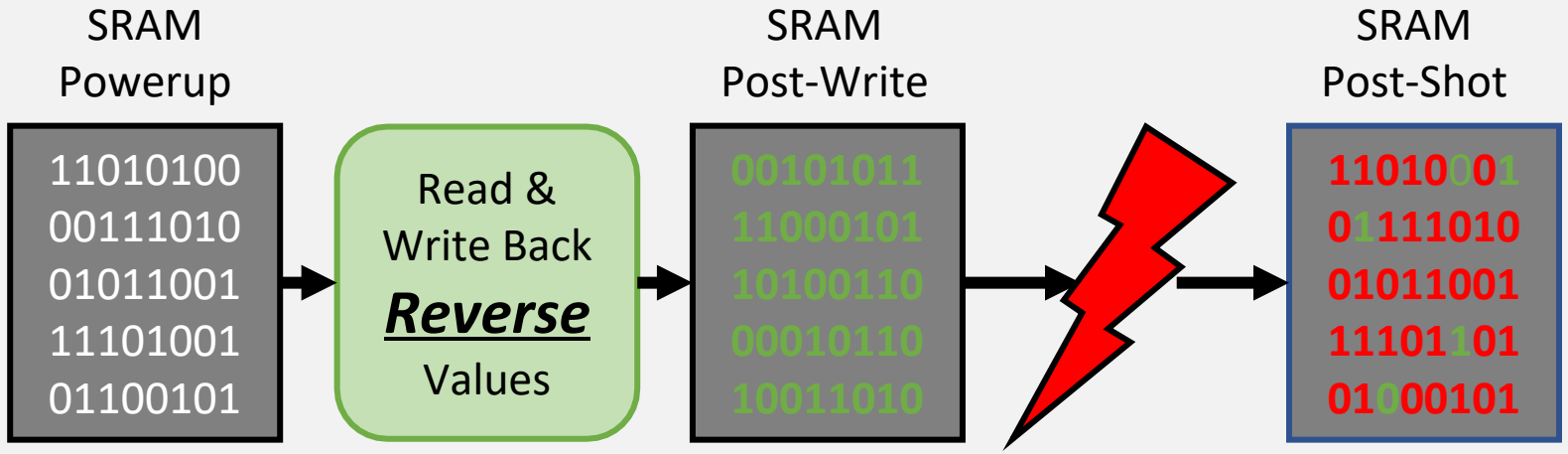


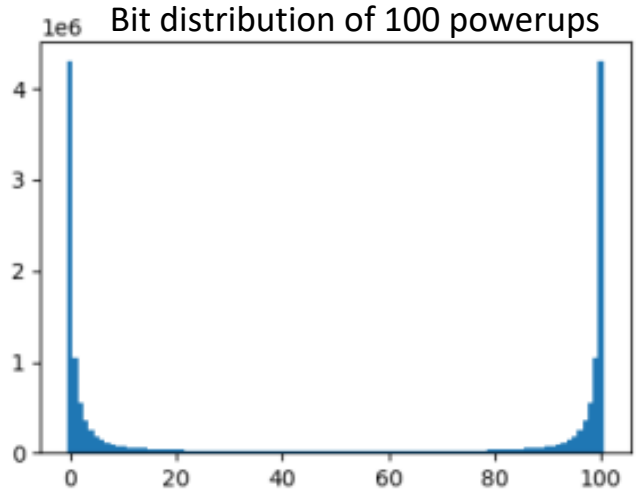
<20% of bits upset



>80% of bits upset

What is going on?

- SRAM has a preferred powerup state.
- Most bits always power up as a 0 or 1.



Key: This suggests integrated dose is causing mechanism similar to power reset.

Mechanism

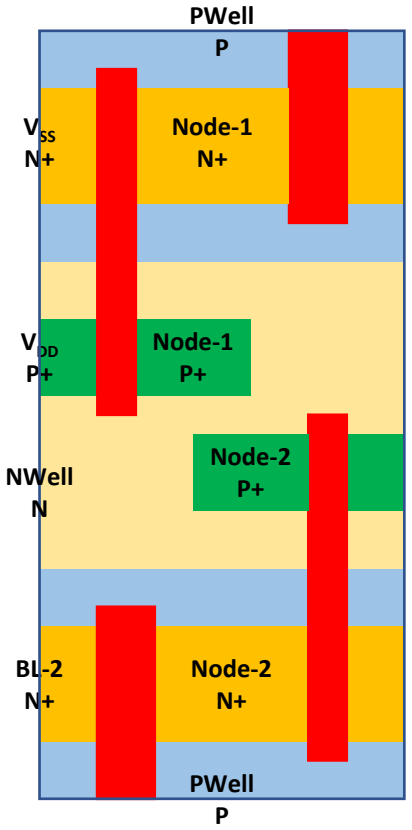
We believe the photocurrent is causing a depletion of charge in the transistor wells.

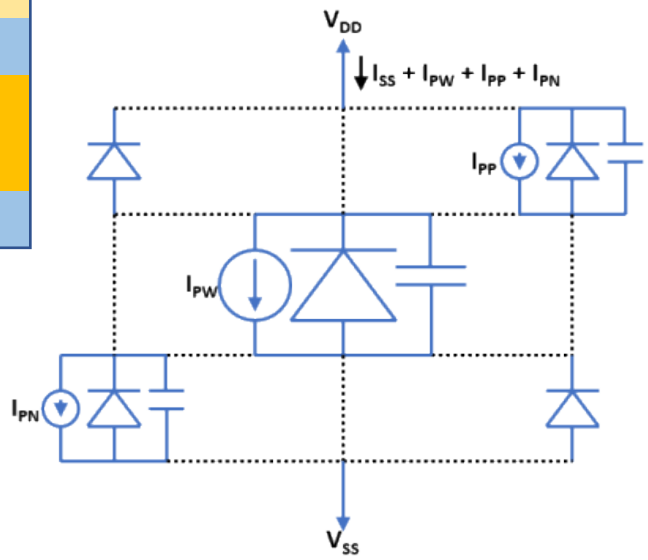
Voltage loss overcomes noise margin, results in data corruption

This model is supported by our results:

1. Upset “step function” mostly a function of integrated dose.
2. Lower voltages require less integrated dose.
3. Corrupted SRAM usually returns to its power-on state
4. (Although not in these slides) At low dose rates, it appears the power delivery can keep up with the photocurrent charge depletion.

Details of mechanism are currently being investigated





Summary

- Explored dose-rate effects of a commercial 65nm SRAM
  - Dose rates: 1.87×10^6 to 2.49×10^8
  - Pulse widths: 50ns to 100μs

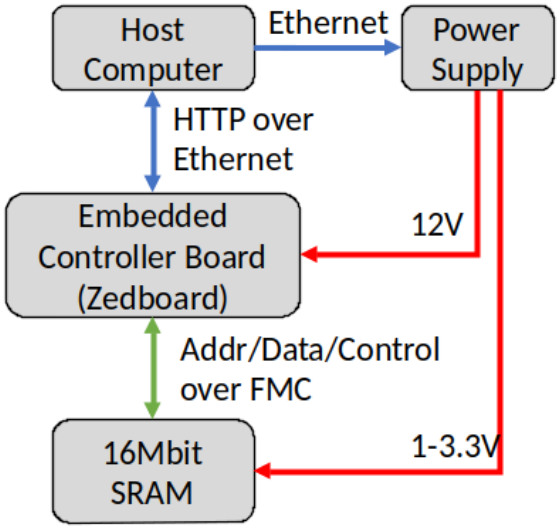
- Developed a highly automated test harness and procedure, which allowed us to sweep parameters and collect a large amount of data

- Trends:
  - Failure step function dependent on **integrated dose.**
  - Requires less integrated dose at low voltages
  - SRAM bits appeared to strongly favor switching to preferred power-up state.

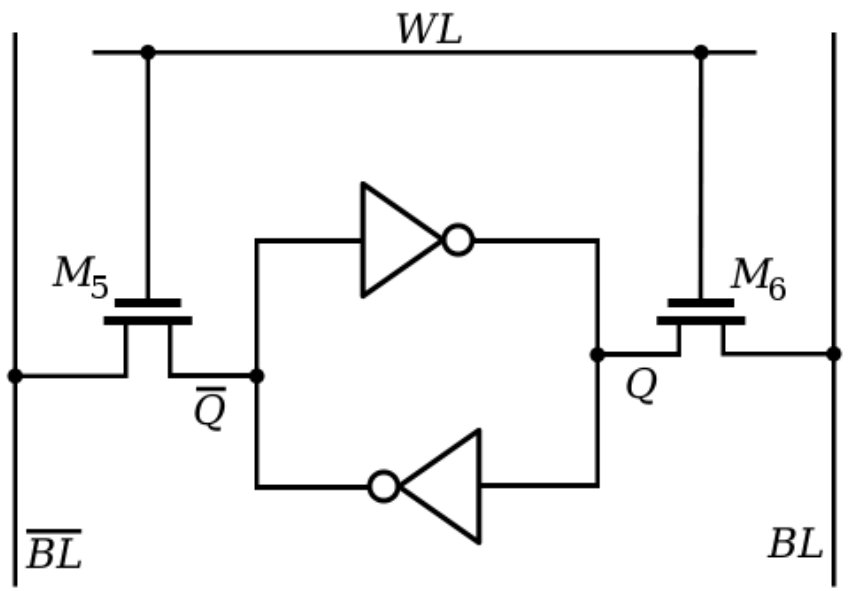
We believe the effect we are observing can be explained by a transistor well collapse caused by the photocurrent.

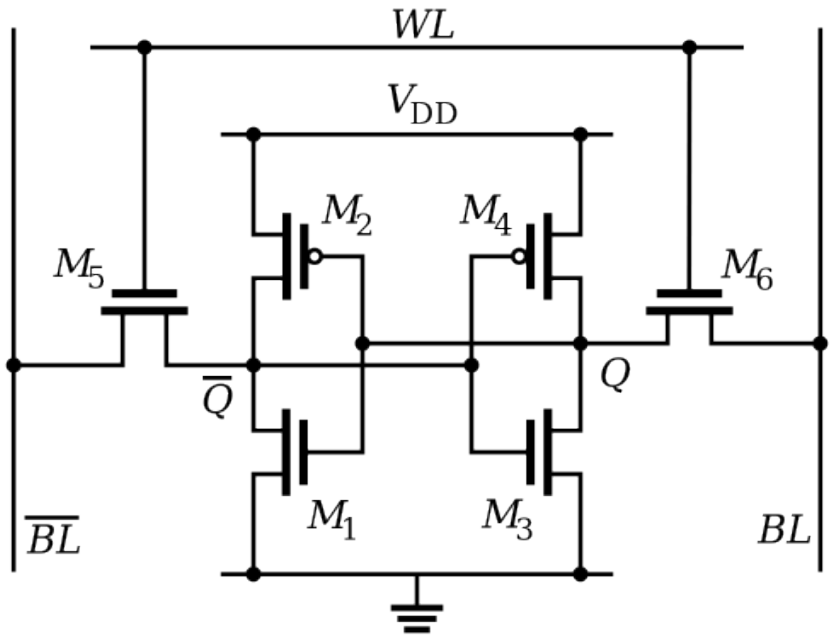
Questions?

Setup Architecture



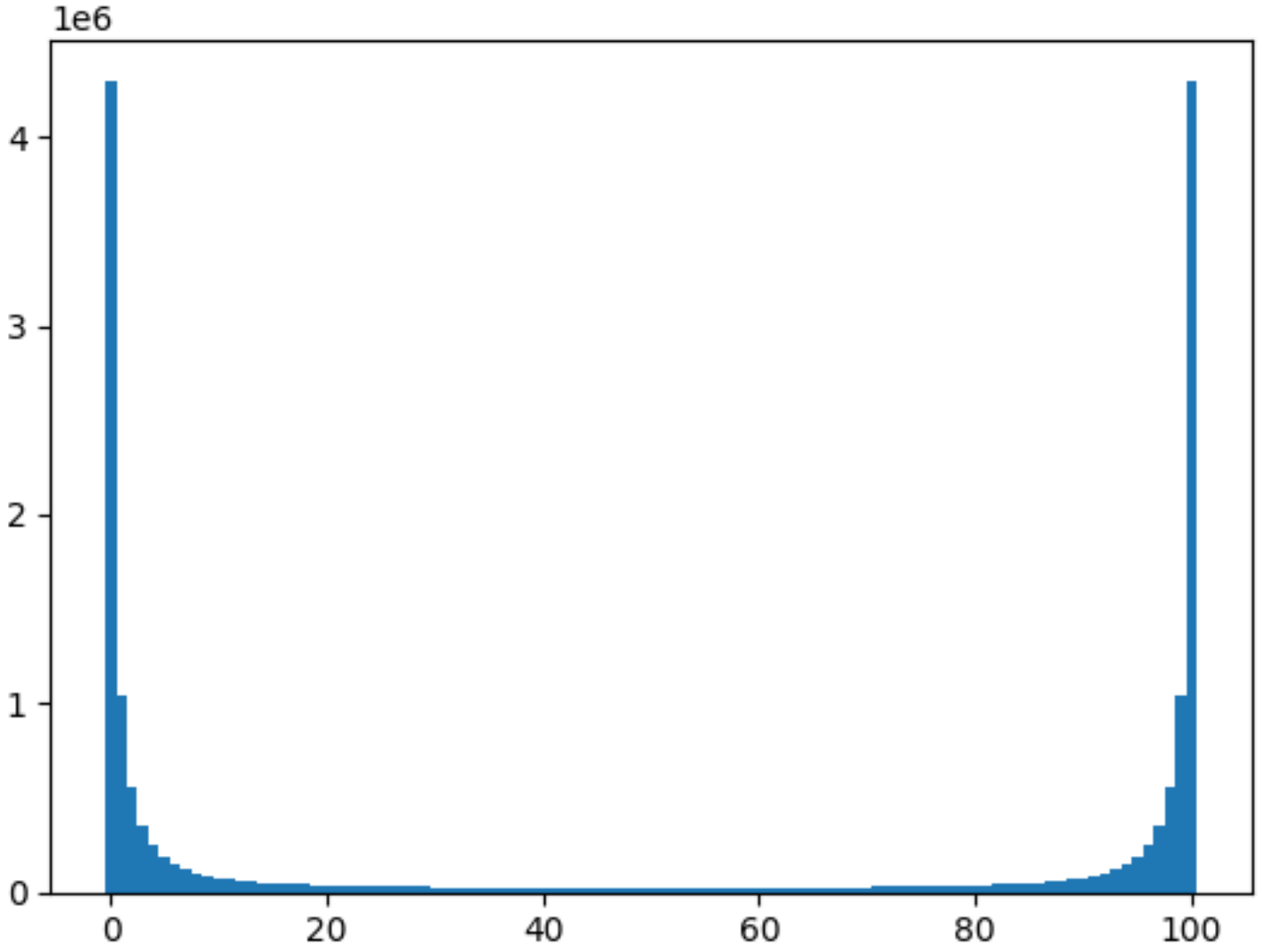
SRAM Schematic





Wikipedia

SRAM Powerup Distribution



Mechanism Explanation – Part I

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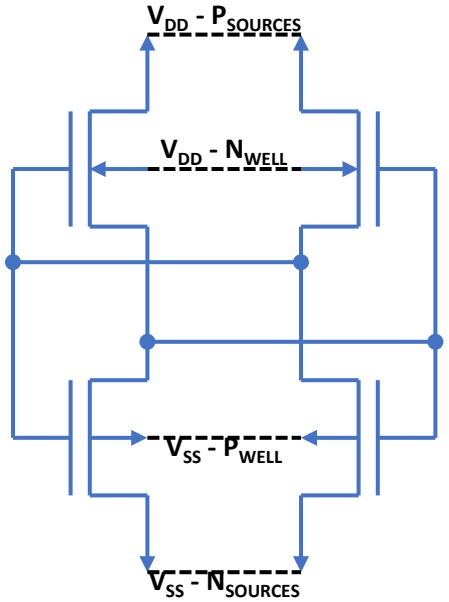
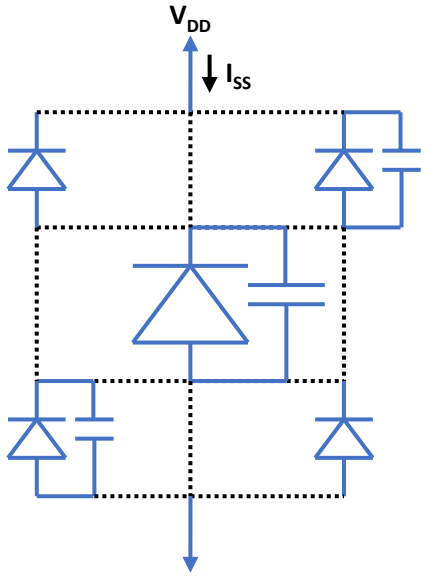


Four internal SRAM transistors with cross-coupled connections. Dashed lines show power contacts to each SRAM cell. The Well power contacts are not explicitly made in each cell, they would be connected to adjacent SRAM cells in the same Wells. There would be Wells power contacts at regular intervals.

The pass gates for reading and writing the SRAM cells are not shown.

The assumption is that 16M x these 4 transistors make up the bulk of the SRAM chip from a power perspective.

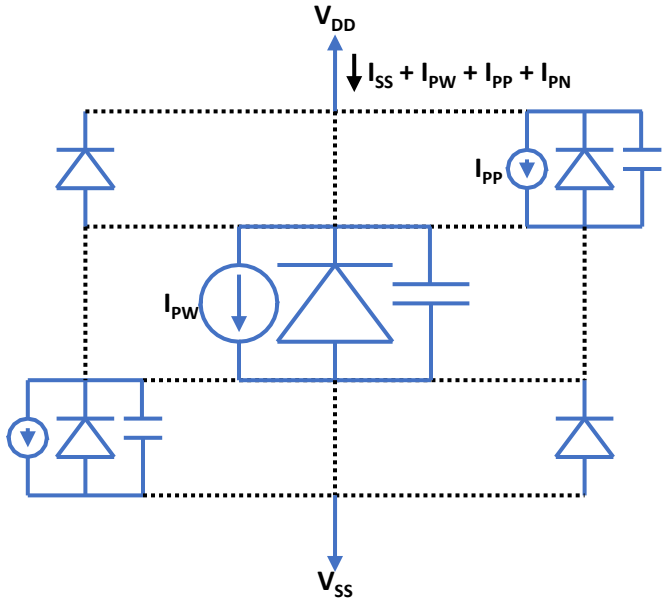


This converts the SRAM transistors into PN junctions, one for each transistor and one much bigger one for the Wells. PN junctions is where charge collects in transient radiation.

Three capacitors are shown, PN junctions capacitance. This is where VDD – VSS charge is stored in each cell, assuming the upper left and lower right transistors are ON, no potential in those transistors.

Dotted lines show resistive connections in the cell.

This figure makes many assumptions, but generally tries to represent where the stored charge is in the DUT and that the current paths are in parallel, summing the currents from each inverter and the Well junction for all 16M cells to provide the DUT standby current (ISS).



Now adding dose rate photocurrent to each PN junction with a high reverse bias. This is an assumption from SEE simulation where the primary charge collection is in OFF transistors.

The main point of this figure is to show the photocurrent is additive to the standby current and to each other. We can probably assume standby current is small compared to the dose rate photocurrent.

Mechanism Explanation – Part II

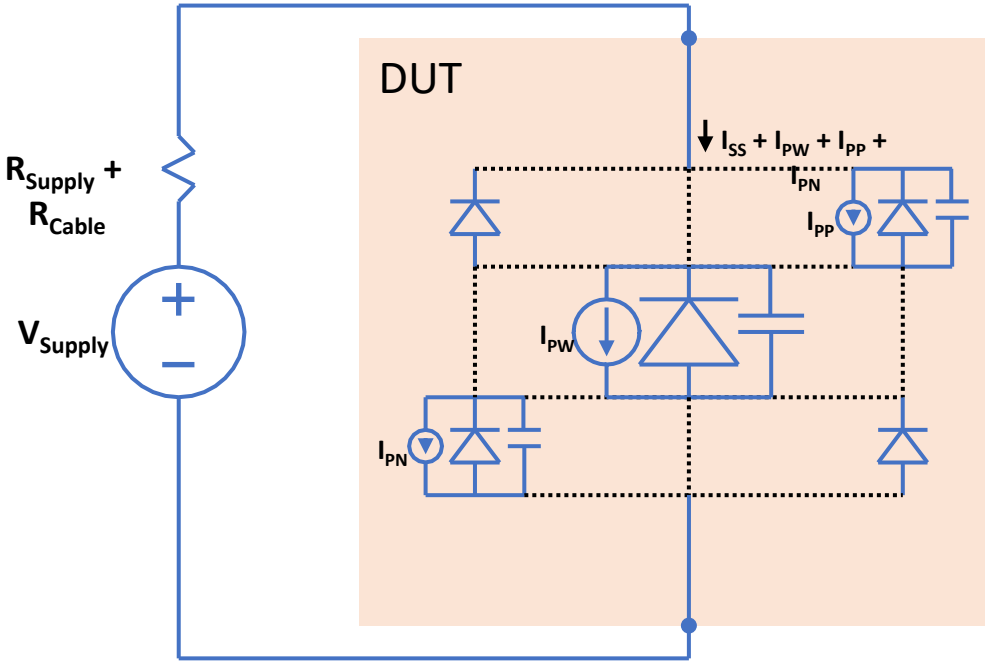
If we assume the figure on the right is a basic representation of our test, then the supply current is limited based upon the RC load. Lets call this limit L.

When the standby and photocurrent are less than L, the power supply is able to recharge the DUT capacitance faster than it is being taken out, so the rail span collapse is not significant. Note: I think we should use the term “rail span collapse” as that was used earlier in studies.

When the standby and photocurrent is greater than L, the charge in the DUT depletes and the noise margin of the SRAM cells are reduced, leading to upsets. The fixed charge in the SRAM DUT will then correspond to an integrated dose to remove that charge.

At low dose rates, the photocurrent is less than L, so we see a small number of upsets. At high dose rates, the photocurrent is higher than L, so the upset threshold is determined by integrated dose. The closer the photocurrent is to L, the more integrated dose it takes to lower the noise margin to start causing upsets.

This also relates to lowering the supply voltage, since that reduces the charge stored in the DUT, taking less integrated dose to cause upsets.



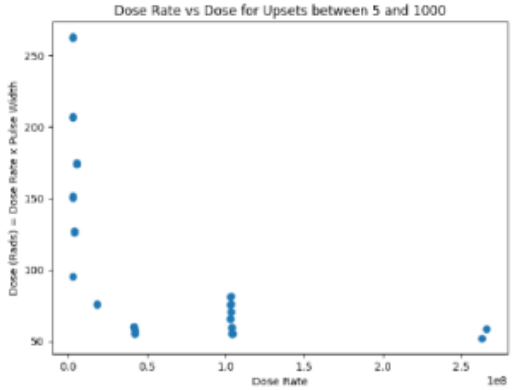
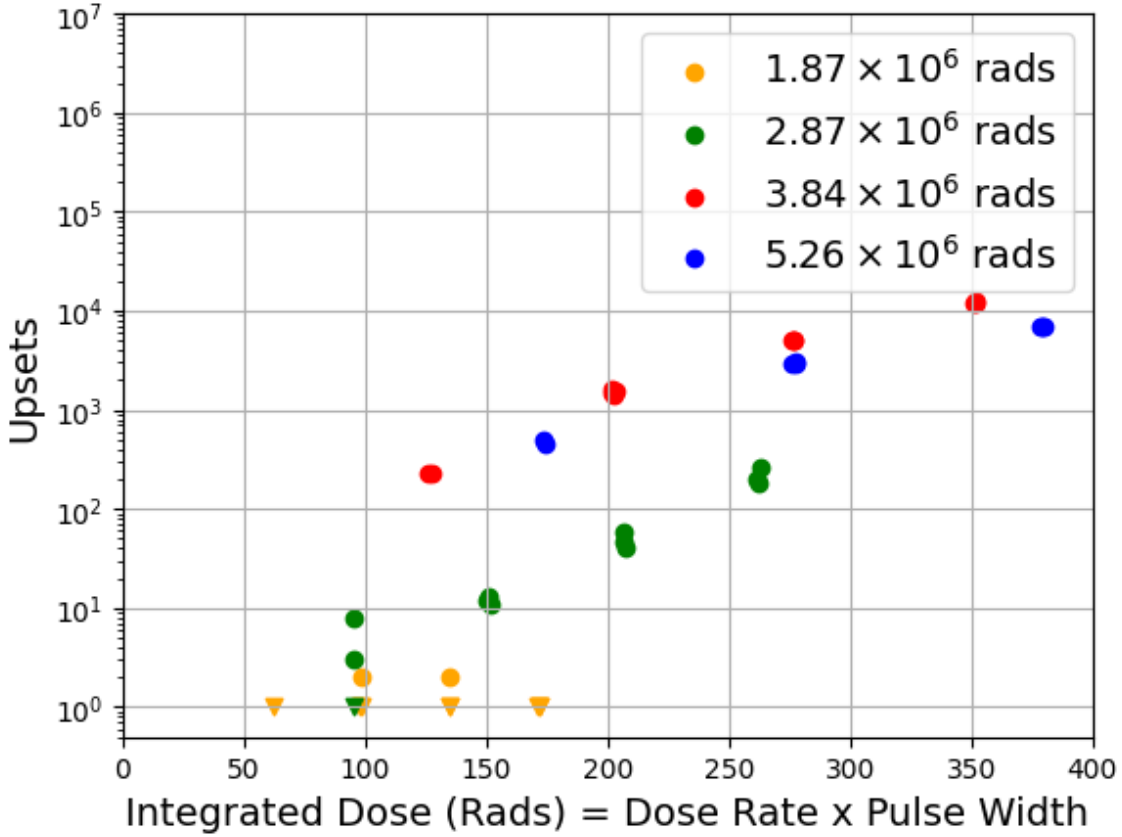
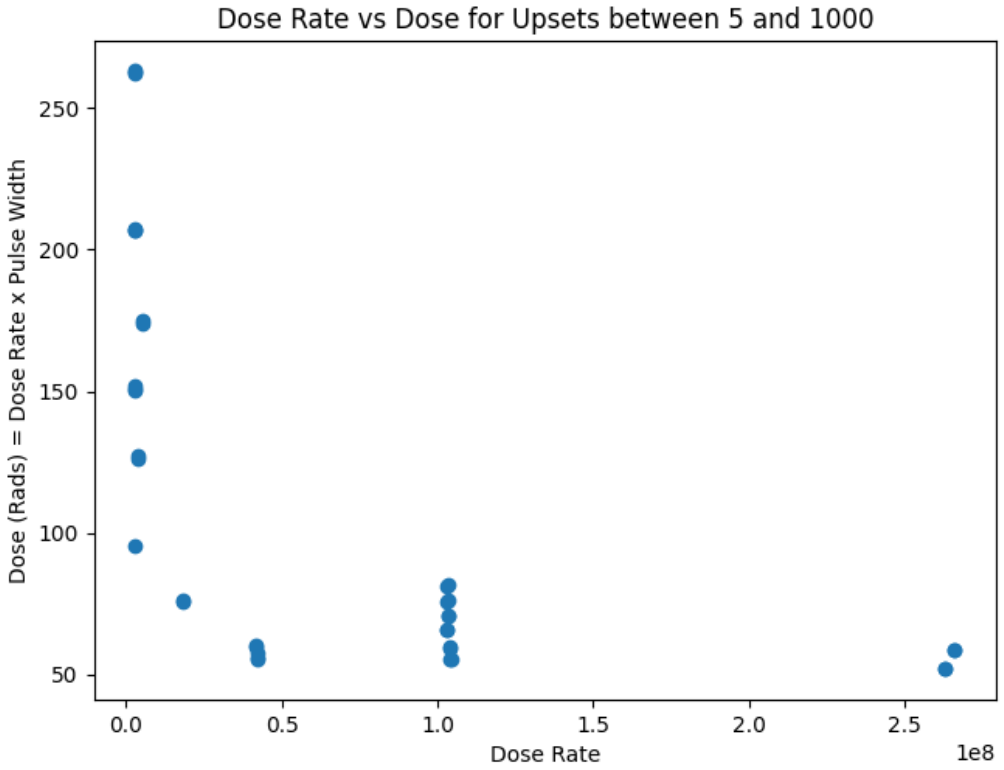


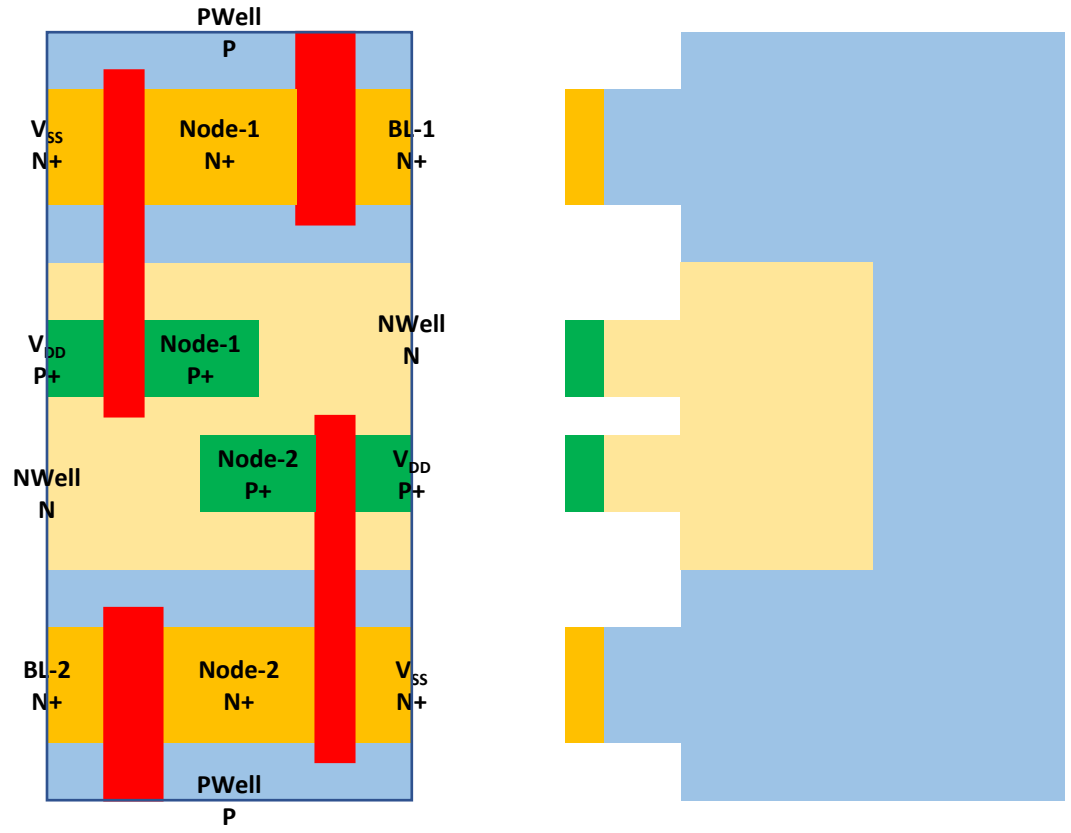
Fig. 9: Dose Rate Threshold vs Dose Rate

Results – Low Dose Rate





SRAM Layout Example – Top and Side View



Colors

- Light Blue – PWell/PSubstrate (We are assuming dual well process and not triple well in this figure
- Light Yellow – NWell
- Gold – N+ Implants for NMOSFET drain/source
- Green – P+ Implants for PMOSFET drain/source
- Red – Gate Polysilicon

In the side view, you can see that the transistors sit above the wells – The white space between the transistors would be trench oxide

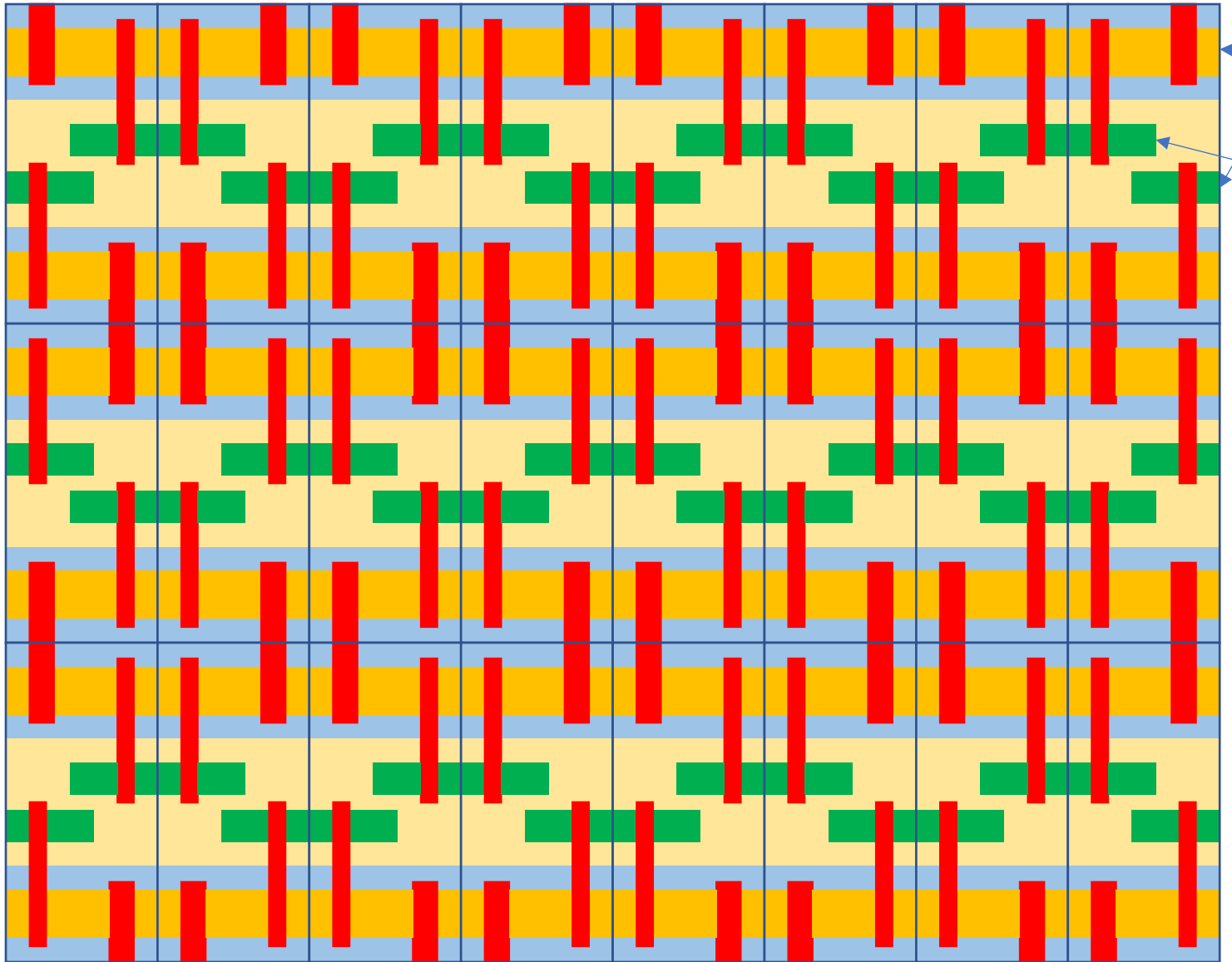
If we showed the other side view – it would be very complicated, but not show that much

The transistor nodes are all shown. If the implant goes to the edge of the box in the top view, then that implant and node is shared with an adjacent cell (cell tiling will be shown in next chart).

The Wells will go a long way in the left-right direction (from top view). There will be a Well contact every so many cell. That would be a N+ implant in the Nwell and a P+ implant in the Pwell

Underneath the Gate Polysilicon will be the Well, which is the body of the transistor. This will be shown in a subsequent chart as well

SRAM Layout Tiling

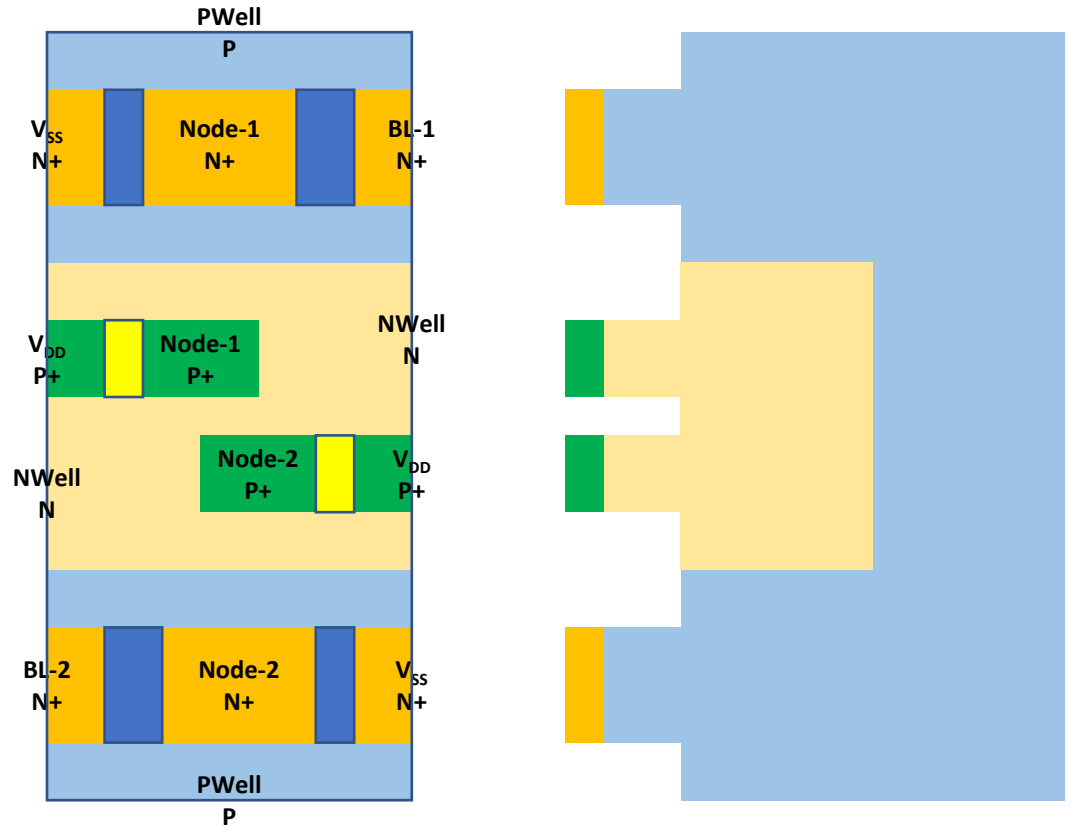


NMOSFET Transistor Area Above the PWell is long like the well

PMOSFET Transistor Area Above the NWell is broken up, just shared between 2 cells

Note that the basic SRAM cell is mirrored both vertically and horizontally to adjacent cells

SRAM Layout Example – Without Gate Poly

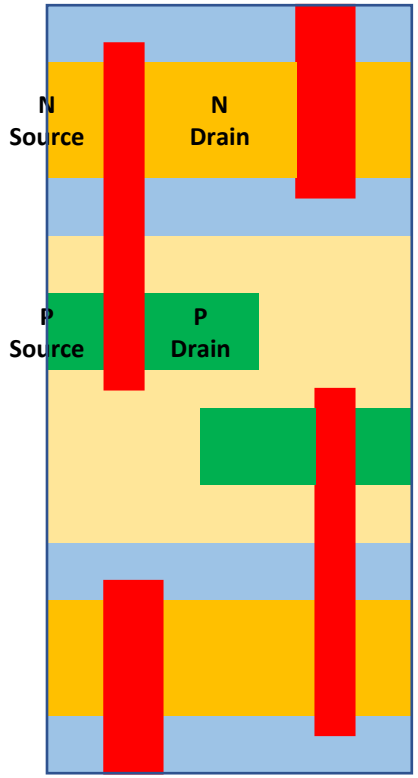


New Colors

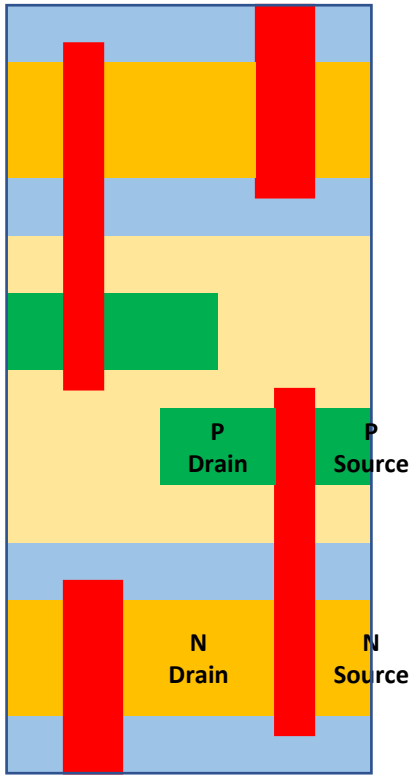
- Blue – PWell at the same height as the N+ implants, just drawn a slightly different color to show it is at a different height.
- Yellow – Nwell at the same height as the P+ implants, just drawn a slightly different color to show it is at a different height

Note the Well dopant levels near the transistor are much lower than down in the Wells. Down in the Well, the higher dopant level will reduce resistivity, so that there is better conduction of the potential from the Well contacts to all transistors. The dopant level at the transistor is based upon the needs of the transistor. Well resistivity is going to be in the kohm range, just to give you some insight

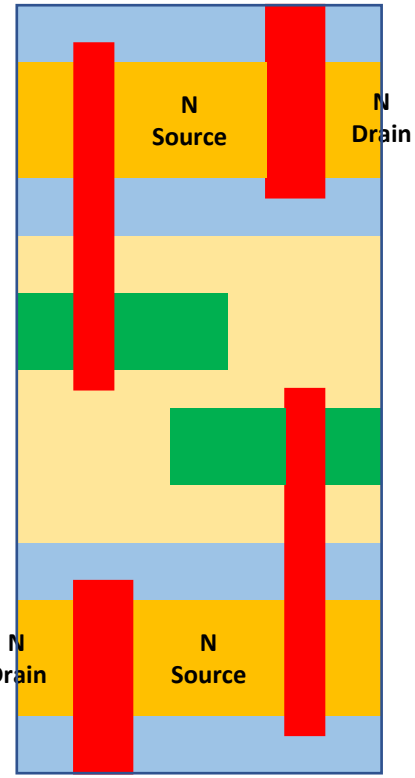
SRAM Layout Example – Transistor Identification



Inverter #1



Inverter #2



Access Transistors

SRAM Potential Change with Dose – Prerad

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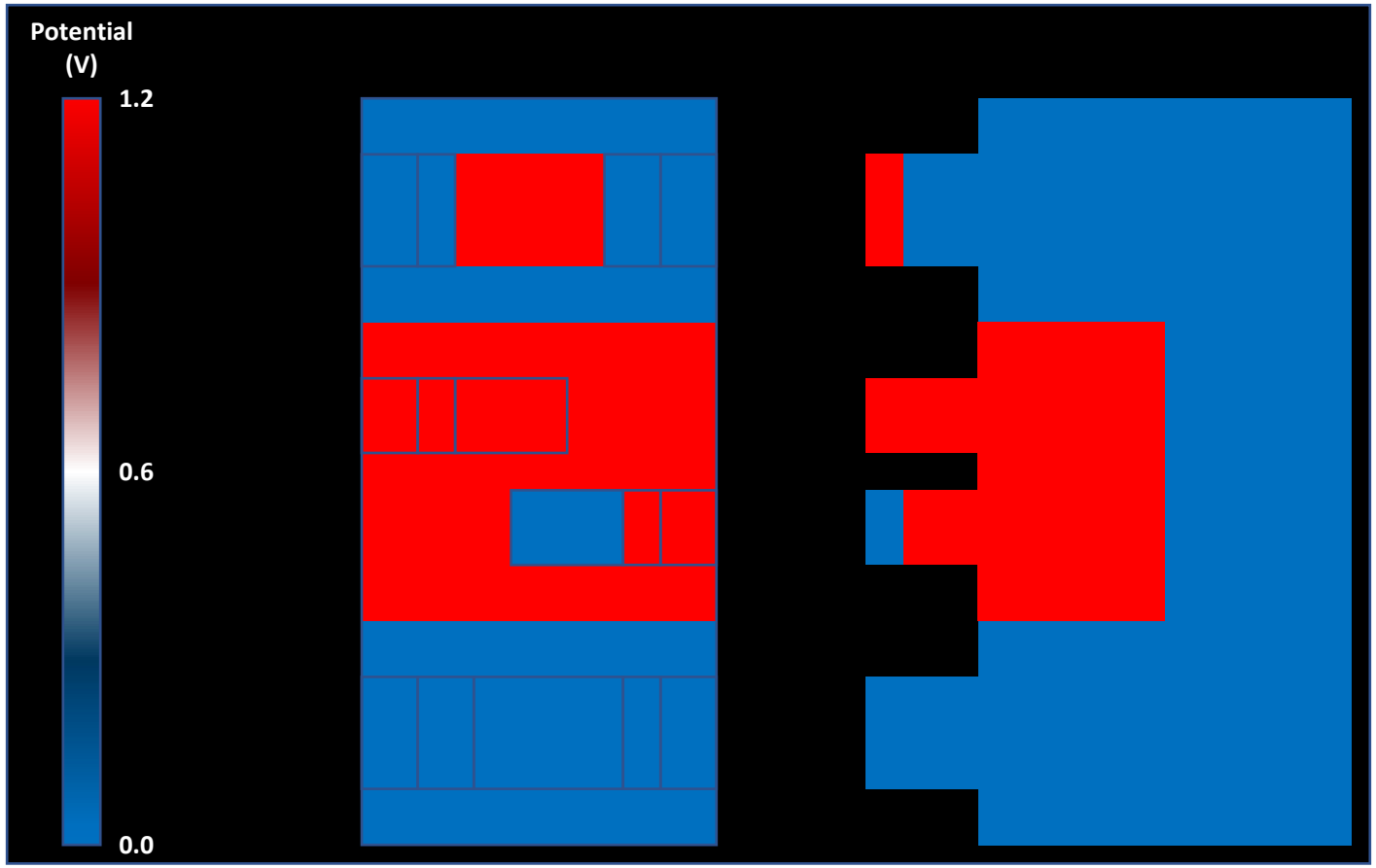
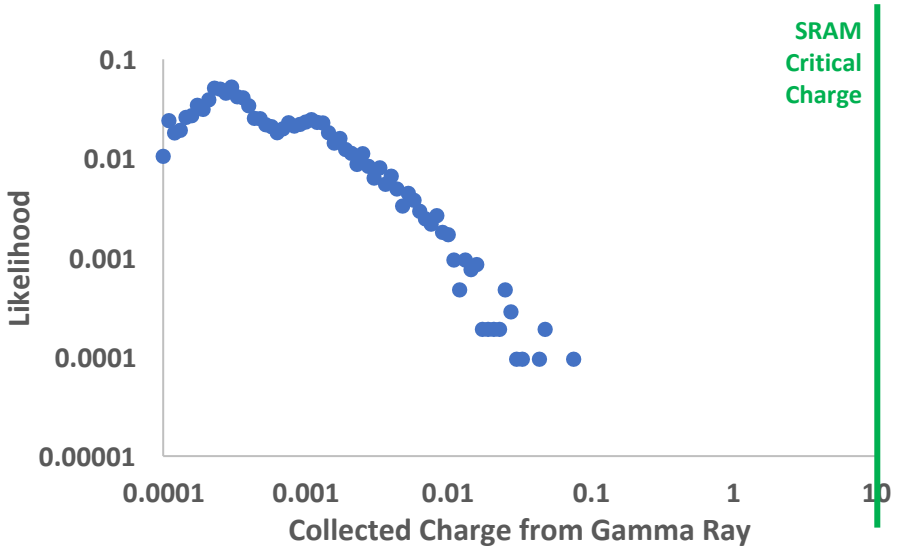
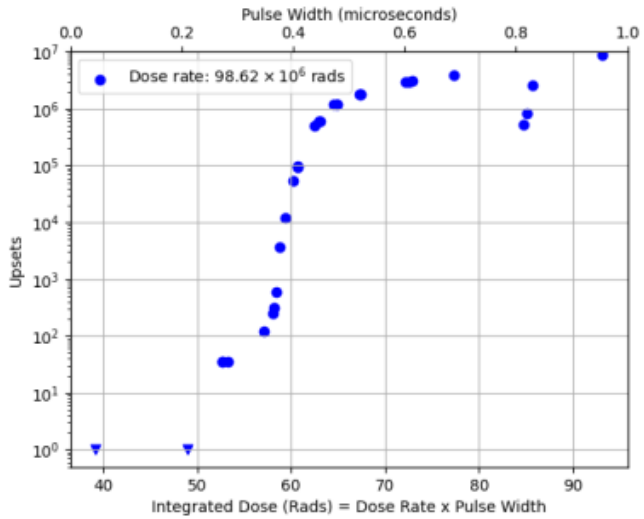


SRAM Critical Charge



Integrated Dose



SRAM Potential Change with Dose – Rad, No Upsets

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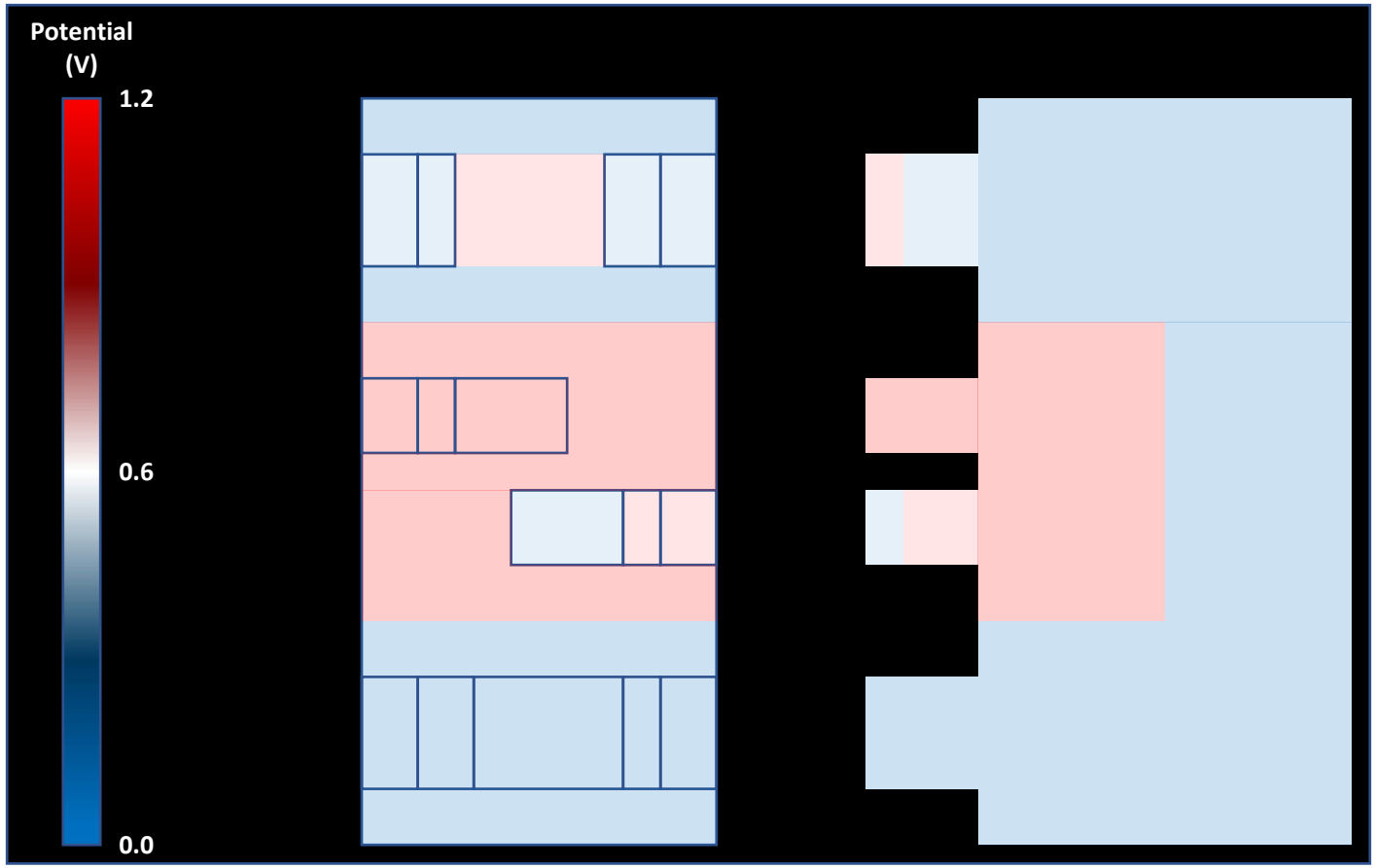

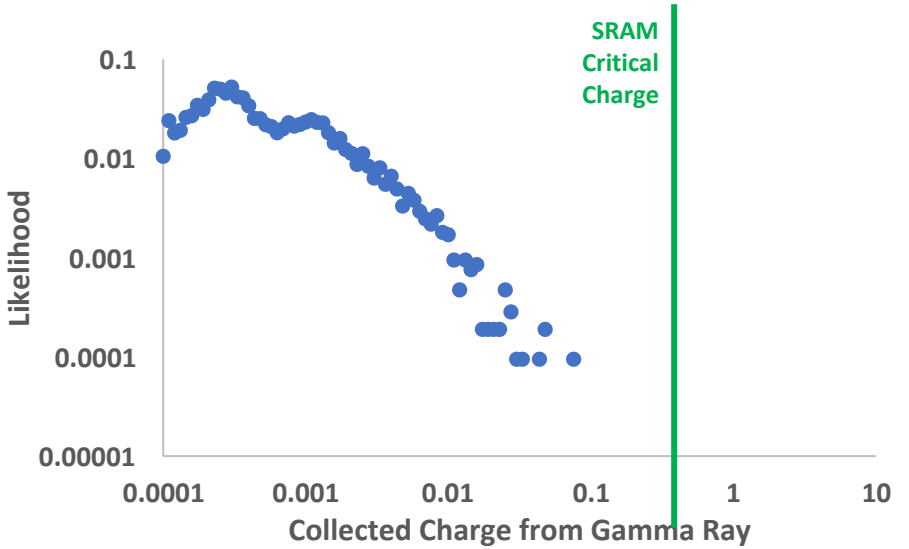

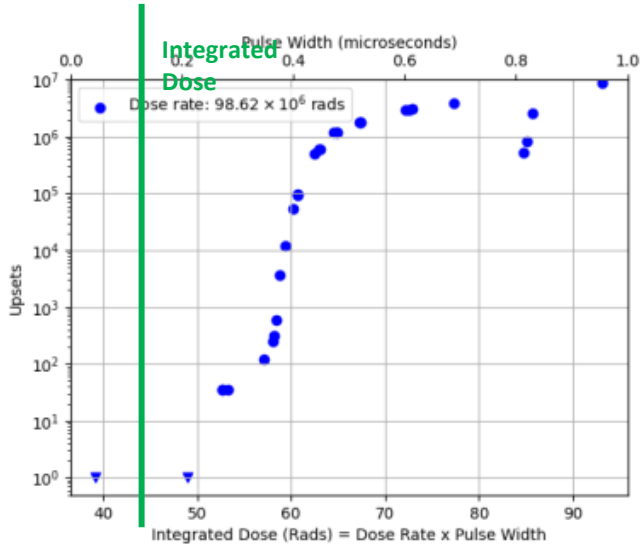

SRAM Potential Change with Dose – Rad, Some Upsets

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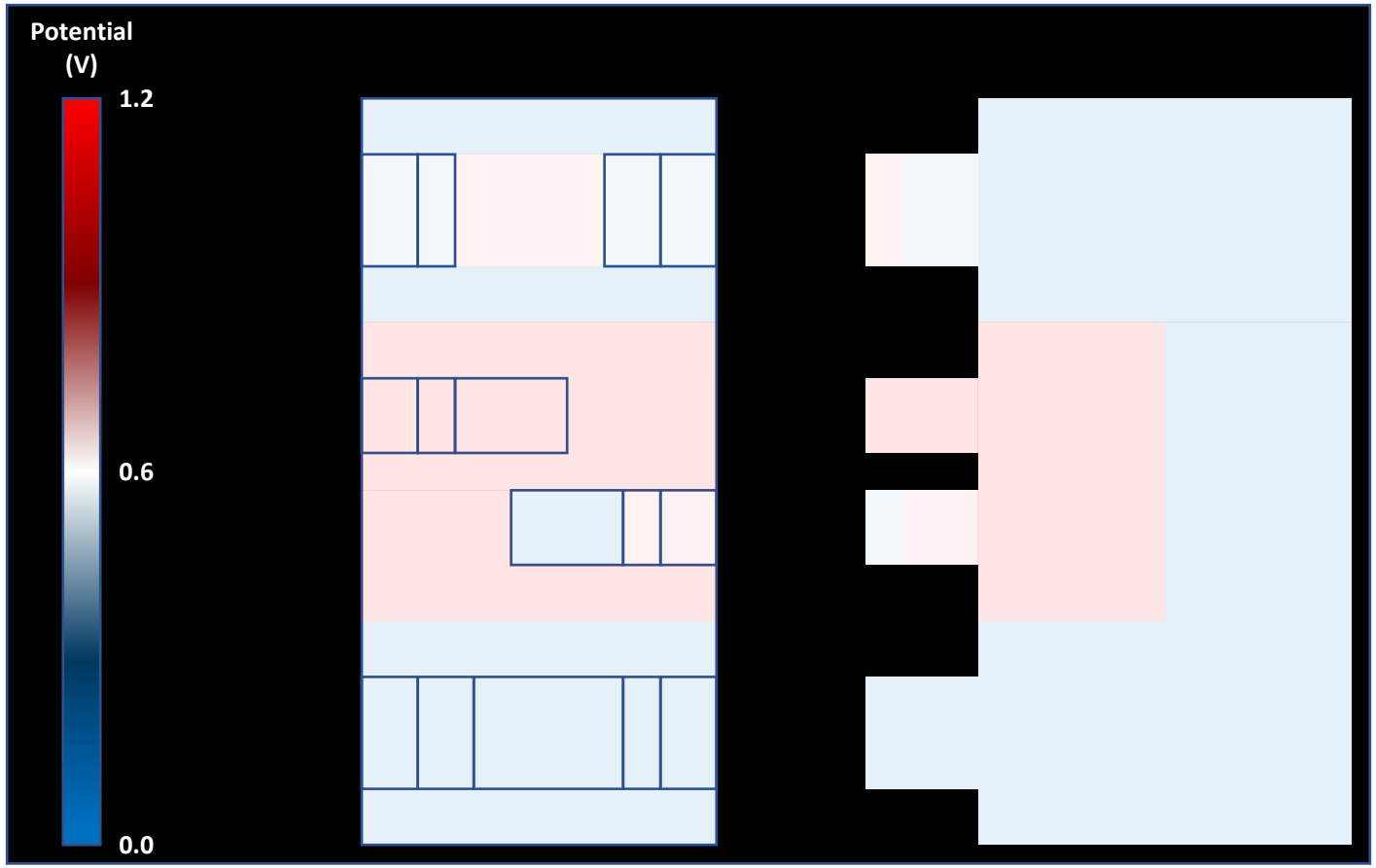

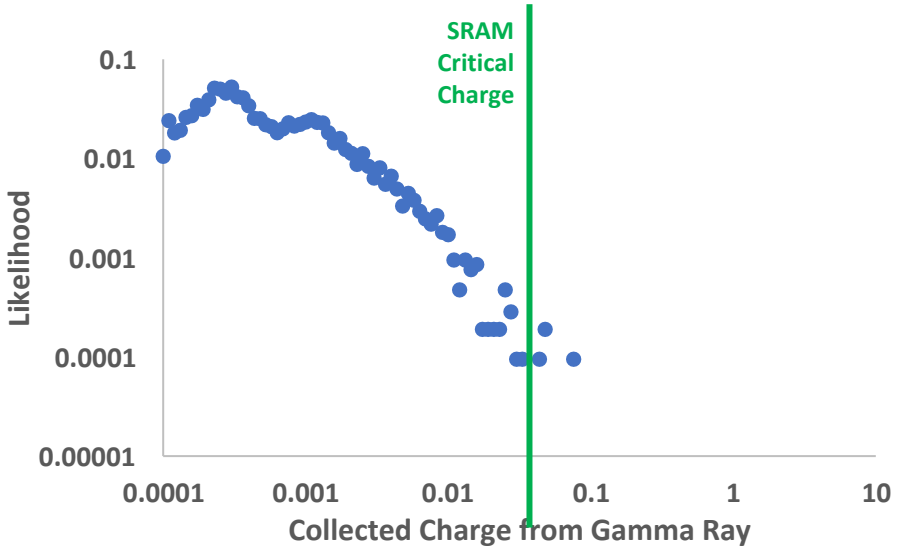

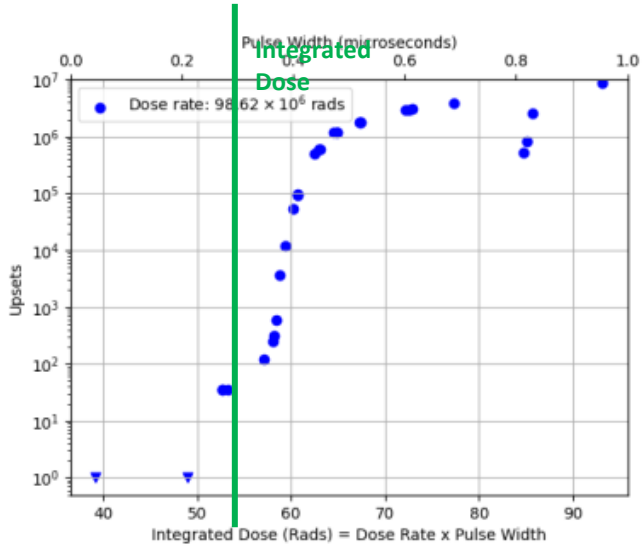

SRAM Potential Change with Dose – Rad, Many Upsets

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