Final Technical Report (FTR)

a. *Federal Agency*	Department of Energy	
b. *Award Number*	DE-EE0008348	
c. *Project Title*	Modular, Multifunction, Multiport and Medium Voltage Utility Scale SiC PV Inverter	
d. *Recipient Organization*	University of Texas at Austin	
e. *Project Period*	*Start: 9/1/2018*	*End:* 6/30/2022
f. *Principal Investigator (PI)*	Alex Q. Huang, Professor Email: aqhuang@utexas.edu Tel: 512-232-6647	
g. *Business Contact (BC)*	Elena Mota Assistant Director, Office of Sponsored Projects Email: osp@austin.utexas.edu Tel: 512-471-6424	
h. *Certifying Official (if different from the PI or BC)*	N/A	

Signature of Certifying Official

Revised 8/2023
Date

By signing this report, I certify to the best of my knowledge and belief that the report is true, complete, and accurate. I am aware that any false, fictitious, or fraudulent information, misrepresentations, half-truths, or the omission of any material fact, may subject me to criminal, civil or administrative penalties for fraud, false statements, false claims or otherwise. (U.S. Code Title 18, Section 1001, Section 287 and Title 31, Sections 3729-3730). I further understand and agree that the information contained in this report are material to Federal agency's funding decisions and I have any ongoing responsibility to promptly update the report within the time frames stated in the terms and conditions of the above referenced Award, to ensure that my responses remain accurate and complete.

1. **Acknowledgement:** "This material is based upon work supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under the DE-FOA-0001740 Award Number(s) DE-EE0008348."

2. **Disclaimer**: “This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.”

3. **Protected Rights Notice:** *(If applicable, per the award Intellectual Property Provisions (Attachment 4).* N/A

4. Table of Contents

5. Executive Summary:

This project is to develop and demonstrate a Modular, Multi-function, Multiport and Medium Voltage utility scale SiC solar inverter (M4 Inverter). The M4 Inverter is a next generation utility scale PV + storage inverter that can substantially reduce the levelized cost of energy (LCOE) while providing grid friendly ancillary services. Conventional utility scale solar inverters includes three parts, a megawatt rated solar inverter, a low frequency transformer (LFT) and a medium voltage switch gear. The proposed M4 Inverter directly converts the DC output of solar panels to medium voltage AC, eliminating the bulky and costly LFT. The M4 Inverter also has a DC port to interface with an additional energy storage device. This plus its bidirectional power flow capability, allows multiple functions in addition to PV maximum power tracking be achieved. These additional functionalities include but not limited to reactive power support, peak shaving, fast frequency regulation and synthetic inertia. Predicted LCOE reductions with these added functionalities, improved efficiency and longer lifetime time are more than 30% compared with the 2017 utility scale solar LCOE. A 1MVA SiC M4 Inverter was developed and tested at high power level. The project has also advanced the state of the art in controller hardware in the loop simulation capability. Power electronic innovations introduced in the M4 Inverter includes 1700V SiC MOSFET application in 1500V PV system, soft switching three-port power converters and modular converter architecture.

6. Background:

Prior to the start of this project in 2018, there has been a significant interest in developing medium voltage power electronics system for future grid. The FREEDM Systems Center established[1] by Dr. Alex Huang was one of the world's first major effort in developing the medium voltage solid state transformer (SST) as the key technology for the future grid. The work performed at FREEDM Center was based on utilizing the emerging medium voltage SiC power devices[2] [3]. While substantial progress was made and a 7.2 kV SST was demonstrated, it became clear that replacing 100-year-old 60Hz transform with a SST is not currently a viable business approach. This is because 60Hz line frequency transformer (LFT) is very low cost and very reliable. A much stronger business case must be identified for SST technology.

A much more promising business model of the SST development roadmap is to develop SST for renewable enable integration, especially for utility scale system. This is because line frequency transformer, switchgear and inverter occupy a substantially land space and increase cost and installation complexity. Replacing them with a single medium voltage inverter has a substantial value. Since PV is a DC energy source, an inverter is needed anyway, this makes the SST based PV inverter very attractive. This trend is becoming increasingly clear in recent years as a number of vendors are embarking in similar direction. In terms of implementation, since medium voltage SiC power devices are still not commercially available, using the modular converter approach is much more attractive since lower voltage devices are commercially available. This approach also enables the solution to be scalable to higher voltage and higher power.

The M4 project was proposed in 2018 based on this new business model for introducing SST as a low LCOE solution for renewable energy integration. In recent year, the cost of storage is becoming attractive and pairing storage with PV is another major trend. This can be accomplished by AC coupled storage system. But a DC coupled system has the opportunity to further reduce the LCOE. This can be easily accomplished in a SST system since it inherently has multiple DC ports.

The M4 Inverter concept, while started in 2018, still represents one of most advanced PV + storage concepts that will have a major impact to the solar energy industry.

7. Project Objectives:

The primary objective of this project is the development and demonstration of a Modular, Multi-function, Multiport and Medium Voltage utility scale SiC solar inverter (M4 Inverter) with integrated storage function that meets or exceeds DOE's SunShot 2030 LCOE

[1] Huang, A.Q.; Crow, M.L.; Heydt, G.T.; Zheng, J.P.; Dale, S.J.; , "The Future Renewable Electric Energy Delivery and Management (FREEDM) System: The Energy Internet," *Proceedings of the IEEE* , vol.99, no.1, pp.133-148, Jan. 2011

[2] Q. Zhu, L. Wang, A. Q. Huang, K. Booth and L. Zhang, "7.2-kV Single-Stage Solid-State Transformer Based on the Current-Fed Series Resonant Converter and 15-kV SiC mosfets," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1099-1112, Feb. 2019

[3] A. Q. Huang, " Medium Voltage Solid-State Transformer: Technology for a Smarter and Resilient Grid," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29-42, Fall 2016

reduction target. The specific project goal is a full power level demonstration of a 1MVA/4160V M4 Inverter system with integrated battery storage. In addition to innovative SiC power electronics R&D, a comprehensive cost and benefit analysis will be conducted to develop a much better LCOE model for the proposed M4 Inverter based PV plus energy storage energy system.

The project is performed by a multidisciplinary team from University of Texas at Austin, Toshiba International, Opal-RT, Argonne National Laboratory, Temple University. The project team has received value advice from ERCOT especially at the beginning of the project.

8. Project Results and Discussion:

The M4 Inverter project accomplished all planned tasks successfully. Table 8.1 summarizes the major accomplishments as measured by the Go/No-Go milestones established in 2018. Most significantly, a 1 MVA SiC medium voltage PV+storage system was developed. This is one of the highest power medium voltage SiC converter system ever demonstrated.

This section summarizes the major technical accomplishments in detail. The accomplishments are divided into four sections: 1) 1MVA M4 inverter system development, 2) Cost-benefit analysis and reliability assessment, 3) Advancement of controller hardware in the loop simulation capability, 4) High power demonstration

Table 8.1: Summary of major Go/No-Go Milestones

	Metric Definition	***Success Value***	***Measured Value***	***Assessment Tool***	***Goal Met (Y/N)***
GNG 1.1	LCOE reduction for each proposed multi-function	The highest reduction is 15%	The LCOE reduction based on FRRS grid service is around 19%	Analysis and Simulation	Y
GNG 1.2	Peak efficiency of 1700V SiC Module Based Alpha Prototype Converter Tested with isolated DC/AC power conversion function	>95% when tested above 80% rated power	200kW DC/DC real power mode and 70kVar DC/AC reactive mode tested	Test	Y
GNG 1.3	Charge and Discharge rates for battery	5C	3.3C discharge and 5C charge tested	Test	Y
GNG 2.1	Efficiency of Beta version prototype of modular converter	> 97% from DC port to AC port	97.5% peak efficiency at 70kVar DC/AC reactive power mode	Experiment	Y

Deliverable 3.1	Megawatt M4 inverter tested according to the approved test plan	1) Packaged 1MVA M4 Inverter 2) 1MVA PV generation mode testing. P=1MW and thermal test satisfactory 3) >97% peak efficiency from DC port to AC port 3-phase test, P varies from 100kVA to 1 MVA 4) Reactive power demonstration with Q capability match or exceed the IEEE-1547-2018 specification	2.4kV/250kW DC/AC real power mode demonstrated at TIC with 98.6% peak efficiency	Test	Y
Deliverable 3.2	Final Project Report	Delivered	Report Delivered	report	Y

8.1 1MVA SiC M4 inverter system development

M4 Inverter system architecture

The proposed novel M4 Inverter is shown in Fig. 8.1.1 which is effectively a PV Plus Storage SST. The PV power is converted directly to 4.16kV through a single DC to AC conversion stage. The battery can be charged directly by the DC power from the PV or from the AC grid. Therefore, the M4 Inverter is basically a DC coupled PV plus storage system without the 60Hz transformer. The galvanic isolation and voltage step-up are performed by the M4 directly. High AC output voltage is obtained by series connection of a number of converter modules on the AC side while the DC side is in parallel. A high voltage BES system is connected to the 1500V PV bus through a boost converter. In the proposed 4.16kV/1MVA M4 design, 9 modular converter modules (3 modules/per phase, 111kVA/per module) are needed. The modular converter topology is a single stage DAB based DC/AC converter using 1700V SiC MOSFET. The half sine output voltage Vrec is converted to full sine wave by a silicon IGBT unfolding bridge. Table 8.1.1 summaries the key specifications of the M4 Inverter targeting 1500V PV application and 4.16kVac grid connection in Y configuration.

Major technical accomplishments of the 1MVA M4 system development consist of system-level simulation, Dual-Active Bridge (DAB) based single stage DC/AC power converter operation and optimization, medium voltage isolated Medium Frequency Transformer (MFT), 4.16 kV modular converter (input parallel output series) system architecture, and 5C fast charge battery storage system development.

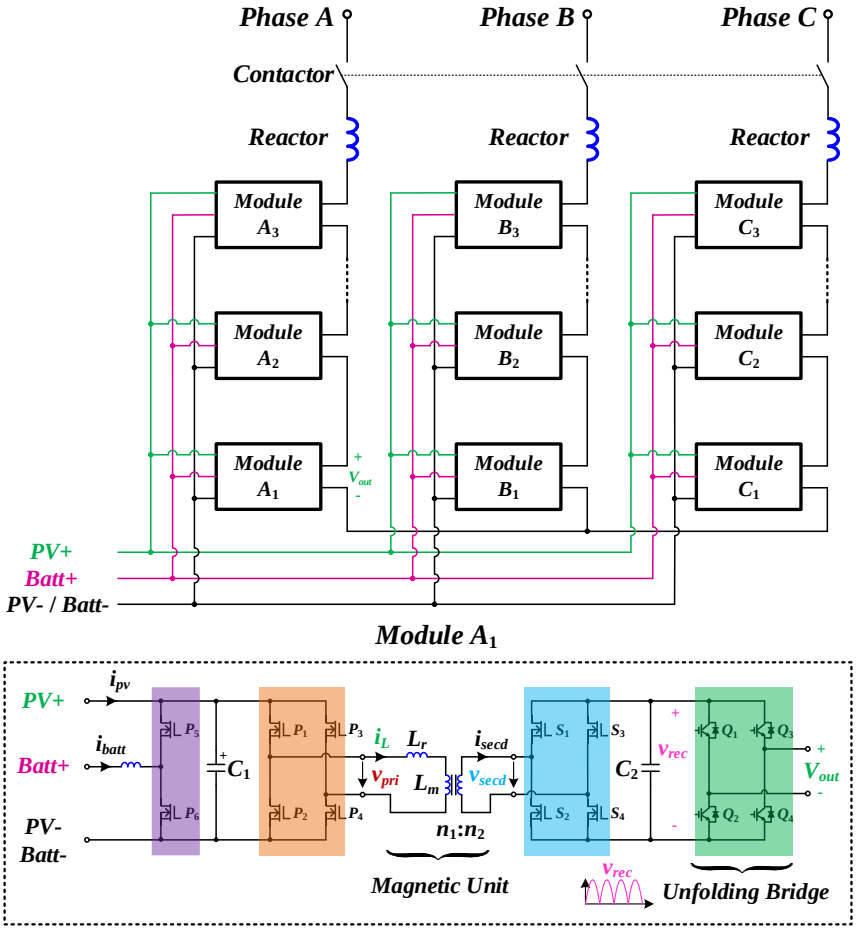


Fig. 8.1.1. Circuit Topology of the proposed 4.16/1MVA M4 system

TABLE 8.1.1
SPECIFICATIONS OF THE PROPOSED UTILITY-SCALE M4 SYSTEM

Symbol	Descriptions	Design Value
V_s	System line to line voltage	4.16kV
P_o	Rated power capacity	1MVA
I_o	Rated output current	138A
V_{MPPT}	PV MPPT voltage range	900V~1300V
I_{PV}	PV input current	770A~1100A
V_{Batt}	Battery voltage	504V~907V
P_{Batt}	Battery energy capacity	35kWh
I_{Batt}	Maximum charging current (5C)	200A
f_s	SiC switching frequency	15~60kHz
η	Expected efficiency (PV to grid)	>98%

M4 Inverter system-level modeling and simulation

A. MPPT Simulation

The M4 Inverter is formed by nine (9) modular converters with a lot of transistors and magnetic components. Simulation of such a large system itself is a challenge using today's software platform. Project conducted a PLECS simulation of the M4 converter in a reduced model configuration. A 3-ph 3-module (1 module per phase) configuration was simulated, with the objective of studying converter operation with PV panels subjected to changing irradiation conditions. 3-ph 3-module simulation approach provides the following advantages:

- 3-module simulations run much faster than 9 module simulations and are a good first step to verify adequate converter operation.
- 3-ph 3-module configuration allows effective study of converter dynamics in a 3-ph system and smoothens the power drawn from the PV panels. This is considerably different from the 1-ph case where a pulsating power draw on the PV panels affects MPPT (Maximum Power Point Tracking) tracking.

The modular converter topology used in the M4 is a novel single stage, isolated DC/AC converter based on the well-known DAB topology. While the topology is well known, the operation as an isolated DC/AC inverter is not well established. The control of such a topology is more complex than a traditional two-level voltage source inverter (VSI). Fundamentally, DAB is not a Pulse Width Modulation (PWM) converter. One has to use multiple phase shifts between the primary and secondary side converter to accomplish the DC/AC power conversion objective[4].

The PV panel model in PLECS was simulated using a 3D look-up table. The PV panel model is implemented as a two-terminal device in PLECS whose outputs are a voltage (V) across the terminals and a corresponding output current (I). The inputs to the table are temperature and irradiance. Thus, the model produces a unique PV curve (power-voltage curve) as a function of irradiance and temperature. Irradiance input is normalized to 1 corresponding to maximum output power and the input temperature is in Celsius.

In real operating conditions, the irradiance is subject to quick changes due to passing clouds which may block the PV panels (in the order of minutes or seconds), and gradual changes during the day between sunrise and sunset (in the order of hours). In the simulations conducted, the irradiance is step-changed between different levels to observe effectiveness of the MPPT controller in tracking the maximum power. It will suffice to observe MPPT tracking with respect to quick changes, as slower changes will be well within the bandwidth of the controller.

The converter control is structure as follows: The MPPT controller is implemented in MATLAB using a modified perturb and observe (P&O) algorithm. The controller compared present PV voltage and power to that of the previous step and makes a decision to either increase or decrease the power command. This power command is then used to generate

[4] A. Vetrivelan, W. Xu, R. Yu and A. Q. Huang, "Triple Phase-Shift Optimization of SiC-based Dual-Active Bridge DC/AC Converter," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), 2022, pp. 70-77

a current reference for each of the three modules. Here, the modules control their current using a simple PID controller which generates a phase-shift for each module. PID controller is used here for simplicity of design and fast simulation characteristic.

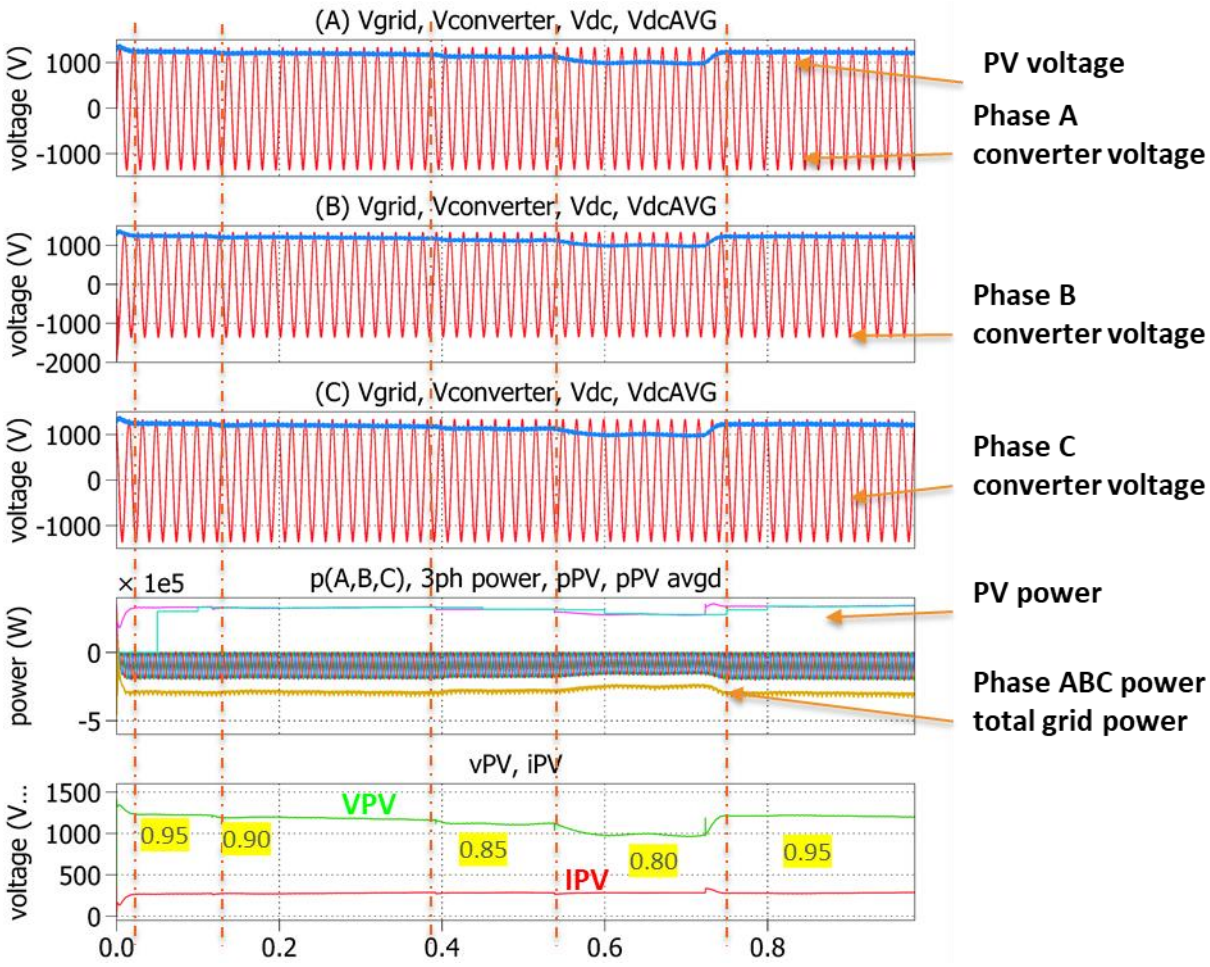


Fig. 8.1.2 3-ph 3-module PV operation

Fig. 8.1.2 shows the results of the 3-ph 3-module PV simulation. From top to bottom, the plots are:

i. Phase A converter voltage in red, and PV voltage shown in blue
ii. Phase B converter voltage in red, and PV voltage shown in blue
iii. Phase C converter voltage in red, and PV voltage shown in blue
iv. PV power (cyan) and grid injected power (yellow)
v. PV voltage (green) and current (red)

The plots in fig. 8.1.2 show the change in the PV voltage, current, power when subjected to step changes in the irradiance (marked in yellow on the last plot). The 3ph quantities also change during these steps and track the maximum power. Fig 8.1.3 shows a zoomed

in shot of the irradiance transition from 0.8 to 0.95. As seen, the power increases to move to the PV panel to the new maximum power point.

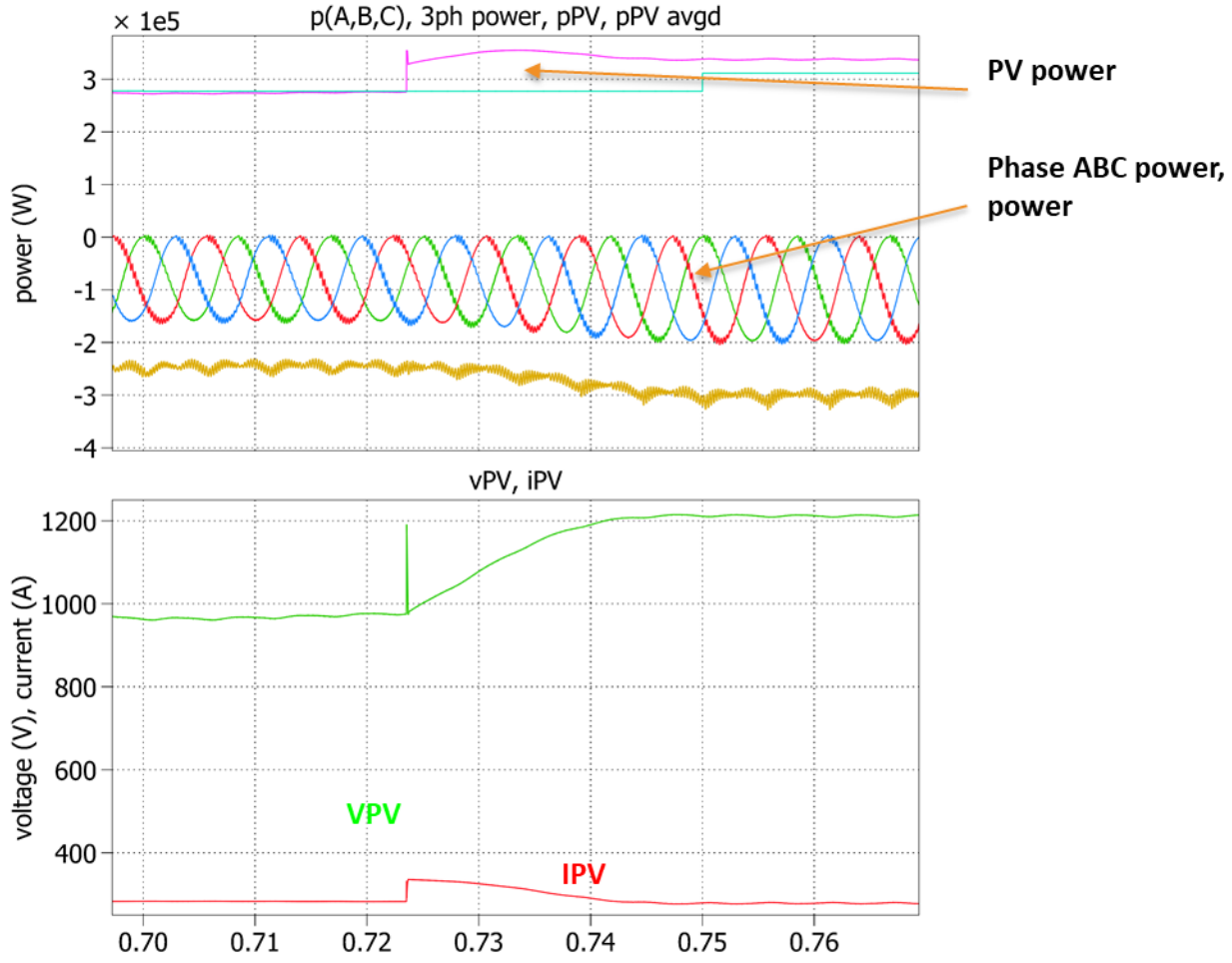


Fig. 8.1.3 PV irradiance transition from 0.8 to 0.95

Finally, the MPPT tracking along the panel's PV curve is shown in Fig. 8.1.4. Here it is seen that apart from the transition times, the MPPT controller moves the system to the maximum power point.

This simulation effectively established that the M4 Inverter can be utilized as a utility scale PV inverter with MPPT capability.

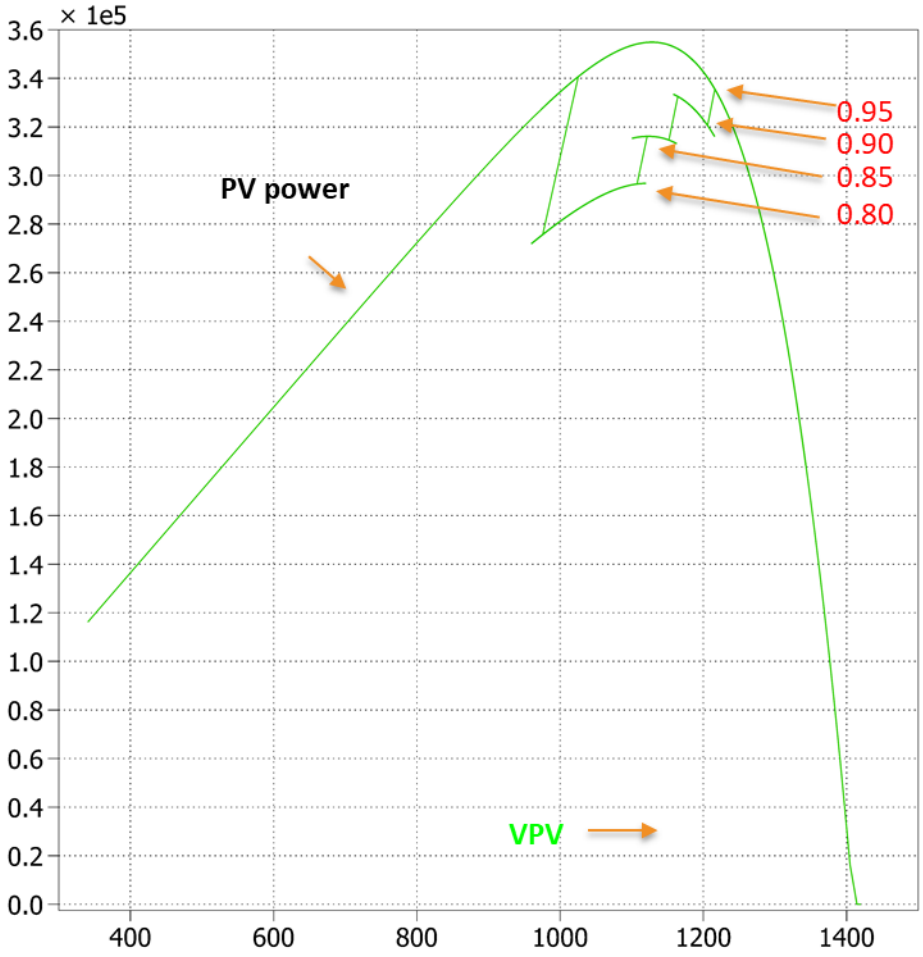


Fig. 8.1.4 PV curve during MPPT operation

B. Reactive Power Mode Simulation

DAB based DC/AC converter has never been reported or studied for reactive power compensation. However, as a utility scale PV system, providing reactive power support is an important function and therefore must be studied and established.

PLECS simulation was also used to verify the capability of the converter to supply leading and lagging reactive power to the grid, while keeping the THD (total harmonic distortion) and TDD (total demand distortion) low in accordance with IEEE 1547-2018. Figure 8.1.5 below show the results of the simulation which employed closed-loop control. The result demonstrates that the M4 Inverter indeed can provide reactive power support.

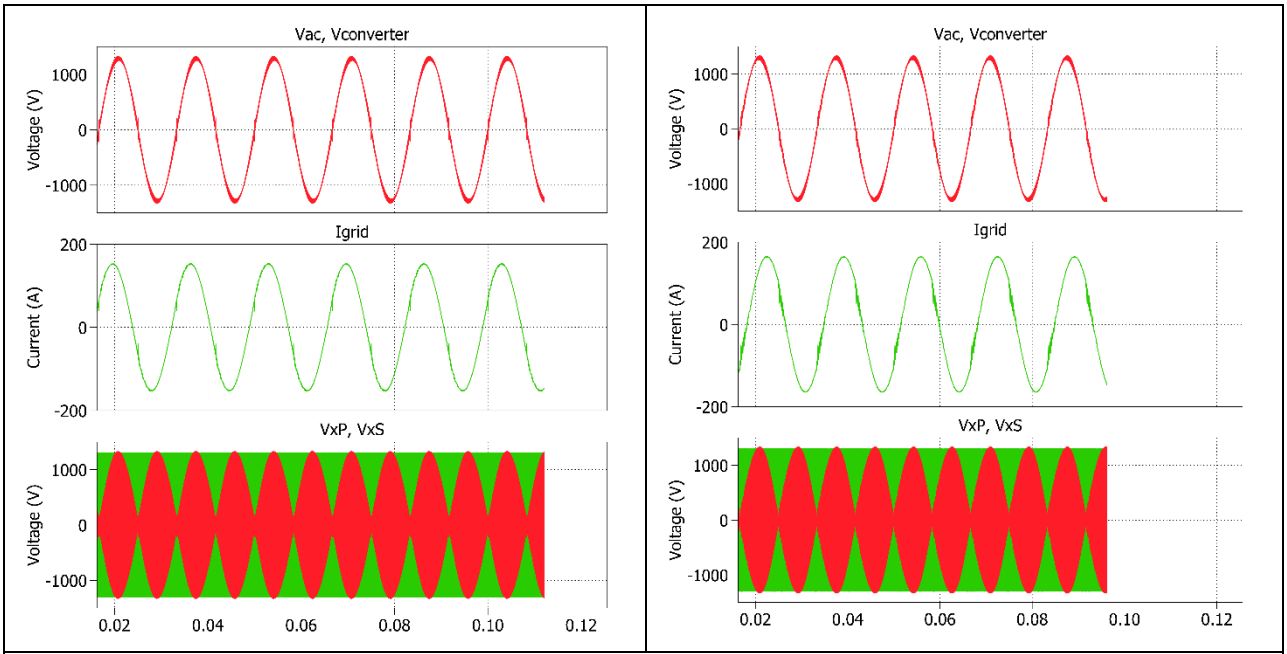


Fig. 8.1.5 3ph 3module simulation results, with real and reactive power transfer to grid. Only one phase shown for clarity. Current injected to grid leading (left, THD 2.7%), lagging (right, THD 4.7%)

C. Voltage-Balancing Control

One of the challenges in utilizing modular converter in series to achieve higher grid voltage is the voltage balancing among the modular converters. Natural balancing cannot be assumed. PLECS simulation of the M4 converter in a 3-ph 9-module configuration was conducted with the dual objectives of developing and verifying voltage balancing control across the modules, and observing neutral point voltage. Voltage balancing is a crucial aspect of control of the M4 system since the devices in each module are rated for 1700V and the module voltage should never exceed this limit. Also, the variation in the floating neutral point voltage must be kept low to ensure safe operation.

Further, in the real operating conditions the individual modules may differ from each other slightly in their component parameters such as secondary side capacitance, leakage inductance, grid-tie resistance etc. In the absence of a balancing scheme, these small differences may lead to disparate voltage and current stresses on the modules. Figures 8.1.6 and 8.1.7 show the system operation under an example set of differing component parameters, without and with the balancing control.

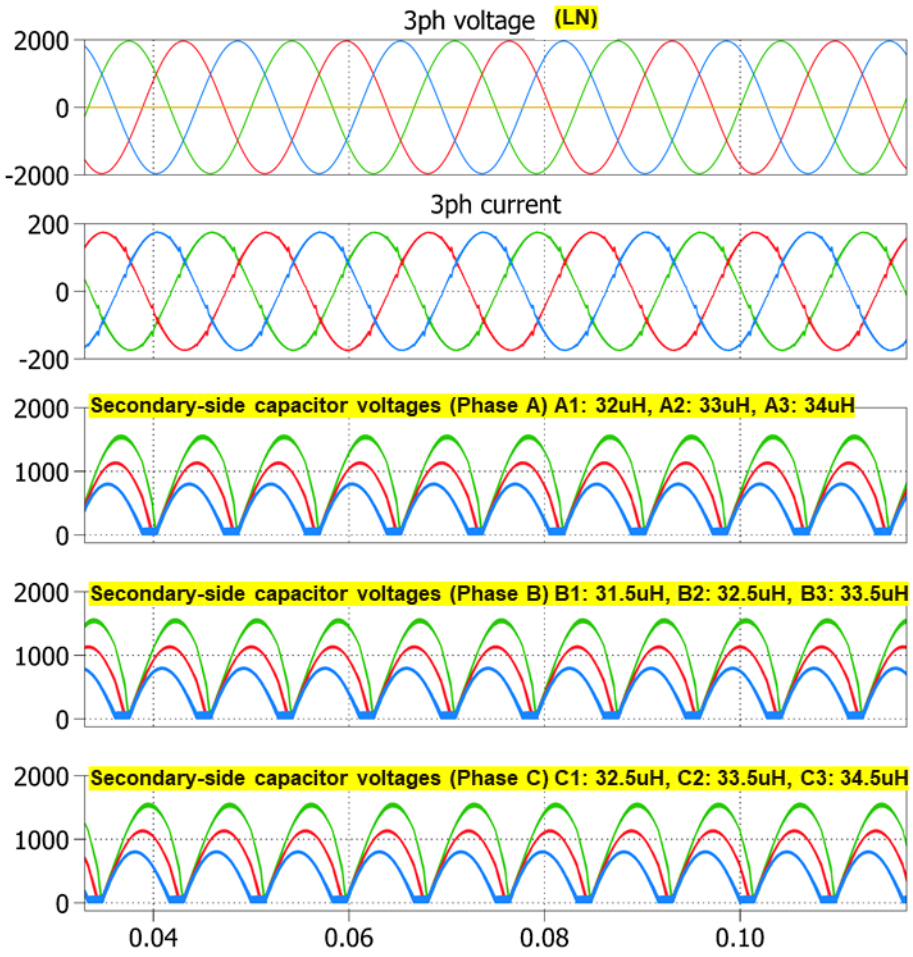


Fig. 8.1.6 3ph 9module Wye-connected floating neutral simulation results, without voltage balancing control, could lead to module overvoltage if not corrected

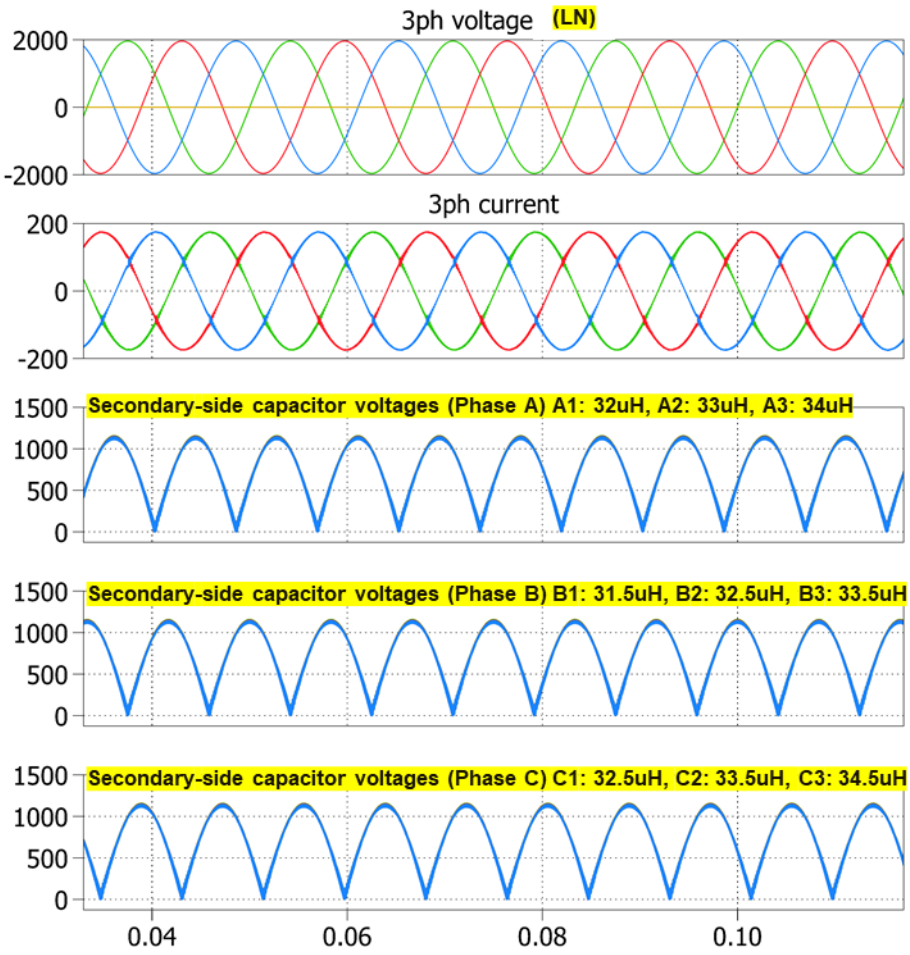


Fig. 8.1.7 3ph 9module Wye-connected floating neutral simulation results, with voltage balancing and real power injection to grid

Figures 8.1.6 and 8.1.7 shows the simulation results. From top to bottom, the plots are:

i. 3ph grid voltage
ii. 3ph grid current
iii. Capacitor voltages A1, A2, A3
iv. Capacitor voltages B1, B2, B3
v. Capacitor voltages C1, C2, C3

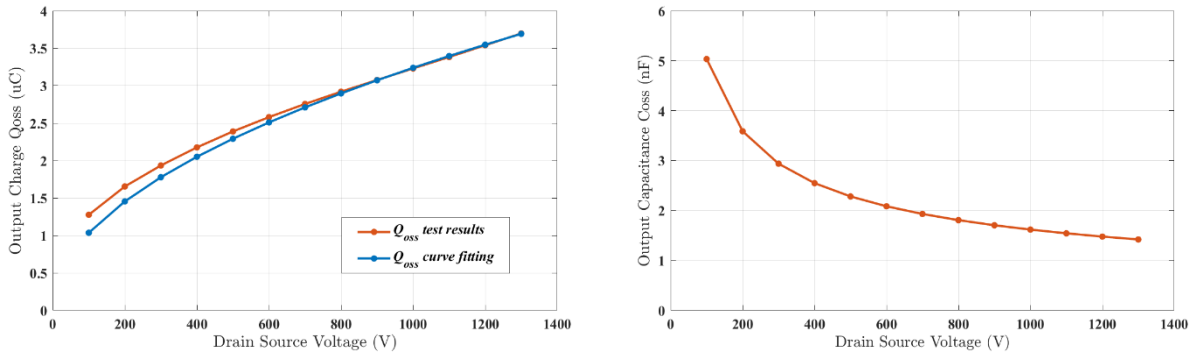
Figure 8.1.6 shows the results of system operation for a case where the leakage inductances are slightly differing values and there is no balancing control. It is seen that the voltages across the secondary-side capacitors (and hence the SiC devices) vary by a lot and risk overvoltage. This is in contrast to figure 8.1.7 which shows system operation with balancing control. the voltage balancing control works very well to the point that the differences in the capacitor voltages in the figure 8.1.7 are indistinguishable.

MOSFET module-level C_{oss} Extraction and turn-off voltage overshoot prediction

Fig. 8.1.8. 1700V SiC power MOSFET half bridge module from Wolfspeed.

Low switching loss SiC power MOSFET and GaN HFET are two emerging power device technologies that enable efficient power converters with compact sizes. For high power applications, a number of SiC power modules are now available for MW applications. For the proposed M4 system, 1700V SiC MOSFET half-bridge module from Wolfspeed® as shown in Fig. 8.1.8 is used due to its ultra-low loop inductance (7nH) and low on-resistance (2.5mohm). For a 1500V PV inverter system, the MPPT voltage is in the range of 900V to 1300V. The low loop inductance, together with proper bus bar design can ensure the device voltage overshoot is less than 1450V at the highest turn-off current. The power module also has a very low thermal resistance $R_{th,jc}$=0.068°C/W and a high temperature housing allowing $T_{j,max}$=175°C operation. The low drain-source on resistance and excellent heat dissipation capability result in a device current handling capability of 393Amps at T_C=125°C, T_J =175°C. This ensures forced air cool can be used for the 111kVA modular converter.

The proposed DAB DC/AC converter has wide input (MPPT range) and output (half sine waves) ranges. Due to the nonlinearity of MOSFET's Coss/Qoss versus the drain-source voltage, Zero Voltage Switching (ZVS) condition for the primary DC side and secondary AC side are more complicated than that in a DC-DC converter. Besides, even though device turn on loss is eliminated through ZVS, the accurate turn-off loss as well as the deadtime loss still depend on the device output capacitance. Therefore, an accurate Coss/Qoss model is needed to ensure ZVS and estimate the converter total loss. The Coss/Qoss model extraction results of the 1700V SiC MOSFET module using a novel test circuit are shown in Fig. 8.1.9.



(a) Output charge Qoss (b) Output capacitance Coss

Fig. 8.1.9. Measured C_{oss}/Q_{oss} results for the 1700V SiC MOSFET module.

In order to evaluate the feasibility of using 1700V SiC devices for 1500V applications, the mechanism of how the optimized PCB-based busbar reduces the voltage overshoot is needed. For simplicity, lossless MOSFET channel model is adopted to replicate the turn off voltage oscillation which could guide the practical PCB copper trace layout.

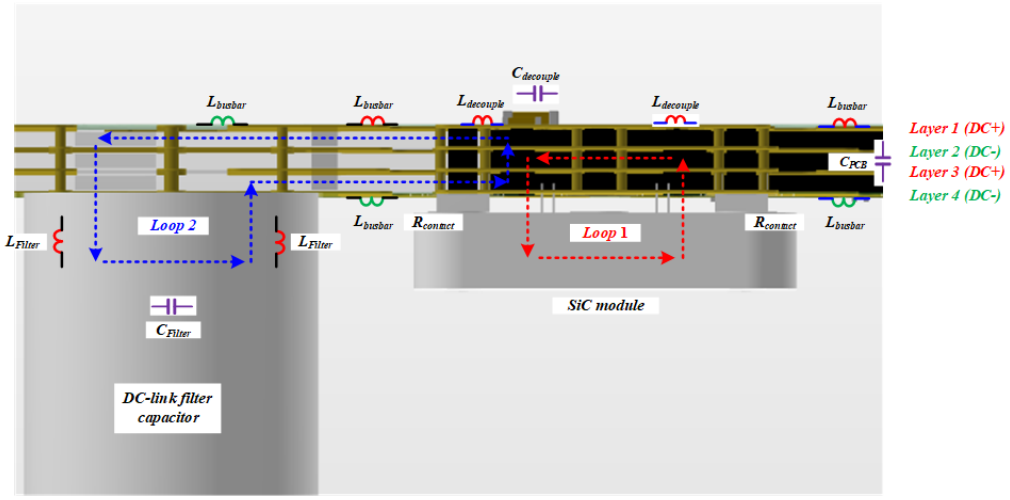


Fig. 8.1.10. Optimized PCB-based busbar layout of the SiC converter.

Fig. 8.1.10 shows the PCB-based busbar design. To reduce commutation length, the middle terminal of the mid-point is eliminated (see Fig. 8.1.8) and high frequency decoupling capacitors are placed there instead to fully utilize the effective area on the top of the SiC module. A sandwich structure of PCB copper trace is adopted to get a higher parasitic capacitance between DC links. Fig. 8.1.11 shows the circuit model of the PCB-based busbar. To simplify the analysis how the PCB busbar and the decoupling capacitor Cdecouple reduce the voltage spike across the turning-off device, assuming the voltage across the decoupling capacitors vdc(t) keep constant when analyzing the commutation loop 1 is appropriate since the resonant frequency of loop 1 is much higher than that of loop 2. Part of the values in equations are extracted from the ANSYS/Q3D simulation.

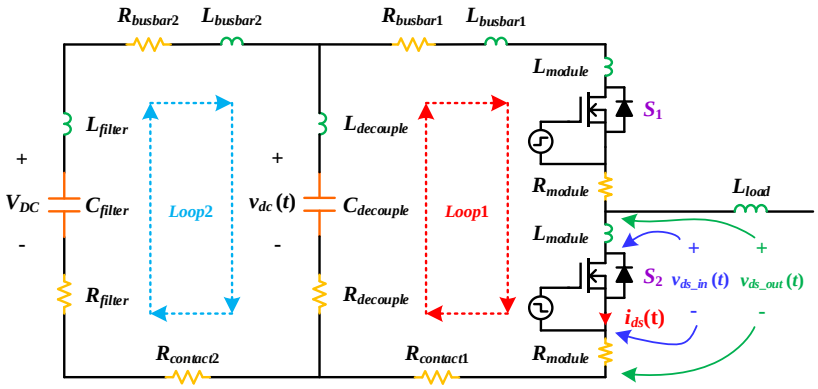


Fig. 8.1.11. Circuit model of the optimized PCB-based busbar.

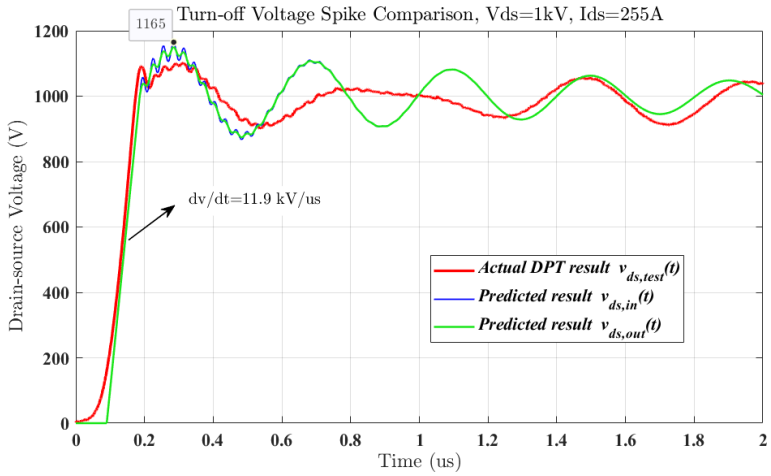


Fig. 8.1.12. 1700V SiC MOSFET hard turn-off waveforms comparison.

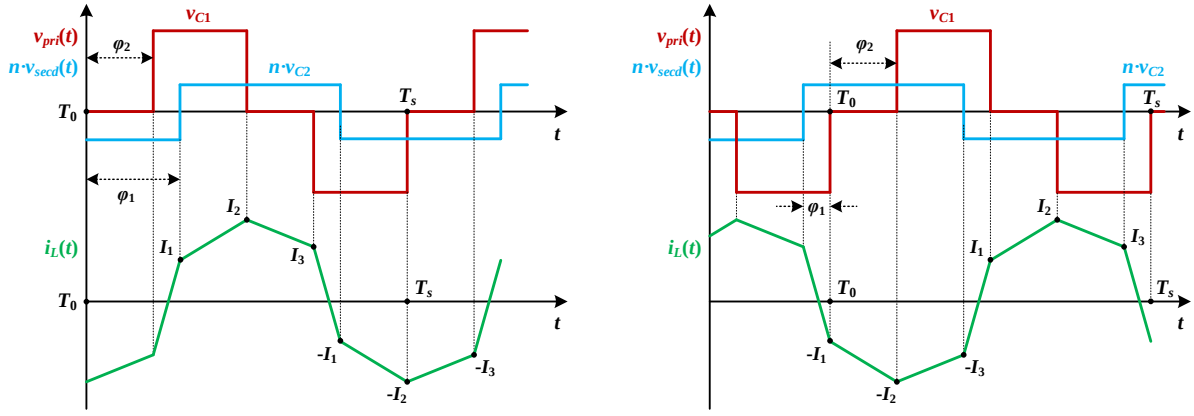
Fig. 8.1.12 shows the theoretical v_{ds_in} (t) and v_{ds_out} (t) calculation and the actual test result v_{ds_test} (t) under 1kV/255A. Due to the loop inductance inside the device, the actual voltage spike across the MOSFET die inside the module is always higher than the measured voltage overshoot across the device outside terminals. The peak drain-source terminal voltage was observed as 1108V from the waveform of v_{ds_test} (t) at dv/dt=11.9kV/us. The calculated voltage spike across the drain source terminals outside the device is 1150V. After taking the internal L_{module} of the device into consideration, the actual voltage across the drain source terminals is around 1166V. Therefore, the prediction model and the test results suggest that around 75V margin can be guaranteed under 1.5kV/250A hard turn-off condition. This value would be lower when snubber capacitor is connected between the drain and source terminal. Compared to traditional laminated busbar, the optimized PCB busbar significantly reduced the overshoot voltage across the device, and the proposed voltage overshoot prediction model validates the design can be used for the 1700V SiC module in 1500V applications.

DAB based power converter operation and optimization

The proposed M4 system is a modular SST where 9 identical power modules are connected in input parallel output series (IPOS) configuration as shown in Fig. 8.1.1. Each power module has the same efficiency performance as the whole system. The DAB

topology is selected due to its inherent ZVS and buck-boost operation capabilities. Single or dual phase shift can be used to achieve the required modulation. The ZVS conditions for DAB converter under DC/AC mode are more complicated than that under DC-DC mode due to the half sine voltage across the AC-link capacitors. Besides, one drawback of the DAB converter is the high turn-off loss when the current and frequency are high. The turn-off loss can become the dominant loss at heavy load.

The proposed M4 system adopts Dual Phase Shift (DPS) modulation. Referring to Fig. 8.1.1, the single stage DAB inverter consists of the primary and secondary side full bridges connected with the MFT. The two full bridges produce phase shifted voltages vpri and vsecd, resulting in an inductor current iL. AC components of iL and isecd are rectified by the two active full bridges, leading to net DC currents i_1 and i_2 on both sides. Filter capacitors C_1 and C_2 absorb the high frequency components of i_1 and i_2. Rectified AC voltage $v_{rec}(t)$ is generated on the secondary side capacitor through the DAB converter which operates under variable switching frequency 15~60 kHz. The rectified AC voltage $v_{rec}(t)$ is connected to the grid through an IGBT unfolding bridge which switches at 60 Hz. The MFT transformer turns ratio $n=n_1:n_2$ is used in the analysis.



(a) $P_{DAB} > 0$, buck mode (b) $P_{DAB} < 0$, buck mode

Fig. 8.1.13. Typical operating waveforms of the DAB converter with DPS.

Typical waveforms of the DAB converter with DPS modulation over one switching cycle are shown in Fig. 8.1.13. φ_1 is the phase shift between DC and AC side, φ_2 is the phase shift between the two half-bridge legs of the DC side. $P_{DAB} > 0$ means the power flows from the DC to the AC grid. To guarantee ZVS for all switches under light load (LL), the energy stored in the inductor L_r is required discharge/charge the junction capacitance.

To achieve ZVS for all devices in a full bridge, a sufficient transformer current and deadtime are required to charge/discharge the four power MOSFETs equivalent capacitance C_{MOS}/Q_{MOS}. A minimum deadtime DT_{min}=500ns is used in the optimization algorithm to avoid the half bridge short circuit and a maximum deadtime DT_{max}=2us is used to allow partial ZVS turn on under light load condition.

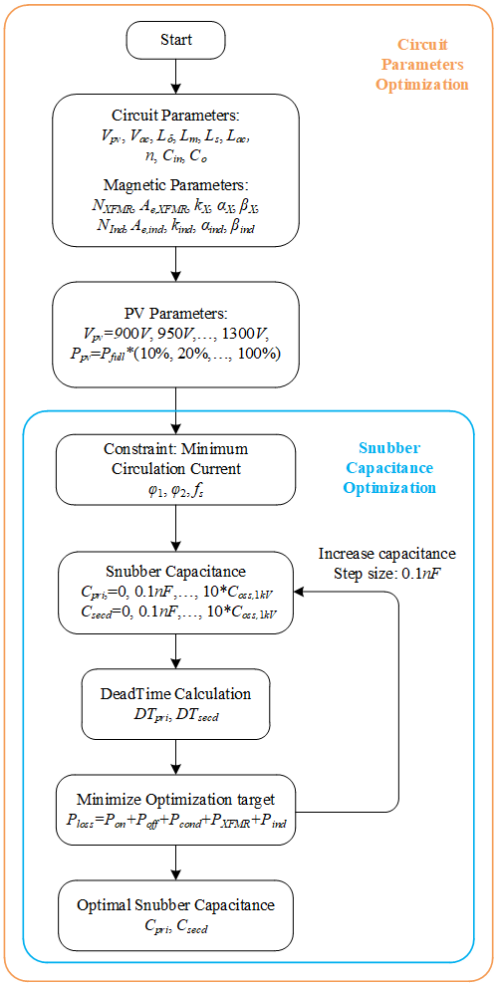


Fig. 8.1.14. Flow chart of the comprehensive optimization strategy.

Minimizing the DAB circulation current must be satisfied while meeting the ZVS condition. The turn-off loss reduction from the external snubber capacitance C_{extn} has to be traded off with the deadtime diode conduction loss. Therefore, the external C_{extn} on both the primary and secondary side could be one optimization target based on this algorithm. For a given set of hardware parameters and operation range, other parameters such as DAB high frequency inductor L_r and transformer turns ratio n, can be another optimization objective if necessary. Moreover, typical PV input voltage range V_{PV}=900V, 950V …, 1300V and load conditions P_{PV}=P_{full}*(10%, 20% …, 100%) are adopted in the optimization model in order to achieve the highest California Energy Commission (CEC) efficiency. The flow chart of the proposed optimization strategy is shown in Fig. 8.1.14.

200 kVA Medium Frequency Transformer

For the proposed M4 system, each modular converter needs a 111 kVA MFT. The peak power level is 222 kVA due to the DC/AC operation condition. The primary design challenges for the MFT are to balance the competing objectives including reliable electrical insulation, high efficiency, high power density, and superior thermal performance.

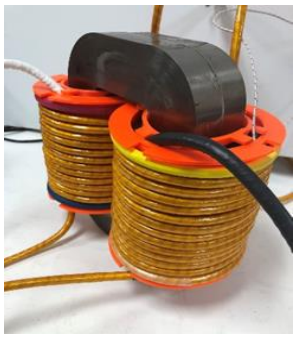


Fig. 8.1.15. Prototype picture of the fabricated MFT.

Achieving a good thermal performance is another major challenge for high power MFT due to the very unfavorable mechanical structure for heat dissipation in the MFT. Heat sources are winding and core losses. For the proposed M4 system the peak power of the MFT is 222 kVA due to the DC/AC operation characteristic. The first priority is to ensure the efficiency of the design is very high, so the heat generation is minimized. To achieve a superior cooling performance, a novel cooling structure is proposed which utilizes two 3D-printed bobbins layers, as shown in Fig. 8.1.15. The 3D printed structure can provide airflow channels for the core and windings.

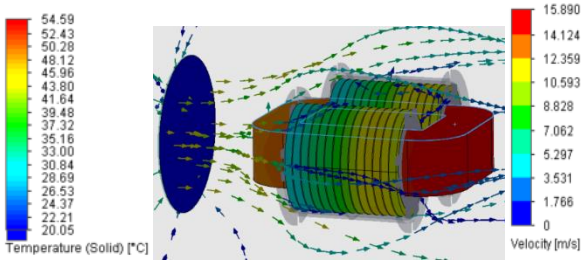


Fig. 8.1.16. Fluid thermal simulation of MFT with 15m/s airflow.

To illustrate the effectiveness of the proposed cooling system, a 3D thermal simulation is conducted with forced air-cooling condition as shown in Fig. 8.1.16. The MFT hotspot temperature is around 54°C which matches well with the 200kW experimental results as shown in Fig. 8.1.17.

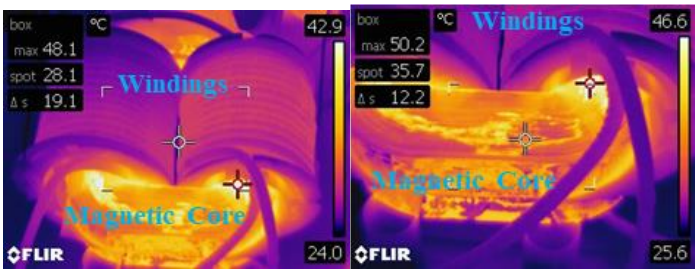


Fig. 8.1.17. Thermal test results of the MFT in DAB DC/DC test at 200kW.

Fig. 8.1.18 shows the calculated MFT efficiency and hotspot temperature at power ratings up to 400 kW. The hotspot is at the inner windings, and it rises rapidly at higher power levels. The designed MFT can safely operate at 340kW with steady-state temperature lower than 100°C.

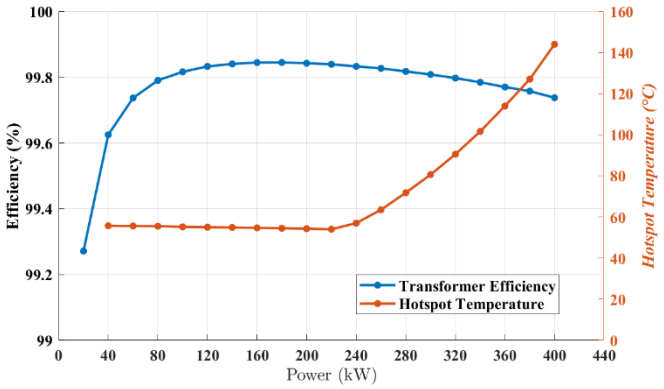


Fig. 8.1.18. MFT efficiency and hotspot temperature estimation.

For the parallel-concentric winding structure shown in Fig. 8.1.5, the well-coupled layout of the primary and secondary windings creates a challenge for achieving good electrical insulation. To address this issue, a new insulation structure is proposed, which utilizes two 3D printed bobbin layers separated by an air channel. The new design has passed 7.5kV PD and 25kV DC insulation test as shown in Fig. 8.1.19 and Fig. 8.1.20. These results indicate that the developed MFT is capable of the 4.16kV operation condition.

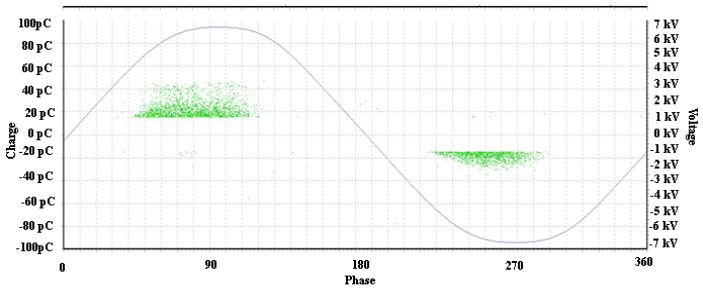


Fig. 8.1.19. PD pattern diagram at AC 60 Hz 7.5 kV peak (5-minute test data).

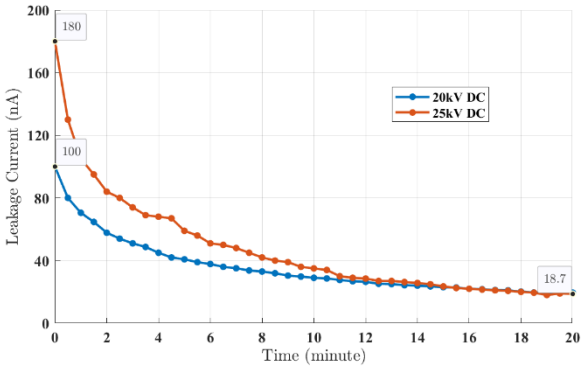
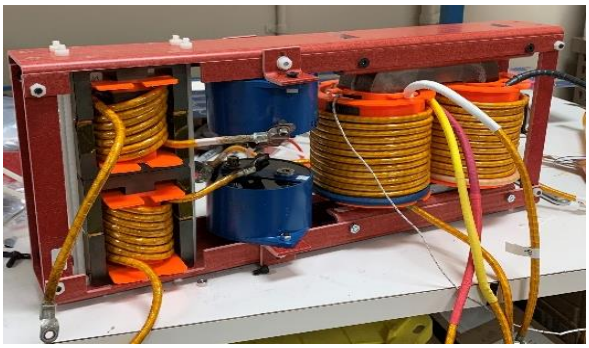


Fig. 8.1.20. DC insulation test of the developed MFT.

Fig. 8.1.21 shows the final fabricated SiC submodule. The power density is 26W/inch^3 (1.6MW/m^3) which is higher than most of industry product.

(a) primary and secondary power stage

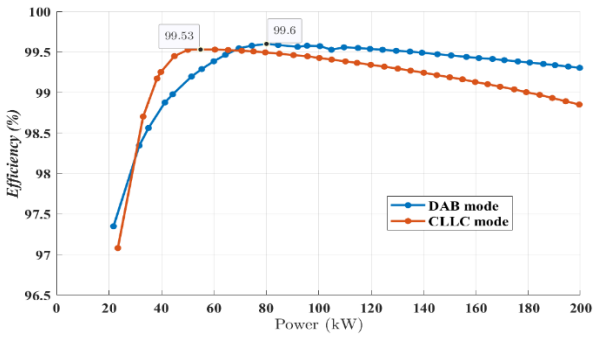


(b) magnetics

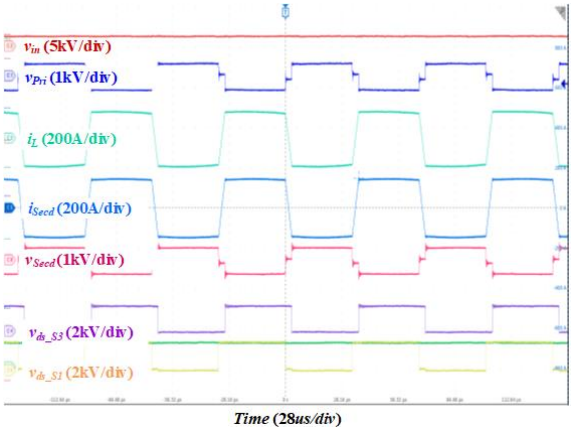
Fig. 8.1.21. Fabricated 111kVA SiC M4 submodule.

M4 submodule experiment results

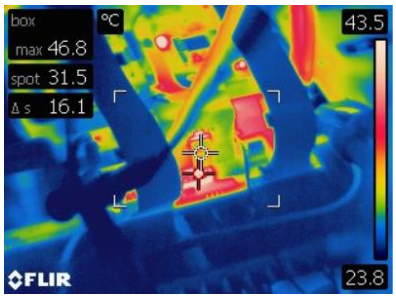
In order to justify the proposed hardware design and optimization strategy, and to verify the sufficient capability of the proposed M4 submodule for supporting multiple functionalities as a whole system, necessary experiments of both the PV and battery ports are performed and tested.



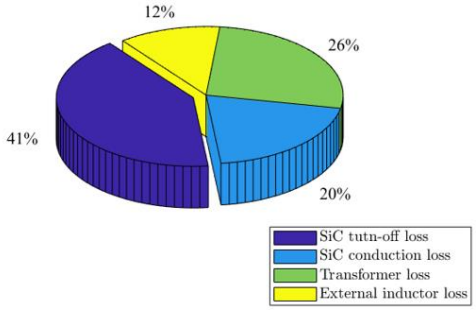
(a) 1.3kV DC/DC back-to-back efficiency curves



(b) Key waveforms under 200 kW



(c) PCB surface temperature rise under 200 kW



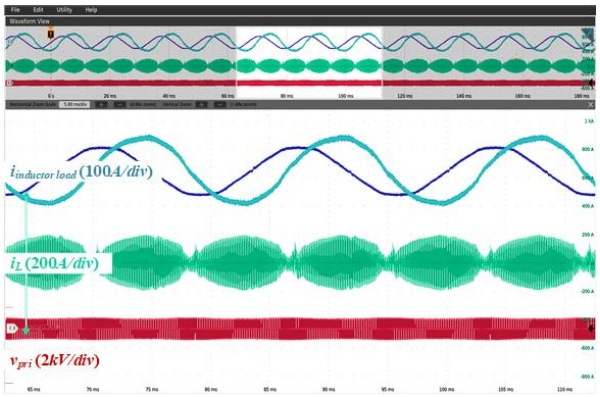
(d) Loss breakdown under 200 kW/98.85%

Fig. 8.1.22. M4 submodule DC/DC back-to-back experimental results.

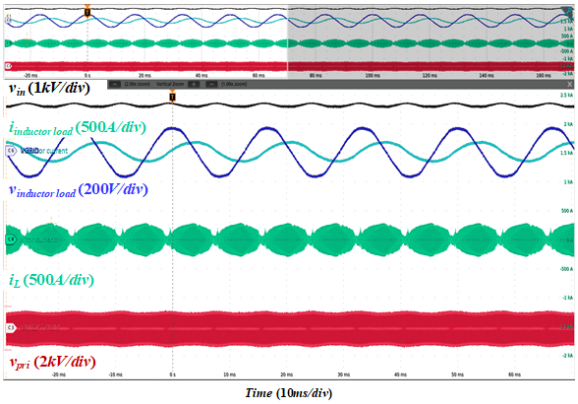
To verify the thermal and electrical performance of the converter, a 1.3kV/200kW DC/DC test is conducted using the designed MFT. The switching frequency is 15kHz. The maximum efficiency point is 99.53% at 60 kW and 98.85% at 200kW as shown in Fig.

8.1.22(a). The 99.53% peak efficiency is the highest DAB converter ever reported in this power range. The HIOKI power analyzer PW6001 with 1500V voltage range and 500A/±0.02% high-accuracy sensors CT6875 is used in the high power test.

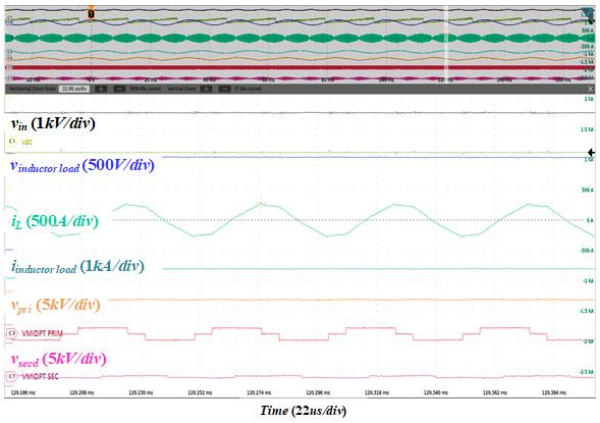
The blue curve is the efficiency of DAB operating in resonant (CLLC) mode which has higher efficiency (99.6% peak), especially under heavy load. Some key waveforms are listed in Fig. 8.1.22(b), the maximum turn-off current of the primary side MOSFETs is around 180A. The voltage overshoot across the drain source terminal is less than 100V under this condition. The temperature rises on the PCB surface is only 23°C as shown in Fig. 8.1.22 (c). The temperature rises of transformer core, winding and external inductors are detailed in section IV. The 200kW DC/DC back-to-back test is performed for totally around 2 hours in order to get a steady state thermal result.



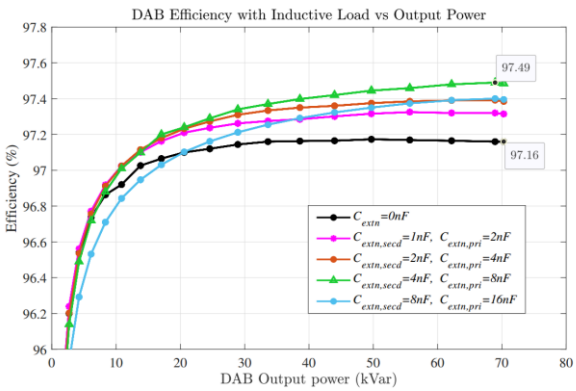
(a) Key waveforms under 31kVar



(b) Key waveforms under 70kVar



(c) Zoomed in waveforms at voltage zero crossing



(d) DAB efficiency curves comparison with C_{extn}

Fig. 8.1.23. M4 submodule DC/AC inductive load experimental results.

The developed SiC submodule is also tested in DC/AC mode with an inductive load. The DC side voltage is 1000V. Dual phase shift is used in this test. This condition is the worst operation condition for the DAB DC/AC converter. In addition to the dual phase shifts, the switching frequency is also varied from 15kHz to 40kHz. The maximum tested efficiency is 97.49% at 70kVar as shown in Fig. 8.1.23 (d). Some key test waveforms and the zoomed in waveforms over few switching cycles is shown in Fig. 8.1.23 (a)-(c). The

maximum turn-off current of the primary side MOSFETs is around 290A under inductive mode which is higher than that under real power DC/AC mode. The THD of inductive load current as shown in Fig. 8.1.23 (b) is 4.5%. The voltage overshoot across the drain source terminal is around 150V under this condition.

900V Battery Energy Storage System Development

The M4 Inverter is designed for 1500V PV system with a DC coupled storage port. The storage is interfaced with the PV via a SiC boost converter. Therefore the battery voltage need to be lower than the PV voltage. Potential storage devices include lithium ion battery. In this project, the high reliability LTO battery from Toshiba International used. The advantages of the LTO battery are

- Made with Lithium Titanate, Providing Exceptionally Long Life
- Provides Up to a 100% Usable Range of SOC without Compromising Cycle Life, Allowing for More Use of Rated Capacity
- High Output Performance Equivalent to Ultra-Capacitors, Ensuring Sufficient Power Output for High Power Application Needs
- Superb Performance Even at Temperatures as Low as -30°C, Providing Excellent Application Performance in Extreme Environmental Conditions
- Produced on State-of-the-Art Automated High Volume Production Line, Ensuring the Highest Quality & Stable Supply

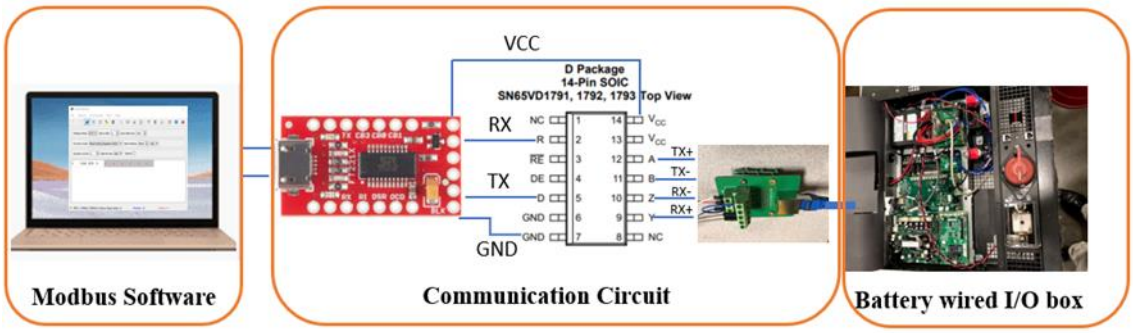
Toshiba International team has a developed a 900V LTO battery system for the M4 Inverter. The battery cabinet has been completely assembled as shown in Fig. 8.1.24. The I/O containing all of the PCBs and BMU (BMS) are wired. BMU and Host boards have been tested and the battery rack has been tested for 5C discharging, 3C charging. These test meet or exceed the project milestone targets.

(a) Wired I/O box

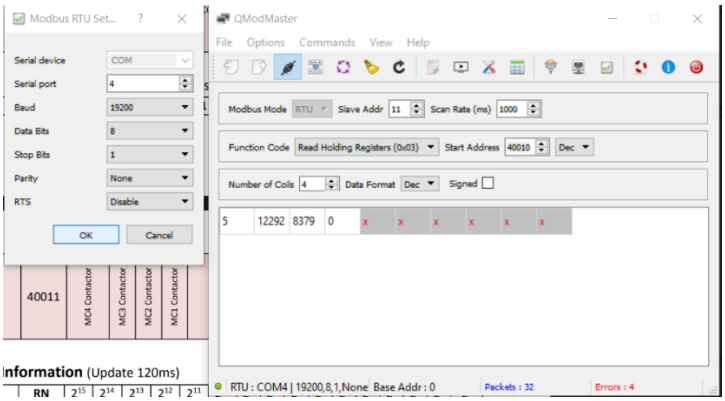
(b) Battery cabinet and wired batteries

Fig. 8.1.24 New cabinet design for the M4 battery string (28 battery modules)

The battery communication test has been verified. Fig. 8.1.25(a) shows the Battery communication system diagram which includes Modbus software, communication circuit and battery I/O box. Fig. 8.1.25(b) shows the workspace of Modbus software which shows the read information of battery. All required battery information like string voltage, string charge current successfully, can be read and displayed on the screen.



(a) Battery communication test diagram



(b) Battery information shows with Modbus software

Fig. 8.1.25 Battery communication test results

8.2 Cost-Benefit Analysis and Reliability Assessment

The project from University of Texas at Austin, Argonne National Lab, Temple University, and ERCOT are involved in this major activity.

The major outcomes include: (1) The multi-function cost-benefit analysis of M4 inverter and related rating optimization; (2) The design and technical details of a holistic LCOE evaluation framework of PV systems. Particularly, compared to conventional approaches, the grid support function is valuated and incorporated into the LCOE calculation. A typical example with field data from ERCOT (Texas, United States) is selected to show the procedure of the grid support function valuation. (3) Further, the service lifetime of the critical components (i.e., semiconductor devices and capacitors) in PV systems is specifically evaluated. More importantly, it clarifies the relationship between lifetime estimation and LCOE evaluation and highlights the developed LCOE evaluation framework. (4) Meanwhile, to address the uncertainties, sequential Monte Carlo simulation (SMCS) is integrated into the lifetime estimation procedure, which further addresses the impacts of parameter uncertainties in LCOE calculation. (5) Field data are collected to validate the proposed LCOE evaluation framework and to provide guidance on the tradeoff between reliability improvement and O&M cost reductions.

A: Cost Benefit Analysis and System Operation Optimization

The major accomplishments are:

- Conducted deterministic analysis on the fast responding regulation service (FRRS) based on field data from ERCOT.
- Designed operational mechanism of M4 inverter during FRRS to evaluate and ensure performance of photovoltaic (PV) system with M4 inverter.
- Calculated energy constraints and power constraints of battery in PV system with M4 inverter based on the guideline that the battery associated with the PV systems will operate between specified range of state-of-charge (SOC) and respond to all the requests from ERCOT without any violations.
- Working on the FRRS simulation with uncertainty to provide boundary of battery constraints based on the data patterns observed in actual implementation.
- Conducted the LCOE comparison based on different battery requirements of benchmark PV system and PV system with M4 inverter, focusing on providing FRRS.
- Provided illustration on the definition of benchmark PV system and corresponding revision (equipped with a standalone battery system) for participating in FRRS.

Deterministic Analysis on the FRRS

The team has conducted deterministic analysis on the FRRS based on the actual implementation data in ERCOT. The objective of this task is to evaluate the operational requirements we need to put on M4 inverter in order to participate in FRRS at ERCOT without violations.

The FRRS implementation data on both responsibility and command values are provided by the team partner ERCOT, as included in their datasets of ERCOT FRRS in January 2017. The PV profile data is obtained from historical data of solar panel at University of Houston in January 2017.

Operation Mechanism of M4 Inverter during FRRS

In order to properly evaluate the operation of M4 inverter, specifically the 3 ports at PV side, battery side and AC side, the project team designed the mechanism to evaluate and ensure the suitable operation scheme of PV system with M4 inverter.

The operation mechanism during FRRS-Up service is given in Fig. 8.2.1. (1) When FRRS-Up is requested, the PV system with M4 inverter will keep PV generation at the original level according to ERCOT's requirements. On the other hand, the battery will discharge to satisfy the requirements of FRRS-Up command. (2) When there are not any requests of FRRS-Up, the PV panel will charge the battery until the battery reaches the specified SOC level (50% in current analysis), and the surplus power will be delivered to AC grid. In the meantime, the battery will try to stay at the specified SOC level.

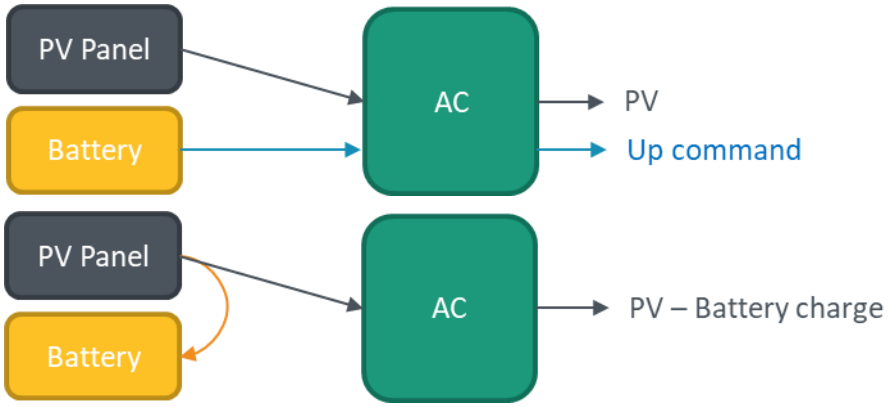


Fig.8.2.1 Operation mechanism of FRRS-Up service.

The operation mechanism during FRRS-Dn service is given in Fig. 8.2.2. (1) When FRRS-Dn is requested, the PV system with M4 inverter will keep PV generation at the original level according to ERCOT's requirements. On the other hand, the battery will be charged using the PV system at the power level of FRRS down service. (2) When there are not any requests of FRRS-Dn, there are two mechanisms to ensure AC port limit. When there is PV output power to the AC side, the battery does not discharge; When there is not any PV output power, the battery is discharged at a specified power level (0.5MW in current analysis). In the meantime, the battery is maintained at the specified SOC level.

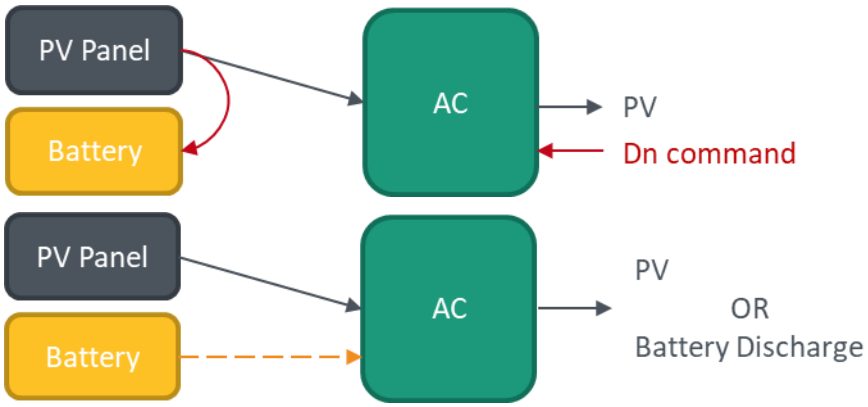


Fig.8.2.2 Operation mechanism of FRRS-Dn service.

The participation in FRRS-Up or FRRS-Dn will be determined by the daily revenue known in the Day-Ahead-Market (DAM). According to the historical data obtained from ERCOT, the daily revenue to participate in FRRS-Up and FRRS-Dn are shown respectively in Fig. 8.2.3. After choosing the highest daily revenue, the participation choice for each day in Jan 2017 is determined in Fig. 8.2.4.

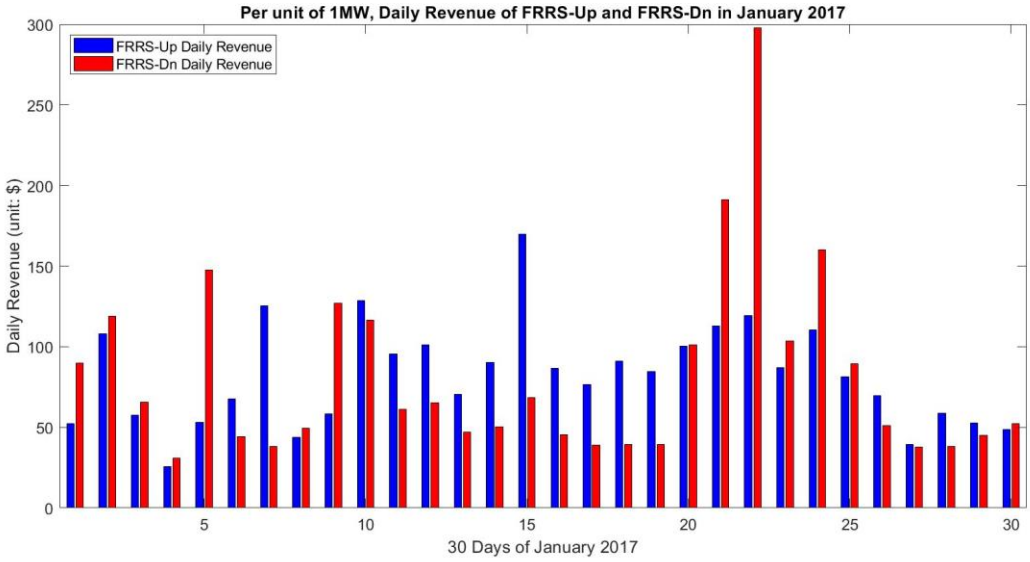


Fig.8.2.3 Daily revenue of FRRS-Up and FRRS-Dn services in Jan 2017.

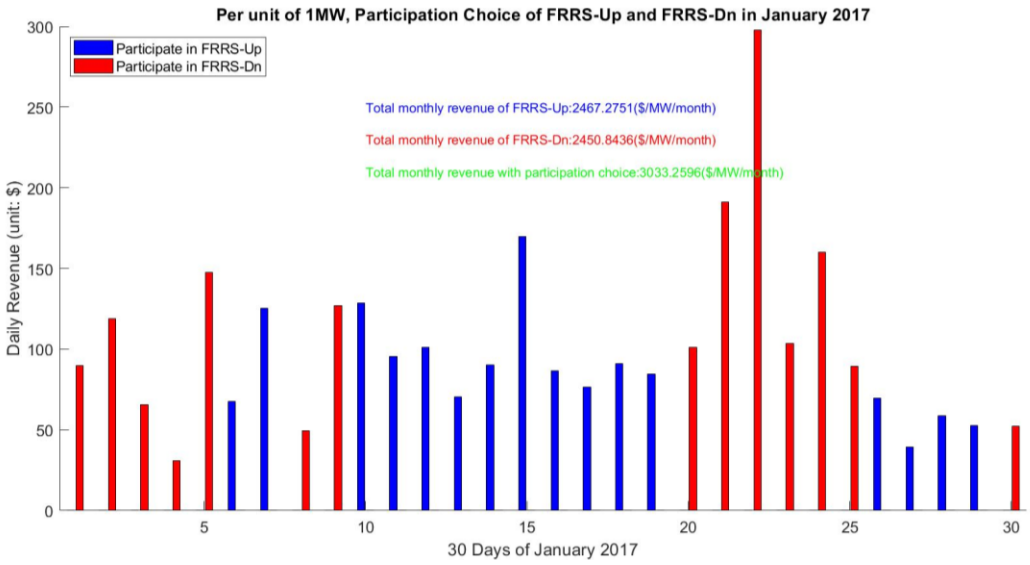


Fig.8.2.4 Participation choice based on daily revenue.

Capacity and Power Constraints of Batteries for Participation in FRRS

Based on the above preparation, the deterministic analysis of FRRS based on ERCOT historical data can be conducted to obtain the remaining energy and the charge/discharge rate of battery. In order to participate in FRRS without violations, it is required to design the battery of M4 inverter that satisfies the minimum energy and power constraints based on the thresholds observed in this analysis.

As shown in Fig. 8.2.5, the plot in the first panel is the remaining energy of battery in this deterministic analysis; the plot in the second panel is the PV profile of Jan 2017; the plot in the third panel is the FRRS commands from ERCOT, the choice of participation is determined in DAM.

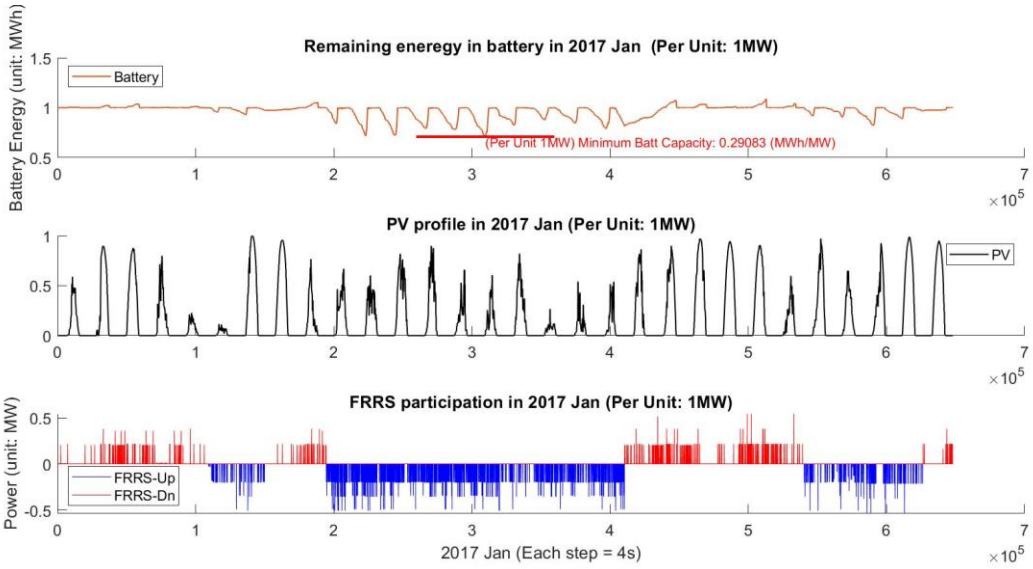


Fig.8.2.5 Remaining energy of battery, energy constraint of battery.

According to operation mechanism described earlier, the battery SOC is maintained at around 50% with repetitive charging and discharging. The maximum deviation from 50% SOC is the minimum requirement on the battery if the PV system with M4 inverter wants to participate in FRRS without violations.

It is seen in Fig. 8.2.5 that the maximum deviation is around 0.3 MWh in the 1 MW per unit analysis. Therefore, the energy constraint of battery in the PV system with M4 inverter should be 0.6 MWh.

On the contrary, for a benchmark PV system to participate in FRRS, it would need a standalone battery to meet the requirement. In addition, due to the lack of coordination function, such as that provided by the M4 inverter, the capacity of battery in the benchmark PV system would be much larger because it will have marginal support from PV panel to charge/discharge back to a specified SOC level after participating in FRRS. Based on the industrial practice experience from project team partners and the FRRS command data from ERCOT, in order to fully supply the 8 MWh of total energy requirement in FRRS command without violation, the energy constraint of battery in the

benchmark system is set at 2.5 MWh in this analysis, which is much higher compared with PV system with M4 inverter at 0.6 MWh.

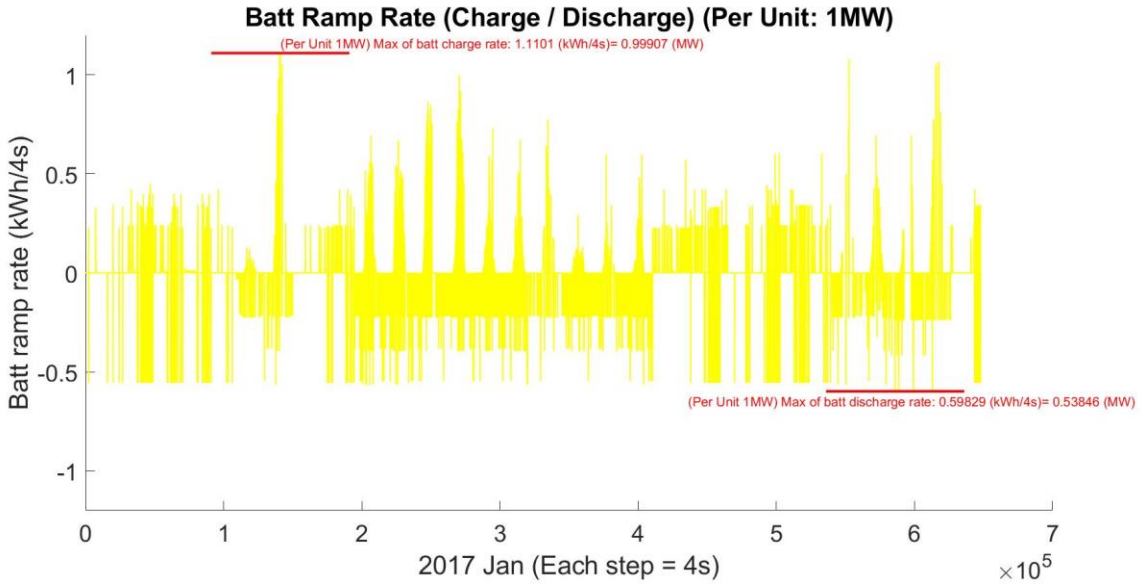


Fig. 8.2.6 Charge/discharge rate of battery, power constraint of battery.

As shown in Fig. 8.2.6, the team also evaluated the charge/discharge rate of battery in order to determine the power constraint on the battery system in the PV system with M4 inverter. As observed in the figure, the minimum power constraint should be 1MW. Combined with the energy constraint obtained earlier, the battery price should be categorized in “1-hour” type. This price information will be utilized to calculate LCOE later.

On the contrary, the benchmark PV system with the standalone battery should also have power constraint of 1 MW to ensure no violation. However, this would make the battery in benchmark system“4-hour” type[2]. Noted that the per MWh battery cost would be lower in the benchmark system but the total cost of battery would be higher in the benchmark system due to the large energy constraint in the benchmark system without M4 inverter.

FRRS Simulation with Uncertainty

Furthermore, in order to include the data variations in the actual implementations, we are currently working on extracting the data patterns from historical data and conduct simulation with uncertainty in PV profile, FRRS operation and participation of PV system with M4 inverter.

Some preliminary results are shown in Fig.8.2.7.

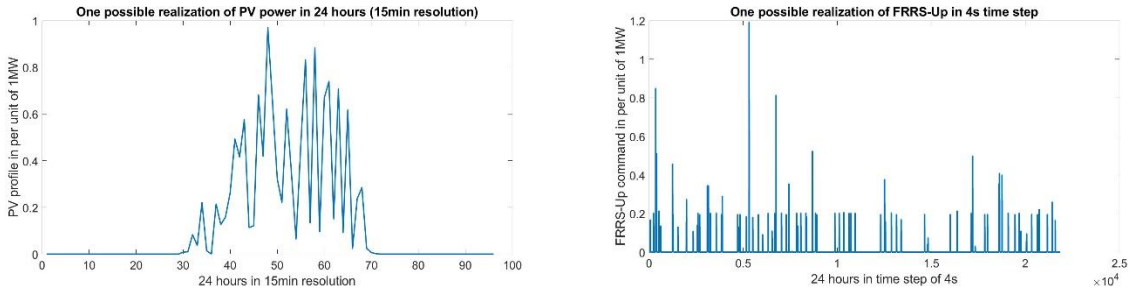


Fig.8.2.7 Preliminary results of FRRS simulation with uncertainties.

As shown in Fig.8.2.7, the PV profile and FRRS commands are possible realizations in the FRRS simulation with uncertainties. The PV profile obeys the data pattern extracted from historical data, while the FRRS commands are modeled as 2-state component with patterned interval time and command time.

Calculation of LCOE Reduction based on FRRS's Constraints on Batteries

Based on the abovementioned work, the team has calculated the LCOE difference based on battery difference between benchmark PV system and PV system with M4 inverter system in order to participate in FRRS.

The calculation formula of LCOE is originated from NREL's report in November of 2018[2] and shown in (1).

$$\boldsymbol{LCOE} = \frac{(\text{PV module cost} + \text{Battery cost} + \text{Inverter cost} + \text{Electrical/Structural BOS cost}) + \text{O\&}M\ cost + Misc\ cost}{\text{Total energy produced over lifetime}} \quad (1)$$

There are several differences between benchmark PV system and PV system with M4 inverter. However, in the LCOE comparison based on the participation of FRRS, the major difference is focused on the difference between battery cost and inverter cost.

Here the benchmark PV system is updated since in order to participate in FRRS PV system with M4 inverter has to be equipped with a battery system. In this calculation, the benchmark PV system has PV plus battery at different sites. According to the above analysis, the benchmark system would have cheaper solar inverter and directional inverter; however, it needs a more expensive battery system with 2.5 MWh capacity in the 1 MW per unit PV system to participate in FRRS without reaching the capacity and power constraints.

The PV system with M4 inverter would have M4 inverter with higher inverter cost, however, its battery capacity required to participate in FRRS is reduced to 0.6 MWh.

Table 8.2.1 LCOE calculation of benchmark PV system and PV system with M4 inverter

	Inverter Price ($/ W)	**Inverter Cost ($)**	**Battery + Misc Price ($/kWh)**	**Battery Size (MWh)**	**Battery+Misc Cost ($)**	**LCOE ($ /kWh)**	**LCOE Reduction**
Benchmark PV System (Different Site)	0.172564	172,564	380	2.5	950,000	0.1105	

PV system with M4 inverter	0.210927	210,927	601	0.6	360,600	0.0860	**- 22.13%**

According to Table 8.2.1, the LCOE is calculated for both PV system and the estimated LCOE reduction from FRRS perspective in utilizing M4 inverter is around 22%.Noted that in this comparison, the designed operation mechanism could be revised in actual implementation and the M4 inverter cost could further reduce in mass production, so there could be some variations in the reduction percentage observed in the progress of future analysis.

Revised the LCOE Calculation

In project team has revised the LCOE calculation to specifically address the comment from DOE, which is to compare the LCOE of PV system w/ M4 inverter against the existing standalone PV systems.

In this updated calculation, the team further considered the revenue from grid service to provide a comprehensive evaluation of the LCOE. The comparison results are shown in Fig. 8.2.8.

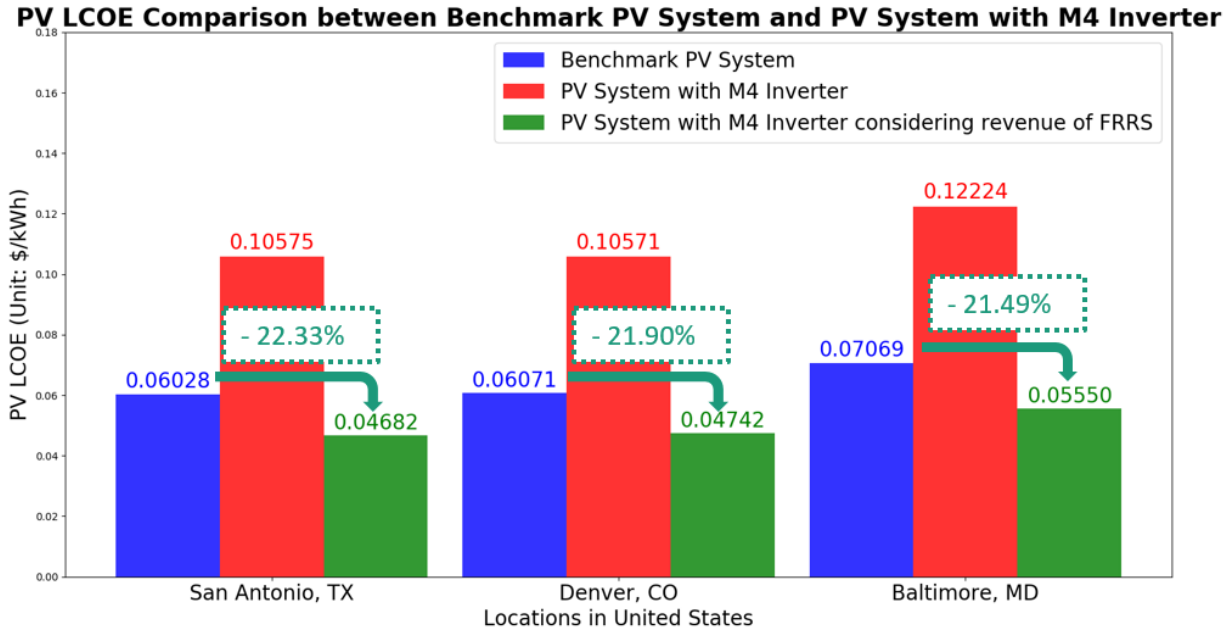


Fig. 8.2.8. Updated LCOE calculation.

As shown in Fig. 8.2.8, the three bars are derived following a similar setup as presented in BP1-Q4. The x-axis represents the LCOE measured at 3 different locations in the United States. The blue bar shows the results of the benchmark system in the comparison, which is a standalone PV system without battery considered. The red bar shows the LCOE calculated in the past quarter, while the green bar shows the updated LCOE of PV systems with M4 inverter considering the revenue of FRRS.

The differences among these three bars are illustrated in below equations

$$LCOE_{benchmark} = \frac{Becnharmakr\ cost}{Total\ energy}$$

$$LCOE_{Previous\ PV\ with\ M4\ inverter} = \frac{Becnharmakr\ cost + M4\ inverter\ cost + Battery\ cost}{Updated\ total\ energy}$$

$$LCOE_{Updated} = \frac{Becnharmakr\ cost + M4\ inverter\ cost + Battery\ cost - Revenue\ from\ FRRS}{Updated\ total\ energy}$$

In summary, the revised LCOE calculation showed that the LCOE of the PV system with M4 inverter, even compared with the standalone PV system, still has around 20% reduction in LCOE, which satisfies the criteria in the corresponding milestone.

Design of Reliability Assessment Framework

In the most recent quarter, we further polished the reliability assessment framework considering the detailed steps of deriving the inverter reliability model. The original reliability assessment framework is depicted in Fig. 8.2.9. It can be seen that the thermal model plays an important role in the entire reliability assessment framework, and we further identified that the most critical part is to design the approach of converting the thermal model of a particular inverter into its lifetime (or mean time before failure). Therefore, we focused on identifying the critical factors that should be involved in this conversion and derived the corresponding reliability model that translates the thermal characteristics into the lifetime.

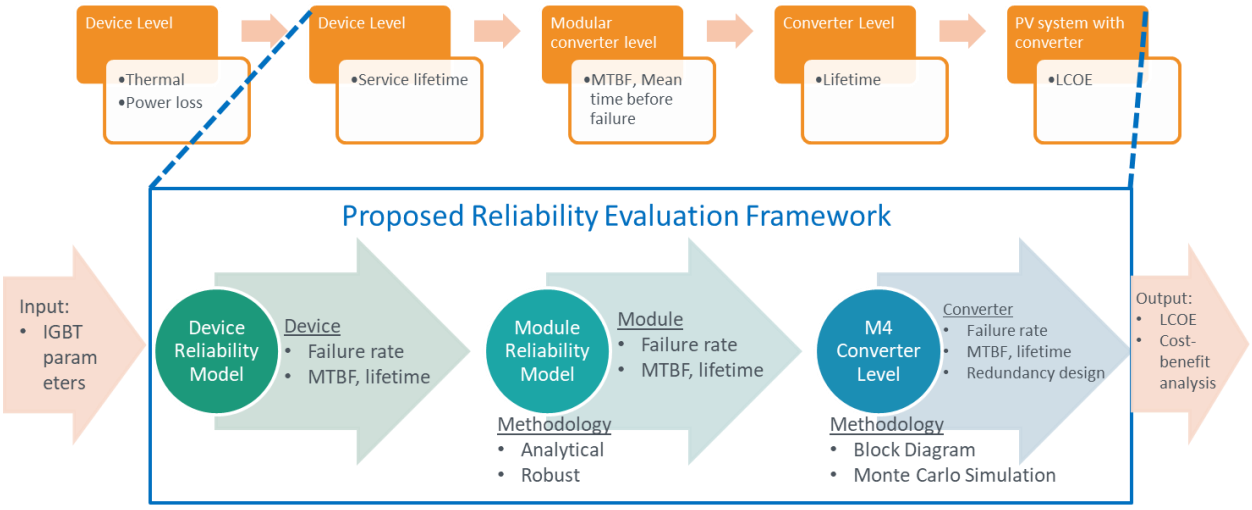


Fig. 8.2.9. Reliability assessment framework.

In the past quarters, the lifetime of inverter was derived from the empirical formulas in (7.1), but it is not generally applicable in some cases due to the determined coefficients.

$$N_f = A \cdot (\Delta T_j)^{\alpha} \cdot (ar)^{\beta_1 \Delta T_j + \beta_0} \cdot \left[\frac{C + (t_{on})^{\gamma}}{C + 1} \right] \cdot \exp\left(\frac{E_a}{k_b T_{jm}}\right) \cdot f_d \qquad (7.1)$$

where parameters A, α, β_1, β_0, C, γ, f_d, E_a and k_b are given.

On the contrary, a generic lifetime model that quantifies the impacts of multiple critical factors is adopted in (7.2)[5], where the coefficients of the estimated formula can be identified by the optimization analysis.

$$N_{\mathrm{f}} = K \cdot \Delta T_{\mathrm{j}}^{\beta_1} \cdot e^{\frac{\beta_2}{T_{\mathrm{j}}+273}} \cdot t_{\mathrm{on}}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{7.2}$$

where N_f is the number of estimated cycles, ΔT_j is the variations of junction temperature per cycle (peak-peak); T_j is the junction temperature; t_{on} is the on-state time; V is the blocking voltage; I is the current per wire; D is the diameter of the bonding wire; $\beta_1 \sim \beta_6$ and K are parameters used in this generic model.

For (7.2), N_f is the number of cycles to failure of each power electronic device, which shows the estimated cycles under the given operational stress. Assuming T_{cycle} is the time duration of each period, the lifetime L of each device can be estimated as:

$$L = T_{\mathrm{cycle}} \cdot N_{\mathrm{f}} \tag{7.3}$$

Therefore, the lifetime of the entire inverter is the minimum lifetime of all the devices.

Reliability Model of Modular M4 Inverters

To conduct a comprehensive and comparative reliability analysis, we estimated the lifetime of modular M4 inverters based upon both Si IGBT and SiC MOSFET.

For the lifetime estimation with Si IGBT, the empirical formula in (7.2) is used. Note that $\beta_1 \sim \beta_6$ and K are the parameters that need to be determined during the lifetime estimation. We selected three typical devices in the modular M4 inverters to derive their thermal dynamics and other operational parameters, and thereby derive the estimated lifetime. The three typical devices are selected. Among them, P_1 and S_1 (high-frequency switching) are the devices at the primary and secondary sides of the dual active bridge (DAB), and the Q_1 (line-frequency switching) is the device at the unfolding stage.

A 24-hour operational cycle is selected based on the field operational conditions (e.g., solar profile, ERCOT Fast Responding Regulation Service [FRRS], etc.) we derived in the BP1. The thermal changes of the three devices are shown below in Fig. 8.2.10.

[5] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for Power Cycling Lifetime of IGBT Modules - Various Factors Influencing Lifetime," *in Proc. IEEE CIPS*, 2008.

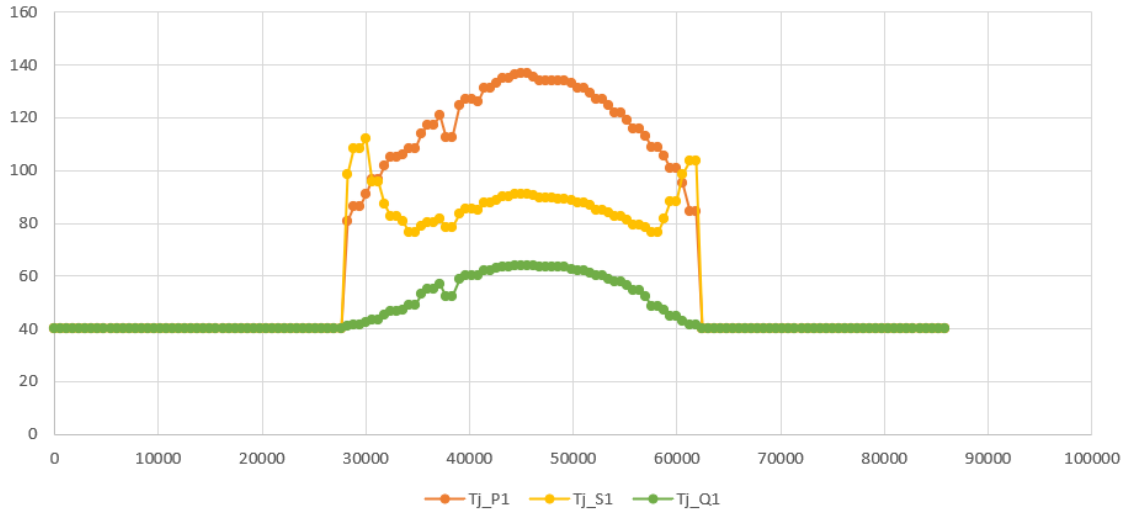


Fig. 8.2.10. Thermal changes of three typical devices in M4 inverters during a 24-hour cycle.

Given the inverter lifetime data (e.g., warranty or maintenance cycle) of industrial inverters and the operational parameters extracted above, the unknown parameters in (7.2), i.e., β_1 ~ β_6 and K, can be determined using a regression approach with the following constraints:

$$\begin{cases} \beta_{1\_0} - \Delta\beta_1 \le \beta_1 \le \beta_{1\_0} + \Delta\beta_1 \\ \beta_{2\_0} - \Delta\beta_2 \le \beta_2 \le \beta_{2\_0} + \Delta\beta_2 \\ \quad \cdots \\ \beta_{6\_0} - \Delta\beta_6 \le \beta_6 \le \beta_{6\_0} + \Delta\beta_6 \\ 0 < K \end{cases} \tag{7.4}$$

where $\Delta\beta_i$ (i = 1, 2, …, 6) is the confidence interval of the corresponding β_i.

In the current study, based on the conditions extracted from the operational data, listed in Table 8.2.2, the above unknown parameters can be determined, as shown in Table 8.2.3.

Table 8.2.2. Operational Parameters

Parameter	Value	Parameter	Value
ΔT_{j_P1}	96.53	t_{on}	186000
ΔT_{j_S1}	71.92		
ΔT_{j_Q1}	23.77	V	120
T_{j_P1}	72.43	I	1300
T_{j_S1}	58.82		
T_{j_Q1}	45.73	D	500e-6

Table 8.2.3. Estimated Parameters in (7.2)

Parameter	Value	Parameter	Value	Parameter	Value
β_{1_0}	-3.483	$\Delta\beta_1$	0.263	β_1	-3.22
β_{2_0}	1.917×10^3	$\Delta\beta_2$	413.137	β_2	2.33×10^3

β_{3_0}	-0.438	$\Delta\beta_3$	0.101	β_3	-0.337
β_{4_0}	-0.717	$\Delta\beta_4$	0.24	β_4	-0.477
β_{5_0}	-0.751	$\Delta\beta_5$	0.176	β_5	-0.575
β_{6_0}	-0.564	$\Delta\beta_6$	0.496	β_6	-1.053
				K	6.852×10^7

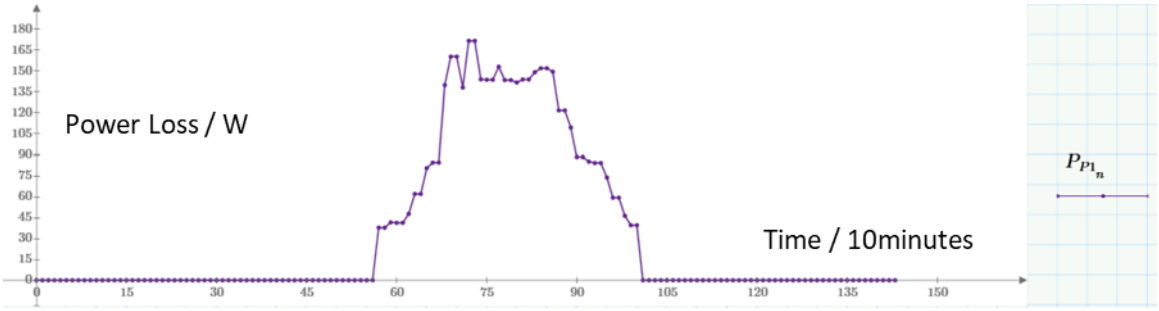
Furthermore, to evaluate the reliability of 1700V SiC power module HT-3234, a typical lifetime prediction methodology is used in this project which could be divided into three parts as below: 1) Modeling of the number of cycles to failure (N_f) using the data from the qualification report; 2) Actual daily mission profile extraction and ambient temperature ripple; 3) Miner's law for cumulative damage (the final number of cycles to failure (N_f) is determined when the cumulative damage greater than 1, which means failure will occur).

According to the estimated equation (1) of Number of cycles to failure (N_f), in which ΔT_j is the junction temperature ripple (°C), T_{j_max} is the maximum junction temperature(°C), t_{on} is the total conduction time per cycle (s).

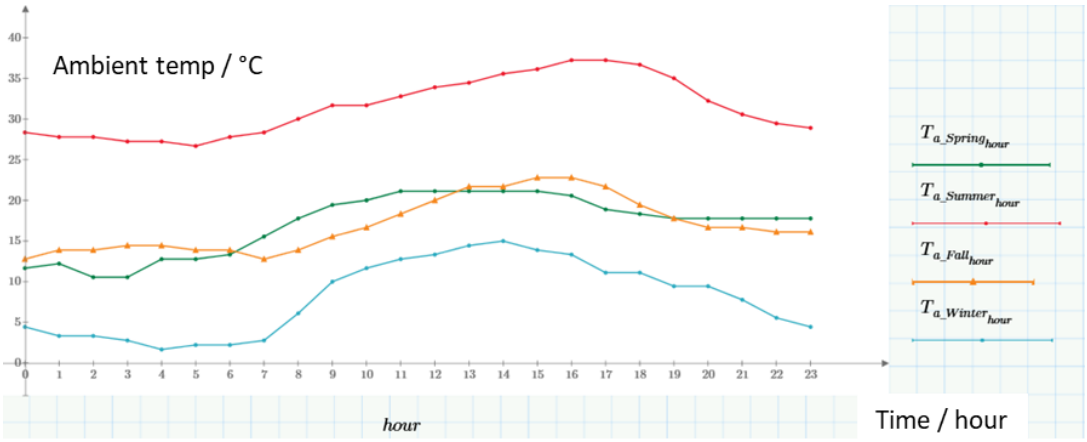
$$N_f = K \cdot \left(\Delta T_j\right)^{\beta_1} \cdot e^{\frac{\beta_2}{T_{j\_max}+273}} \cdot t_{on}^{\beta_3} \tag{7.5}$$

Reasonable values of β_1, β_2, β_3, K could be solved based on the qualification report from CREE. Note that to solve the coefficients β_1, β_2, β_3, K, we assume the module will fail immediately after the given cycles in each test specified in the qualification report. Therefore, the final lifetime results could be very conservative.

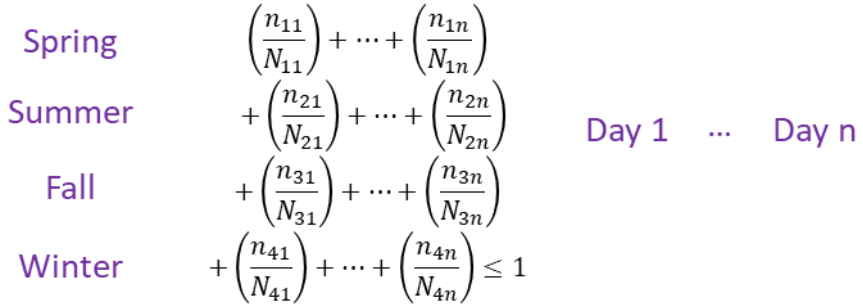
Based on the daily output power mission profile of the M4 inverter, power loss distribution profile, and typical ambient temperature ripples in Austin, Texas, and the fatigue estimation approach: Miner's rule as shown in Fig. 8.2.11, we can estimate the equivalent lifetime of the M4 inverter is 12.11 years. Fig. 8.2.11 also shows a typical daily power loss distribution profile and ambient temperature ripples in Austin, Texas.



(a) Daily power loss distribution.



(b) Ambient temperature.



(c) Fatigue estimation approach: Miner's rule.

Fig. 8.2.11. Power loss distribution, ambient conditions, and fatigue estimation approach.

Additionally, since electrolytic capacitors have a significant impact on the reliability modeling of inverters, the lifetime estimation of electrolytic capacitors is incorporated to enhance the whole reliability evaluation framework.

Based on the failure mechanisms of electrolytic capacitors, electrical stress and thermal stress play vital roles in the lifetime of electrolytic capacitors in power applications. Specifically, the voltage influence and temperature influence can be represented by the power law relationship and Arrhenius equation in (7.7) and (7.8), respectively. Moreover, the ripple current influence is another critical factor for the capacitor lifetime estimation. The capacitor generates more internal heat leading to the temperature rise when a ripple current flows through it, which can significantly accelerate the degradation of the capacitor. In the proposed model, other influences (e.g., humidity) that have minor effects on the lifetime of electrolytic capacitors are neglected.

Particularly, the empirical model of lifetime estimation for electrolytic capacitors in terms of influences of voltage stress, temperature, and ripple current can be expressed as:

$$L_c = L_0 \cdot K_V \cdot K_T \cdot K_R \tag{7.6}$$

where L_c and L_0 are estimated actual operating lifetime and rated lifetime (hour), respectively; K_V, K_T and K_R are designed for the voltage influence, temperature influence,

and ripple current influence of lifetime estimation model, respectively. They are detailed as follows:

1) Voltage influence: For the capacitors with smaller size (e.g., radial type), the voltage influence can be ignored (K_V = 1), while for the capacitors with larger size (e.g., snap-in and screw terminal types), the voltage influence is described by:

$$K_{\mathrm{V}} = \left(\frac{V}{V_0}\right)^{-n} \tag{7.7}$$

where V and V_0 are actual operating voltage and rated voltage, respectively; n is the exponent used by various large capacitor manufacturers. Generally, for electrolytic capacitors, n = 3 if $0.5 \le V/V_0 \le 0.8$; n = 5 if $0.8 \le V/V_0 \le 1$.

2) Temperature influence: The electrolytic capacitors follow the industry-wide well accepted 10-Kelvin law of the Arrhenius equation. The temperature factor is detailed as:

$$K_{\mathrm{T}} = 2^{\frac{T_0 - T}{10}} \tag{7.8}$$

where T is the actual ambient temperature in Kelvin; T_0 is the upper category temperature or maximum ambient temperature in Kelvin.

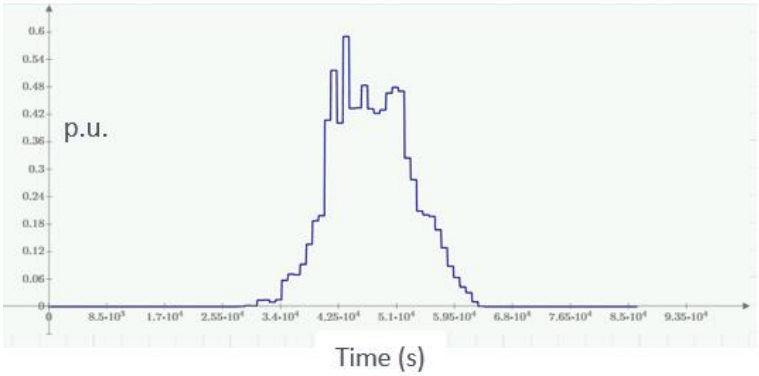
2) Ripple current influence: The effect of the ripple current on the lifetime model is given by:

$$K_{\mathrm{R}} = K_{\mathrm{i}}^{\left[1-\left(\frac{I_{\mathrm{A}}}{F_{\mathrm{c}} I_0}\right)^2\right]\frac{\Delta T_0}{10}} \tag{7.9}$$

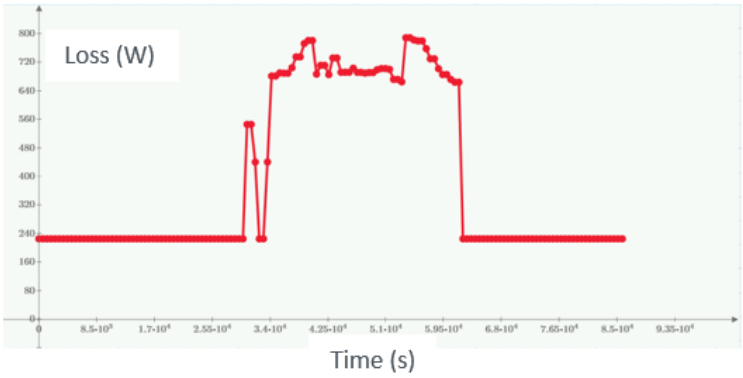
where I_A and I_0 are actual operating ripple current and rated ripple current of the capacitor, respectively; ΔT_0 is the core temperature rise of the capacitor due to rated ripple current; K_i is empirical safety factor (K_i = 4 if $I_A > I_0$; K_i = 2 if $I_A \le I_0$); F_c is the frequency correction factor that needs to be applied if I_A is not given at the same frequency as I_0.

Reliability Model considering Redundancy Design

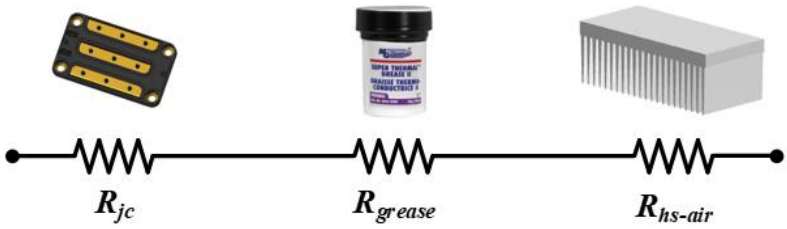
Furthermore, to evaluate the influence of redundancy design since modular architecture and hot-swappable function are adopted in the M4 system, proper reliability, or lifetime (Mean Time Between Failures, MTBF) prediction model is necessary. The lifetime model is separated into five steps, daily output power mission profile, power loss distribution profile, temperature rise daily curve, failure rates (FIT) of all components, and reliability model. Fig. 8.2.12 summarizes some typical profiles or curves.



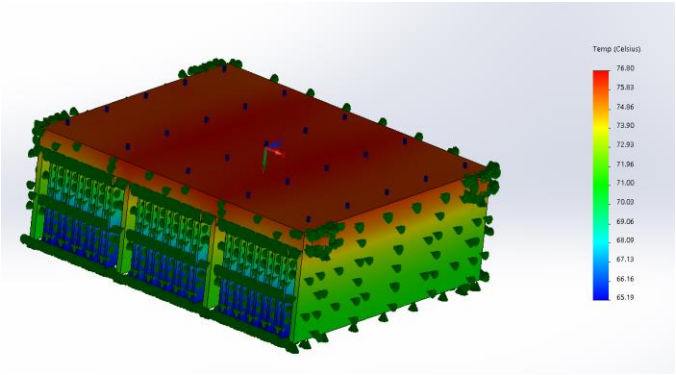
(a) Daily output power mission profile



(b) Power loss distribution profile



(c) SiC module thermal equivalent model



(d) Heatsink thermal equivalent model

Fig. 8.2.12 Different parts in lifetime model

After we get the equivalent failure rates of each power components, the equivalent failure rate (FIT) for the power submodules could be computed using the equations with different combinations are shown in Fig. 8.2.13. Each subsystem in Fig. 8.2.13 represents one power component in the M4 power submodule, such as SiC modules, transformer, DC link capacitors, and external inductors, etc. *R* in Fig. 8.2.13 represents Reliability function which is the probability that the device is still functioning at time t, i.e. $R(t)= e^{-\int_0^t \lambda(t)dt} = e^{-\lambda t}$. Mean Time Between Failures (MTBF, 1/λ) is defined as the time between two errors of an assembly or device. The Greek letter λ is the failure rate (FIT) which is defined as a failure rate per 1 billion hours.

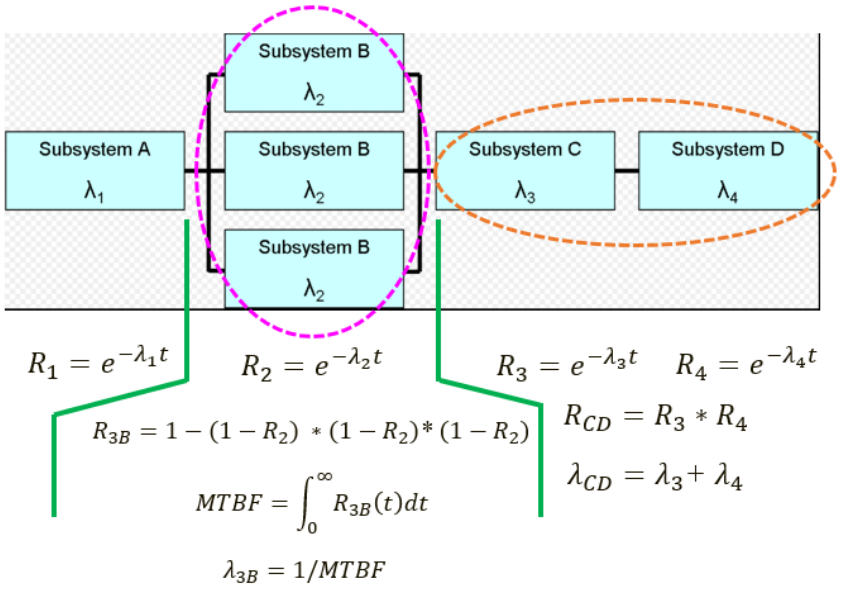
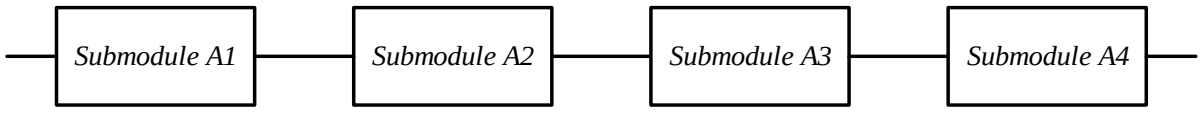


Fig. 8.2.13 Subsystems equivalent FIT equations with different combinations

Considering one redundant power submodule in the M4 system, the single-phase FIT architecture is shown in Fig. 8.2.14. According to the same algorithm, we can easily get the final FIT equivalent value for the whole M4 inverter system.



$$R_{A1} = e^{-\lambda_{A1} t}$$

$$R_A = 1 - (1 - R_{A1})^4$$

$$MTBF_A = \int_0^\infty R_A(t)dt$$

$$\lambda_A = 1/MTBF_A$$

Fig. 8.2.14 Single-phase FIT architecture with one redundant submodule

Detailed Illustration of Model Details and Data References

In the most recent quarterly review meeting, we introduced the derived LCOE calculation model and showed the comparative study highlighting the cost-benefit merits of the M4 inverter. Based on the DOE comments we received, we were asked to document the details of all the components and equipment that are used to build each model. Per the request from DOE, we further summarized our LCOE calculation. Particularly, we documented the comprehensive data references used in both models and provided detailed illustration on both models with formula breakdown and parameter illustration with data references. This will support the further calibration and revision of the LCOE calculation.

Data Reference Summary

Per the request from DOE, we have provided a comprehensive summary of all the data references used in both LCOE calculation models derived in BP2.

- **PV Benchmark System:**

[1] Fu, Ran, David Feldman, Robert Margolis, Mike Woodhouse, and Kristen Ardani. 2017. U.S. Solar Photovoltaic System Cost Benchmark: Q1 2017. Golden, CO: National Renewable Energy Laboratory. NREL/TP-6A20-68925.
[2] R. Fu, D. Feldman, and R. Margolis, “U.S. Solar Photovoltaic System Cost Benchmark: Q1 2018,” Renew. Energy, p. 63, 2018.

[3] TJ Silverman, MG Deceglie, KA Horowitz. “NREL Comparative PV LCOE Calculator.” Internet: http://pvlcoe.nrel.gov, March 2018.

- **Cost-benefit and Degradation Analysis:**

[4] D. C. Jordan and S. R. Kurtz, “Photovoltaic Degradation Rates—An Analytical Review,” Prog. Photovolt. Res. Appl., vol. 21, no. 1, pp. 12–29, 2013.

- **Battery Cost:**

[5] R. Fu, T. Remo, and R. Margolis, “2018 U.S. Utility-Scale Photovoltaics-Plus-Energy Storage System Costs Benchmark,” Renewable Energy, p. 32, 2018.

- **M4 Inverter Cost:**

[6] Cost summary and estimation of M4 inverter, UT-Austin

- **Grid Service Requirement and Dataset:**

[7] Preliminary grid service simulation

In the following sections, we will illustrate the model details of both LCOE calculation models through:

1. Detailed formula breakdown
2. Parameter illustration with data reference

Detailed formula breakdown

We introduced two LCOE calculation models to highlight different objectives in the comparative study on LCOE. In Model 1, we considered the revenue given by the selected grid service (i.e., fast responding regulation service [FRRS]) to offset the M4 inverter cost; in Model 2, we evaluated the M4 inverter cost reduction by considering the extra cost increase in the benchmark PV systems for providing additional grid services.

The following equations are used for calculating the LCOE in Model 1, and we further breakdown the formula to show the detailed calculation process.

$$\mathrm{LCOE}_{\mathrm{Benchmark}} = \frac{\text{Benchmark Cost}}{\text{Benchmark Generated Energy}} = \frac{\mathrm{Cost}_{\text{PV module}} + \mathrm{Cost}_{\mathrm{BOS}} + \mathrm{Cost}_{\mathrm{OM}}}{\mathrm{Energy}_{\text{lifetime}}}$$

$$= \frac{P_{PV} * S_{PV} + C_{BOS-basic} + \sum_{t=1}^{t=T} \frac{\mathrm{C}_{\mathrm{OM}-b}}{(1+d)^t}}{\sum_{t=1}^{t=T} \frac{\mathrm{E}_{yr} * \eta * (1-de)^{t-1}}{(1+d)^t}}$$

where

P_{PV} Represents the PV module price

S_{PV} Represents the PV module size

T Represents lifetime

$C_{BOS-basic}$ Represents the basic balance of system (BOS) cost

C_{OM-b} Represents O&M per year cost in the benchmark PV system

d Represents the discount rate

E_{yr} Represents energy generation per year

η Represents energy efficiency

de Represents degradation rate

$$\mathrm{LCOE}_{\text{PV system with M4 inverter}} = \frac{\text{Benchmark Cost} + \text{M4 Extra Cost}}{\text{Increased Generated Energy}}$$

$$= \frac{\mathrm{Cost}_{\text{PV module}} + \mathrm{Cost}_{\text{BOS}} + \text{Extra Cost}_{\text{M4 inverter}} + \text{Extra Cost}_{\text{M4 battery}} + \mathrm{Cost}_{\text{OM}} + \text{Extra Cost}_{\text{OM\_M4}}}{\text{Increased Energy}_{\text{Increased\_lifetime}}}$$

$$= \frac{P_{PV} * S_{PV} + C_{BOS-basic} + C_{BOS-inverter\ extra} + C_{BOS-batt} + \sum_{t=1}^{t=T} \frac{\mathrm{C}_{\mathrm{OM}-b} + \mathrm{C}_{\mathrm{OM}-batt}}{(1+d)^t}}{\sum_{t=1}^{t=T} \frac{\mathrm{E}_{yr} * \eta * (1-de)^{t-1}}{(1+d)^t}}$$

The items in red highlight the differences compared to the benchmark calculation.

where

$C_{BOS-inverter\ extra}$ Represents inverter cost difference

$C_{BOS-batt}$ Represents battery cost

$\mathrm{C}_{\mathrm{OM}-batt}$ Represents battery O&M cost

$$\mathrm{LCOE}_{\text{PV system with M4 inverter considering revenue}} = \frac{\text{Benchmark Cost} + \text{M4 Extra Cost} - \text{Revenue}}{\text{Increased Generated Energy}}$$

$$= \frac{\mathrm{Cost}_{\text{PV module}} + \mathrm{Cost}_{\text{BOS}} + \text{Extra Cost}_{\text{M4 inverter}} + \text{Extra Cost}_{\text{M4 battery}} + \mathrm{Cost}_{\text{OM}} + \text{Extra Cost}_{\text{OM\_M4}} - \text{Revenue}_{\text{FRRS}}}{\text{Increased Energy}_{\text{Increased\_lifetime}}}$$

$$= \frac{P_{PV} * S_{PV} + C_{BOS-basic} + C_{BOS-inverter\ extra} + C_{BOS-batt} + \sum_{t=1}^{t=T} \frac{\mathrm{C}_{\mathrm{OM}-b} + \mathrm{C}_{\mathrm{OM}-batt}}{(1+d)^t} - R * T}{\sum_{t=1}^{t=T} \frac{\mathrm{E}_{yr} * \eta * (1-de)^{t-1}}{(1+d)^t}}$$

where

R Represents revenue rate

For Model 2, the formulae used for calculating the LCOE are similar to those in Model 1 except for the terms in red in the benchmark system for providing additional grid service.

$$\mathrm{LCOE}_{\text{Benchmark PV System to Provide Grid Service}} = \frac{\text{Benchmark Cost} + \text{Benchmark Extra Cost}}{\text{Benchmark Generated Energy}}$$

$$= \frac{\mathrm{Cost}_{\text{PV module}} + \mathrm{Cost}_{\text{BOS}} + \text{Extra Cost}_{\text{Benchmark Battery}} + \mathrm{Cost}_{\text{OM}} + \text{Extra Cost}_{\text{OM\_benchmark}}}{\text{Energy}_{\text{lifetime}}}$$

$$= \frac{P_{PV} * S_{PV} + C_{BOS-basic} + C_{BOS-batt} + \sum_{t=1}^{t=T} \frac{C_{OM-b} + C_{OM-batt}}{(1+d)^t}}{\sum_{t=1}^{t=T} \frac{E_{yr} * \eta * (1-de)^{t-1}}{(1+d)^t}}$$

where

$C_{BOS-batt}$ Represents battery cost in the benchmark model

$C_{OM-batt}$ Represents battery O&M cost in the benchmark model

In this section, we document the detailed formula breakdown of both LCOE models, and in the following section, we will provide parameter illustration with data references.

Parameter Illustration with Data References

The parameters used in both LCOE calculation models are summarized in Table 8.2.4 and Table 8.2.5, respectively. Further, in this report, we will provide illustrations on these parameters, linking them to the data reference we used.

TABLE 8.2.4. COMPONENT COSTS USED IN THE LCOE CALCULATION MODEL 1

TX Location 1MW System	PV Module Cost	BOS			O&M	Generated Energy		Revenue	LCOE	LCOE Reduction
		Inverter Price ($/W)	Battery Size (MWh)	Per-Unit Total Battery Cost ($/W)	Per-Unit O&M Cost ($/W/yr)	Service Life (yr)	Energy Efficiency (%)	Per-Unit Revenue Rate ($/W/yr)		
Benchmark PV System	Same	0.04	0	0	0.015	25	96	0	0.06028	Benchmark
PV System with M4 Inverter		0.21	0.6	0.45	0.015 + 0.014	30	98	0.036	0.09496	
PV System with M4 Inverter Considering Revenue		0.21	0.6	0.45	0.015 + 0.014	30	98	0.036	0.04205	30.25%

TABLE 8.2.5. COMPONENT COSTS USED IN THE LCOE CALCULATION MODEL 2

1MW System	PV Module Cost	BOS			O&M	Generated Energy		LCOE	LCOE Reduction
		Inverter Price ($/W)	Battery Size (MWh)	Per-Unit Total Battery Cost ($/W)	Per-Unit O&M Cost ($/W/yr)	Service Life (yr)	Energy Efficiency (%)		
Benchmark PV System	Same	0.04	0	0	0.015	25	96	0.06028	
Benchmark PV System to Provide Grid Service		0.21	2.5	0.95	0.015 + 0.020	25	96	0.12388	Benchmark
PV System with M4 Inverter		0.21	0.6	0.45	0.015 + 0.014	30	98	0.09496	23.34%

We categorized the parameters used in the following groups to provide detailed illustrations. All the data references used are documented in the 'data reference summary' section.

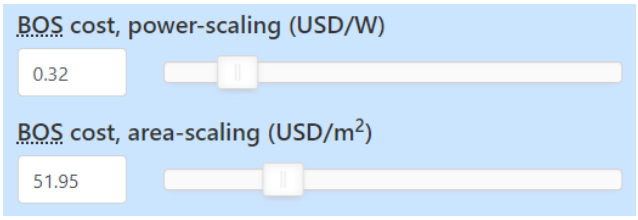
- PV Module Cost

PV module cost is shown in the first column of Table 8.2.4, and they are extracted from [1] on Page 35.

Module price	$0.35/Wdc	Ex-factory gate (first buyer) price, Tier 1 modules	Bloomberg (2017), NREL (2017)

- Basic BOS Cost

The basic BOS cost is extracted from [3] for both power-scaling and area-scaling components. The figure below shows the values with a preset location at TX.



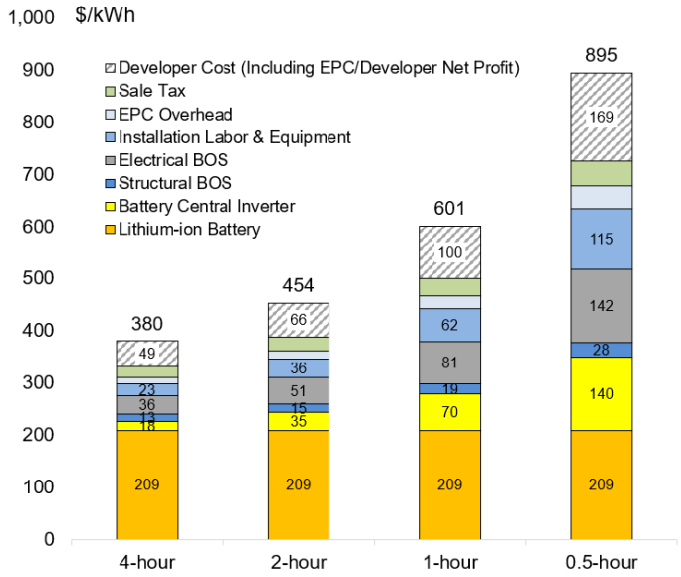
- Inverter Cost

The benchmark inverter cost and M4 inverter cost is extracted from Page 31 in [2] and [6], respectively.

Inverter price	$0.04/Wdc (fixed-tilt) $0.05/Wdc (one-axis tracker)	Ex-factory gate (first buyer) price, Tier 1 inverters DC-to-AC ratio = 1.36 for fixed-tilt and 1.30 for one-axis tracker	Bloomberg (2018), Bolinger and Seel (2018), NREL (2018)

- Battery Cost

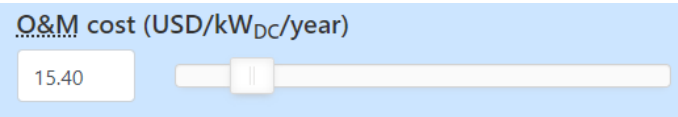
The battery cost is extracted from Page 11 in [5] with the corresponding battery sizes listed below.



- O&M Cost

The O&M cost is extracted from [3] at corresponding locations.

The figure below shows the values with a preset location at TX.



- Generated Energy

The generated energy is extracted from [3] at the corresponding locations. The degradation rate is extracted from Page 18 in [4]

- Revenue

The revenue is determined based on grid service simulation and ERCOT field FRRS data [7].

Development of Reliability Evaluation Framework

In the final year of the project, we are developing the reliability evaluation framework and highlighted the end goal as demonstrating the reliability of M4 inverter. The flow chart below is a figurative summary of the major steps in the framework being developed. In the past quarter (BP3-Q4), we focused on the (1) system-level simulation, (2) LCOE evaluation, (3) Preparations for optimization on LCOE-reliability tradeoff.

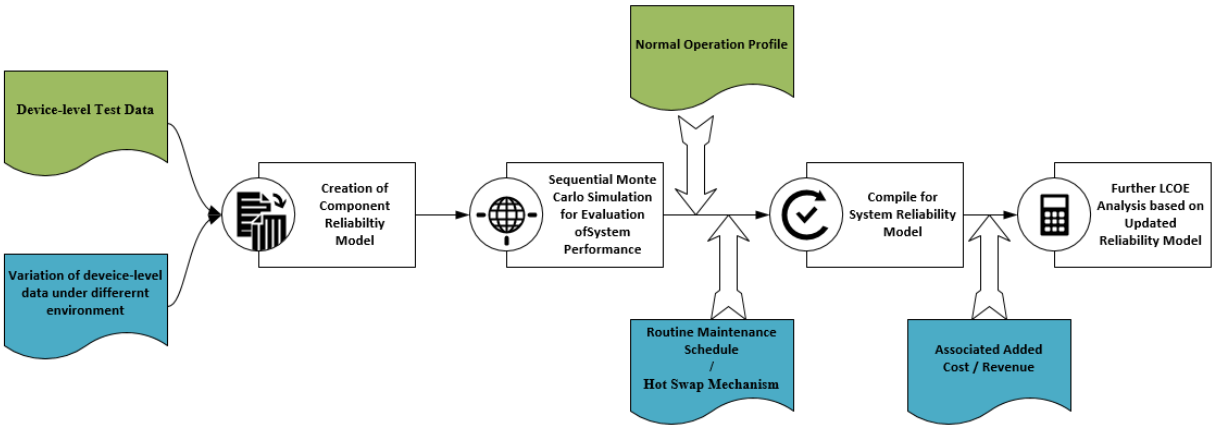


Fig. 8.2.15. System-level reliability evaluation using SMCS.

Based on the collection of reliability data at the device level, we move forward to the system-level evaluation using reliability block diagram and SMCS. The technical details of the reliability block diagram and SMCS have been illustrated in the previous quarterly report.

The regular per-phase maintenance plan is included in the simulation process. The details of the per-phase maintenance plan include the following aspects: (1) One redundant bypass module is integrated into each phase of the PV inverter in the updated PV system. (2) When one of the working modules fails in a certain phase, the bypass module in that phase is utilized to sustain the normal operation. (3) Regular maintenance with specified time intervals (every 20, 40, 60, and 80 years), to inspect the redundant bypass modules and replace them with new ones if any of them has been activated in the operation.

Considering the system-level performance of the PV inverter and the per-phase maintenance plan, the SMCS is repeated for 100,000 runs with the coefficient of variation (COV) below 0.2%. The histogram of the lifetime in 100,000 simulation runs is represented in Fig. 8.2.16 below for different time intervals between regular maintenance (i.e., every 20, 40, 60, and 80 years).

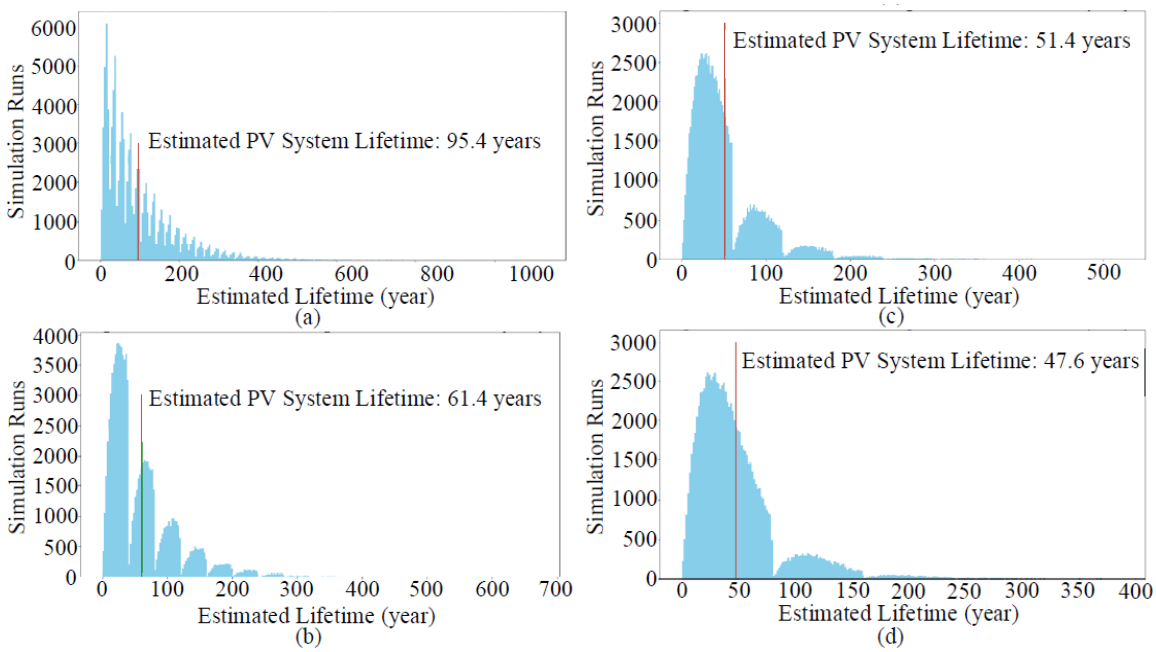


Fig. 8.2.16. (a) Regular maintenance every 20 years. (b) Regular maintenance every 40 years. (c) Regular maintenance every 60 years. (d) Regular maintenance every 80 years.

It is observed that the estimated lifetime of the updated inverter in the SMCS is reduced when the regular maintenance interval is extended from 20 years to 80 years. However, considering the redundant bypass module design, even with the longest regular maintenance interval, the inverter stage in the updated PV system has a 47.6-year estimated lifetime, which is much higher than the service life of the benchmark PV model (25 years).

LCOE evaluation with two models focused on the benefit of integrating M4 inverter

Based on the PV inverter service lifetime estimation, the LCOE calculation is performed using both the ‘application model’ and ‘revenue model’ (Technical details of both models have been illustrated in previous quarterly reports). The comparison is to highlight the differences between the updated PV system and the benchmark PV system. (Left figure using “application model”, and right one using “revenue model”)

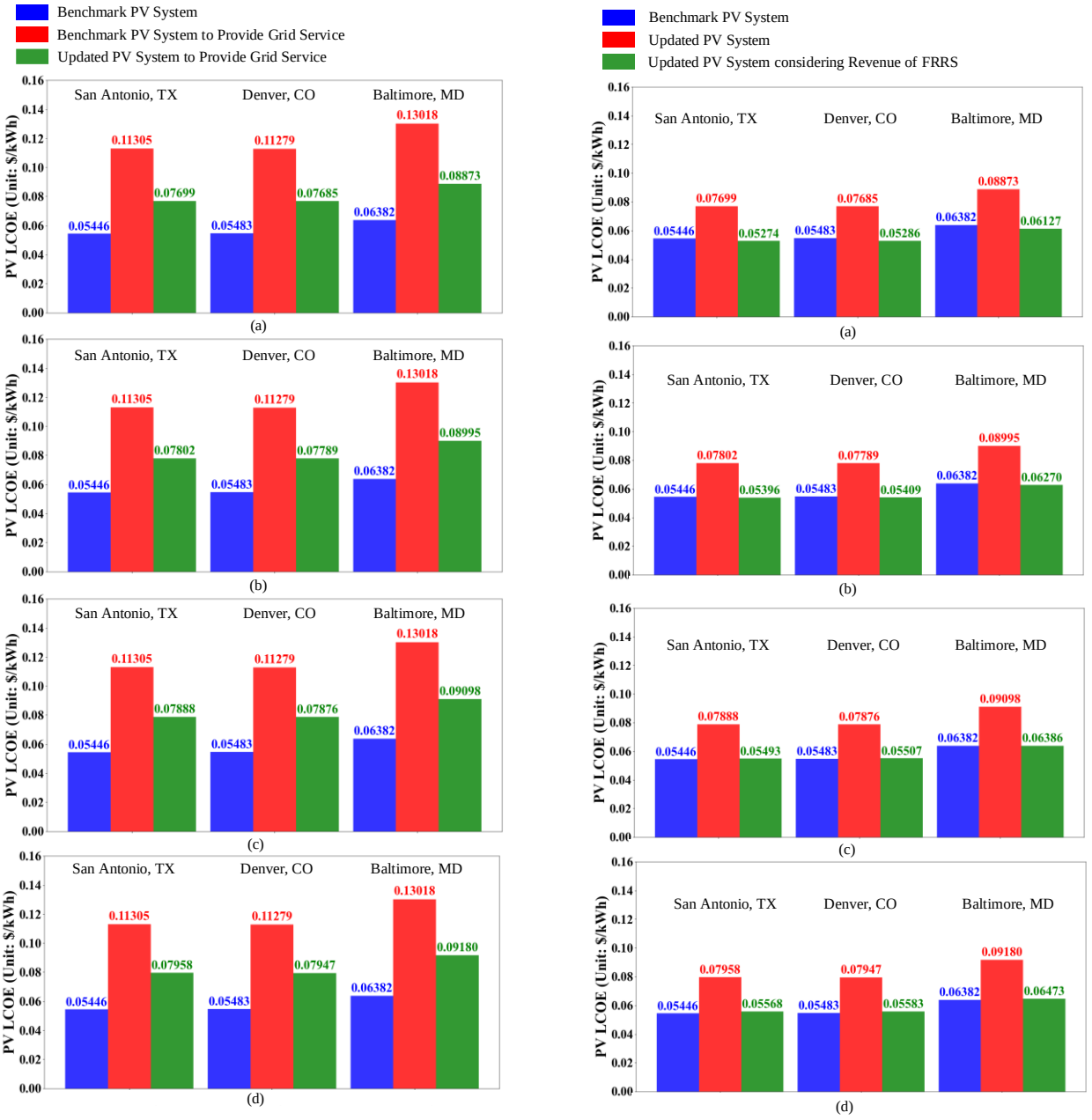


Fig 8.2.17. PV LCOE comparison. Left: application model, right: revenue model.
(a) Regular maintenance every 20 years. (b) Regular maintenance every 40 years. (c) Regular maintenance every 60 years. (d) Regular maintenance every 80 years.

The PV LCOE comparison in the 'application model' is presented in the left figure with regular maintenance every 20, 40, 60, and 80 years. Note that the blue bar represents the LCOE of benchmark PV system; the red bar represents the benchmark PV system with additional cost to achieve defined application (FRRS); the green bar represents the LCOE of the updated PV system with the updated PV inverter to achieve the defined application (FRRS). To show the geographical difference within the United States, three locations are selected in Texas, Colorado, and Maryland, USA, respectively. It is

observed that when achieving the same application (FRRS), the updated PV system (green bar) can reduce the LCOE by 29% to 32%, compared to the benchmark PV system (red bar), over all the three locations in the United States.

The PV LCOE comparison in the 'revenue model' is presented in the right figure with regular maintenance every 20, 40, 60, and 80 years. Note that the blue bar represents the LCOE of the benchmark PV system; the red bar represents the LCOE of the updated PV system to fulfill the defined application (FRRS); the green bar represents the LCOE of the updated PV system considering the revenue from the defined application (FRRS). It is observed that when considering the revenue from grid service, the updated PV system (green bar) can reduce the LCOE by 3% to -2%, compared to the benchmark PV system (red bar), over all the three locations in the United States. It is noteworthy that the LCOE of the updated PV system shows a reduction when regular maintenance is conducted every 20 or 40 years. The LCOE is almost the same with regular maintenance every 60 years. When the regular maintenance interval extends to every 80 years, the LCOE increased by 2%. This could be interpreted as the updated PV system is performing additional grid service at a comparable or even lower LCOE. In addition, the revenue from grid service is limited to data collected in the ERCOT FRRS program, grid service variation and locational difference would have a significant impact on the calculation of LCOE.

Preparations for the optimization based on the tradeoff between Reliability Evaluation and LCOE Calculation

We proposed the calculation below for the coordination of tradeoff between reliability evaluation and LCOE calculation.

$$\mathrm{LCOE}_{\mathrm{Update}} = \frac{\mathrm{Cost}_{\mathrm{PV\ module}} + \mathrm{Cost}_{\mathrm{BOS}} + \mathrm{Cost}_{\mathrm{OM}}}{\mathrm{Energy}_{\mathrm{life\_time}}} = \frac{P_{PV} * S_{PV} + C_{BOS-basic} + \sum_{t=1}^{t=T} \frac{\mathrm{C}_{\mathrm{OM}-b}}{(1+d)^t}}{\sum_{t=1}^{t=T} \frac{\mathrm{E}_{yr} * \eta * (1-de)^{t-1}}{(1+d)^t}}$$

Design with extremely high reliability would definitely extend the lifetime of PV system (represented by the green items), however, the increased O&M cost would also increase the LCOE to a potential unacceptable level (represented by red items). That's why it is critical to strike a balance point in the tradeoff between LCOE and reliability performance.

As shown in previous analysis, regular maintenance frequency play a critical role in the design of maintenance schedule to strike the balance between reliability and LCOE. Firstly, we evaluate the maintenance design from the reliability performance aspect, the main objective here is to maintain the PV system in operational states with longer lifetime compared with benchmark system. As shown in Table 8.2.6, longer interval between maintenance schedule would lead to reduction in the average lifetime of PV system, however, even the longest interval would yield lifetime of 47.6 years, which is drastically higher than the benchmark of 25 years. Secondly, we evaluate the maintenance design from the LCOE aspect, the main objective here is to reduce the LCOE of PV system to lower values that path the way for wide adoptions. As shown in Table 8.2.6, the result values are taken from the TX location for representation of the trend over the U.S., the LCOE reduction percentage is taken from APP model and the updated LCOE value is

taken from the REV model. It is observed that the short interval of maintenance would have better performance in the LCOE reduction in both percentage values and LCOE values.

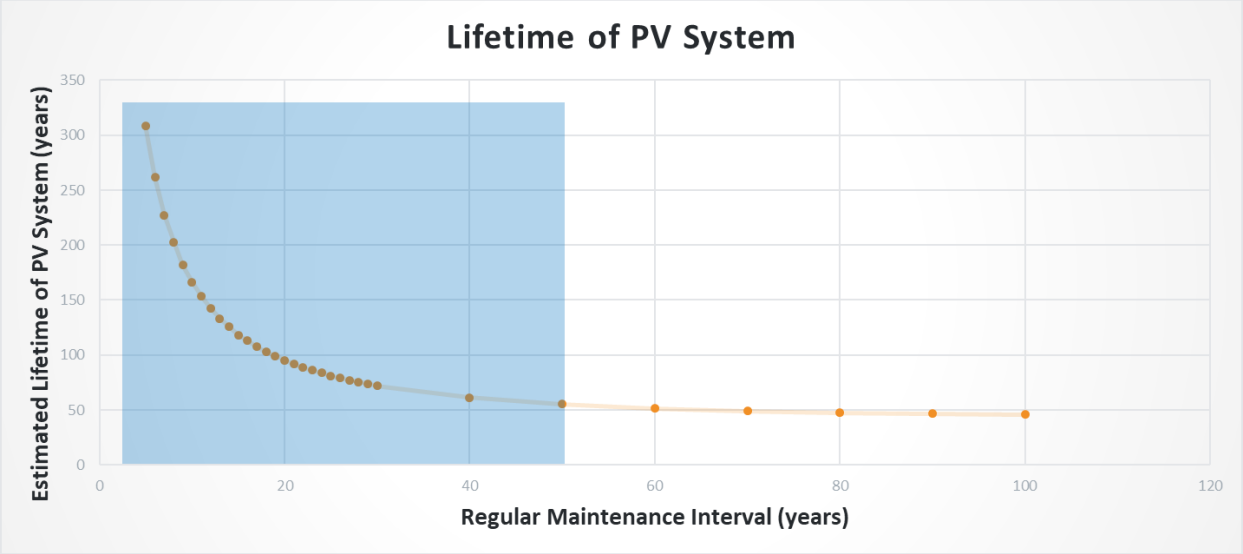
Table 8.2.6 Coordination of tradeoff between reliability performance and LCOE

		Design of intervals between regular maintenance schedules (years)			
		20	40	60	80
Reliability Performance	Lifetime (years)	95.4	61.4	51.4	47.6
LCOE	LCOE Reduction percentage from APP model	32%	31%	30%	29%
	Updated LOCE from REV model ($/kWh)	.05274	.05396	.05493	.05568

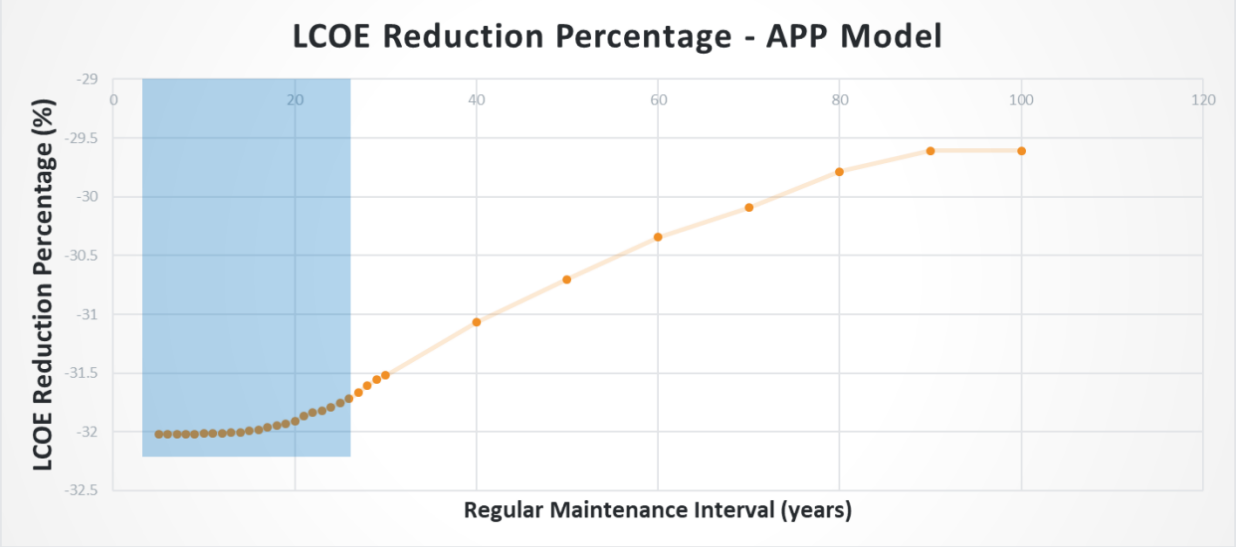
In summary, to coordinate the tradeoff between reliability performance and LCOE, we propose to implement regular maintenance schedules every 20 years (every 40 years as backup plan). With this design of maintenance schedules, we optimized the lifetime of PV system while reducing the LCOE of PV system. It should be noted that the result values in Table 8.2.6 is based on the modular design of M4 inverter and estimated cost of replacement modules. Compared with simulation environment, the less than perfect real-world implementation would introduce additional cost in the replacement of modules, which shift the balanced point from every 20 years to every 40 years, that's why we propose the 40 years maintenance schedules as the backup plan in implementations.

The project team conducted additional SMCS cases with higher resolution of regular maintenance schedules. The performance indicators include (1) reliability performance based on the parameter of lifetime of PV system; (2) LCOE reduction based on the parameter of LCOE comparison with benchmark PV system. The design of additional case studies include: (1) Using case studies within TX state, which is a good representation of implementation trend in U.S. (2) Variations of maintenance interval in regular maintenance plan (case setup include: (i) discount rate at 5%; (ii) one bypass module in each phase; (iii) added bypass module purchased at the first regular maintenance interval). (3) increase of simulation resolution from previous 20/40/60/80 years to (i) 5 to 30 years at the step of 1 year, and (ii) 30 to 100 years at the step of 10 years.

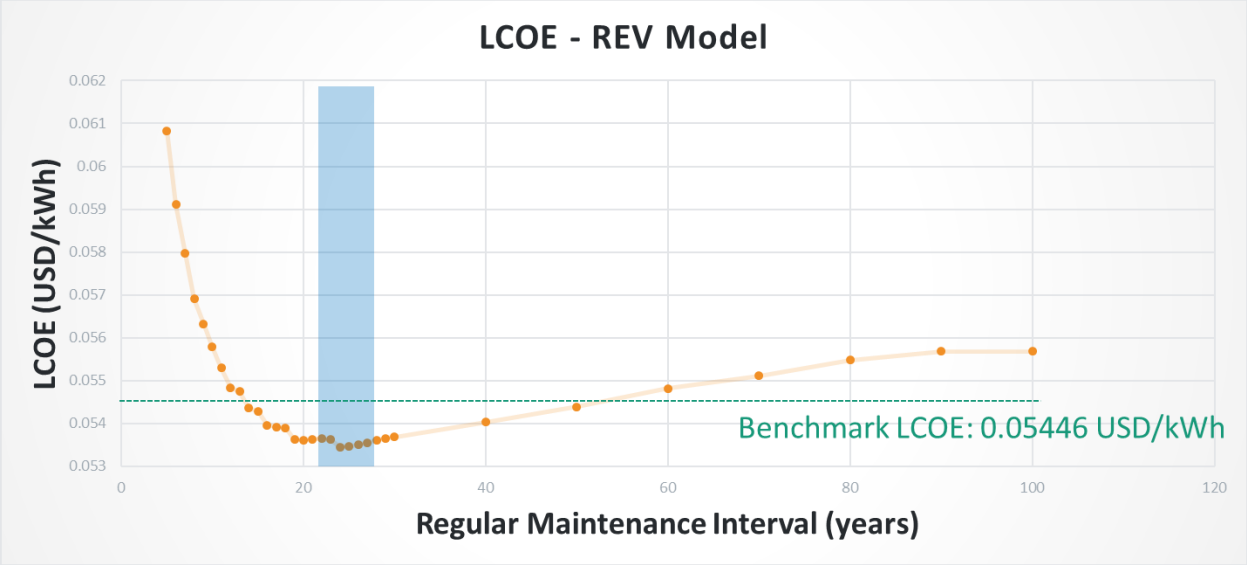
Start with the first set of performance indicator – reliability performance. Figure below demonstrates the relationship between lifetime of PV system and regular maintenance intervals. It is observed that even the worst lifetime (~50 years) is better than benchmark (~25 years), and considering the diminish of returns, we suggest to keep interval of regular maintenance < 50 years



The 2nd set of performance indicator – LCOE reduction include case studies on both APP model and REV model. Figure below demonstrates the relationship between the corresponding parameters and regular maintenance intervals.



It is observed in APP model that even the worst lifetime (29%) is better than milestone requirement (20%), we suggest to keep interval of regular maintenance < 25 years considering the diminish of returns.



It is observed in REV model that there is a turning point around 25 years for the optimization of maintenance schedule.

In summary, based on the two sets of performance indicators, we suggest designing interval of regular maintenance around 25 years, targeting the optimum point between reliability improvement and LCOE reductions. The benefit of M4 inverter is demonstrated in the additional cases that: PV system with M4 inverter is performing additional grid service at comparable or even lower LCOE.

8.3 Advancement of Controller Hardware-in-loop (CHIL) Simulation

M4 real-time model development and verification

For the controller hardware-in-the-loop (CHIL) testing, a high-fidelity, fixed-time step, real-time model of the M4 inverter is needed. Due to the high switching frequency of DAB and a larger number of switches in M4 inverter, a new co-simulation method was used to develop the real-time model of M4 inverter. In this model, the DABs in nine modules of M4 inverter including two H-bridges and high-frequency transformer were modeled by using Time-Stamped Bridge (TSB) (also called switching function). The rest of the circuit in M4 inverter and equivalent DAB circuit was modeled by using OPAL-RT eHSx128 solver. The diagram of TSB based M4 inverter model is shown in Fig. 8.3.1. The voltage of both sides of DAB was measured in eHS solver and sent to TSB model as the inputs. The calculated currents from TSB model were sent back to the DAB equivalent circuit in eHS solver.

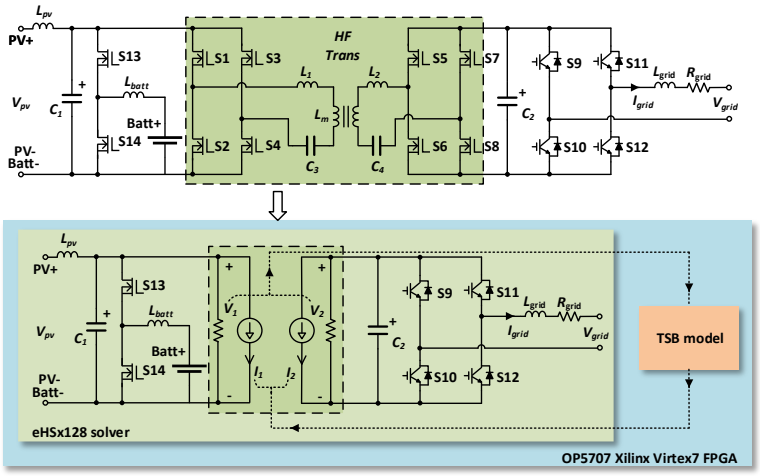


Fig. 8.3.1. Circuit of M4 inverter modeled by the TSB model and eHS solver

Based on this real-time model, the M4 inverter CHIL platform was developed. In this platform, the M4 inverter was simulated in the OP5707 real-time simulator. The customized bitstream which has five switching function cores working with one eHSx128 core was used to simulate the nine modules of the M4 inverter in real-time. The digital input cards were assigned to receive the gating signal from the controller, and analog output cards were assigned to send the grid voltage and current to the controller. Before testing this CHIL platform with the actual embedded controller, a close-loop current controller as shown in Fig. 8.3.2, was used to test the CHIL platform. The controller was run in the OP4510 real-time simulator to control the output current of DABs in the M4 inverter. In the controller, the RT-XSG based PWM generator was developed in the FPGA to generate the gating signals. The inputs of PWM generator were received from the current controller located in the OP4510's CPU model. Additionally, the digital output card and analog input card were assigned to send the gating signals and receive grid voltage and current, respectively. The whole system is shown in Fig. 8.3.3.

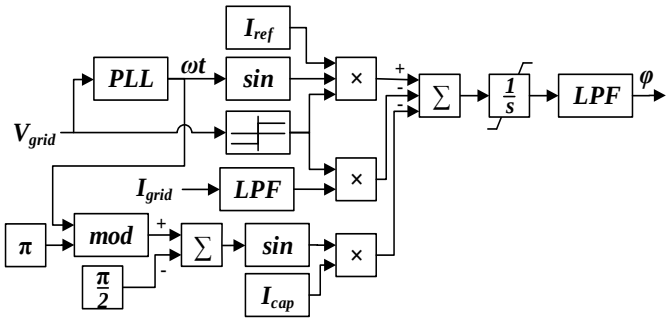


Fig. 8.3.2. Structure of closed-loop controller in M4 inverter CHIL test

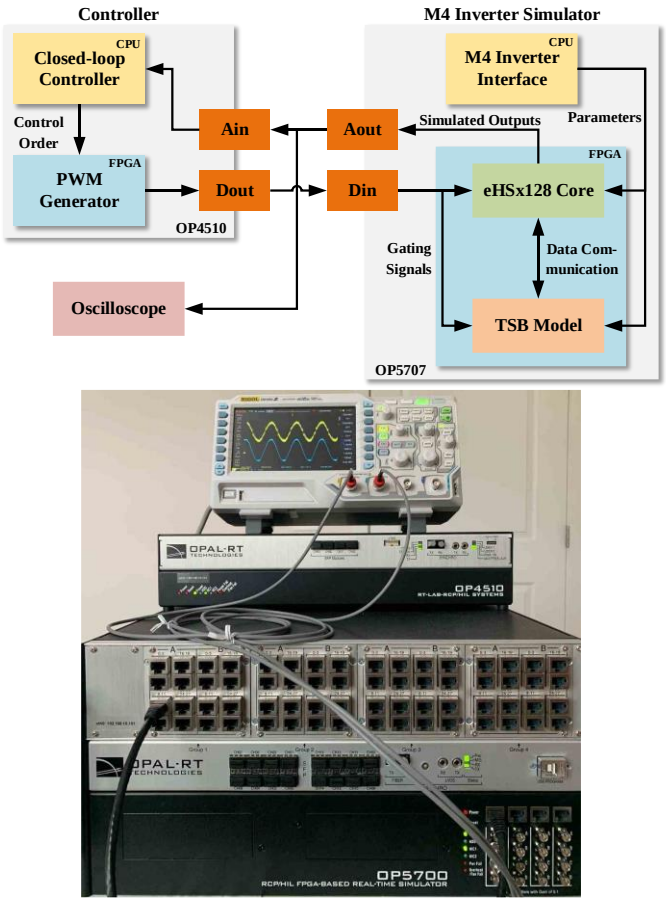


Fig. 8.3.3. Diagram of the M4 inverter real-time CHIL system setup

The closed-loop CHIL test was conducted by using the closed-loop current controller running with 30 µs simulation time step in the OP4510 CPU model. In the OP5707, the CPU model was running with 20 µs simulation time steps, the eHSx128 core and TSB model in the FPGA firmware of OP5707 were running in 1 µs and 470 ns, respectively. Due to the I/O limitation, two different grid connections of three modules of the M4 inverter were tested.

In the first case, three modules of the M4 inverter were connected in parallel with DC bus and in series with single-phase AC grid. One closed-loop controller was implemented to control three modules of the M4 inverter with sending independent gating signals to each module. The grid current results, shown in Fig. 8.3.4, indicate that the peak value of grid current can track the setpoint of reference peak value of 100 A. Comparing with the closed-loop offline simulation, the CHIL simulation provided comparable results. The maximum RMS error of three cycles of grid current signal between two results calculated by using the formula shown below was 3.66%. In this formula, $RMS(I_x)$ represents the point-by-point RMS value calculated for the current I_x over the specified number of cycles.

$$RMS\ error = \frac{\left|RMS(I_{real-time}) - RMS(I_{offline})\right|}{RMS(I_{offline})}$$

In the second case, three modules of the M4 inverter were connected to a three-phase grid in a Wye connection. Three closed-loop controllers were placed to control the output currents of the three modules of the M4 inverter. During the real-time simulation, the CHIL platform worked properly and provided stable three-phase grid current results which are shown in Fig. 8.3.5. By using the equation shown previously, the maximum RMS error in three cycles of results was 3.38% when comparing the CHIL three-phase grid current results with offline simulation results. The comparison between the CHIL results and offline simulation shows that the developed CHIL test platform can provide high-fidelity simulation results and the platform is ready to be tested with the actual embedded controller.

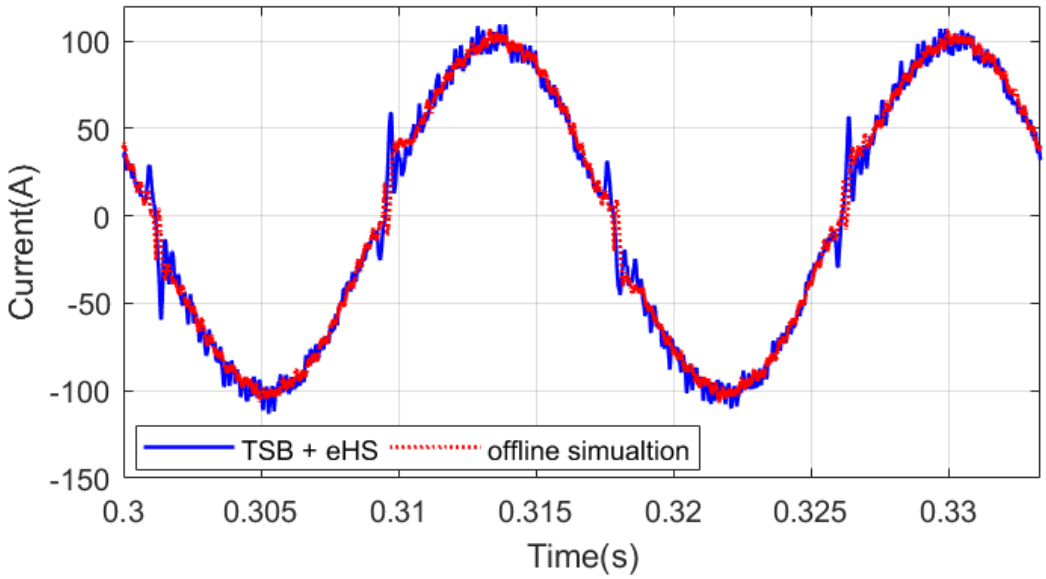


Fig. 8.3.4. Comparison of single-phase grid current between offline simulation and CHIL real-time simulation

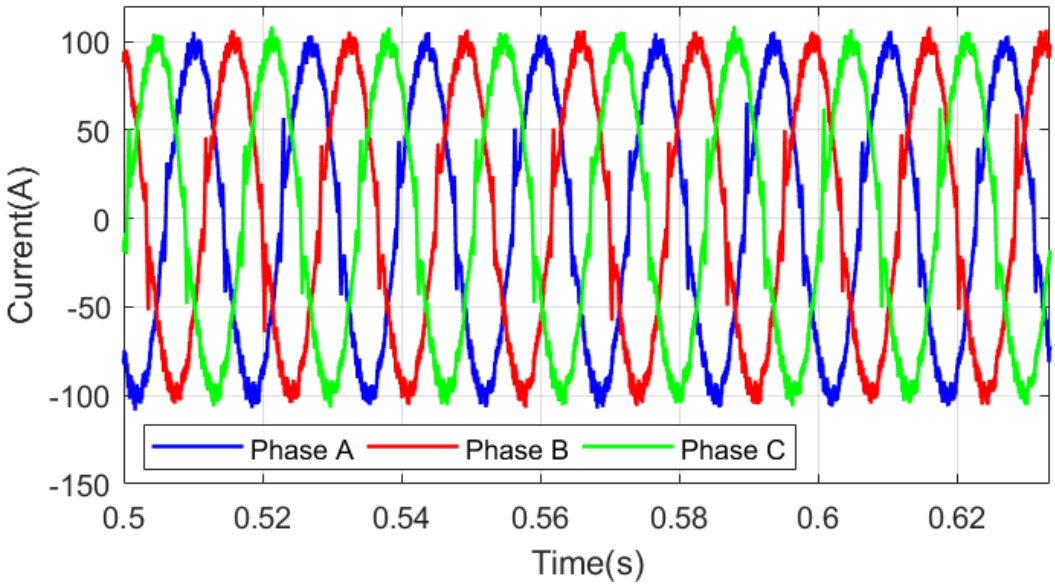


Fig. 8.3.5. Three-phase grid currents in CHIL real-time simulation

Controller Development

The M4 system requires a large number of input and output channels for control. The commercially available ZYNQ-7000 SoC TE0782 board can support the number of digital I/Os, analog measurement channels and communication channels needed for a 1 MVA M4 system. The TE0782 is equipped with a ARM Cortex-A9 processor and an FPGA. Independent programming of the FPGA and ARM core processor allow for a streamlined software development for the control of the M4. The FPGA implements the low-level IP core associated with PWM generation and reading sensors & fault signals. The ARM core implements the higher level control software which operates the M4 and the software to interface with the user interface.

A docking-board was designed for the TE0782, which implements 284 digital IO/s (optical terminals) and three 8-channel Analog measurement ports. Of the 284 digital IO/s, over 120 are PWM outputs. The remainder of the digital IOs are used for digital measurements and fault monitoring. Two of the analog ports are used for voltage and current measurements.

Figure 8.3.6 shows the final controller board along with the voltage sensor board which interfaces with the analog ports.

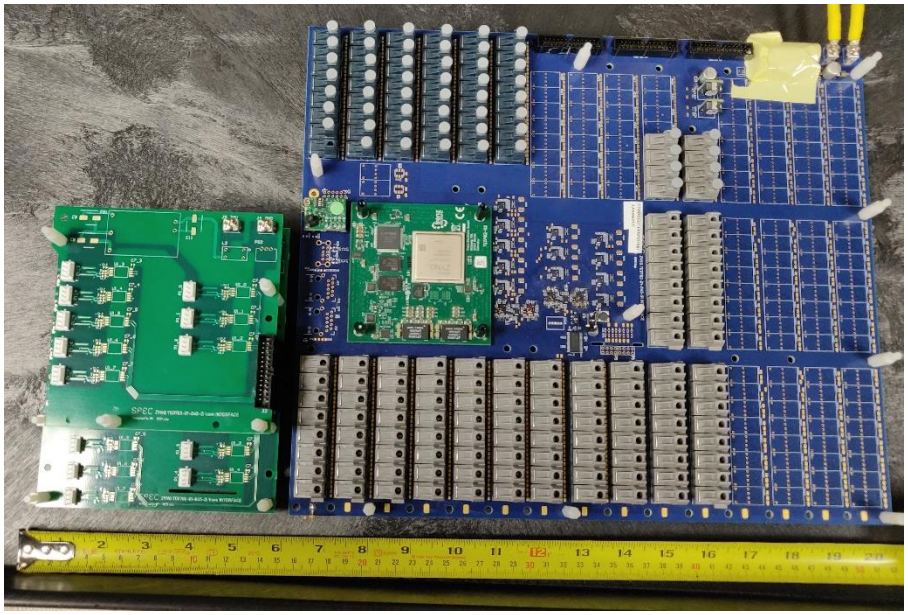
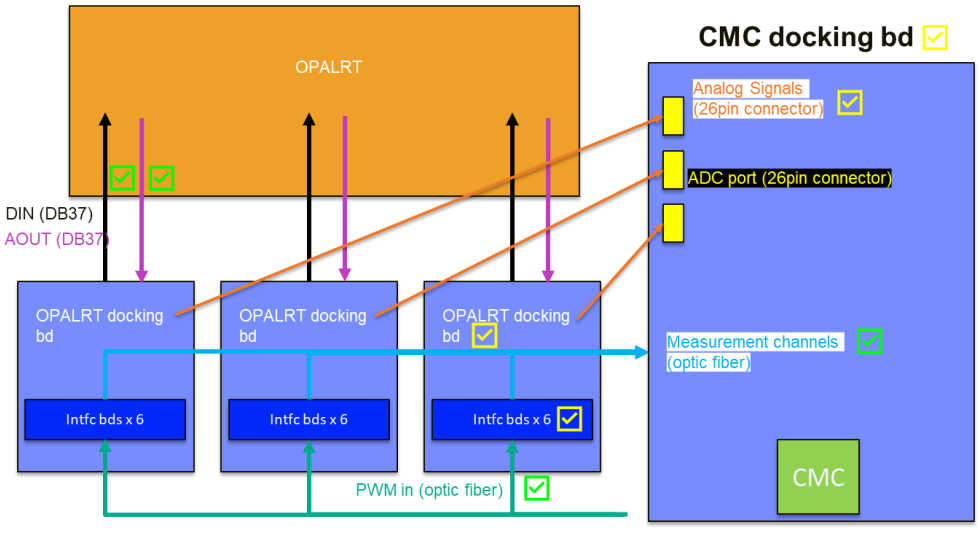


Fig. 8.3.6. Control Cabinet sizing and controller + sensor board positioning

Test Validation of Control Software

A test setup was developed for the controller and real-time model. The general diagram is shown in figure 8.3.7. The docking board developed in the previous section connects to the OPAL-RT system through a series of interface boards. The OPAL-RT system receives the PWM signals from the controller as input, while the analog ports of the controller receive the voltage and current signals from the OPAL-RT system.



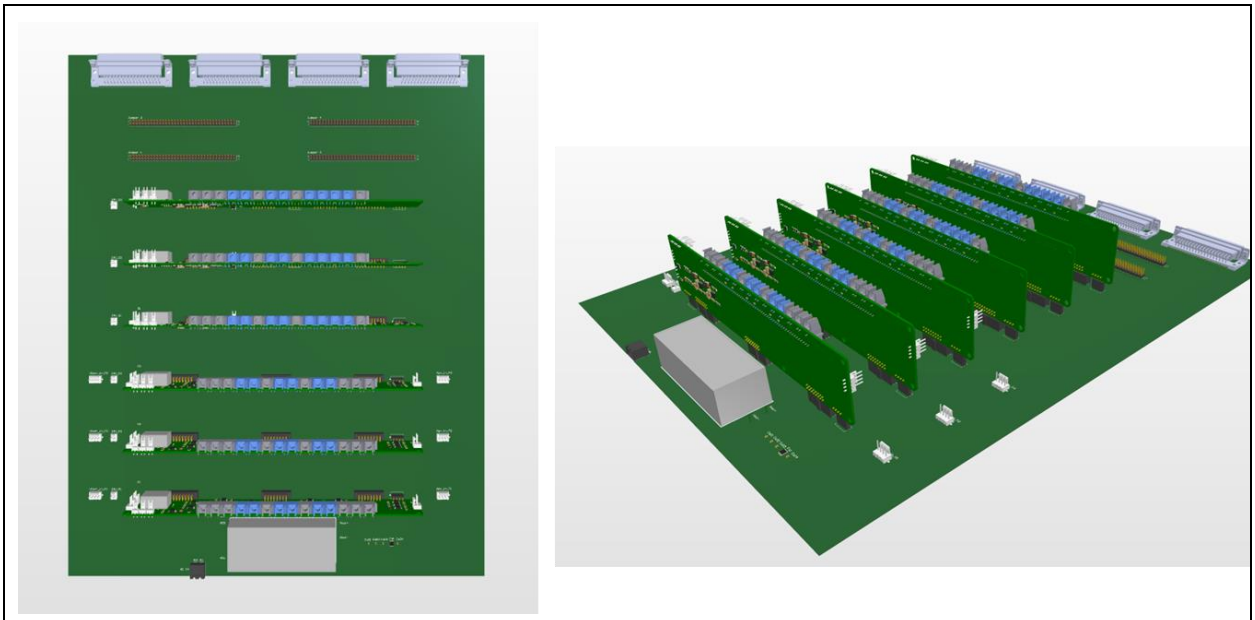


Fig. 8.3.7. (Top) Diagram for controller setup for OPAL-RT testing, (Bottom) Interface boards between OPAL-RT and controller

The setup in shown in figure 8.3.8. With this setup, the system operation was tested. This includes the initialization sequence, grid-synchronization, and power transfer. Further, testing the UI software and observing the effect of control commands was crucial to final hardware testing.

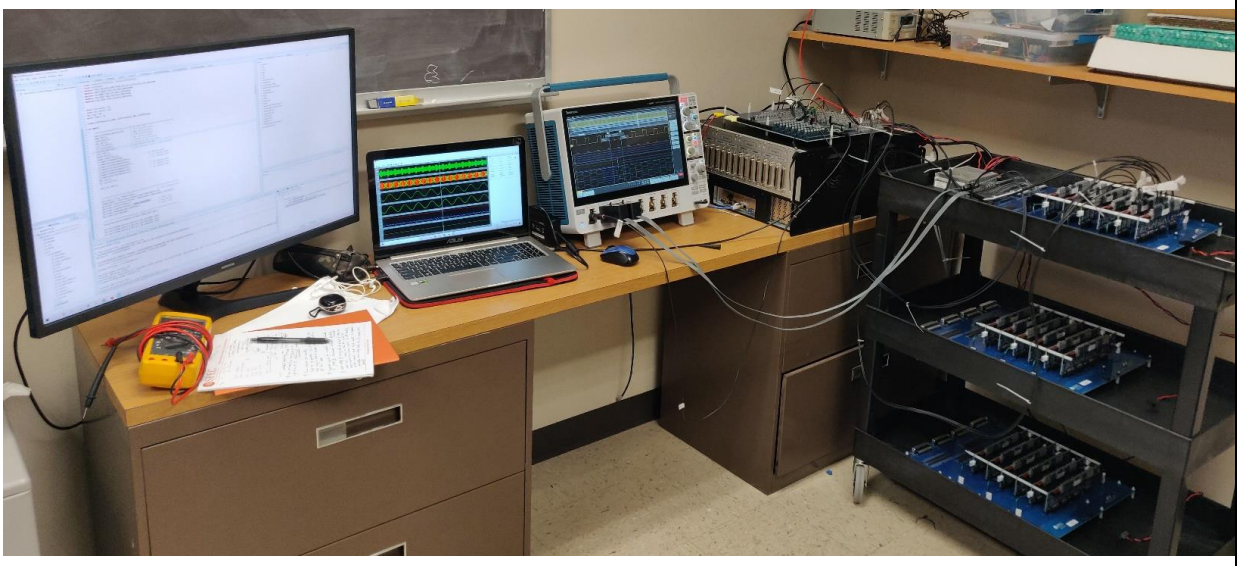


Fig. 8.3.8. Real-time simulation testing setup with Controller Hardware in-the-Loop (CHIL)

CHIL test results are shown in figure 8.3.9. The oscilloscope waveforms are obtained from the output signals of the OPAL-RT system. Waveforms show stable grid-tied operation.

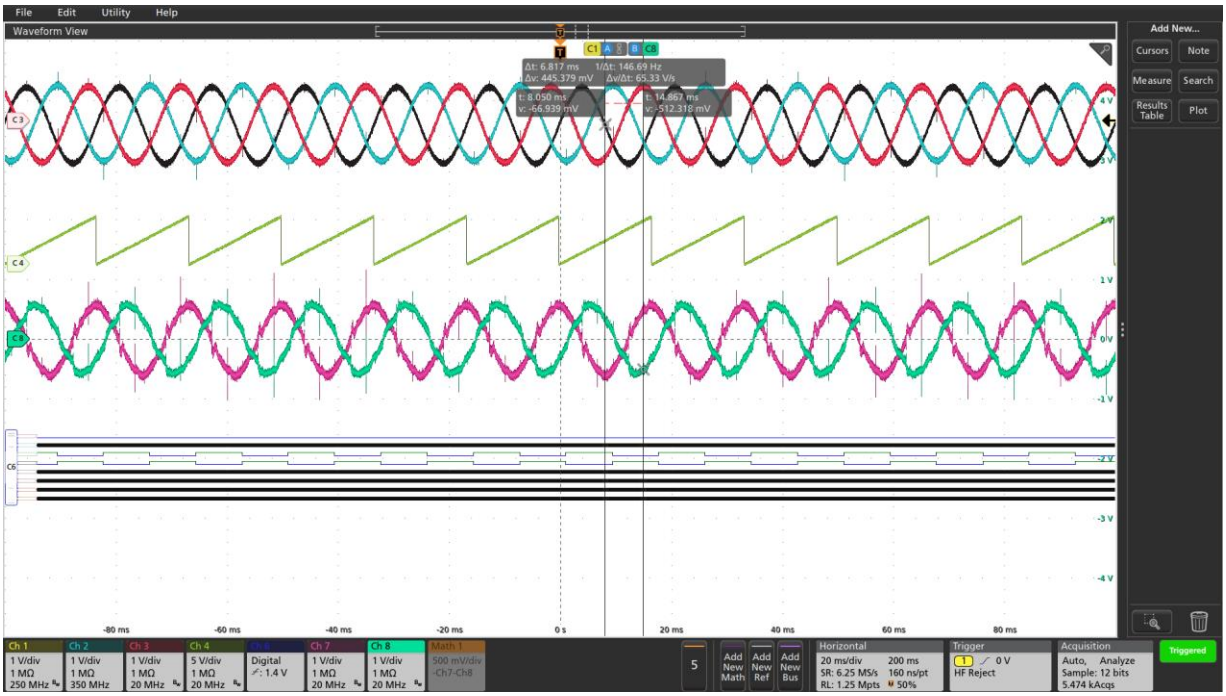


Fig. 8.3.9. CHIL test results:(top-to-bottom) 3ph grid voltage, Phase-locked loop (PLL), Grid current (Ia, Ib)

8.4 High power medium voltage test results

1 MVA M4 Inverter system integration

Project team has successfully developed nine (9) converter modules based on the 1700V SiC technology. Each modular converter has been successfully tested in DC/DC mode up to 200 kW. These modules are then shipped to Toshiba facility for system integration into a customized housing cabinet. Fig.8.4.1 shows the completed M4 Inverter system. The internal view of the converter is shown in the right-hand side picture.

Fig.8.4.1 1 MVA M4 Inverter system. Right hand side picture shows the modular converters.

Grid-tie testing circuit and test setup

The M4 system was set up for grid-tied power testing using a configuration shown in Figure 8.4.2. A 24-pulse rectifier was connected to the M4 DC (PV) and AC ports, and the AC port was tied to the three-phase grid through a transformer.

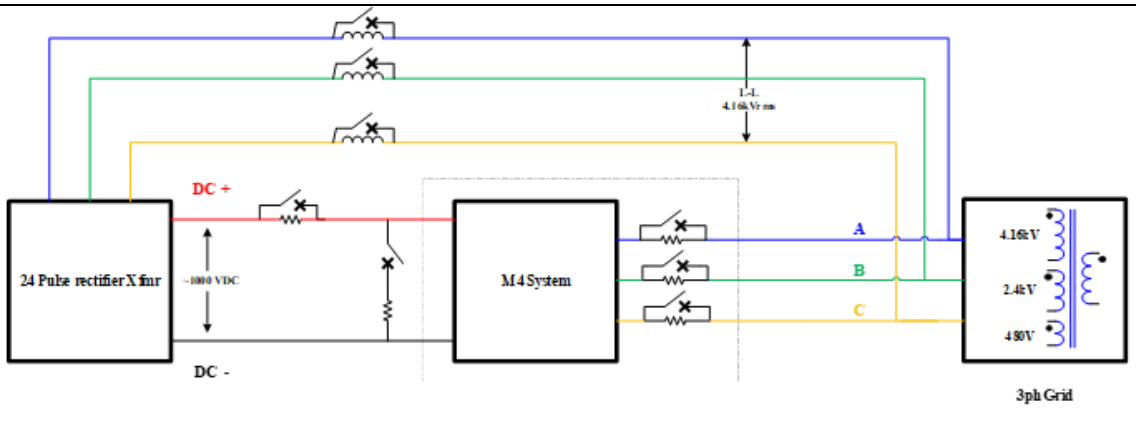


Fig. 8.4.2. Circulating-power test setup at TIC with M4 and 24-pulse rectifier

The setup shows the M4 system and the 24-pulse rectifier with breakers and pre-charge equipment. When the M4 is set up in this configuration and operated to transfer power from the DC port to the AC port, most of the power is recycled back through the 24-pulse rectifier. The power drawn from the grid is only the power required to maintain the continuous operation of the system at the voltage level i.e., the power losses in the 24-pulse rectifier and the M4 system itself. This mode of testing has the advantage of running high voltage testing safely while avoiding large power exchange with the grid. Further, the presence of the 3-ph grid transformer with different tap settings allows scaling up the voltage with taps at 480V, 2.4kV, 4.16kV.

Control Software and Operation Sequence

A critical part of high-voltage testing to verify M4 operation is the development of a user interface for reliable control of the system. To safeguard the computer system and user from any possibility of exposure to high voltage, it is necessary to have this user interface communicate over an isolated optical connection. An external emergency stop signal is also required to intervene and shut off the M4 system in the event of any maloperation. The communication and e-stop boards are shown below in figure 8.4.3.

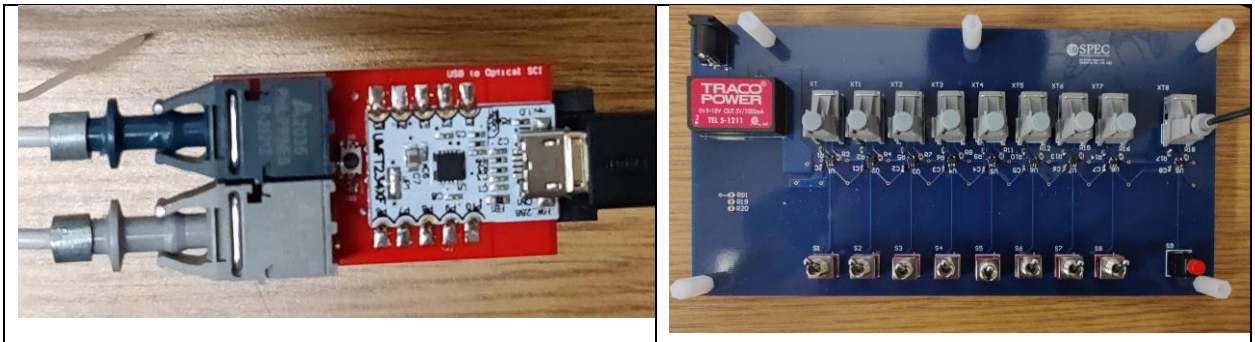


Fig. 8.4.3. External communication hardware: optical communication board (left), emergency-stop control board (right)

Project team has developed a human machine interface for M4 testing at high power levels. Figure 8.4.4 shows the control interface or “QT interface”. The order of operations for grid-tie testing is as follows:

1. Establish connection of the QT software through the optical interface.
2. Turn on the 3-ph AC voltage through the transformer.
3. Close contactors and bypass precharge equipment so that the M4 is energized on the DC and AC side.
4. Synchronize with the grid by enabling the Phase-Locked Loop (PLL).
5. Begin IGBT switching at 60Hz in synchronicity with the grid.
6. Set a current command and begin operation for either few cycles at a time or continuous mode operation.

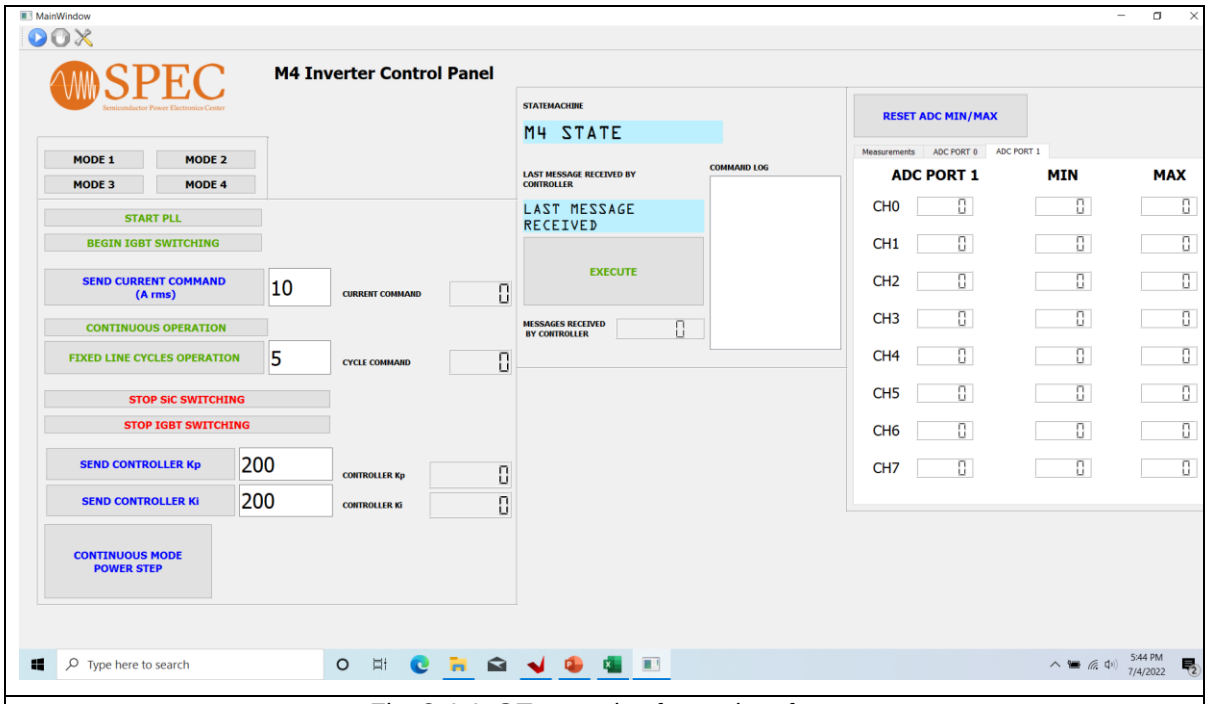


Fig. 8.4.4. QT control software interface

Significant Test Results

Grid-tied tests were performed at various power levels with the M4 system in the circulating power configuration. Waveforms and Efficiency results are presented here.

Test Waveforms

The waveforms in figure 8.4.5 show the test results of M4 at an AC line-line voltage of 2.4kVrms and line-current of 60Arms. At this condition the input current of the rectifier was at its rated limit.

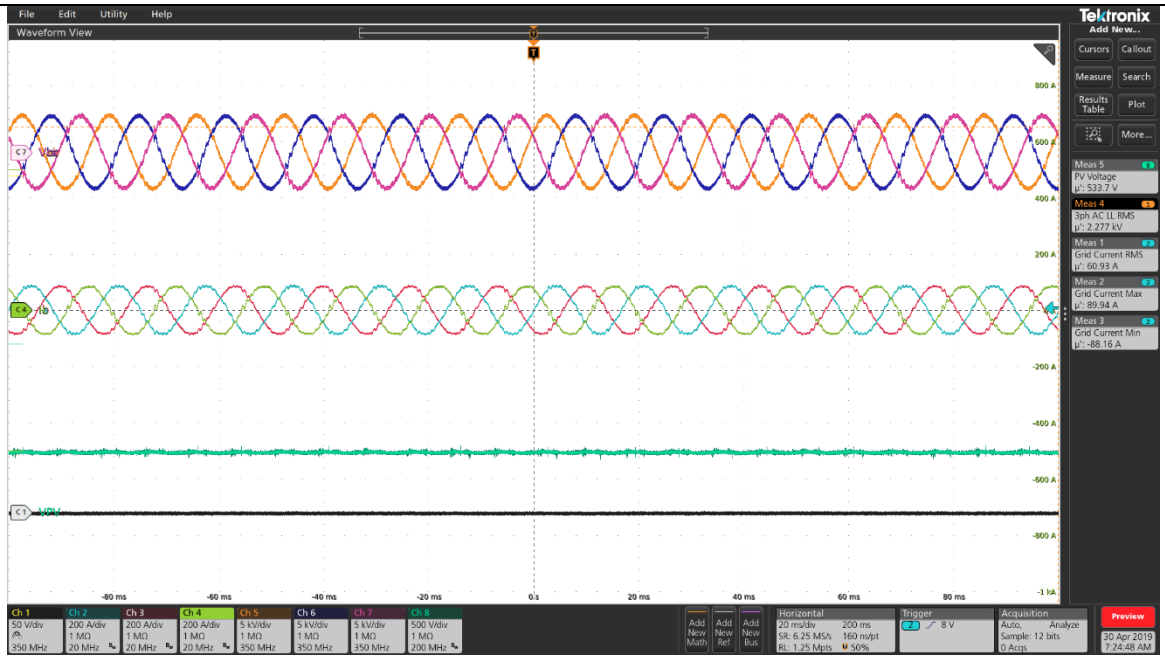


Fig. 8.4.5. M4 grid-tied operation waveforms: (top to bottom) 3ph voltage (2.4kVrms), 3ph current (60Arms), DC voltage (533V)

Efficiency Measurements

Efficiency measurements were recorded for the M4 using a 3ph power analyzer. Figure 8.4.6 below shows the efficiency curve. While the measurement voltage is lower than the rated 4160V, the efficiency is much higher than 97% target.

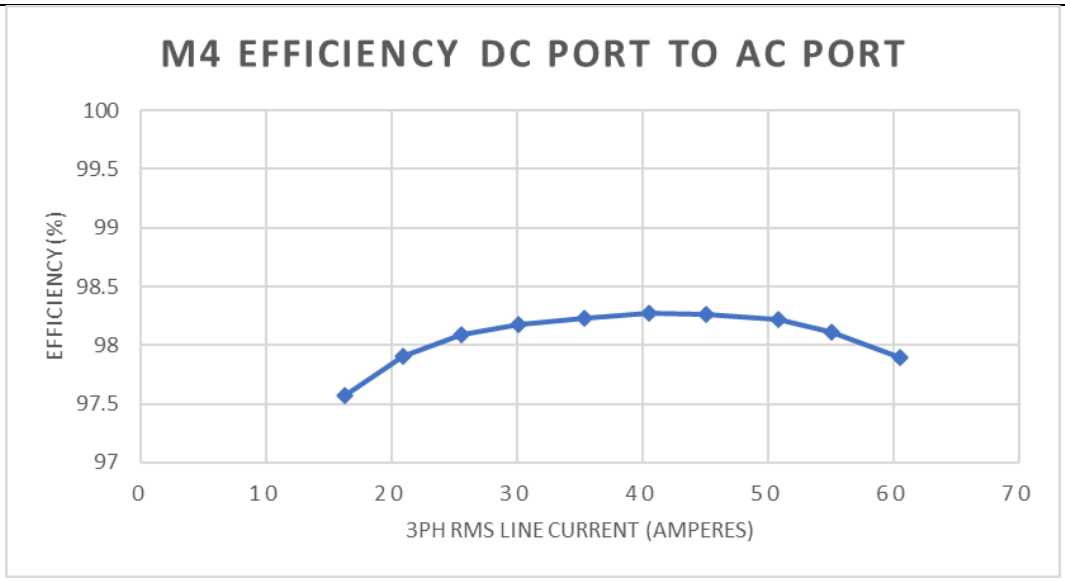


Fig. 8.4.6. M4 grid-tied operation efficiency (DC/AC), Vac=2400V

Dynamic Performance

The waveforms in figure 8.4.7 show the M4 during a load jump for 10 line-cycles at an AC line-line voltage of 2.4kVrmrs. The line-current is 40Arms for 10 cycles and jumps to this value in less than an eighth of a cycle (~2ms). M4 can provide a fast DC/AC step jump in power as required by applications such as Fast Frequency Response (FFR).

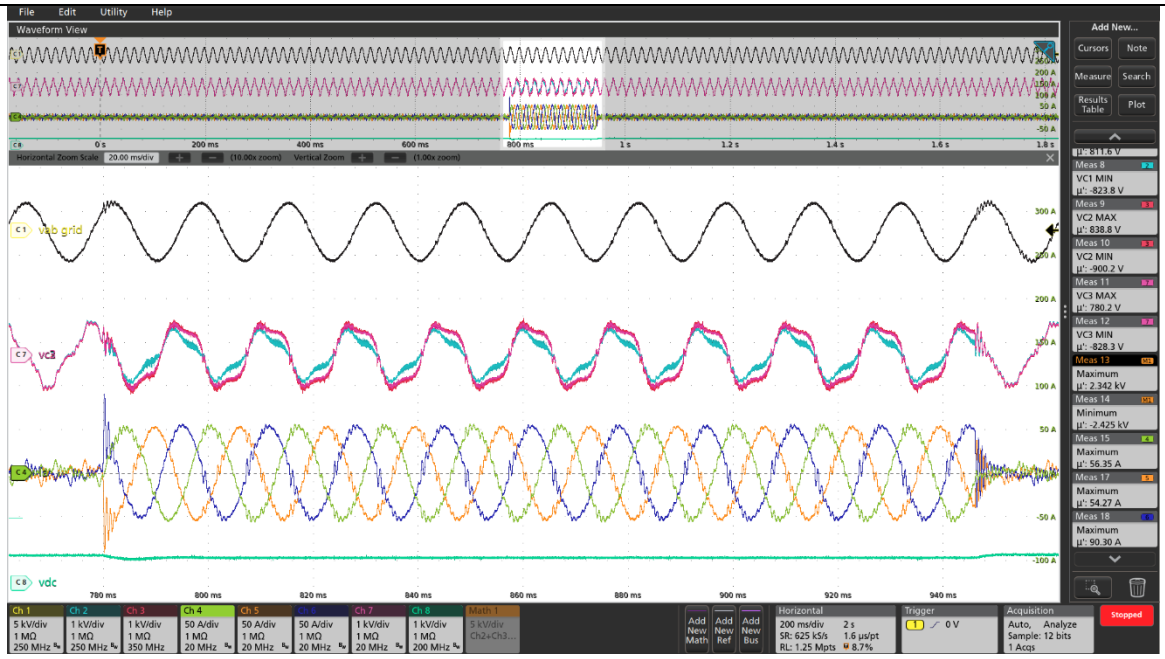


Fig. 8.4.7. M4 dynamic performance waveforms during 40Arms load jump: (top-to-bottom) Vab (2.4kvrms), Phase-C module voltages, Line currents (40Arms), DC voltage (550V)

The waveforms also show the dynamic voltage sharing between modules during operation. In this case the voltages measured are that of Vc1, Vc2, Vc3 i.e., the three modules of phase C. As seen from the waveforms, the voltages across the modules are well-balanced even without module level balancing control.

9. Significant Accomplishments and Conclusions:.

This project enabled the multidisciplinary team to work together in the last three years with the following major accomplishments

1) A 1 MVA medium voltage SiC PV + storage system has been developed and demonstrated. The technology TRL level is close to 5. This is the world's highest power level medium voltage SiC converter with very high efficiency and substantially improved power density compared to silicon IGBT based converters. This work therefore helps the SiC power electronic industry moving closer to introduce medium voltage solutions in renewable energy applications.

The same technology can also be used in electric vehicle fast charging and standalone energy storage applications.

2) The digital control system of the M4 inverter was developed and it has demonstrated numerous functions including MPPT, battery charging and discharge, reactive power compensation and fast frequency response. Excellent voltage balancing is also achieved in the M4 inverter, paving the way for even higher voltage configurations.
3) The 111 kVA DC/AC SiC converter module is one of the most advanced in terms of power efficiency. Its design helps industry of adopting 1700V SiC devices for 1500V
4) Advanced medium frequency transformer design significantly advances the state of the art and the developed transformer is capable of 300 kVA efficient power transfer.
5) Novel LCOE analysis methodology was developed and used to demonstrate the advantage of the DC coupled PV + storage system in lowering the LCOE by more than 30% when compared with benchmark PV system and by 23% when compared with benchmark AC coupled PV + storage system.
6) M4 Inverter reliability is substantially higher than convention system if redundancy cells and active maintenance approaches are adopted.
7) The team has developed an improved real time converter model that could be used to model large complexed SiC converters in real time. This is a major contribution to the real time simulation community.

10. Path Forward:

Moving forward, pilot demonstration in a real PV farm will be useful to further validate the technology and its control. Employ grid forming control functions in the M4 is also a necessary next step.

Recently, the project team has obtained a new SETO project to develop a lower cost commercialization ready M4 inverter. This will bring additional advancements in the medium voltage power electronics technology with commercial impact.

11. Products:

The following publications are produced under this project.

[1] Wei Xu, Z. Guo, A. Vetrivelan, R. Yu and A. Q. Huang, "Hardware Design of a 13.8-kV/3-MVA PV Plus Storage Solid-State Transformer (PVS-SST)," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 4, pp. 3571-3586, Aug. 2022, doi: 10.1109/JESTPE.2021.3082033.

[2] Zhicheng Guo, R. Yu, W. Xu, X. Feng and A. Q. Huang, "Design and Optimization of a 200-kW Medium-Frequency Transformer for Medium-Voltage SiC PV Inverters," in IEEE Transactions on Power Electronics, vol. 36, no. 9, pp. 10548-10560, Sept. 2021, doi: 10.1109/TPEL.2021.3059879.

[3] Wei Xu et al., "Hardware Design and Demonstration of a 100kW, 99% Efficiency Dual Active Half Bridge Converter Based on 1700V SiC Power MOSFET," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 1367-1373, doi: 10.1109/APEC39645.2020.9124401.

[4] S. Milad Tayebi, Wei Xu, H. Wang, R. Yu, Z. Guo and A. Q. Huang, "A Single-Stage Isolated Resonant SiC DC/AC Inverter for Efficient High-Power Applications," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 399-404, doi: 10.1109/APEC39645.2020.9124343.

[5] Haoming Wang et al., "Thermal Design Consideration of Medium Voltage High Frequency Transformers," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 2721-2726, doi: 10.1109/APEC39645.2020.9124264.

[6] Wei Xu, R. y. Yu, Z. Guo and A. Q. Huang, "Design of 1500V/200kW 99.6% Efficiency Dual Active Bridge Converters Based on 1700V SiC Power MOSFET Module," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 6000-6007, doi: 10.1109/ECCE44975.2020.9235903.

[7] Wei Xu, A. Vetrivelan, Z. Guo, R. Yu and A. Q. Huang, "Efficiency Optimization of Dual Active Bridge Converter Based on dV/dt Snubber Capacitors," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 2021, pp. 647-653, doi: 10.1109/APEC42165.2021.9487159.

[8] Adithyan Vetrivelan, Wei Xu, R. Yu and A. Q. Huang, "Triple Phase-Shift Optimization of SiC-based Dual-Active Bridge DC/AC Converter," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), 2022, pp. 70-77, doi: 10.1109/APEC43599.2022.9773574.

[9] S. Zhao, Y. Men, X. Lu, D. Zhao and A. Huang, "Photovoltaic (PV) System Levelized Cost of Energy (LCOE) Evaluation with Grid Support Function Valuation and Service Lifetime Estimation," IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society, 2021, pp. 1-6, doi: 10.1109/IECON48115.2021.9589478.

[10] Z. Dong et al., "Real-time Implementation of a Dual-Active-Bridge Based Multi-Level Photovoltaic Converter," 2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2021, pp. 1-6, doi: 10.1109/PEDG51384.2021.9494236.

12. Project Team and Roles

The project team members are listed below.

Team Member	Major Role
University of Texas at Austin	Project management, development of the hardware and software of the M4 Inverter
Toshiba International	Battery energy storage system development, M4 Inverter mechanical system and system integration, high power system testing
Argonne National Lab	Develop LCOE and reliability analysis platform, conduct LCOE and reliability assessment of the M4 Inverter
Temple University	

Opal-RT	Developed improved simulation model of SiC converter and support the CHIL validation of the M4 Inverter.
ERCOT	Advisory role on frequency regulation functionality