

Integrating Si/SiGe quantum devices with on-chip classical circuitry



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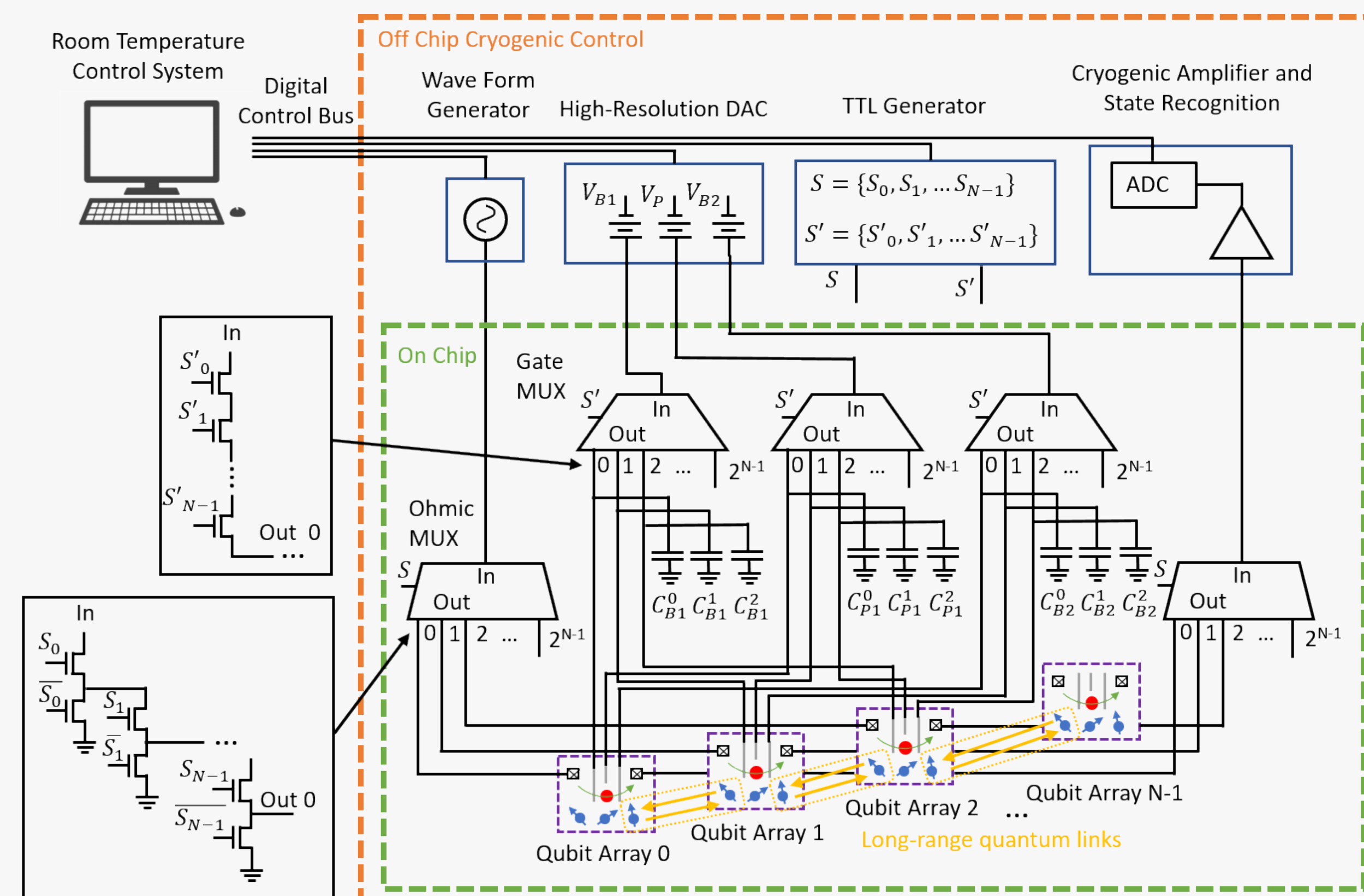
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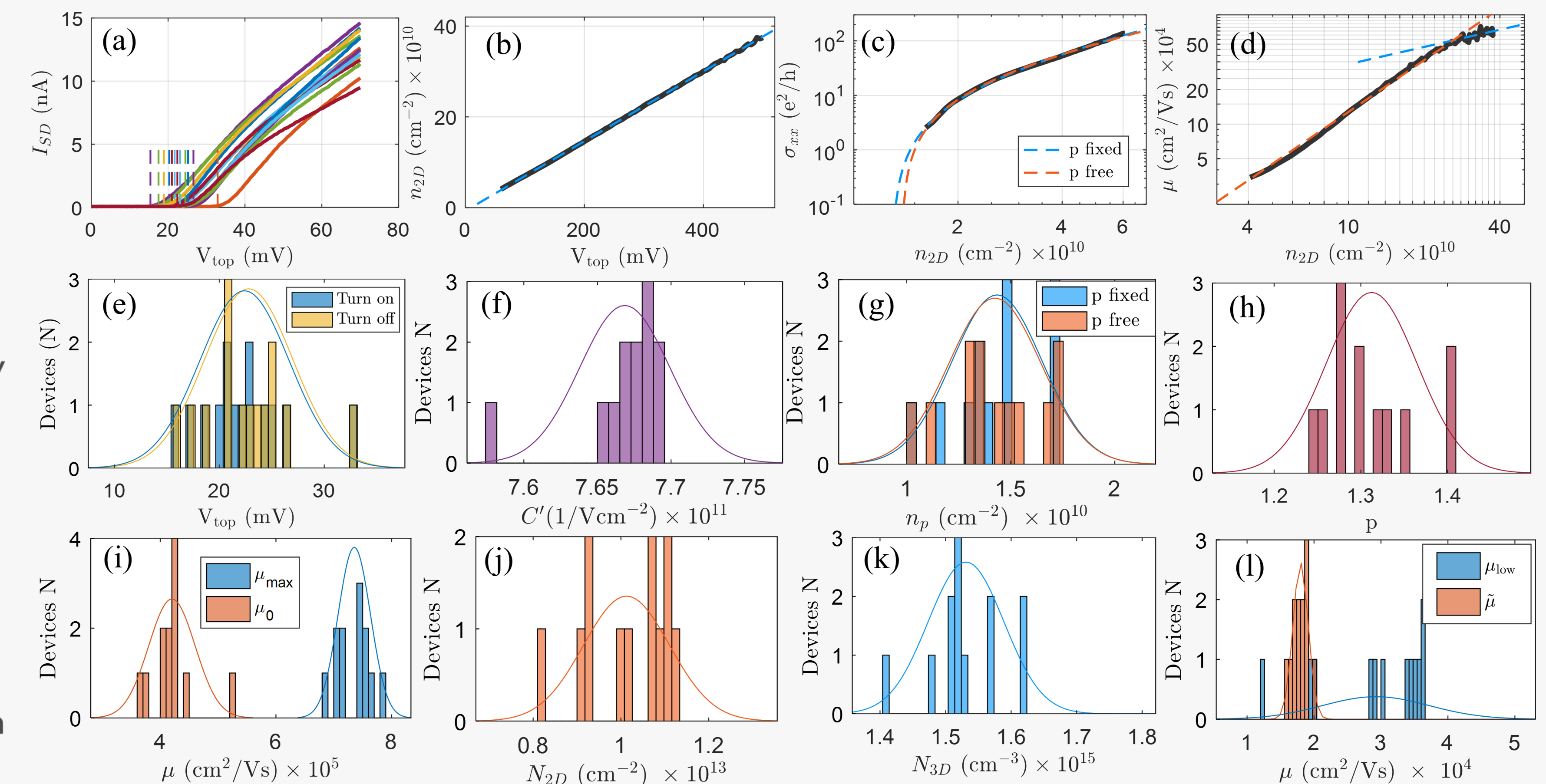
Scalable readout for silicon qubits

The rapid acceleration of quantum computing technologies is poised to reach an interconnect bottleneck, where the qubit count in a quantum processor is limited by the number of input/output (I/O) connections. Quantum processors in silicon provide natural integration of on-chip control logic in the host semiconductor. This work demonstrates multiplexing on-chip which takes advantage of the fabrication compatibility between silicon quantum devices and classical transistor technology.

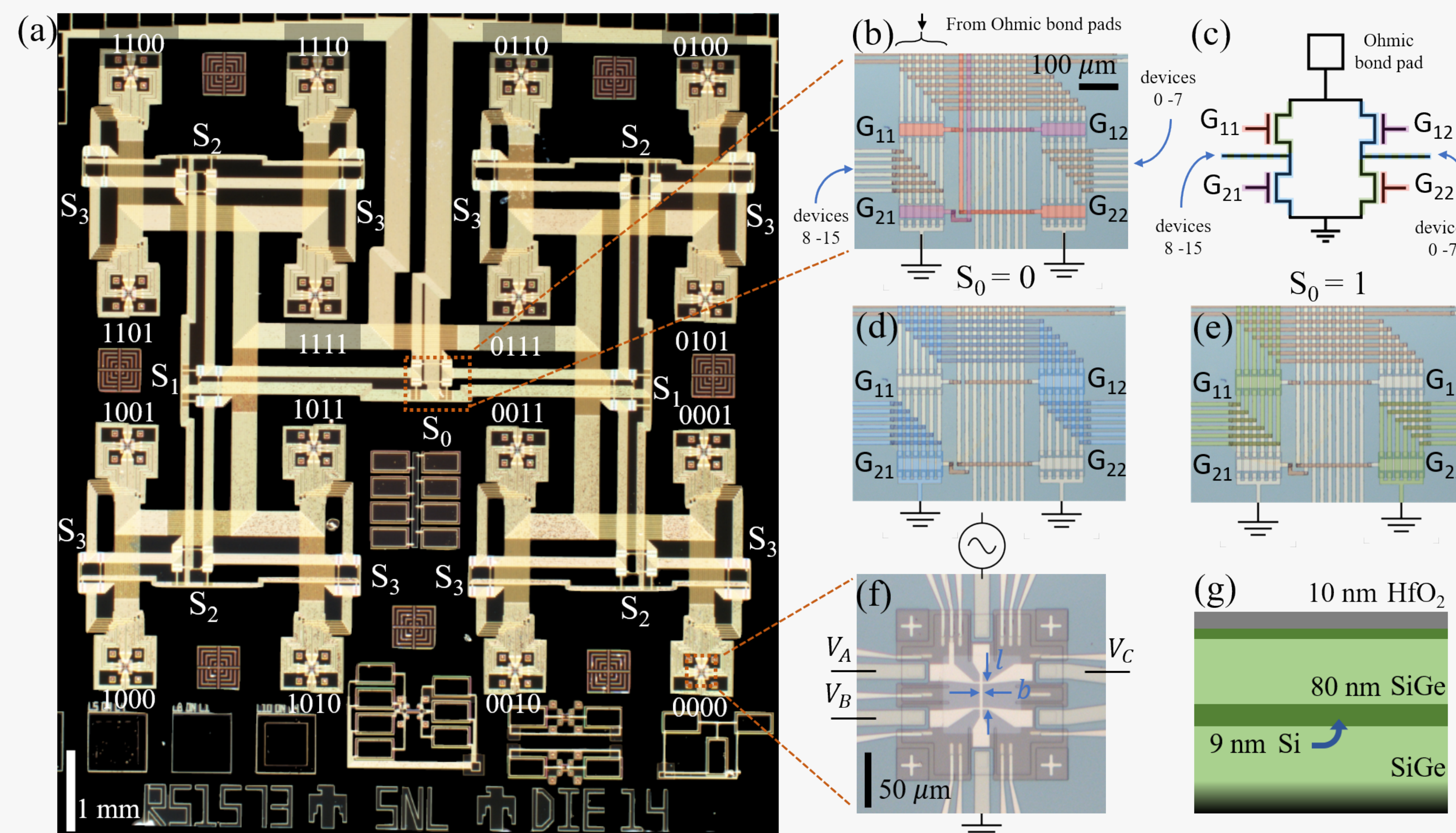


Operation of multiplexers to assess Hall bar device uniformity

(a) Turn-on curves overlaid for each Hall bar. (b) Hall bar capacitance, (c) percolation density, (d) mobility for the $S_0 = 0000$ device. Statistical histograms for (e) threshold voltage, (f) Hall bar capacitance, (g) percolation density, (h) percolation density exponent, (i), mobility fixed at $n_{2D} = 2 \times 10^{11} \text{ cm}^{-2}$ and max mobility, (j) defect density for remote impurities, (k) defect density in the background quantum well, (l) lowest measurement mobility and mobility extracted from tur-on curve.

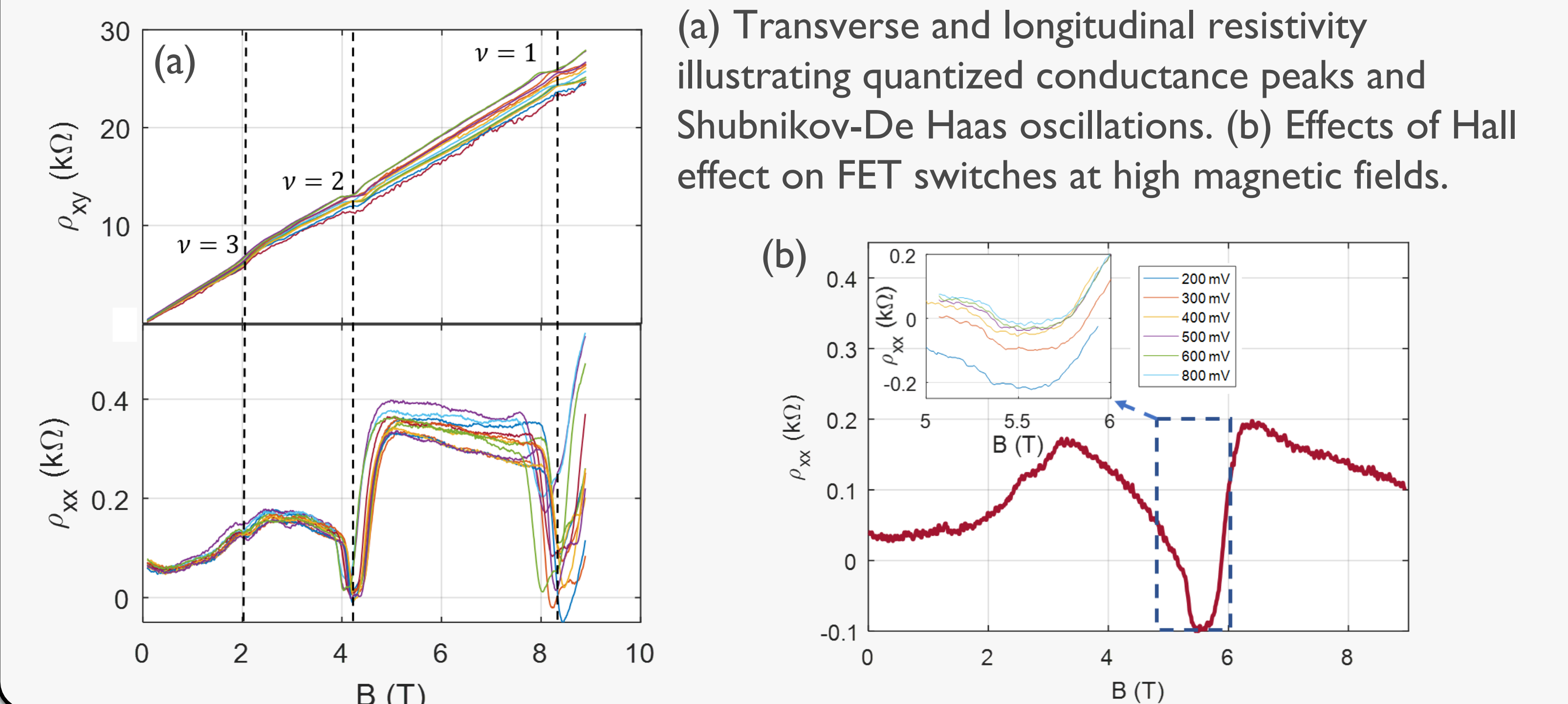


Fabrication and Integration of Si/SiGe on-chip multiplexers



(a) Sixteen quantum device construction zones are multiplexed across a single 11.5 cm x 11.5 cm chip. (b)-(c) Each switch is composed of four FETs for signal routing of ohmic contacts. (d) Operation of switch in $S_0 = 0$ state and (e) $S_0 = 1$ state. (f) Example of quantum Hall device fabricated with electron-beam lithography. Sixteen non-multiplexed Hall bars require 112 electrical connections. This chip requires a total of 16 wire bonds. (g) Si/SiGe heterostructure stack of the mesa for each device in the construction zone.

Operation in large magnetic fields



Acknowledgements

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