

Case Study: Metallurgical and Mechanical Analysis of *Castellated Via* Rigid-Flex Connection

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ABSTRACT

A *castellated via* solder joint is a joint configuration where a semi-circular surface area or *castellation* is soldered to a flat solder pad. The castellated via joint configuration is common in industry, specifically for connecting complex modules to simple board designs to reduce overall board complexity. The reliability and performance of castellated vias as a rigid-flex interconnection method is evaluated here.

This evaluation is split into 2 discreet elements: 1) metallurgical aging of joints and 2) investigating mechanical robustness/integrity of the joints. The metallurgical analysis involved isothermally aging joints and 70 or 100°C for 0, 25, 50, or 100 days. Metallographic cross-sections were cut for several joints per aging condition, and scanning electron microscopy (SEM) imaging was used to evaluate metallurgical reactions within the bulk solder joints and along the joint interfaces.

The mechanical integrity of rigid-flex connections was evaluated by comparing the mechanical performance of as-fabricated joints with that of thermally cycled joints. Two mechanical test methods were employed: 1) Shear; and 2) Peel. Rigid boards soldered to flex cable with this castellated via configuration were cycled from -55°C to 125°C with 10-minute dwells and 10°C/min ramps, between 300-1000 cycles prior to shear and peel testing. Shearing and peeling present different loading conditions to the joints, so different failure modes are observed. Assembly, storage, and service conditions are more likely to induce peel-type loading conditions due to the strain associated with the bent flex cables. Peak failure loads are the metric for comparison. Results to date indicate that the castellated via joint configuration retains high mechanical integrity after 1000 temperature cycles.

Rigid-flex, castellation, mechanical testing, interface

INTRODUCTION

A *castellated via* solder joint is a joint configuration where a semi-circular surface area or *castellation* is soldered to a flat solder pad, shown in Figure 1 [1-2].

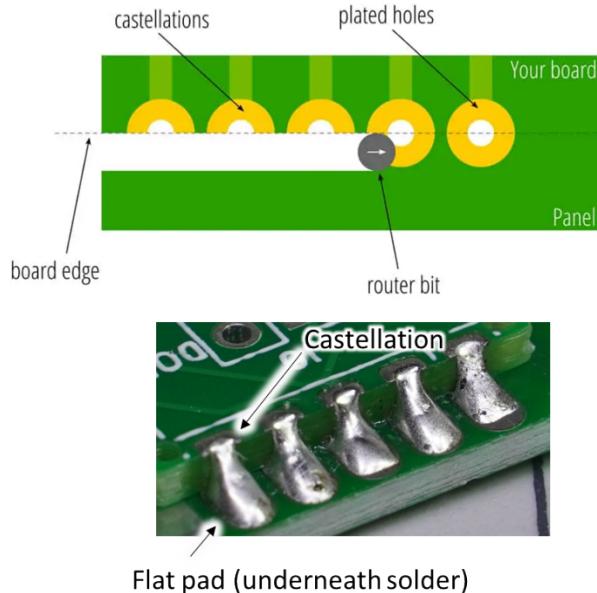


Figure 1. Top view schematic of a castellation (top), and the final joint geometry (bottom).

The castellated via joint configuration is common in industry, specifically for connecting complex modules to simple board designs to reduce overall board complexity [1-4]. This joint

configuration has limited reliability data regarding performance in high reliability rigid-flex connections. A generic rigid-flex printed wiring assembly is shown in Figure 2.

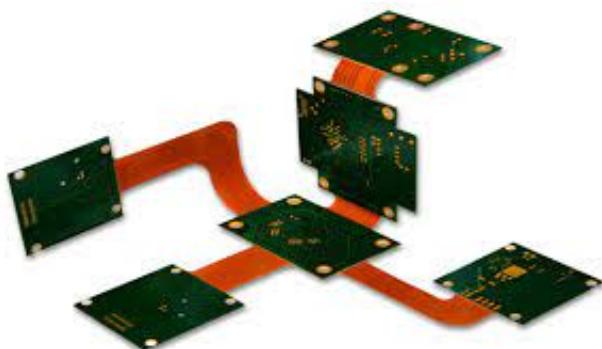


Figure 2. A generic printed wiring assembly (PWA) where 6 rigid boards are mechanically and electrically connected using 5 flex cables. These connections are called rigid-flex connections.

A development design proposed rigid-flex connections using the castellated via configuration, instead of 2 other common methods: 1) through-hole pins or 2) Cu tab connections.

Cu tab connections, shown in Figure 3, consist of a flat, conductive (Cu) lead soldered to a flat pad on the rigid board. The mechanical robustness of this joint configuration is poor, and mechanical failures have been observed.

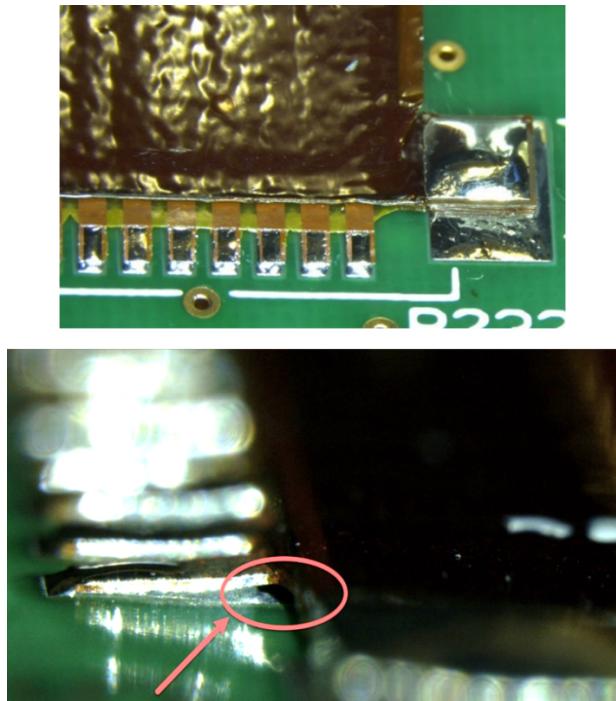


Figure 3. Top and side views of “finger” solder joints connecting a flex cable to a rigid board.

By replacing Cu tab lap joints with castellated via joints, it is predicted that the solder volume per joint would increase and

thin, high stress concentrations would be eliminated, producing more mechanically robust joints.

The purpose of this evaluation is to compare the mechanical performance of as-fabricated joints with that of joints which have undergone thermal cycling conditions, which impose thermal mechanical fatigue on the joints. “Finger” joint configurations were not available for this study, so only the performance for the castellated via configuration is compared, pre- and post- thermal fatigue conditions. This work should provide a baseline for understanding mechanical survivability of these joints.

A complimentary metallurgical evaluation was performed on units to assess any interface reactions and potential instability, which may result in degraded performance over time. These units are independent from those that underwent thermal cycling; they were isothermally aged.

APPROACH

This evaluation is split into 2 discreet elements: 1) assessing the mechanical robustness/integrity of the joints; and 2) assessing the metallurgical aging of joints. Procedures for both studies are described below.

Mechanical Integrity

Baseline mechanical tests were performed on 2 units of the as-received hardware. 2 sections were sheared to failure and 2 units were peeled to failure. Peak failure loads are the metric for comparison.

8 remaining units were cycled 300-1000 times, according to IPC 9701A, from -55°C to 125°C with 10-minute dwells and 10°C/min ramps, prior to shear and peel testing [5]. Figure 6 shows temperature measurements at 6 locations on a board.

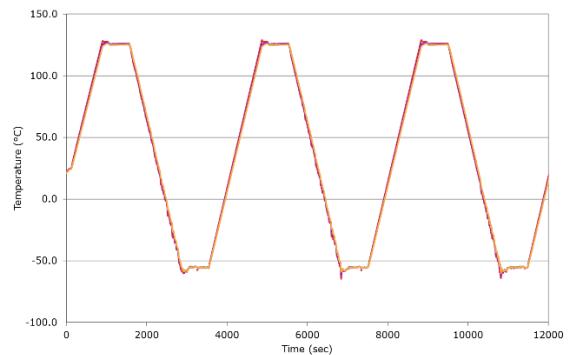


Figure 6. Measured thermal profiles at 6 locations on a given board.

Mechanical testing was performed with an MTS tabletop frame. Test setups for both the shear and the peel tests are shown in Figure 7.

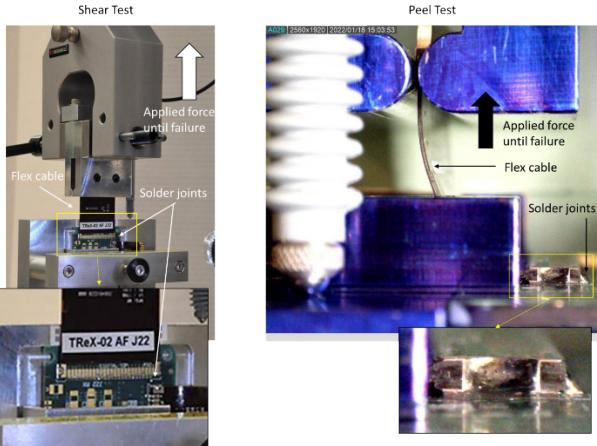


Figure 7. Setups for shear (left) and peel (right) testing.

Actuator rating was ± 5.5 kip, ± 2.25 inches. The system load cell rating was ± 1100 lbf. The linear variable differential transformer (LVDT) probe was a MacroSensors series with a range of ± 200 mils.

Metallurgical Aging

The objective of metallurgical aging is to induce the same metallurgical reactions that would be expected at room temperature, but faster than would occur at room temperature. Solder metallurgical reactions are largely diffusion driven, so accelerated aging can largely be achieved by aging at elevated temperatures. Eutectic 63Sn-37Pb solder was used for all joints.

Solder joints were isothermally aged at either 70°C or 100°C for 0, 25, 50, or 100 days. Metallographic cross-sections were cut for 3 joints per aging condition, and scanning electron microscopy (SEM) imaging was used to evaluate metallurgical reactions within the bulk solder joints and along

the joint interfaces. This analysis also serves to evaluate the quality and consistency of initial solder joints.

RESULTS

Mechanical Integrity

Results for both shear and peel tests are presented below.

Shear Test

Figure 8 shows the force-displacement curves for each shear test. Table 1 highlights the peak forces and observations for each test.

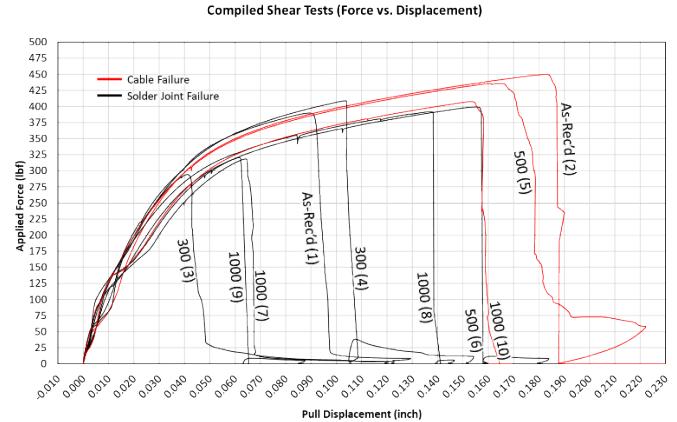


Figure 8. Force vs. displacement plots for all shear tests. Each curve is labeled with its aging condition in number of cycles and its sample ID in parenthesis. Black curves indicate solder joint failures and red curves indicate flex cable failures.

3 out of the top 4 peak load values are due to failures at the flex cable, rather than at the solder joints.

Table 1. Shear test results for each board. “C” and “P” refer to “castellation” and “pad”, respectively. Numbers in parenthesis indicate the individual joint failures for a given cable connection.

ID	Cycles	Failure Description	Peak Force (lbf)	Alignment	Solder Coverage	Castellation Failures	PWB Pad Failures
1	0	Mixed mode (ductile shear, interfacial, pad)	392	Poor	Poor C Poor P	Ductile (12) Interfacial (9)	Peel-Off (4)
2	0	Flex cable tearing at grip	450	Poor	Poor C Moderate P	None	None
3	300	Majority ductile shear	294	Good	Poor C Poor P	Ductile (24) Interfacial (1)	Peel-Off (4)
4	300	Majority ductile shear	409	Good	Poor C Poor P	Ductile (23) Interfacial (4)	Peel-Off (4)
5	500	Flex Cable Tearing at Grip and PWB ends	435	Good	Excellent C Moderate P	None	None
6	500	Mixed mode (ductile shear, interfacial, pad)	399	Good	Poor C Moderate P	Ductile (9) Interfacial (16)	Peel-Off (9)
7	1000	Mixed mode (ductile shear, interfacial, pad)	318	Poor	Poor C Moderate P	Ductile (4) Interfacial (17)	Peel-Off (8)
8	1000	Mixed mode (ductile shear, interfacial, pad)	392	Good	Poor C Poor P	Cohesive (6) Interfacial (18)	Peel-Off (6)
9	1000	Mixed mode (ductile shear, interfacial, pad)	320	Good	Poor C Poor P	Ductile (19) Interfacial (6)	Peel-Off (19)
10	1000	Flex cable tearing at grip	408	Good	Poor P Poor C	None	None

While the table above does identify common failure modes, note that these identifications have been made using only optical imaging. While the ductile and interfacial failure modes are likely to be correct, scanning electron microscopy (SEM) imaging is required to confirm.

Representative low magnification, optical images for pre-and post-tested samples are shown for the as-received, 300 cycle, 500 cycle, and 1000 cycle conditions in **Figure 1**, **Figure 3**, **Figure 5**, and **Figure 6**, respectively.

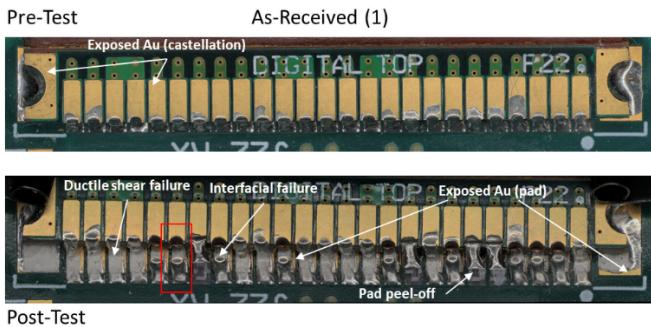


Figure 1. Top views of a flex cable connected to the PCB with castellated via solder joints, before (top) and after (bottom) shear testing. The red box highlights the inset shown in Figure 2. This unit was tested in the as-received condition. Sample ID is shown in parenthesis.

A higher magnification image of a potential interfacial failure highlighted in the red box above is shown in **Figure 2**. The failure occurs along the castellation-Cu interface. The two options for the exact interface are: 1) along a board-Cu

plating interface; or 2) along a Cu-Cu₆Sn₅ interface. SEM imaging is required for confirmation, however.

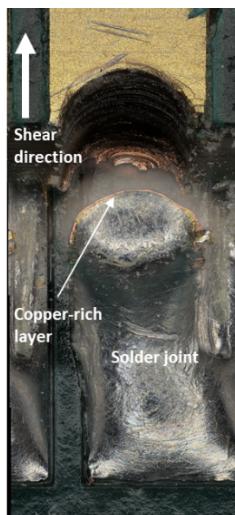


Figure 2. Higher magnification optical image of a potential interfacial failure at the castellation-Cu plating interface.

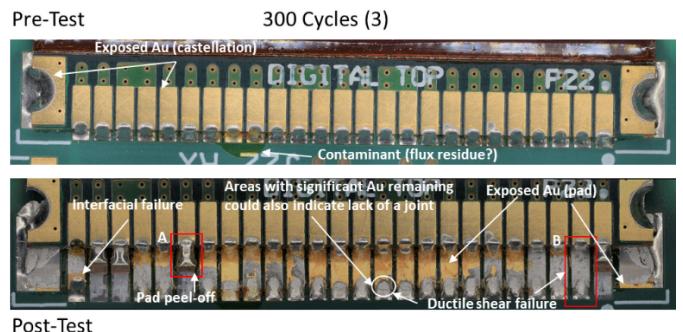


Figure 3. Top views of a flex cable connected to the PCB with castellated via solder joints, before (top) and after (bottom) shear testing. The red box highlights the insets shown in Figure 4. This unit was tested after 300 cycles. Sample ID is shown in parenthesis.

A higher magnification image

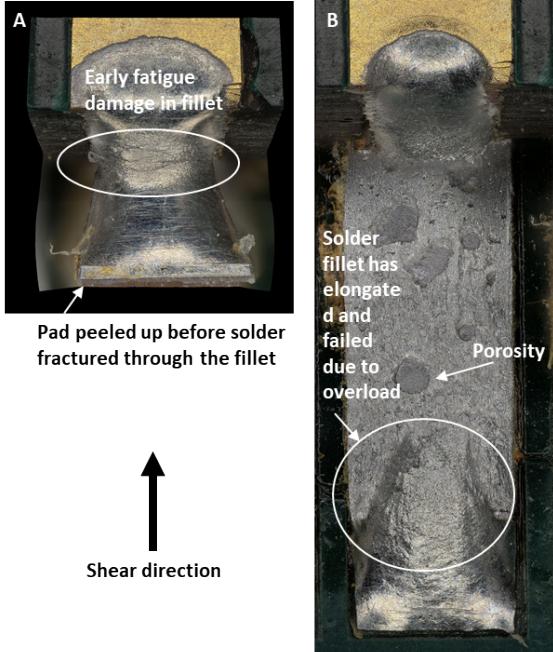


Figure 4. Higher magnification optical images highlighting pad peel-off (A) and ductile shear (B) failure modes.

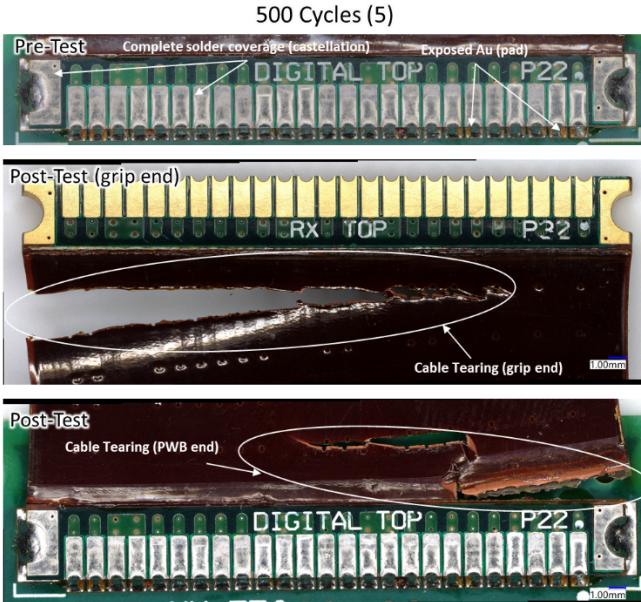


Figure 5. Top views of a flex cable connected to the PCB with castellated via solder joints, before (top) and after (middle, bottom) shear testing. This unit was tested after 500 cycles. Sample ID is shown in parenthesis.

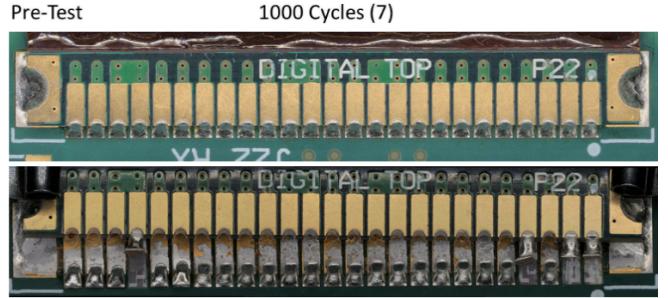


Figure 6. Top views of a flex cable connected to the PCB with castellated via solder joints, before (top) and after (bottom) shear testing. This unit was tested after 1000 cycles. Sample ID is shown in parenthesis.

Peel Test

Figure 7 shows the force-displacement curves for each shear test. Table 2 highlights the peak forces and observations for each test.

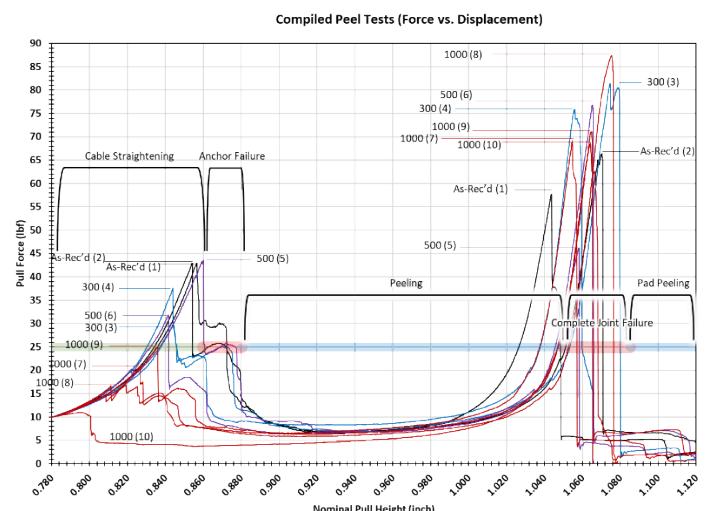


Figure 7. Force vs. displacement plots for all peel tests. Each curve is labeled with its aging condition in number of cycles and its sample ID in parenthesis. Black, blue, purple, and red curves denote as-received, 300 cycle, 500 cycle, and 1000 cycle conditions, respectively. The curves are broken into 5 regions, denoting observed behavior during testing.

Table 1. Peel test results for each board. Numbers in parenthesis indicate the individual joint failures for a given cable connection.

ID	Cycles	Anchor		Castella tion Failure Load (lbf)	Castellation Failure Mode
		Failure Load (lbf)	Anchor Failure Mode		
1	0	33.3	Cu Interface	57.9	Cu Interface (4) Ductile Solder (10) Gap (11)
		43	Cu Interface	57.7	Cu Interface (4) Ductile Solder (6) Gap (15)
2	0	63.7	Cu Interface	28	Cu Interface (9) Ductile Solder (8) Gap (2) Board Pad (6)
		43	Cu Interface	66.4	Cu Interface (4) Ductile Solder (3) Gap (18)
3	300	18.3	Cu Interface	92.6	Cu Interface (10) Ductile Solder (6) Gap (9)
		10	Cu Interface	81.5	Cu Interface (3) Ductile Solder (10) Gap (12)
4	300	23.2	Cu Interface	82.3	Cu Interface (1) Ductile Solder (18) Gap (6)
		37.6	Cu Interface	76	Cu Interface (10) Ductile Solder (10) Gap (5)
5	500	36.5	Cu Interface	71.5	Cu Interface (7) Ductile Solder (10) Gap (7) Board Pad (1)
		43.6	Cu Interface	46.3	Cu Interface (0) Ductile Solder (7) Gap (15) Board Pad (3)
6	500	20.6	Cu Interface	85.6	Cu Interface (0) Ductile Solder (11) Gap (14)
		31.9	Solder Interface, Cu Interface	77	Cu Interface (0) Ductile Solder (7) Gap (18)
7	1000	20	Solder Interface, Cu interface	62	Cu Interface (5) Ductile Solder (12) Gap (8)
		20.9	Solder interface	69.3	Cu Interface (0) Ductile Solder (12) Gap (13)
8	1000	15.1	Cu interface, board pad	90.3	Cu Interface (9) Ductile Solder (15) Gap (1)
		16.9	solder interface	87.4	Cu Interface (1) Ductile Solder (18) Gap (6)
9	1000	29.8	solder interface	55.1	Cu Interface (0) Ductile Solder (12) Gap (13)
		25.2	Cu interface, solder interface	71.3	Cu Interface (1) Ductile Solder (3) Gap (21)
10	1000	23.1	Cu interface, board pad	82.5	Cu Interface (10) Ductile Solder (11) Gap (4)
		11	Cu Interface, solder interface	68.8	Cu Interface (6) Ductile Solder (16) Gap (3)

Figure 16 shows an optical image of a cable assembly post-peel test, with various failure modes identified.

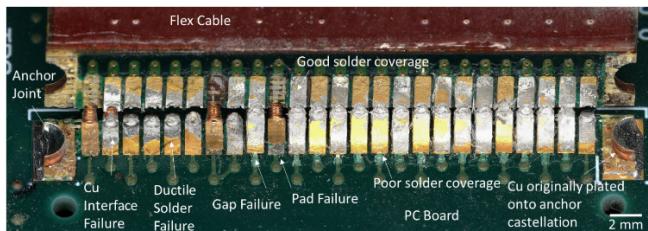


Figure 8. Top view of a flex cable connected to the PCB with castellated via solder joints, after peel testing. This unit was tested in the as-received condition.

Metallurgical Aging

Figure 17 shows the general cross-sections that were cut through the castellation joints and highlights the key areas for potential Au embrittlement (yellow boxes). The red boxes indicate the higher magnification SEM inset images shown in Figure 18.

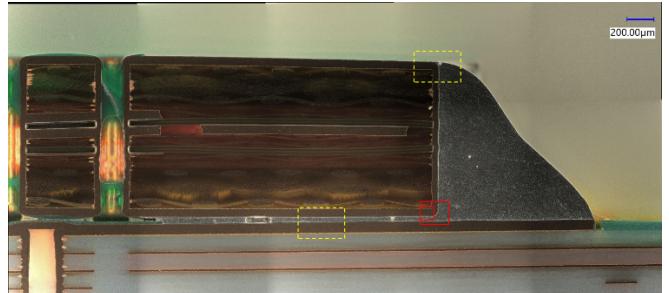


Figure 17. Optical image showing a low magnification cross-section through a castellated via solder joint. Yellow boxes highlight the high-risk locations for potential Au embrittlement. The red boxes highlight the locations where EDS maps were acquired, in Figure 19.

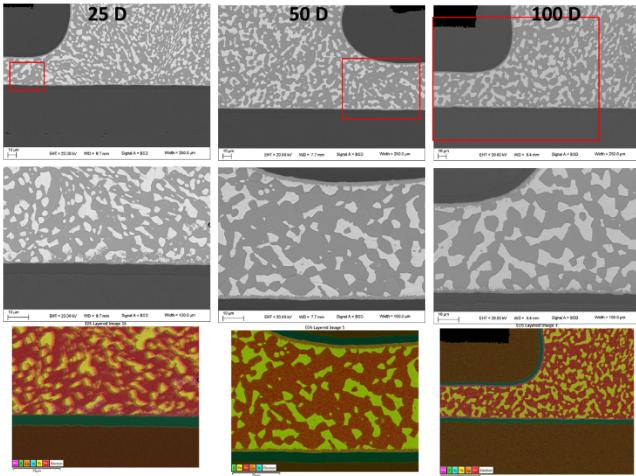


Figure 18. Higher magnification SEM images of the red insets from Figure 17. The columns represent a given aging condition: 25, 50, and 100 days (left, middle, and right, respectively). The middle row shows a higher magnification image highlighted by the red inset box. The bottom row shows corresponding EDS maps. All three samples were aged at the more extreme 100C.

DISCUSSION

Mechanical Testing

Shear Test

Peak failure loads varied between 294 and 450 lbf with no obvious trend between number of thermal cycles and peak failure load is observed. The highest peak loads are exhibited by the units where the cable failed rather than the solder interconnections. The 3 cable failures indicate that the solder joints are not necessarily the limiting factor in mechanical strength. Aging appears to have had little impact on the cable performance either, as these failures included an as-received assembly and an assembly cycled 1000 times.

Failure modes at the castellation remain split between ductile failure through the solder joint and interfacial failure along the solder interface. The exact interface is still under investigation but is either the board-Cu plating interface or the intermetallic-solder interface. Empirically, more cycles tended to cause more interfacial failures, but the small sample size precludes any confident trend identifications here. Pad failures on the board side were also common and tended to increase with thermal cycles, suggesting thermomechanical stresses are present and potentially significant over time between board, pad, and solder joint.

The main discussion point is the solder joint from a fabrication standpoint. These joints were fabricated with a hand soldering method. The workmanship is generally inconsistent. Complete solder coverage on the board side pads is rare, and this inconsistency in solder volume is likely to contribute to mechanical strength more than simply aging. While the ENEPIG surface finish likely prevents Au embrittlement at the solder interface, this degradation method should still be considered with large areas of Au still present

post-soldering. The top surface of the castellation also includes a pad, but minimal solder coverage is ever observed. IPC-A-610H, section 8.3.4 addresses the acceptance criteria for castellated vias, but top pads are not considered, so it isn't clear if the joints would even pass inspection per IPC-A-610 [6].

Even with the workmanship and consistency concerns, the mechanical performance does not appear to be a significant concern over time. Aging in a built up condition, where the flex cables are in their bent configuration would help provide further confidence.

Peel Test

The force-displacement curves highlight several distinct loading conditions imposed and associated observations of the flex-cable assembly and solder joints. A bimodal distribution of failures is evident. 2 distinct failures were observed in every test: 1) failure of the 2 larger anchor joints; and 2) failure of the remaining 25 castellations between the anchors.

Anchor joints failed at much lower loads, relatively, and should thus be considered the limiting factor for interconnection failure. Figure 19 highlights the average failure loads of the anchor joints compared to the inner castellations as a function of aging condition.

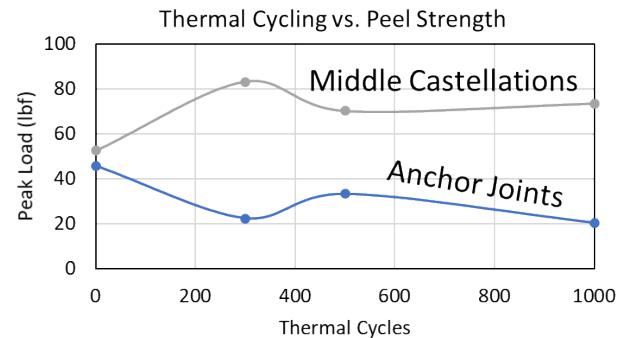


Figure 19. Plot that compares average failure loads of middle castellations (gray) and anchor joints (blue).

The main difference between the side castellations and inner castellations is size and orientation to loading direction; the lower failure loads makes sense, as the solder volume shared between these 2 joints is much less than that between the 25 other joints. If the anchor joints are meant to provide the bulk of the mechanical performance for the cable, larger and or more anchor joints may be desirable. The anchor joints do appear to successfully isolate early mechanical failure though, while presumably still permitting the inner joints to provide the electrical connectivity and performance for cable functionality.

Unlike the shear testing, some correlation between aging and mechanical performance is observed, only for the anchor joint failures. More cycling leads to faster failures at lower

loads. Beyond 500 thermal cycles, the failure mode shifts from the castellation-Cu interface to a mixed mode failure at this same interface as well as at an interface adjacent to the bulk solder. It is likely that cycling exacerbated the solder-intermetallic interface integrity and the peel stress concentrated at that location. Metallurgical evolution at this interface is also a likely contributor and is still currently under investigation.

Trends between failure loads and aging conditions are not observed for the failure of the inner castellations. Failure loads in this case are at least 2x those of the outer, anchor joints. Failure modes are split between interfaces, bulk solder, and the bottom gap, but variation in solder volume between these joints is likely a key contributor to failure mode. The same fabrication and workmanship concerns that were highlighted in the shear test results are visible after the peel tests.

Peel stress appears to be a more concerning loading condition relative to the shear condition (as expected). Since the bent cable geometry of fully built-up units will impose more of a peel stress, these results will provide more relevant failure data than the shear test, in terms of failures that may be observed during fabrication, storage, and service.

Metallurgical Aging

The joint microstructure appears to be relatively stable with increasing time at 100C. The 70C results are not shown here because the 100C condition is expected induce more significant microstructural change, if any. While coarsening of the bulk solder microstructure (Fig. 18) is evident, the interfaces appear to remain stable over time, both the Cu-SnPd intermetallic and the SnPd intermetallic-solder. No voiding is observed, so the concern for microstructural instability over time is relatively low.

Au signals were absent within the bulk solder and along the interfaces where solder was present. No signs of Au intermetallic formation or Au embrittlement along the interfaces was observed, even at the high-risk areas where the solder does not fully wet the pads, leaving elemental Au adjacent to solder. The lack of Au embrittlement can be attributed to the small Au concentration and thickness of the ENEPIG finish. further investigation into microstructure continues but is unavailable at the time of publishing this report.

CONCLUSIONS

1. An empirical reliability evaluation was performed on the castellated via interconnection for rigid-flex connections. Shear and peel tests were performed on as-received and thermally cycled units.
2. Thermal cycling appears to have a negligible impact on shear performance of the joints.
3. A bimodal failure distribution is observed during the peel tests: anchor joints fail at lower loads than the

inner joints. Increased thermal cycling appears to decrease the failure loads only for the anchor joints.

4. This castellated via joint configuration retains high mechanical integrity after 1000 temperature cycles.
5. The current hand-soldering process that produced the castellated via solder joints for this study is not consistent. Neither cable alignment nor solder volume is consistent throughout the samples. These 2 variations alone may have more of an impact on mechanical performance than thermal cycling. More process control and/or developing a semi-automated reflow process is recommended.
6. Exposed Au present on nearly every solder pad, both on the PCB side and on the cable side. While evidence of Au embrittlement is lacking, retained Au is not a best practice.

REFERENCES

1. Cook, J. "How to design castellated PCBs for Board-to-board attachment." *Embedded Computing Design*, blog. 2021.
2. Peterson, Z. "How to Design Castellated Holes for an SMD Module." *Altium*. 2021.
3. E. W. Wells, H. H. Sigmarsson and J. W. McDaniel, "Design of a Frequency-Agile and Surface Mountable Suspended Integrated Strip-Line Bandpass Filter Using Castellated Vias," *2022 IEEE 22nd Annual Wireless and Microwave Technology Conference (WAMICON)*, 2022, pp. 1-4, doi: 10.1109/WAMICON53991.2022.9786093.
4. S. Sirci, J. D. Martínez, R. Stefanini, P. Blondy and V. E. Boria, "Compact SMD packaged tunable filter based on substrate integrated coaxial resonators," *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1-4, doi: 10.1109/MWSYM.2014.6848557.
5. IPC-9701A, Specification. "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments." 2006.
6. IPC-A-610H, Specification. "Acceptability of Electronic Assemblies." 2020.