



Sandia
National
Laboratories

High-level benchmarks and low-level characterization

PRESENTED BY

Timothy Proctor

Quantum Performance Laboratory

@ Sandia National Laboratories
Livermore, CA and Albuquerque, NM, (and Chicago, IL)

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.



Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Outline



1. Holistic benchmarking

- Volumetric benchmarking
- Algorithmic benchmarks

2. Detailed error characterization

- State and process tomography
- Gate set tomography

Outline

1. Holistic benchmarking

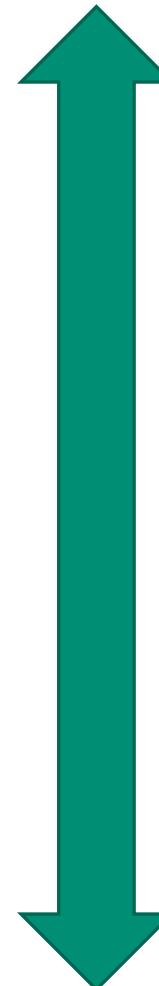
- Volumetric benchmarking
- Algorithmic benchmarks

Many methods sit between these two extremes

- One/two-qubit RB¹
- Cycle benchmarking²
- Pauli noise learning³
-

2. Detailed error characterization

- State and process tomography
- Gate set tomography



High-level performance assessment

Aims to answer questions like:

- What's this device's failure rate when running many-qubit circuits?
- What algorithms can this device run?
- Is device X or device Y better?

Low-level performance assessment

Aims to answer questions like:

- What kinds of errors are occurring?
- What's the error rate of each kind of fundamental error on each gate?
- What's the process fidelity of this gate?

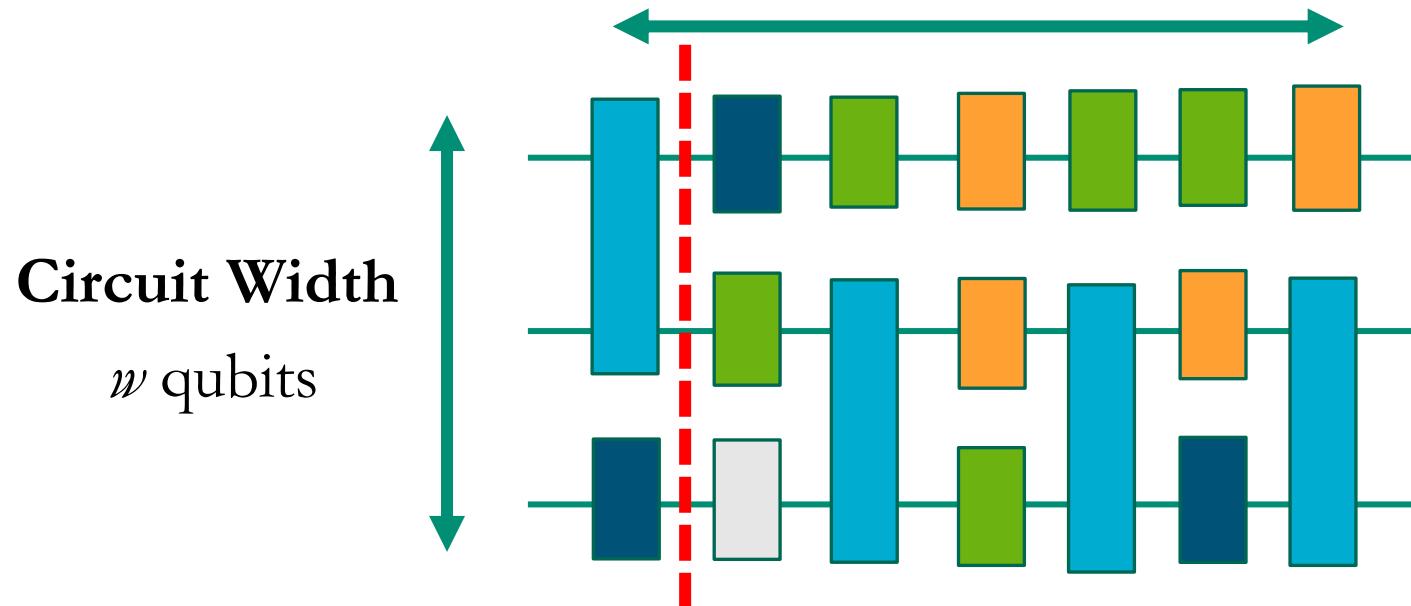
¹E. Magesan et al., Phys. Rev. Lett. 106, 180504 (2011), ²A. Erhard et al, Nat. Commun. 10, 5347 (2019). ³R. Harper et al, Nat. Phys. 16, 1184 (2020).

Recap: what is a quantum circuit?



Circuit Depth

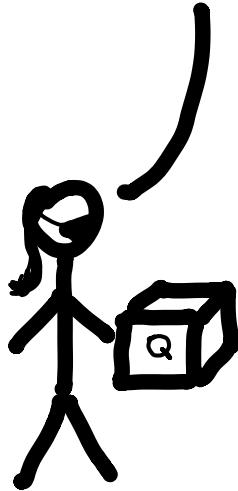
d layers (“cycles”) of logic gates



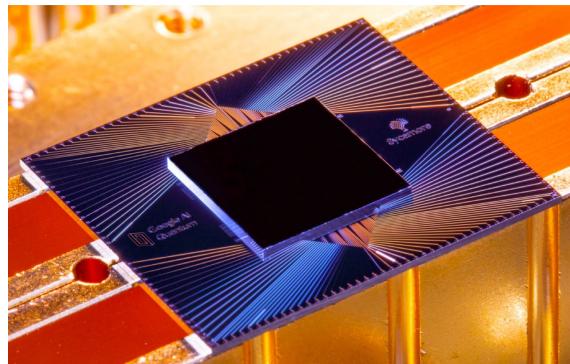
Many methods assume implicit “barriers” between every layer that prevent *compilation*, i.e., collapsing the circuit to a simpler circuit that implements the same unitary.

Holistic benchmarking

Want to buy my quantum computer?

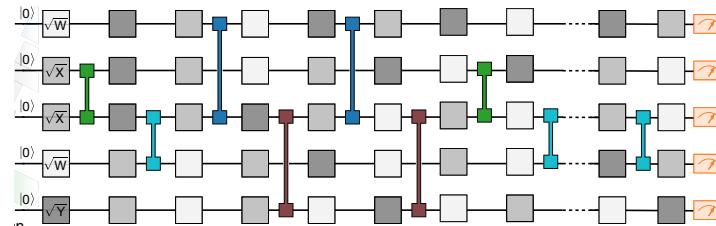


What applications or algorithms can it run?



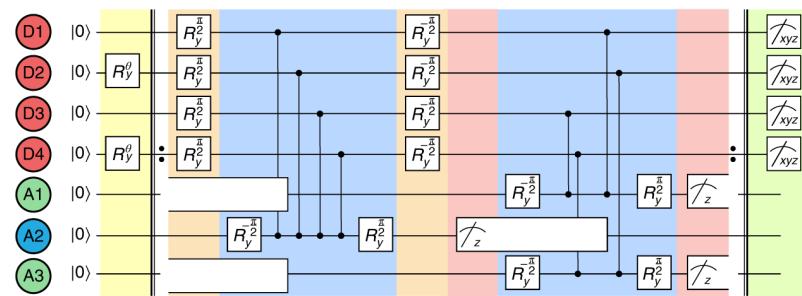
Arute et al., Nature 574, 505 (2019)

Can it run random circuit sampling?



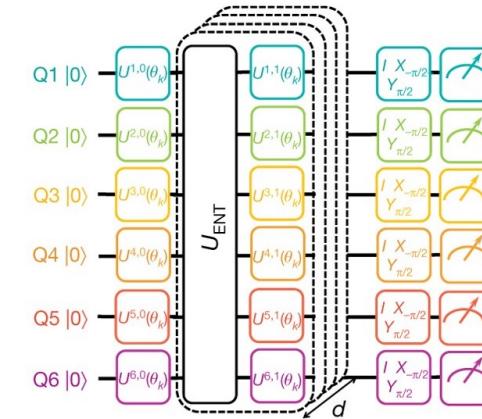
Arute et al., Nature 574, 505 (2019)

Quantum error correction?



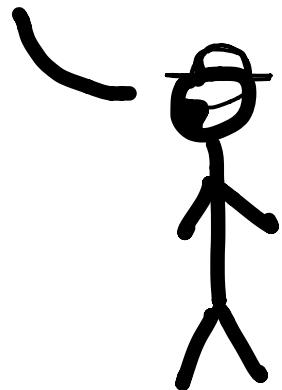
Anderson et al., Nat. Phys. 16, 875 (2020)

What about QAOA?



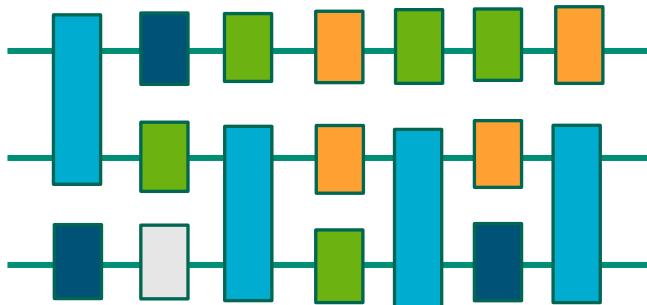
Kandala et al., Nature 549, 242 (2017)

What about VQE? What about Phase Estimation? The QFT? Etc... etc...

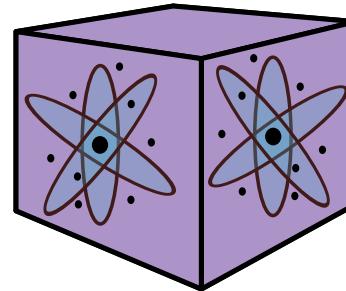


Noisy quantum computers

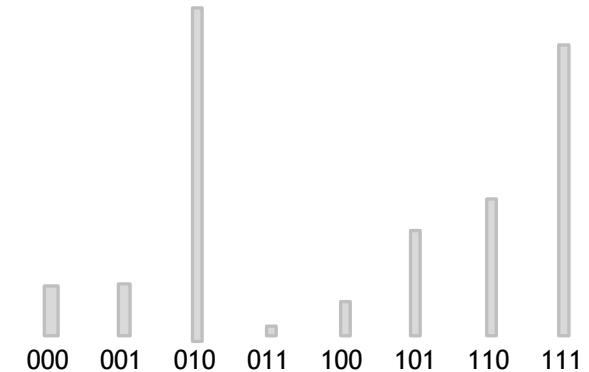
My quantum circuit



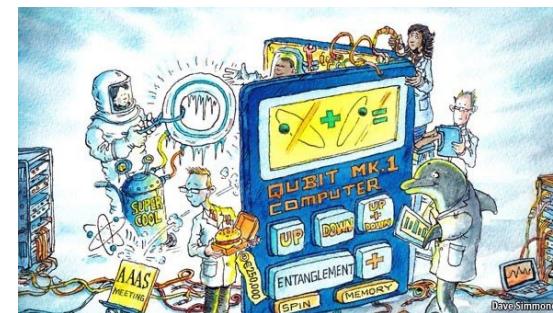
My (imaginary) perfect quantum computer



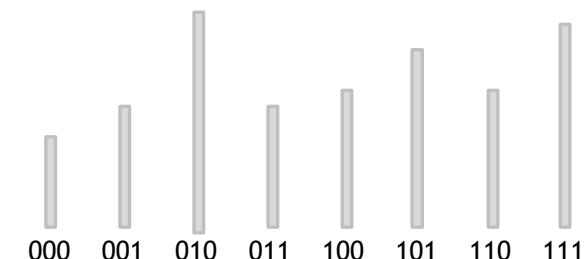
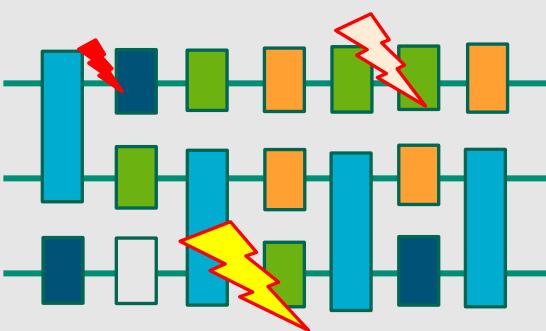
Distribution over bit strings



A real quantum computer



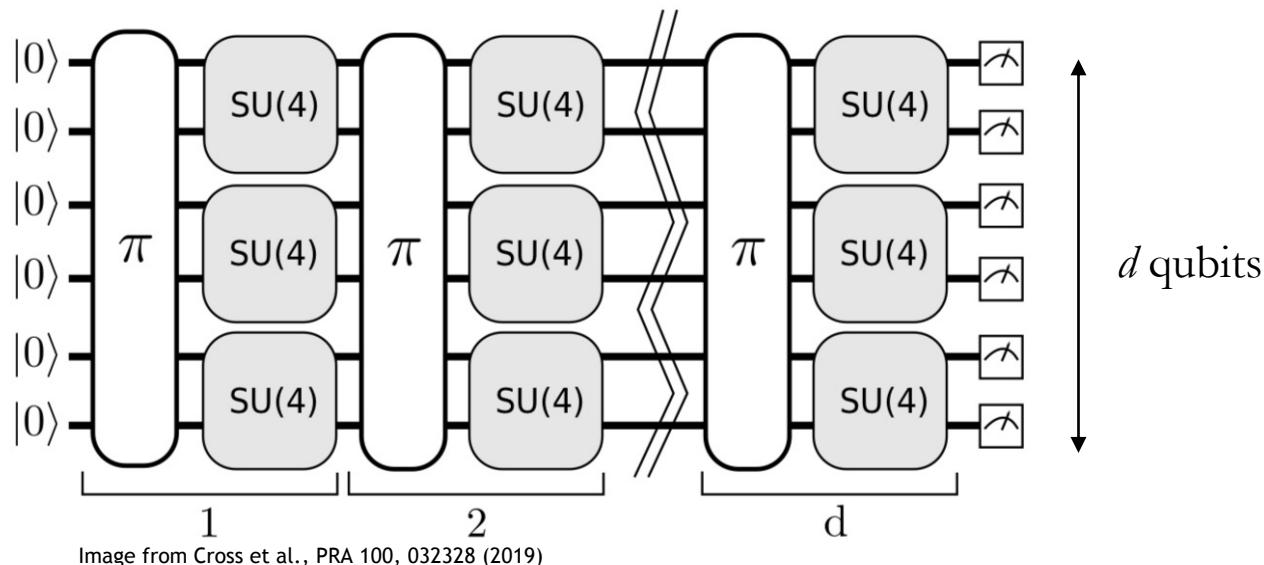
Errors occur when circuits are run on real quantum computers!



“Success probability” = “Distance between these distributions”

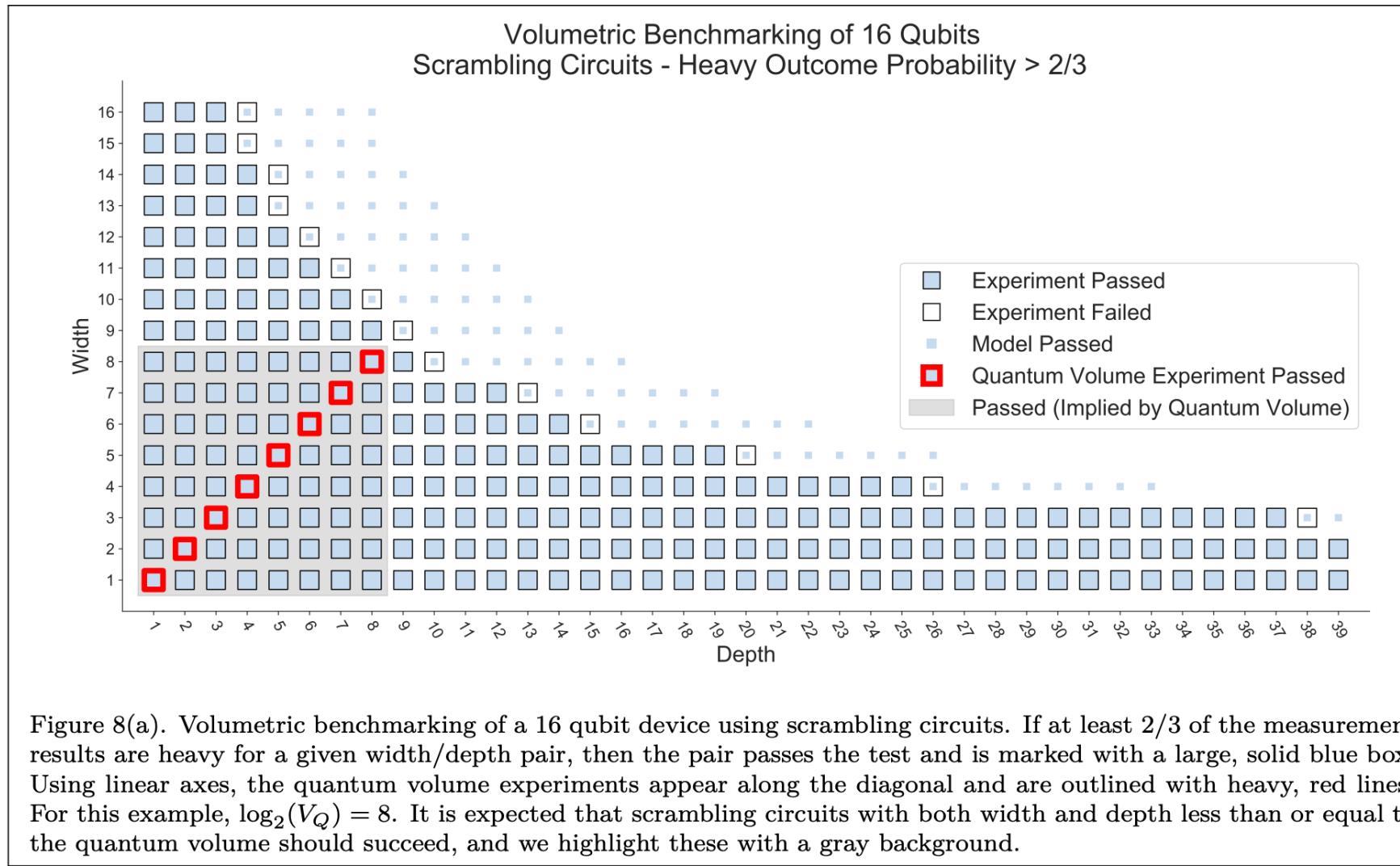
The quantum volume benchmark

- The quantum volume benchmark¹ is based on a particular family of random circuits:



- The quantum volume benchmark is a “full stack” benchmark: it permits **compilation**: you’re only required to implement approximately the same unitary as the circuit.
- Therefore quantum volume does not isolate gate performance: it quantifies a complex combination of gate performance, compiler performance, and programmability limitations.

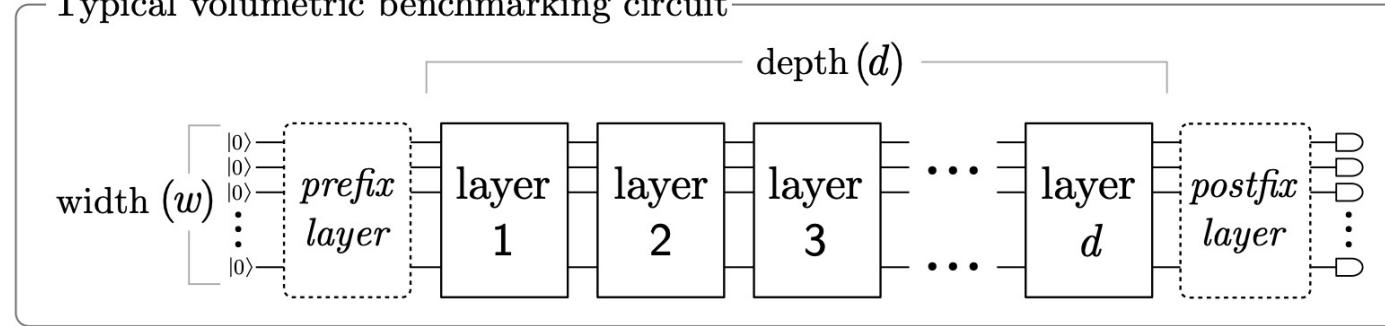
Beyond square circuits: volumetric benchmarking with quantum volume's circuits



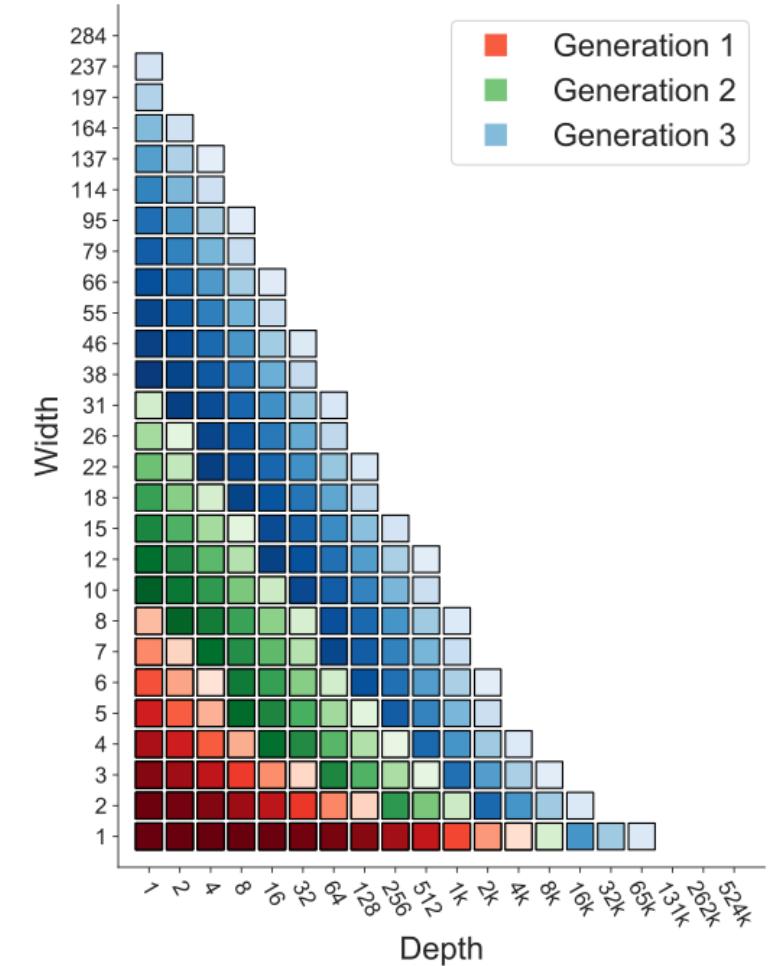
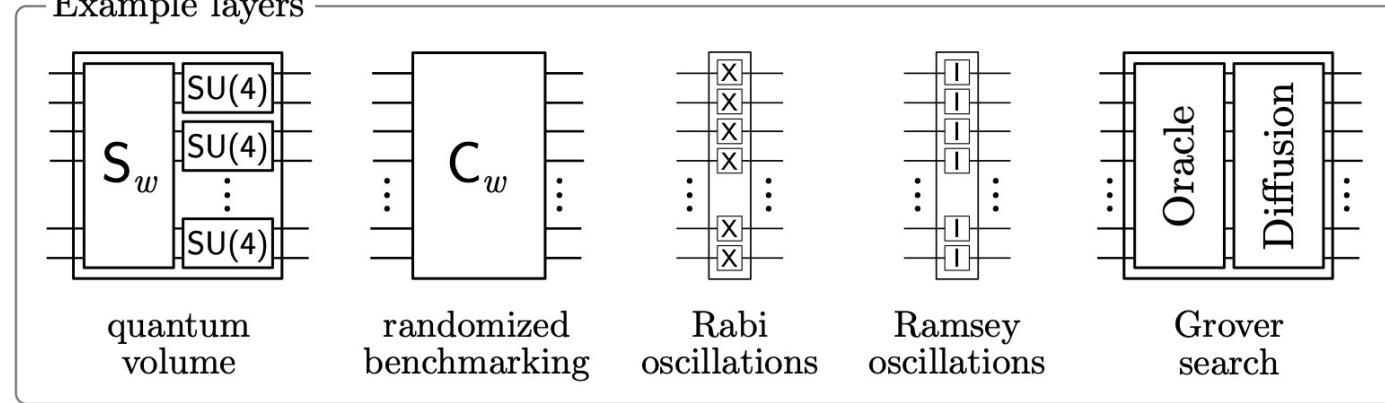
Beyond the QV circuits: general volumetric benchmarking



Typical volumetric benchmarking circuit



Example layers



Almost any family of circuits can be used for volumetric benchmarking!

Holistic benchmarking aims to probe a quantum computer's "capability"

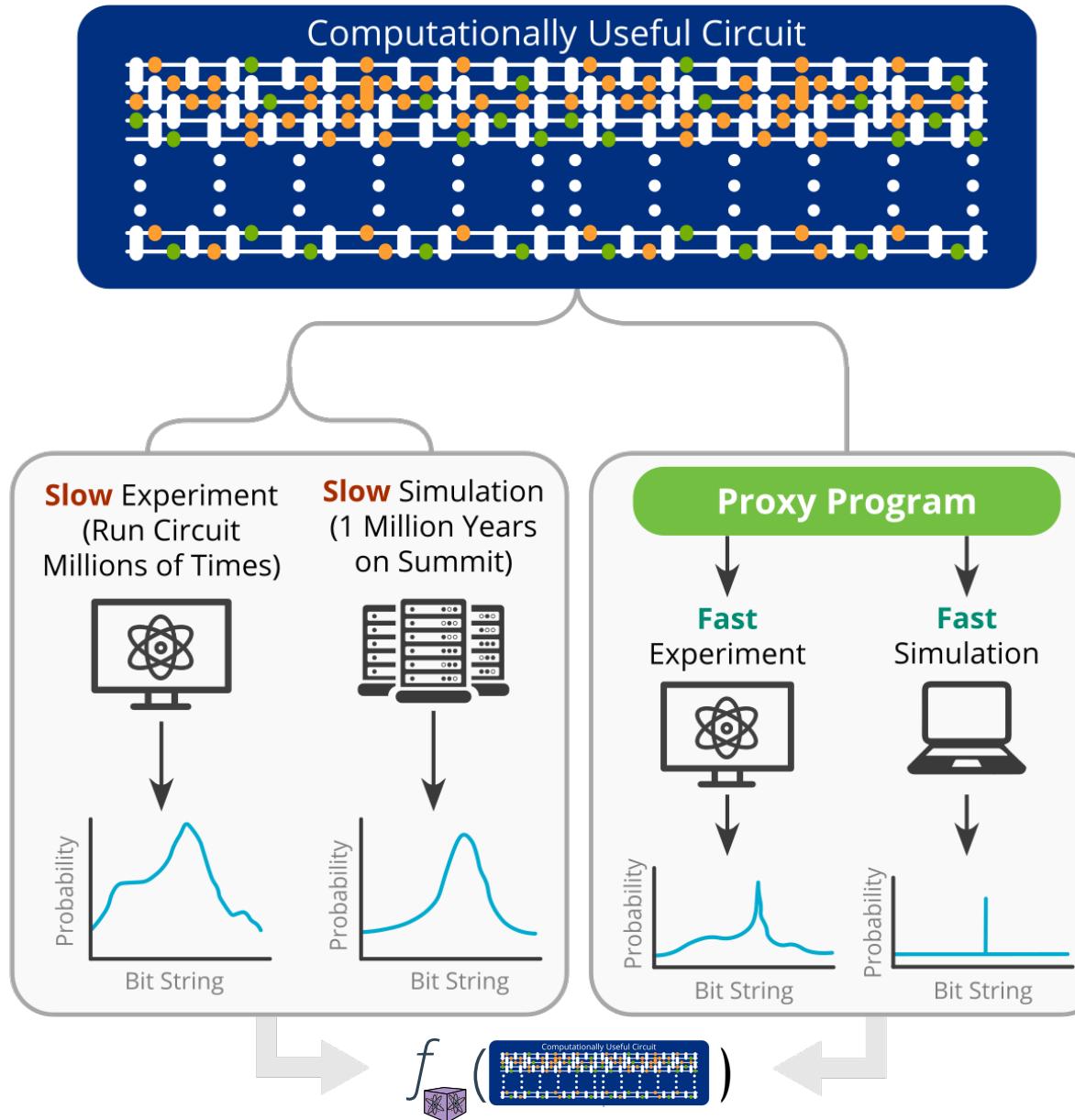
- We define a quantum computer's *capability* to be a map from the space of circuits to the circuit's success rate (quantified, e.g., by fidelity).

$$f \left(\begin{array}{c} \text{Quantum Circuit} \\ \text{Diagram} \end{array} \right) = 94\% \text{ Success probability}$$

- This function is what (most) holistic benchmarks are trying to probe and understand.
- But we can't just measure $f(C)$ using an experiment...

The long-term challenge: avoiding exponential resource scaling

The obvious approach to benchmarking

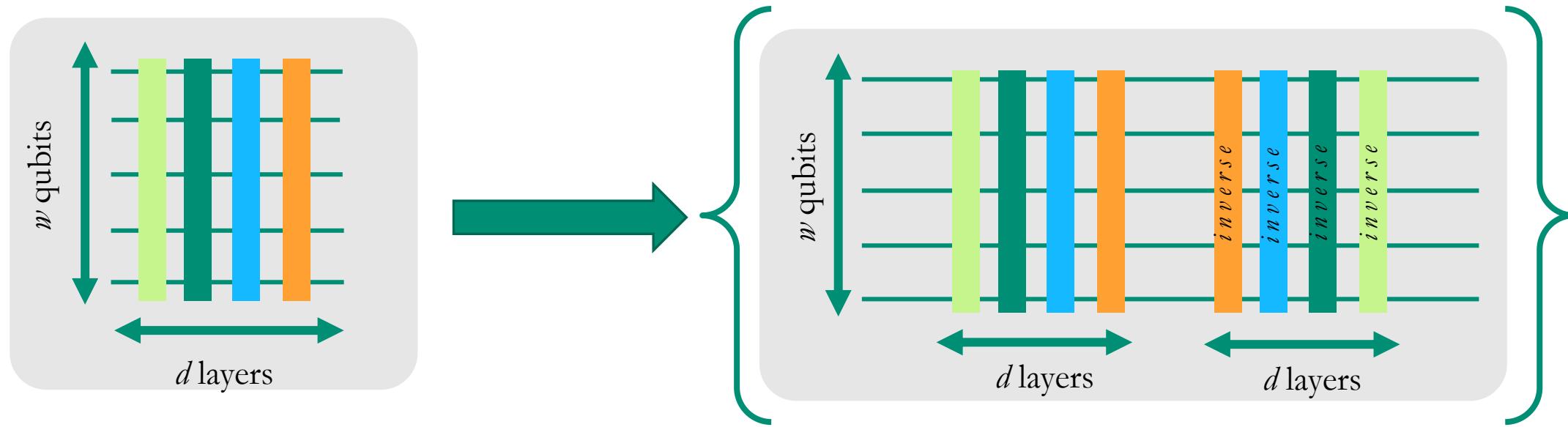


Instead we must use carefully designed, efficiently verifiable “proxy programs”



Mirror circuit benchmarks

One solution – converting any circuit C to a set of “mirror circuits”:

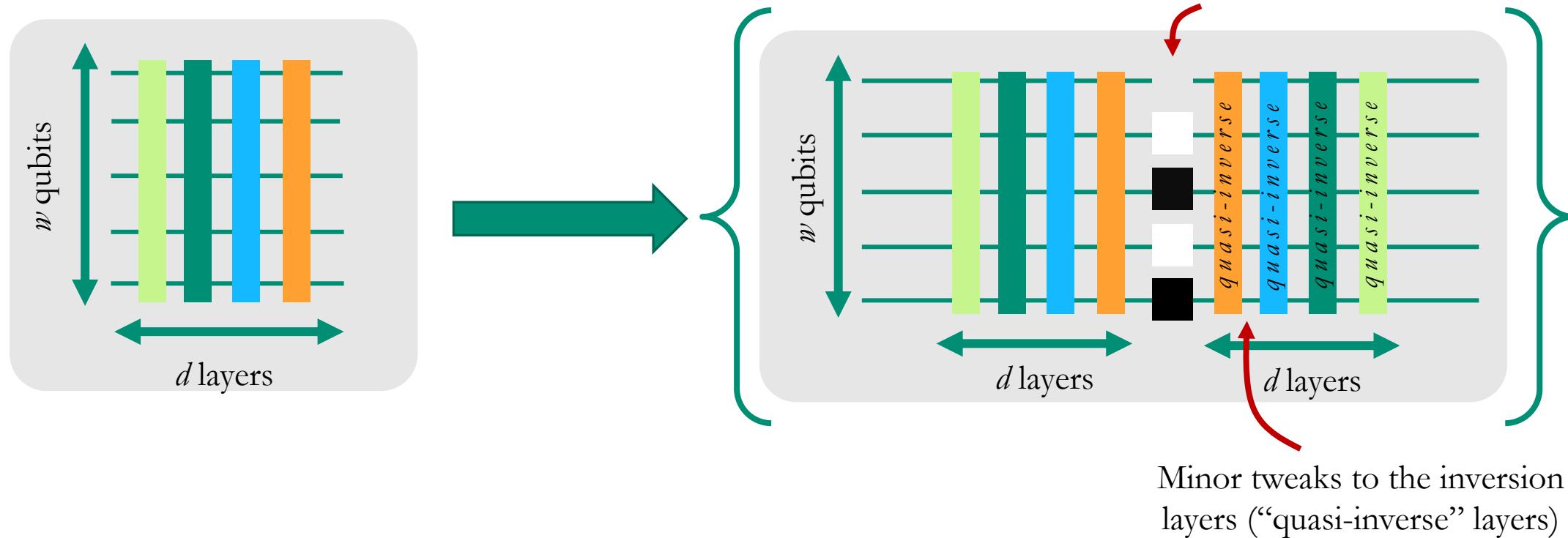


Flawed due to error
cancelation/addition!

Mirror circuit benchmarks

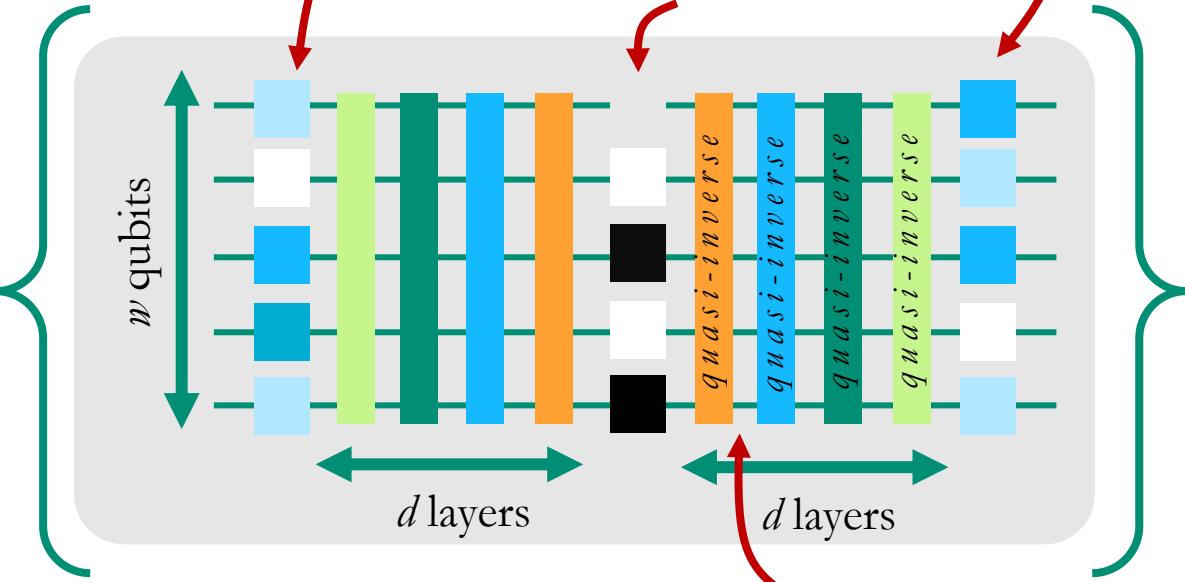
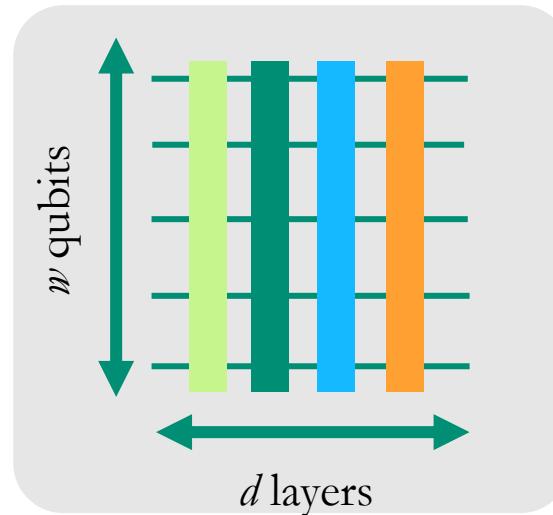


One solution – converting any circuit C to a set of “mirror circuits”:



Mirror circuit benchmarks

One solution – converting any circuit C to a set of “mirror circuits”:



Properties:

1. Every mirror circuit has an efficiently verifiable output.
2. A processor’s performance on these mirror circuits is representative of how well it will perform on C .

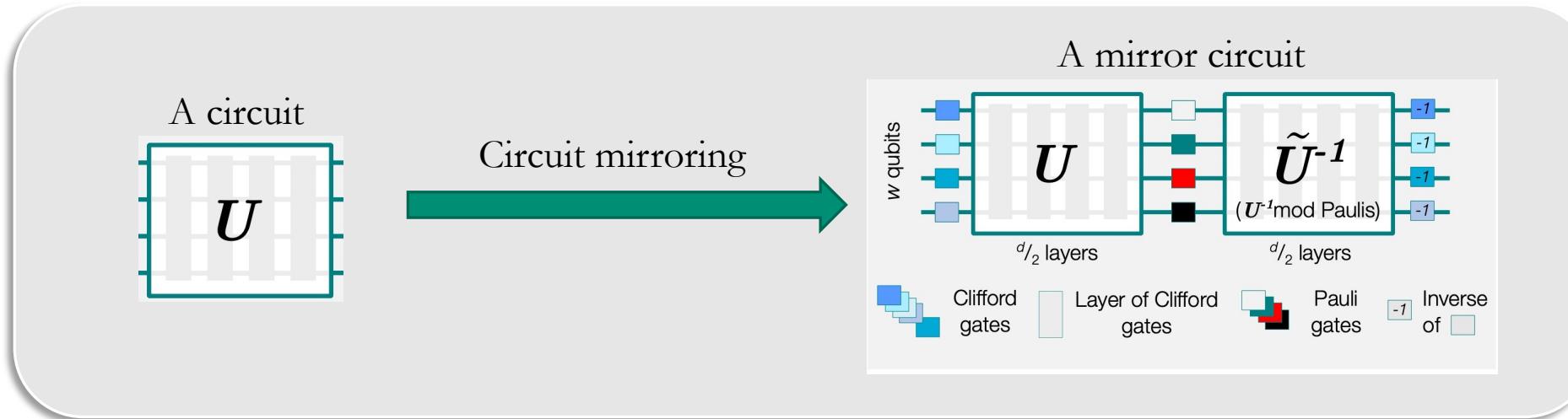
Minor tweaks to the inversion layers (“quasi-inverse” layers)

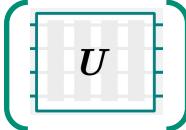
These circuit’s success probabilities
are related to fidelity of C !

Creating scalable and flexible benchmarks using mirror circuits

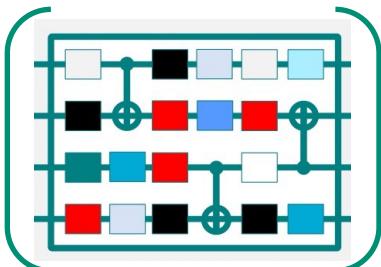


Circuit mirroring is a mapping that needs input circuit(s) to create a benchmark.



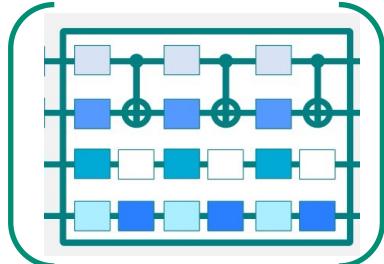
What circuits  create useful benchmarks?

- Randomized, unstructured circuits



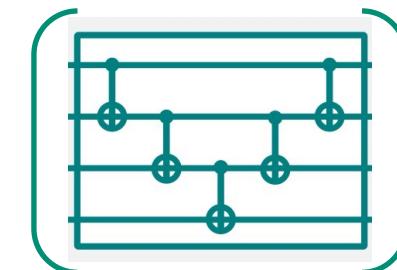
Generic benchmarks

- Repetitive error-amplifying circuits



Application-specific benchmarks

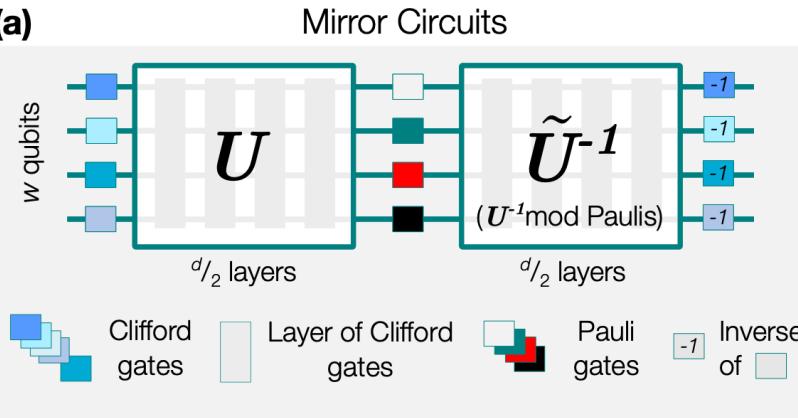
- An algorithm's circuit(s).



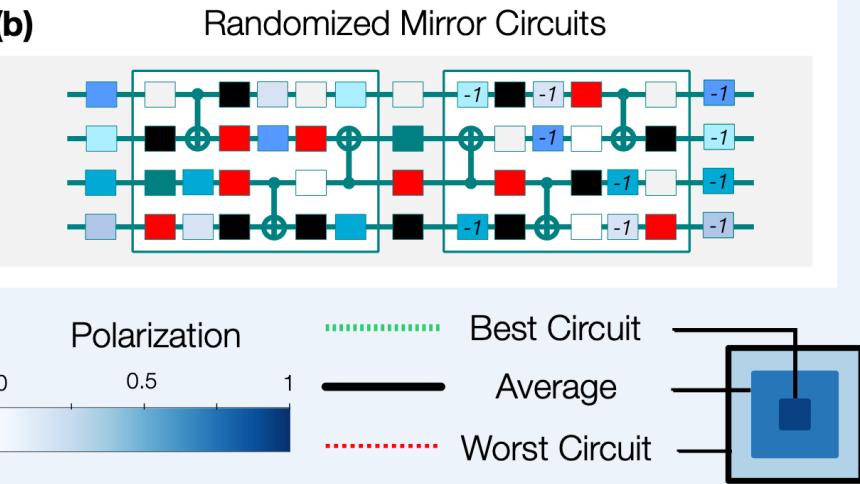
Experimental demo

Benchmarking 12 publicly accessible processors with randomized mirror circuits.

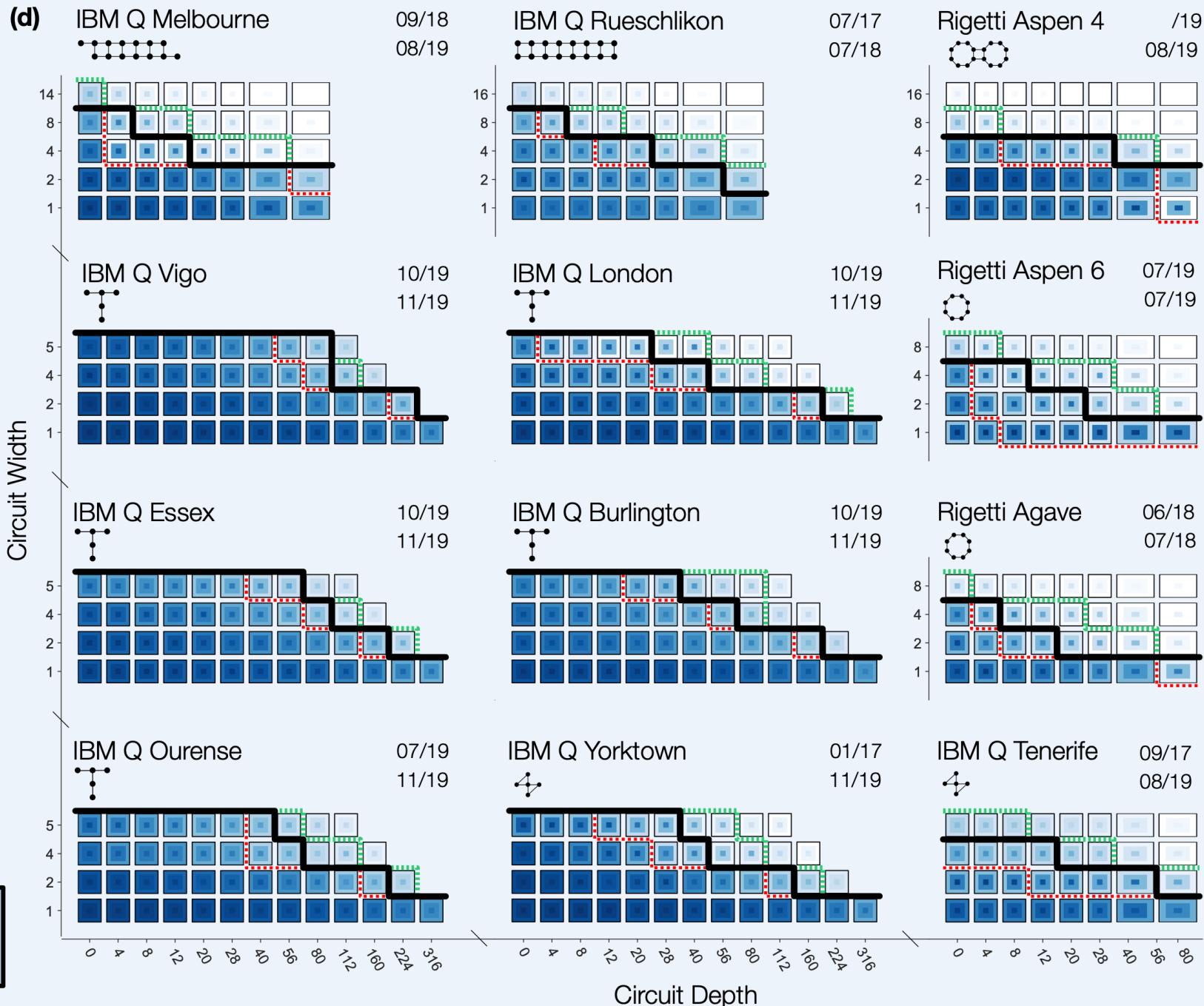
(a)



(b)



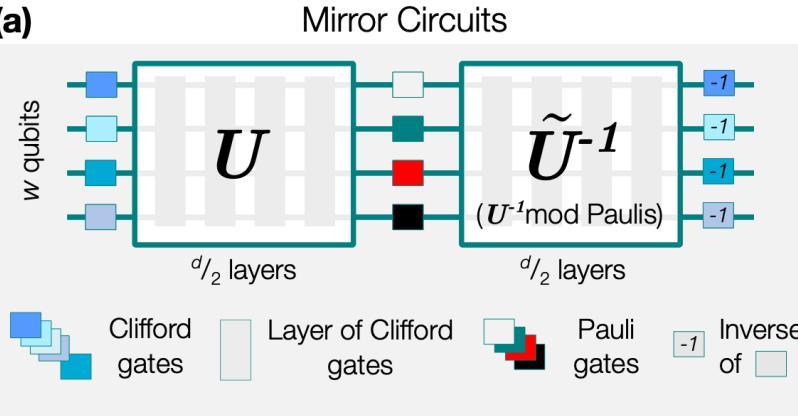
(d)



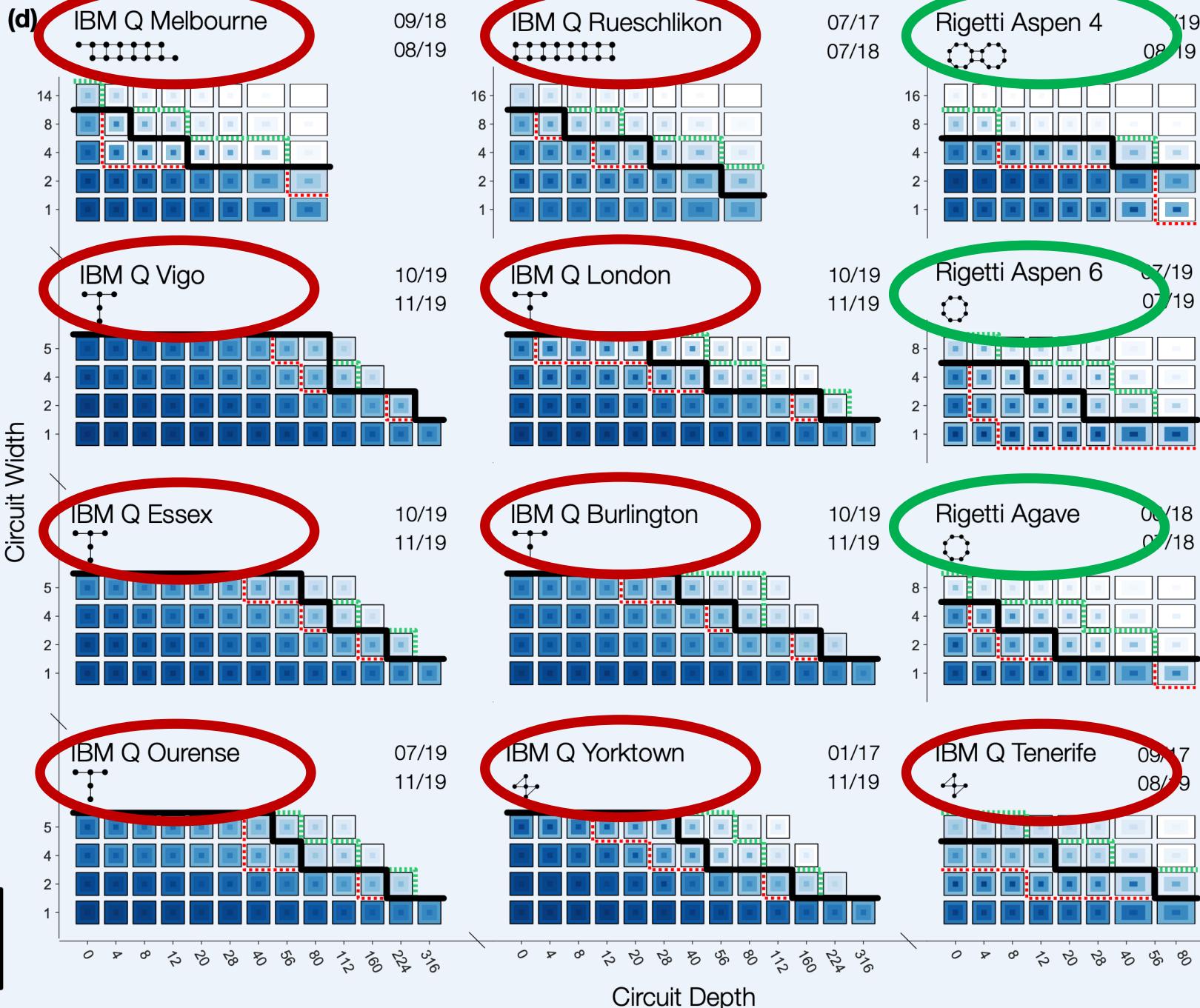
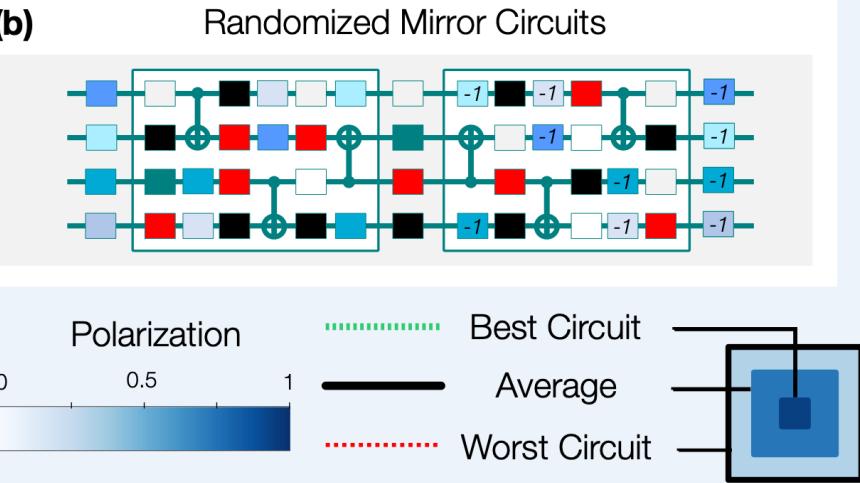
Experimental demo

The processors are from **IBM** and **Rigetti Computing**.

(a)



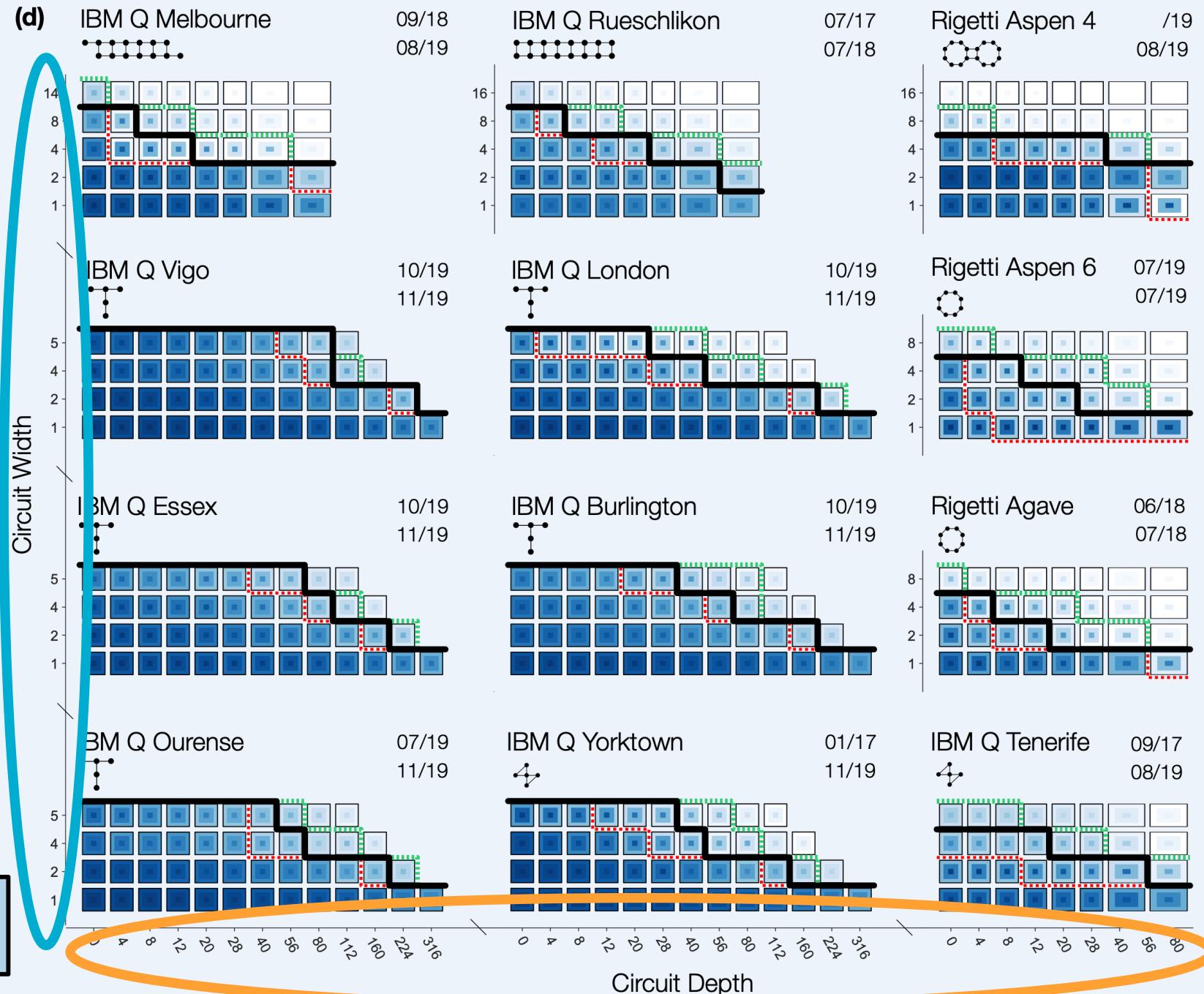
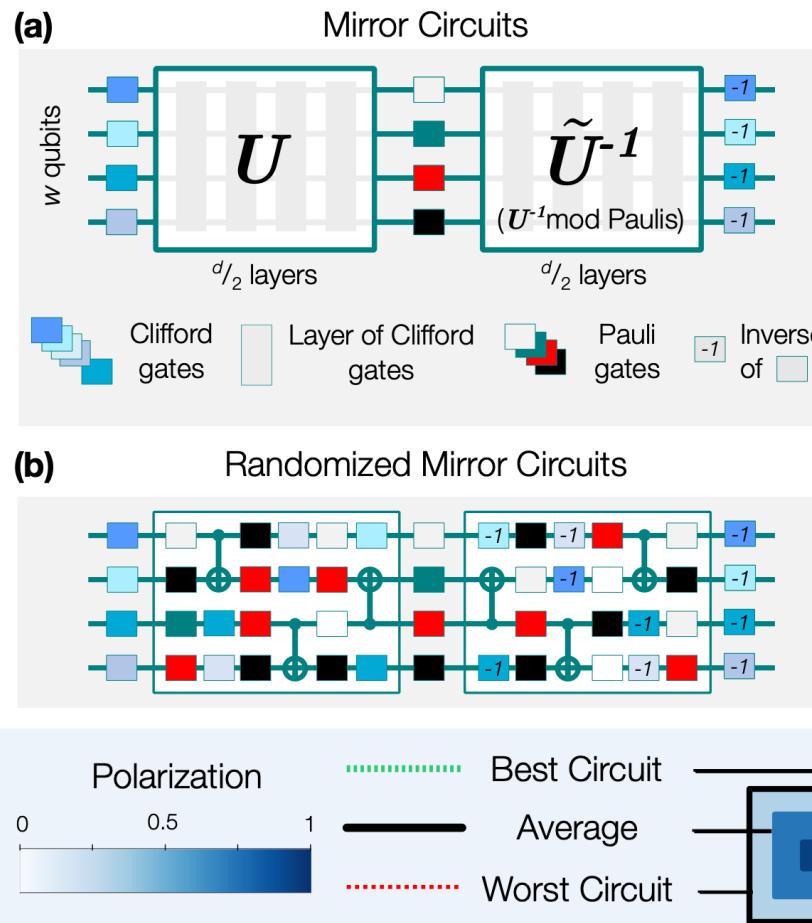
(b)



Experimental demo

We ran varied width and depth randomized mirror circuits, with approximately exponentially spaced **widths** and **depths**.

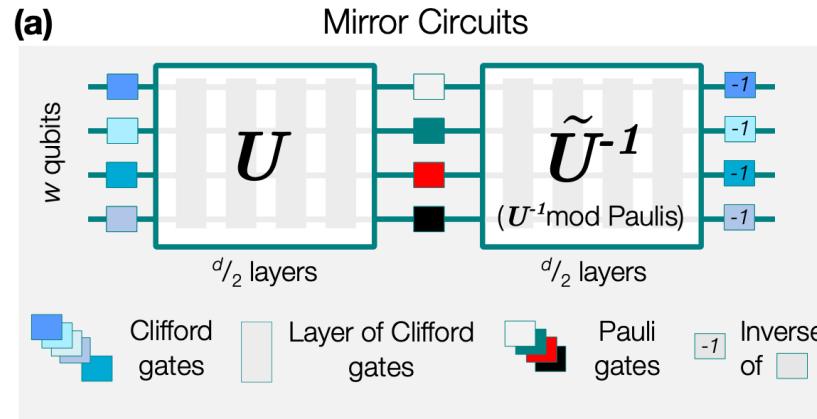
This is volumetric benchmarking.



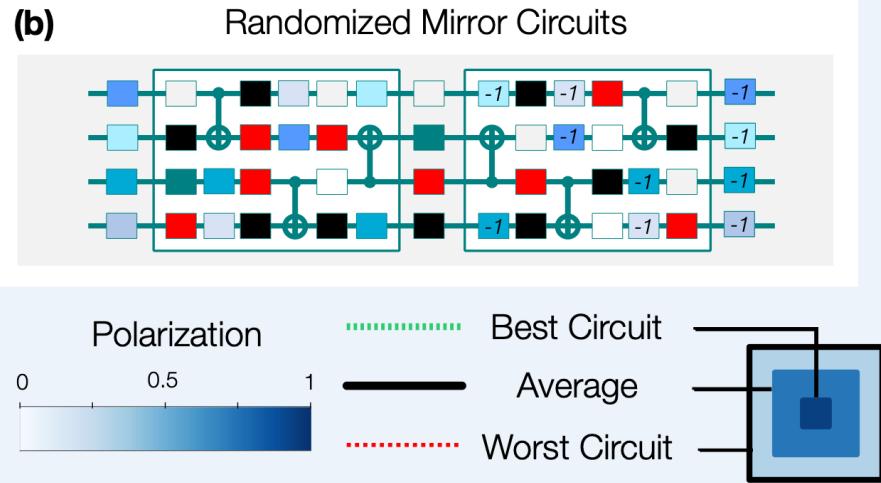
Experimental demo

At each (width, depth) pair we sampled 40 randomized mirror circuits, and we ran each one ~ 1000 times.

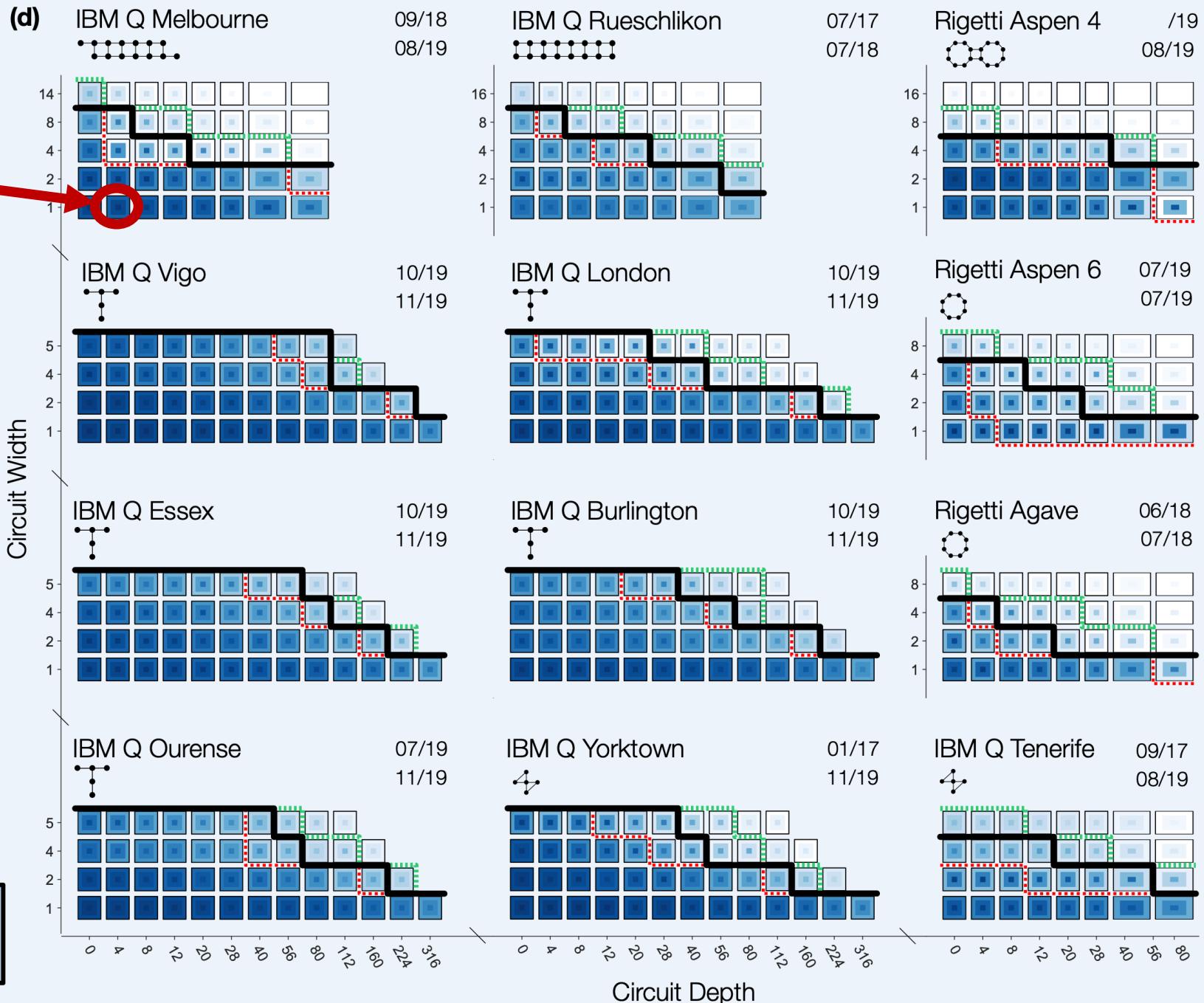
(a)



(b)

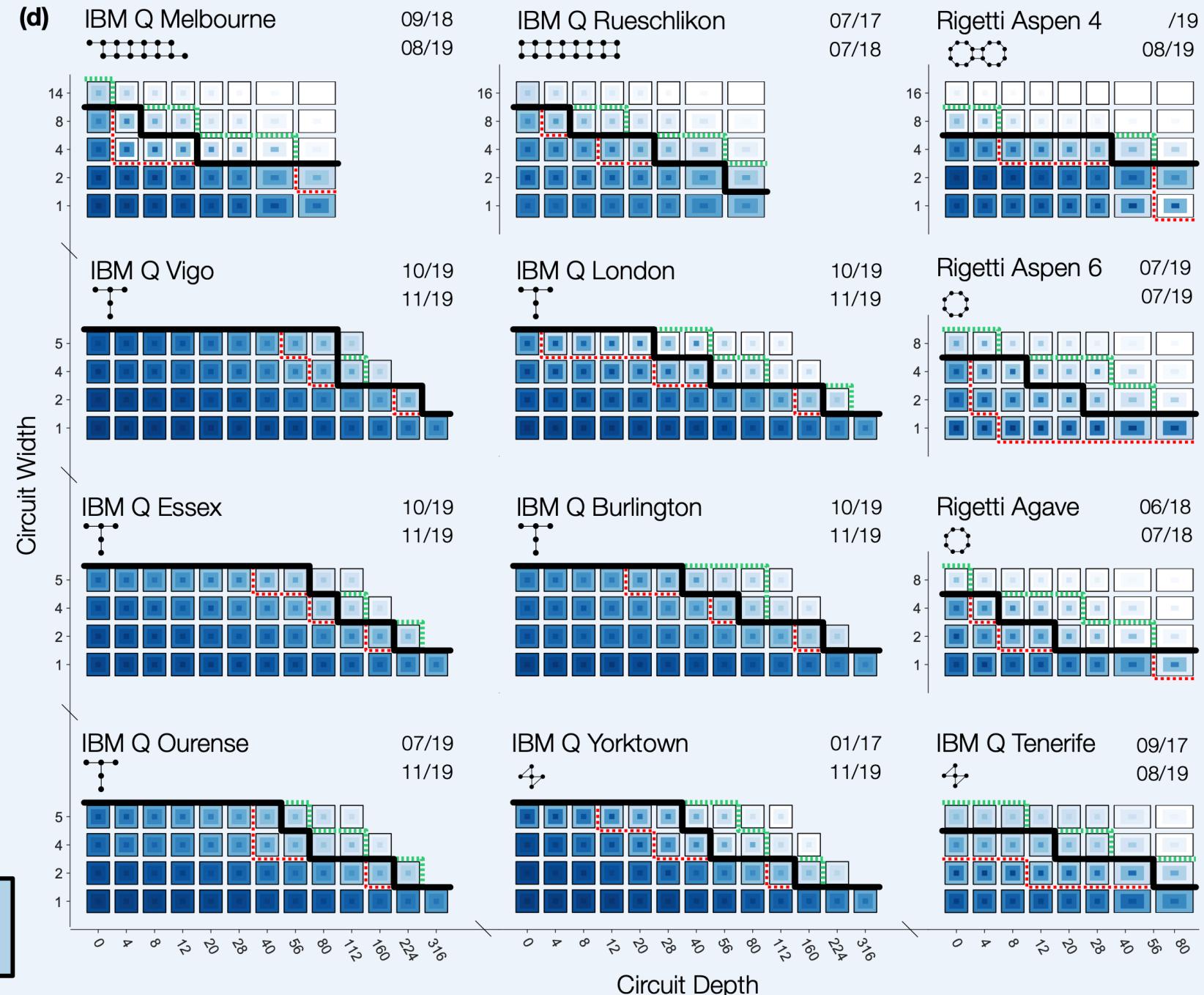
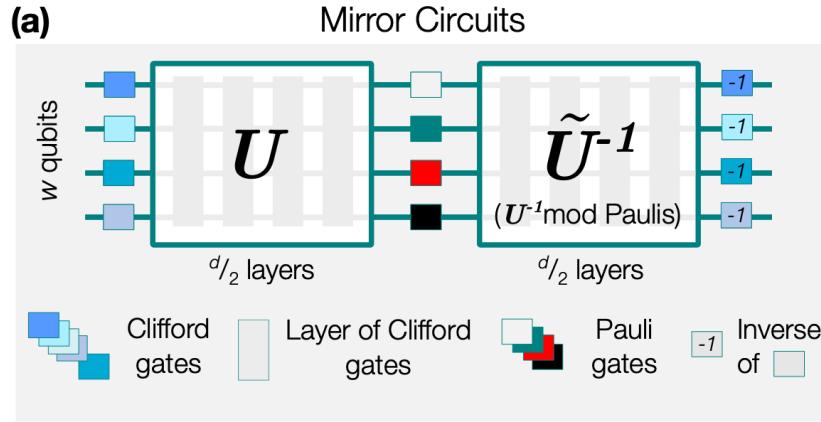


(d)



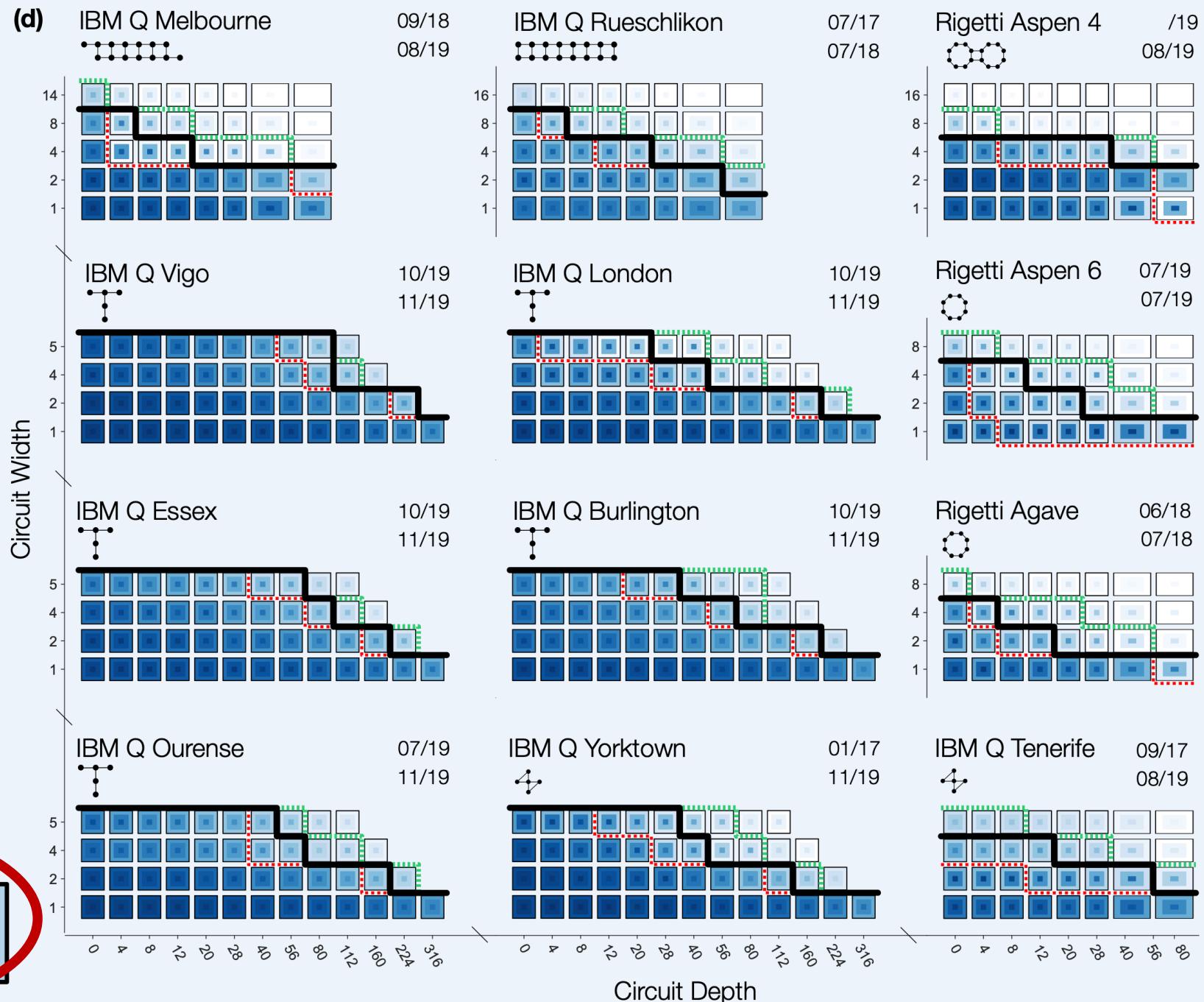
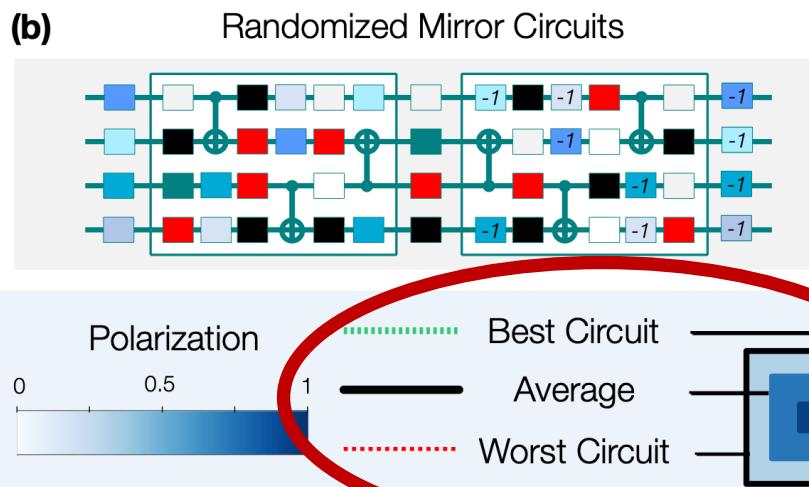
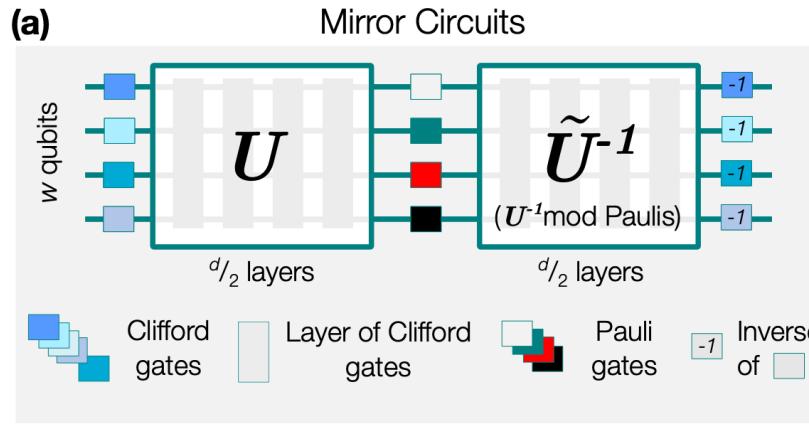
Experimental demo

We summarize performance via
 “polarization” = $(P - \frac{1}{2}^w) / (1 - \frac{1}{2}^w)$ where
 P is the probability that the correct bit-
 string is output by circuit, and w is its
 width.



Experimental demo

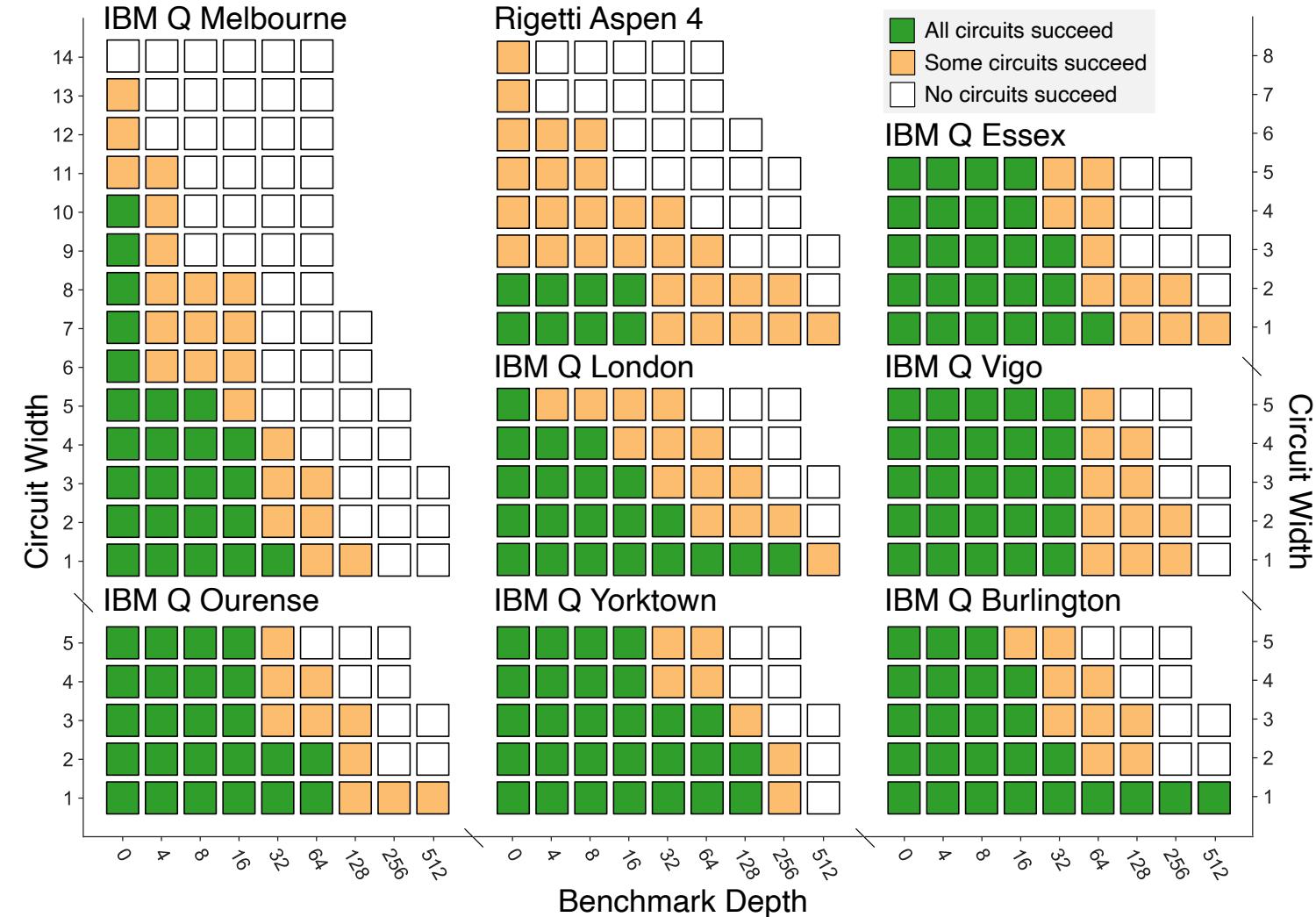
We plot data for the best and worst performing of the 40 circuits – at each width and depth – as well as the mean performance.



Capability regions

- The regions shown here include those circuit shapes where **all** / **some** / **none** of the test circuits within it succeeded with a polarization of at least $1/e$.
- This can be thought of as a simple representation of the capability function

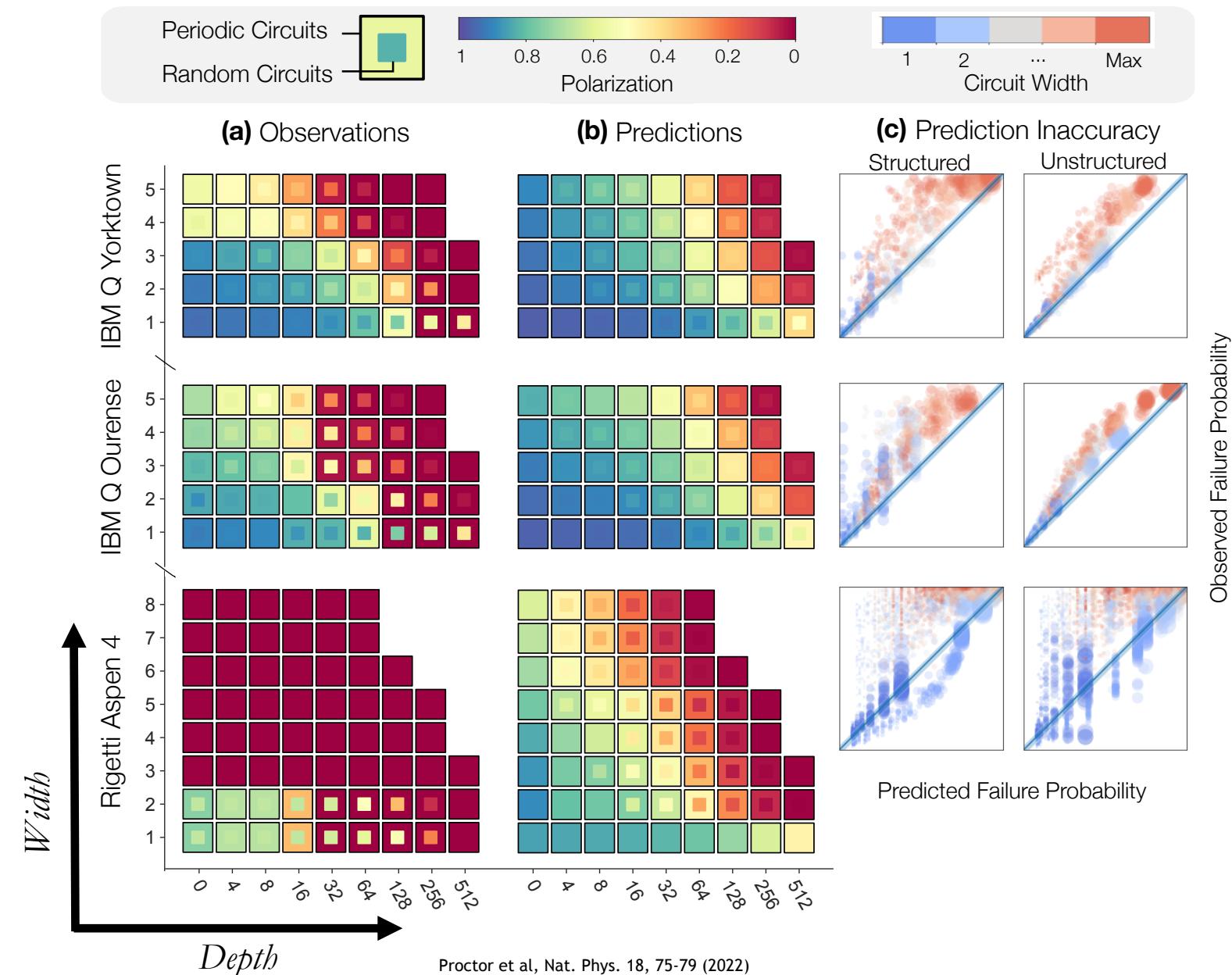
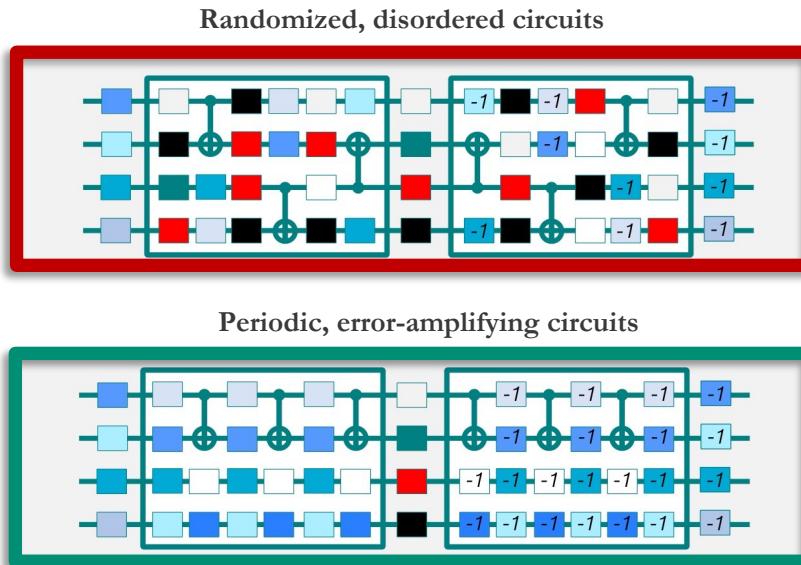
$$f \left(\begin{array}{c} \text{Circuit Shape} \end{array} \right)$$



Do we need anything other than randomized benchmarks? Yes!



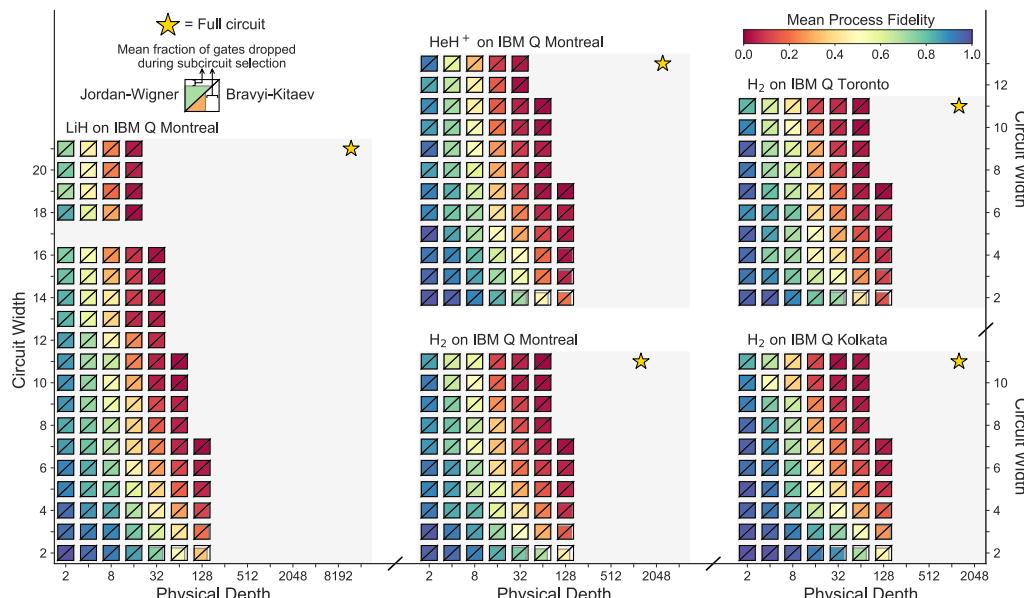
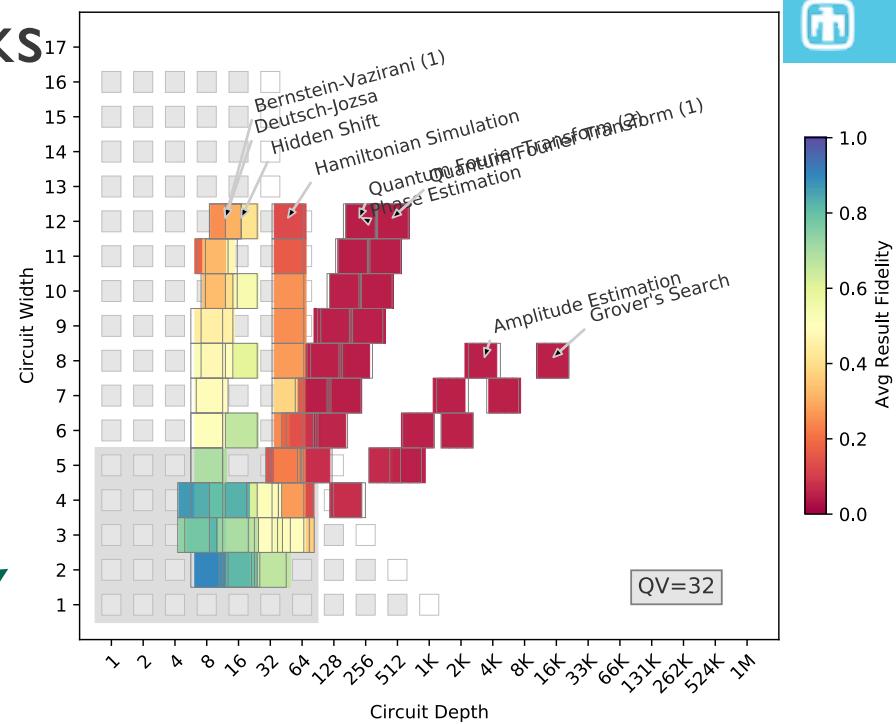
- Performance is typically **much** worse for periodic circuits!
- This is a symptom of **structured errors** that *cannot* be modelled by standard error rates.





Algorithmic benchmarks

- Randomized benchmarks often won't predict other kinds of circuit.
- We need bespoke, application-specific benchmarks.
- There's a growing array of algorithmic benchmarking suites (e.g., the QED-C benchmarks¹).
- Turning an algorithm into a benchmark is non-trivial:
 - Algorithms often have a lot of tunable “parameters”, e.g., the problem instance.
 - Naïve benchmarks (just run the algorithms circuits) are often exponentially expensive to implement – solutions: mirror-circuit based methods² (for general circuits) and trap circuits³ (for randomly compiled circuits).
 - Simple algorithmic benchmarks don't measure progress towards fault-tolerant implementations of algorithms.



How do I run these benchmarks?

Quantum volume

Open source implementation in QisKit:

<https://qiskit.org/textbook/ch-quantum-hardware/measuring-quantum-volume.html>

Volumetric benchmarking & mirror circuit benchmarks

Open source implementation in pyGSTi with a QisKit interface:

<https://github.com/pyGSTi/pyGSTi>

pyGSTi repo contains Jupyter Notebook tutorials!

https://github.com/pyGSTi/pyGSTi/blob/master/jupyter_notebooks/Tutorials/algorithms/MirrorCircuitBenchmarks.ipynb

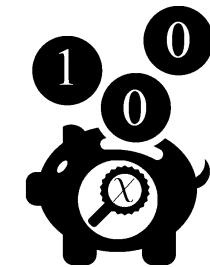
Algorithmic benchmarks

There are many different algorithmic benchmarking suites!

QED-C benchmarking suite: <https://github.com/SRI-International/QC-App-Oriented-Benchmarks>

You can create scalable algorithm benchmarks using mirror circuits via pyGSTi. See:

<https://zenodo.org/record/6617686>



Outline

1. Holistic benchmarking

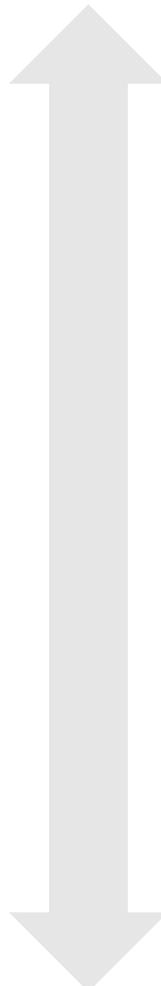
- Volumetric benchmarking
- Algorithmic benchmarks

Many methods sit between these two extremes

- One/two-qubit RB
- Cycle benchmarking
- Pauli noise learning
-

2. Detailed error characterization

- State and process tomography
- Gate set tomography



High-level performance assessment

Aims to answer questions like:

- What's this device's failure rate when running many-qubit circuits?
- What algorithms can this device run?
- Is device X or device Y better?

Low-level performance assessment

Aims to answer questions like:

- What kinds of errors are occurring?
- What's the error rate of each kind of fundamental error on each gate?
- What's the process fidelity of this gate?

Standard tomography: state, process, and measurement tomography

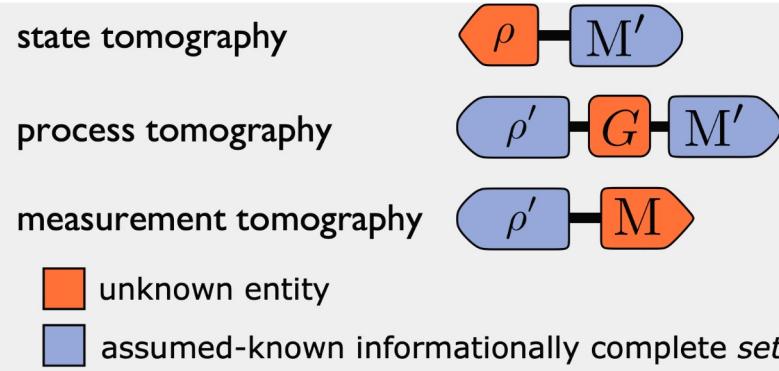


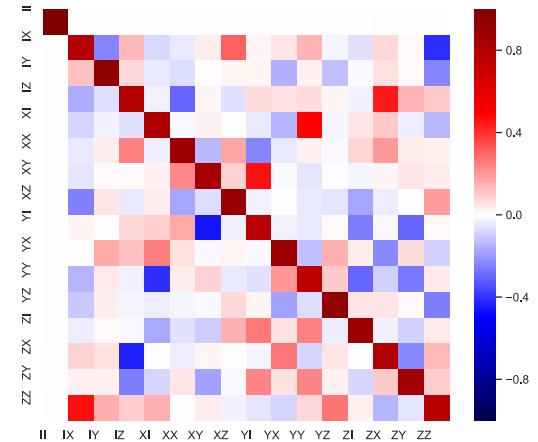
Figure 2: Structure of the circuits required for state, process, and measurement tomography. Each of these protocols reconstructs an unknown entity (a state ρ , process G , or measurement M) by placing that entity in circuits with an assumed-known reference frame formed by an informationally complete set of state preparations or measurements (or both). Primed symbols (ρ' and M') are meant to connote effective state preparations and measurements, which are often implemented by applying gate operations after or before a native state preparation or measurement. A critical problem with these standard tomographic techniques is that ρ' and M' are in practice never known exactly.

Nielsen et al, Quantum 5, 557 (2021)

- Tomography means learning all the elements of a vector (state tomography) or matrix (process tomography).

The normalized Pauli operators

$$E_{ij} = \text{Tr}(P_j E[P_i])$$



- This just requires taking inner products with a known basis, and then applying a matrix inverse.
- This means using *informationally complete* (IC) measurements for state tomography, and IC state preparations and measurements for process tomography.

But there's a critical problem: pre-calibrated reference frames don't really exist!

Gate set tomography – tomography without pre-calibration



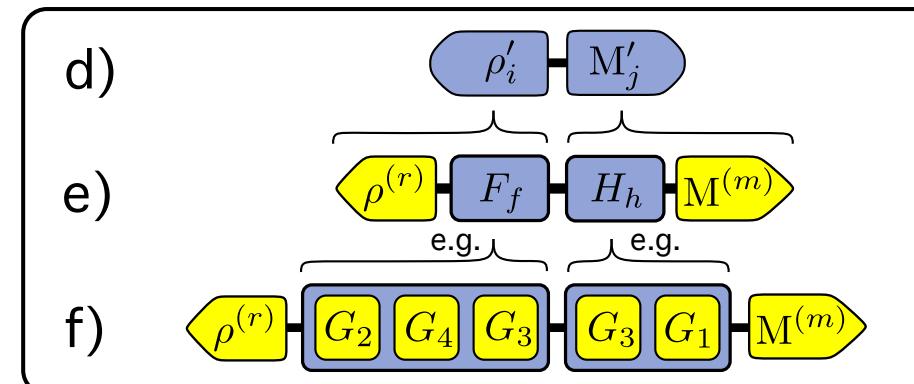
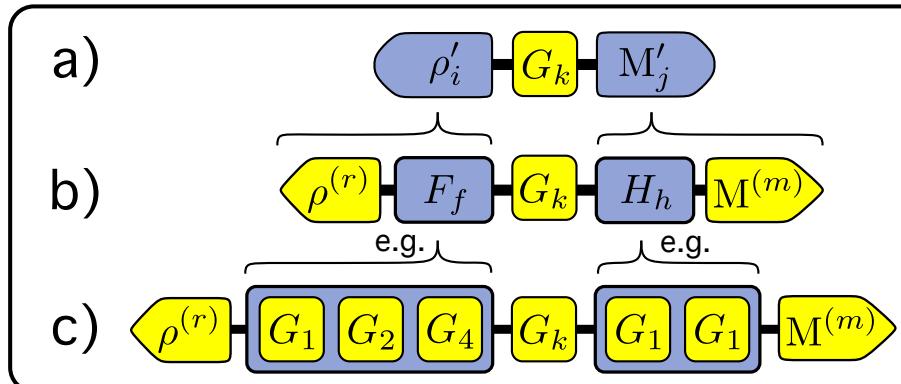
GST estimates all the elements of a *gate set*:

$$\mathcal{G} = \left\{ \left\{ |\rho^{(i)}\rangle\rangle\right\}_{i=1}^{N_\rho}; \{G_i\}_{i=1}^{N_G}; \left\{ \langle\langle E_i^{(m)} | \right\}_{m=1, i=1}^{N_M, N_E^{(m)}} \right\}.$$

It does so up to a fundamental gauge freedom:

$$\begin{aligned} \langle\langle E_i^{(m)} | &\rightarrow \langle\langle E_i^{(m)} | M^{-1} \\ |\rho^{(i)}\rangle\rangle &\rightarrow M|\rho^{(i)}\rangle\rangle \\ G_i &\rightarrow MG_iM^{-1}. \end{aligned}$$

Linear gate set tomography



Process tomography experiments

Reference frame experiments

Gate set tomography – tomography without pre-calibration



GST estimates all the elements of a *gate set*:

$$\mathcal{G} = \left\{ \left\{ |\rho^{(i)}\rangle\rangle\right\}_{i=1}^{N_\rho}; \{G_i\}_{i=1}^{N_G}; \left\{ \langle\langle E_i^{(m)}| \right\}_{m=1, i=1}^{N_M, N_E^{(m)}} \right\}.$$

It does so up to a fundamental gauge freedom:

$$\begin{aligned} \langle\langle E_i^{(m)}| &\rightarrow \langle\langle E_i^{(m)}| M^{-1} \\ |\rho^{(i)}\rangle\rangle &\rightarrow M |\rho^{(i)}\rangle\rangle \\ G_i &\rightarrow M G_i M^{-1}. \end{aligned}$$

Repeating “germs” enables Heisenberg-like estimation error!

Long-sequence gate set tomography

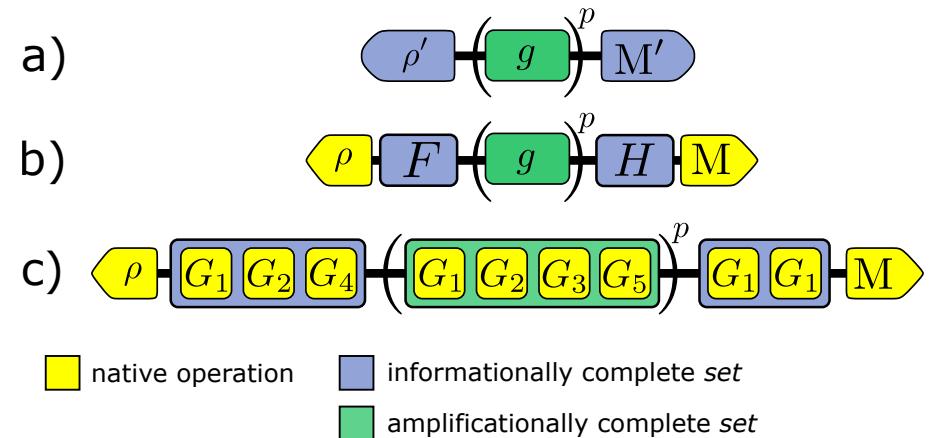


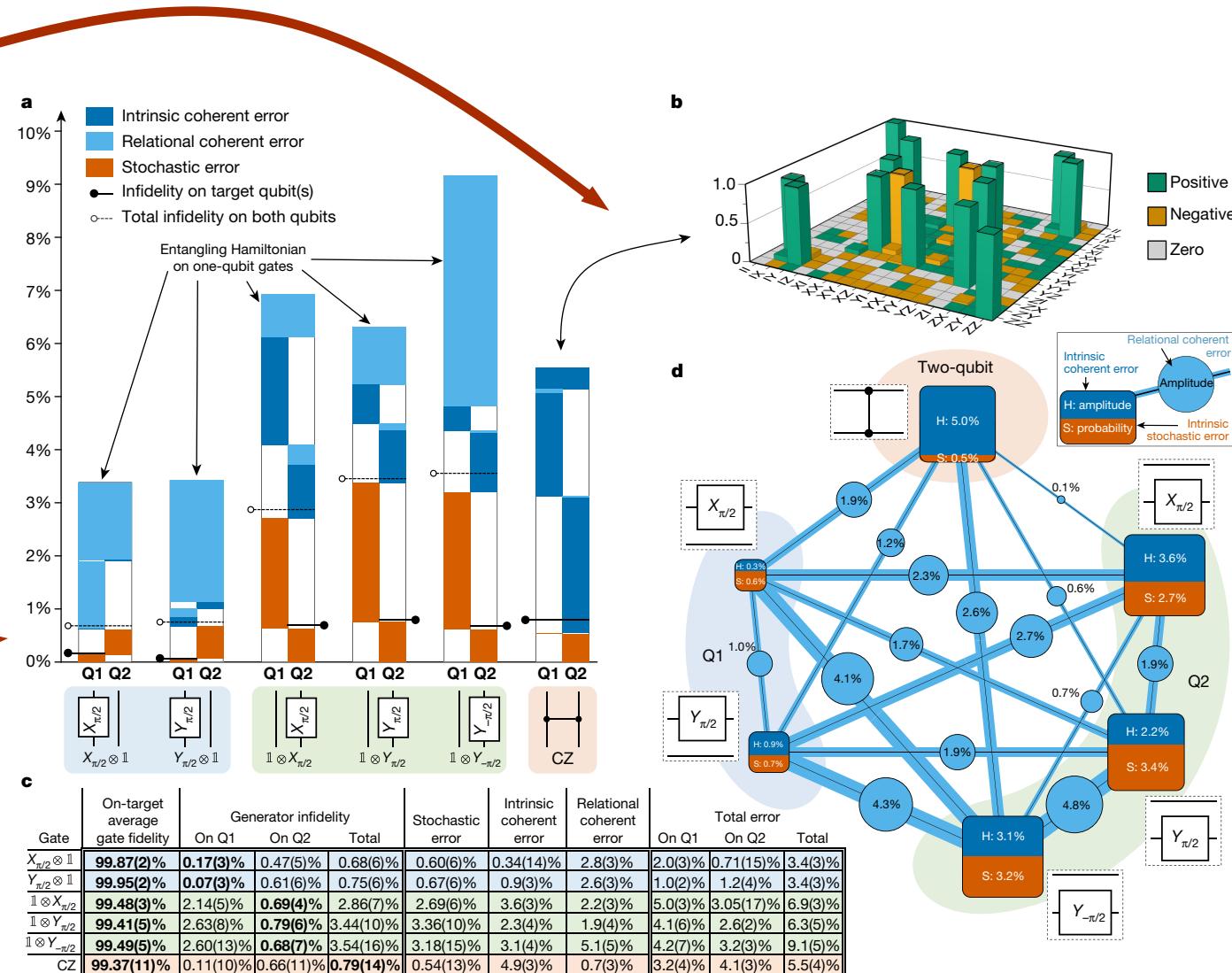
Figure 4: The structure of circuits in the standard GST experiment design, shown in increasing detail. **(a)** Each GST circuit consists of an effective state preparation ρ' (Eq. 52), followed by a *germ* circuit g repeated p times, followed by an effective measurement $M' = \{E'_i\}$ (Eq. 51). **(b)** Effective preparations are often implemented by a native state preparation ρ followed by a *preparation fiducial circuit* F , and similarly effective measurements are often implemented by *measurement fiducial circuit* H followed by a native measurement M . **(c)** Writing the fiducials and germ in terms of native gate operations reveals how the native operations of a gate set compose to form a GST circuit.

Process matrices are mysterious! How can we extract meaning from GST results?

Impenetrable process matrices can be turned into rates for each kind of a set of elementary error processes

| Sector | Dimension | Action | Example effect (Bloch sphere) | ϵ_J (Error Probability) | θ_J (Error Amplitude) |
|--------------------------------|--------------|-----------------------------------------------------------------------|-------------------------------|----------------------------------|------------------------------|
| Hamiltonian | \mathbb{H} | $H_P[\rho] = -i[P, \rho]$ | | 0 | 1 |
| Stochastic (Pauli) | \mathbb{S} | $S_P[\rho] = P\rho P - \mathbb{1}\rho\mathbb{1}$ | | 1 | 0 |
| Stochastic (Pauli-correlation) | $\{P, Q\}=0$ | $C_{P, Q}[\rho] = P\rho Q + Q\rho P - \frac{1}{2}\{[P, Q], \rho\}$ | | 0 | 0 |
| | $\{P, Q\}=0$ | $A_{P, Q}[\rho] = i(P\rho Q - Q\rho P + \frac{1}{2}\{[P, Q], \rho\})$ | | 0 | 1 |
| Active | $\{P, Q\}=0$ | $(d^2 - 1) \choose 2$ | | 0 | 0 |
| | $\{P, Q\}=0$ | $(d^2 - 1) \choose 2$ | | 0 | 0 |

Blume-Kohout et al., PRX Quantum 3, 020335 (2022)



This enables dividing the total error in a gate into different kinds of error – e.g., the coherent error on qubit 1.

How do I run GST?



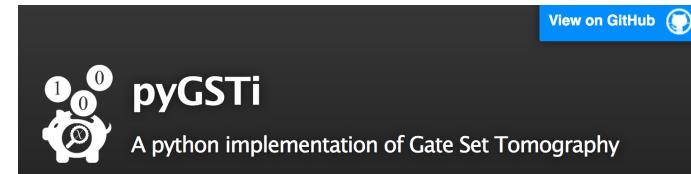
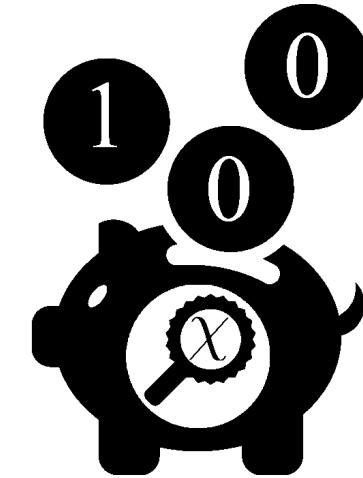
One- and two-qubit GST

Open source implementation in pyGSTi:

<https://github.com/pyGSTi/pyGSTi>

pyGSTi repo contains Jupyter Notebook tutorials!

https://github.com/pyGSTi/pyGSTi/blob/master/jupyter_notebooks/Tutorials/algorithms/GST-Overview.ipynb



Many-qubit GST

GST on many qubits is an in-development technique!

Thanks!



<https://qpl.sandia.gov/>

At the QPL we spend our time developing, understanding and using QCVV+ techniques – from benchmarks to GST and beyond – and we collaborate with experimentalists across the world to understand cutting-edge hardware.

The QPL is hiring postdocs!

So if you're excited to work on QCVV+ research now or in the future please get in touch.

tjproct@sandia.gov

This work was funded in part by Sandia's Laboratory Directed Research and Development program. This material was funded in part by the U.S. Department of Energy, Office of Science, Office of Advanced Scientific Computing Research Quantum Testbed Program. All statements of fact, opinion or conclusions contained herein are those of the authors and should not be construed as representing the official views or policies of the U.S. Government. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.