



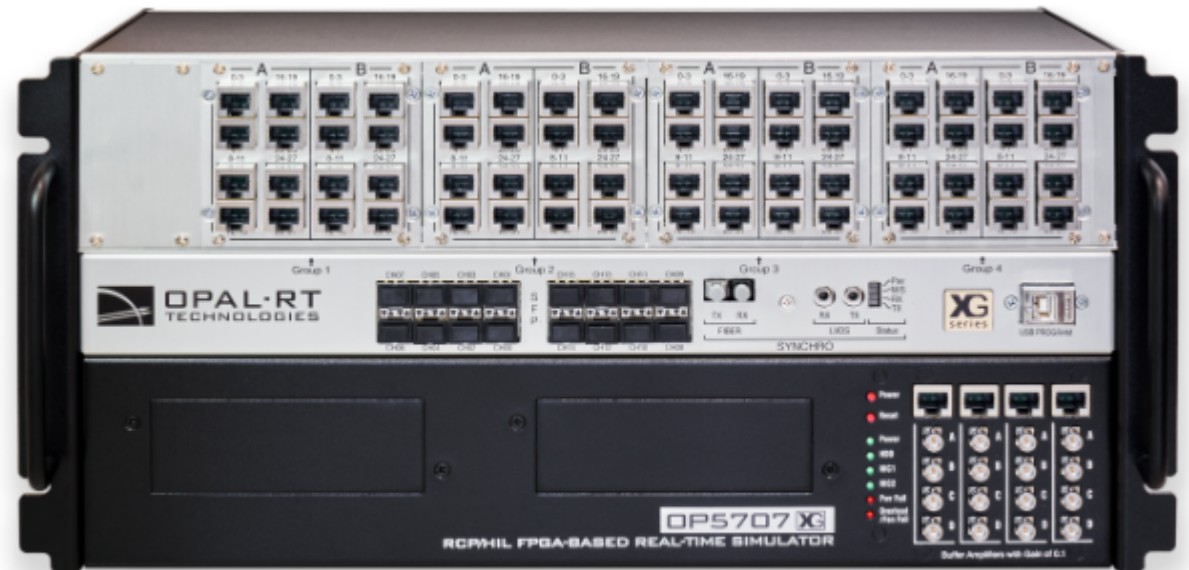
Streamlined Real-Time Model Development for the OPAL-RT Platform Using SwAGSM

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R&D S&E Electrical Engineer

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Sandia National Laboratories

INTRODUCTION: REAL-TIME MODELING

- Real-time modeling allows for an engineer to test controllers and interact with a system as it would operate in the real world.
- Additionally, models which run rather slowly may be easily parallelized on the OPAL-RT platform to allow for faster computation time for more complex systems.



COMPLICATIONS TO REAL-TIME MODEL DEVELOPMENT

Development Time

- Developing OPAL-RT Models involves manually developing Simulink Models
 - Potential for human error during development process
- For large models, Simulink's drag-and-drop interface can be time consuming to utilize.
- Models which run offline may not be immediately compatible with the OPAL-RT platform

All of these can result in additional time spent manually developing and debugging models to run on the OPAL-RT platform.

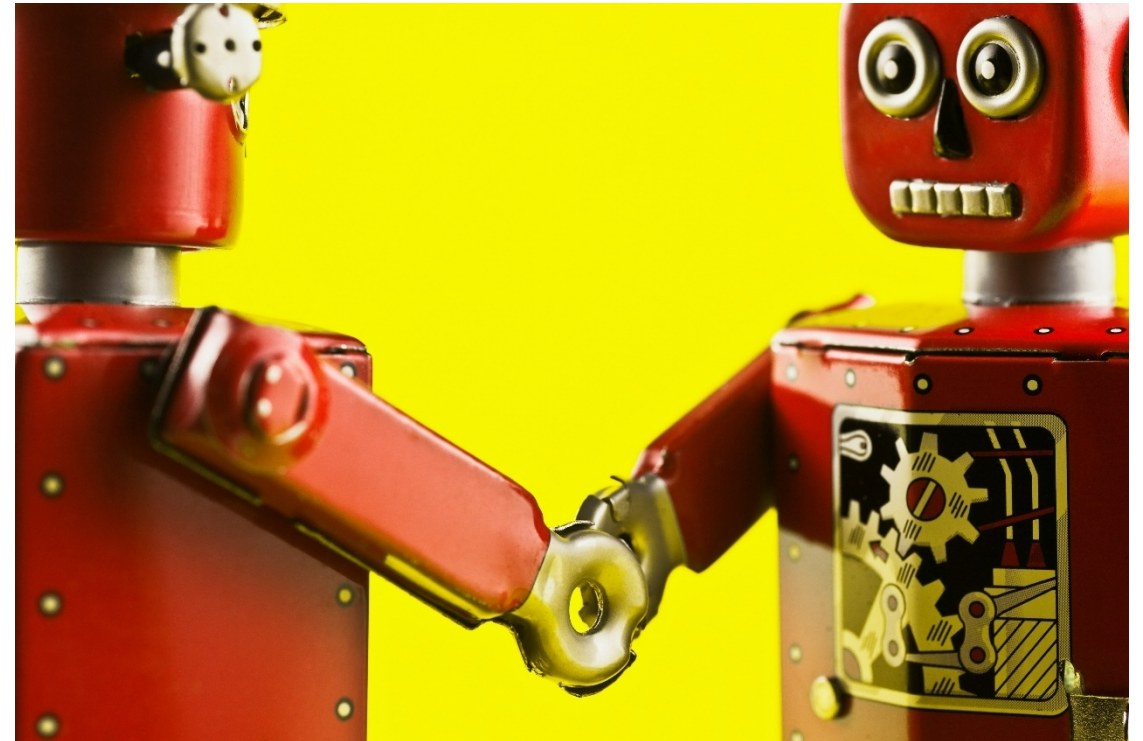


COMPLICATIONS TO REAL-TIME MODEL DEVELOPMENT

Collaboration

- Partners may not have the same number of cores available.
 - Tune all models to operate for whoever has the lowest number of cores available
 - Manually create multiple version of the same model based on the number of cores available to each collaborator

Neither of these choices is optimal. The first option is a waste of resources and the second option is a waste of labor efforts.



PROPOSED SOLUTION: MODEL AUTOMATION

- Skip the drag-and-drop interface
- Skip the Debugging
- Develop models independent of core availability
- Guarantee model is OPAL-RT ready from the start

But How?



SOFTWARE FOR AUTOMATIC GENERATION OF SIMULINK MODELS

Proposed Tool: SwAGSM (**S**oftware for **A**utomatic **G**eneration of **S**imulink **M**odels)

- Requires minimal knowledge of MATLAB/Simulink
- Does not require use of drag-and-drop interface to create OPAL-RT models
- Automatically generated models from Excel Spreadsheets
- Allows for the model core count to be adjusted on-the-fly
 - Simply edit a few values in a spreadsheet.
- No debugging required
- Models automatically formatted to immediately load to OPAL-RT platform.

SOFTWARE FOR AUTOMATIC GENERATION OF SIMULINK MODELS

- SwAGSM is current being utilized at Sandia National Laboratories to aid in the development of electric ship models for NSWC
- In the remainder of this presentation, examples utilized will be those relevant to the electric ship modeling efforts currently in progress.



Image courtesy of Naval Sea System Command (NAVSEA).
<https://www.navsea.navy.mil/Home/Team-Ships/PEO-Ships/DDG-51/>

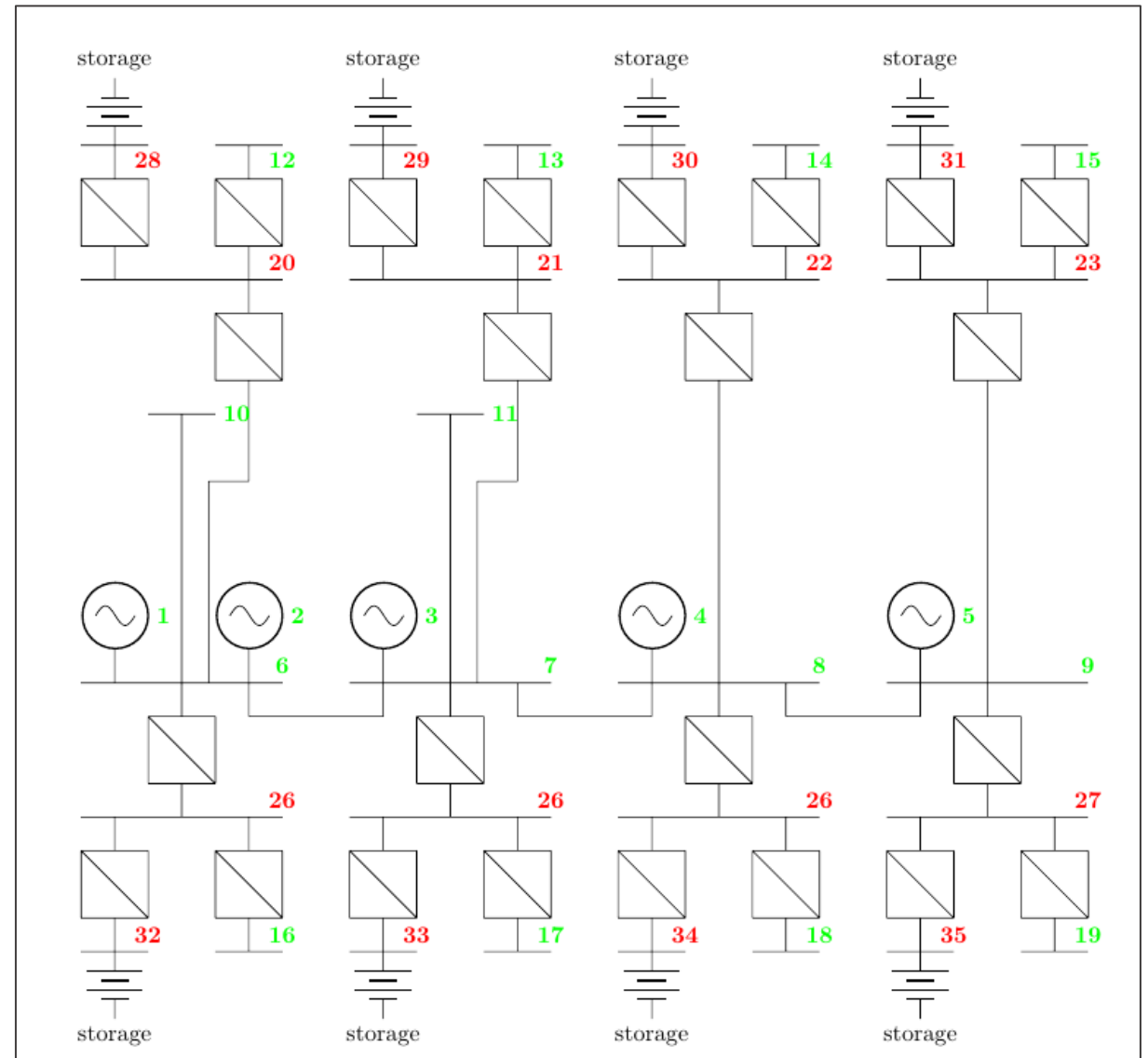
HOW DOES SWAGSM WORK?

- There is no model initially
- Library components are called by MATLAB script
 - System parameters fully defined in Excel Spreadsheet
- The steps as follows
 1. Edit and save spreadsheet
 2. Run script
 1. A new blank Simulink model is automatically opened and populated with requested components
 3. Save model and load to OPAL-RT as normal

EXAMPLE

Consider the generic shipboard network to the right

- The parameters are defined on the preceding slides as
- 3-phase AC buses are labeled in green
- DC buses are labeled in red



BUS PARAMETERS

Available Options:

- 3-phase ac generator
- PV-array
- Battery
- Capacitor

	Q	P
type	delmin	
3-phase ac generator		
1-phase ac generator		
3-phase ac generator		
pv array		
battery		
capacitor		
capacitor (IM)		

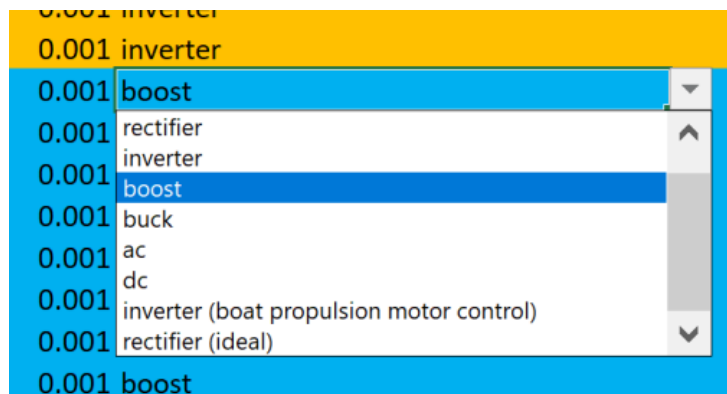
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1	core	bus	ac or dc	C(uF)	active (W)	reactive (VAR)	Vbase	Vmin	Vmax	Pmin	Pmax	Qmin	Qmax	objective	type
2	1	1	ac	0	0	0	3983.717	3784.531	4182.903	0	50000000	-50000000	50000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generat
3	2	2	ac	0	0	0	3983.717	3784.531	4182.903	0	50000000	-50000000	50000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generat
4	1	3	ac	0	0	0	3983.717	3784.531	4182.903	0	10000000	-10000000	10000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generat
5	2	4	ac	0	0	0	3983.717	3784.531	4182.903	0	10000000	-10000000	10000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generat
6	1	5	ac	0	0	0	3983.717	3784.531	4182.903	0	10000000	-10000000	10000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generat
7	2	6	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
8	1	7	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
9	2	8	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
10	1	9	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
11	2	10	ac	1000	18000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
12	1	11	ac	1000	18000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
13	2	12	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
14	1	13	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
15	2	14	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
16	1	15	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
17	2	16	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
18	1	17	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
19	2	18	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
20	1	19	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0		capacitor
21	2	20	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
22	1	21	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
23	2	22	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
24	1	23	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
25	2	24	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
26	1	25	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
27	2	26	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
28	1	27	dc	16000	1000000	0	12000	11400	12600	0	0	0	0		capacitor
29	2	28	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
30	1	29	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
31	2	30	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
32	1	31	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
33	2	32	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
34	1	33	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
35	2	34	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
36	1	35	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery

Core defined in Col A

LINE PARAMETERS

Available Options:

- AC lines
- DC lines
- Buck Converters
- Boost Converters
- 3-phase inverters
- 3-phase rectifiers



	A	B	C	D	E	F	G	H	I	J
1	line no.	from	to	R(ohms)	L(H)	type	ac/dc #	dc/dc #	kp	ki
2	1	1	6	0.1	0.0001	ac			0	0
3	2	2	6	0.1	0.0001	ac			0	0
4	3	3	7	0.1	0.0001	ac			0	0
5	4	4	8	0.1	0.0001	ac			0	0
6	5	5	9	0.1	0.0001	ac			0	0
7	6	6	7	0.1	0.0001	ac			0	0
8	7	7	8	0.1	0.0001	ac			0	0
9	8	8	9	0.1	0.0001	ac			0	0
10	9	6	10	0.1	0.0001	ac			0	0
11	10	8	11	0.1	0.0001	ac			0	0
12	11	6	20	0.01	0.001	rectifier	1		0	0
13	12	7	21	0.01	0.001	rectifier	2		0	0
14	13	8	22	0.01	0.001	rectifier	3		0	0
15	14	9	23	0.01	0.001	rectifier	4		0	0
16	15	6	24	0.01	0.001	rectifier	5		0	0
17	16	7	25	0.01	0.001	rectifier	6		0	0
18	17	8	26	0.01	0.001	rectifier	7		0	0
19	18	9	27	0.01	0.001	rectifier	8		0	0
20	19	20	12	0.01	0.001	inverter	9		0	0
21	20	21	13	0.01	0.001	inverter	10		0	0
22	21	22	14	0.01	0.001	inverter	11		0	0
23	22	23	15	0.01	0.001	inverter	12		0	0
24	23	24	16	0.01	0.001	inverter	13		0	0
25	24	25	17	0.01	0.001	inverter	14		0	0
26	25	26	18	0.01	0.001	inverter	15		0	0
27	26	27	19	0.01	0.001	inverter	16		0	0
28	27	28	20	0.01	0.001	boost		1	0	0
29	28	29	21	0.01	0.001	boost		2	0	0
30	29	30	22	0.01	0.001	boost		3	0	0
31	30	31	23	0.01	0.001	boost		4	0	0
32	31	32	24	0.01	0.001	boost		5	0	0
33	32	33	25	0.01	0.001	boost		6	0	0
34	33	34	26	0.01	0.001	boost		7	0	0
35	34	35	27	0.01	0.001	boost		8	0	0

Model Parameters

Bus Data

Line Connections

Diesel Gen

Model Parameters

Bus Data

Line Connections

Diesel Gen

COMPONENT PARAMETERS

- Component parameters defined by sheets of spreadsheet
- Automatically placed based on core locations defined in “Bus Parameters” sheet

	A	B	C	D	E	F
1	bus	type	Vnom(V)	Ah rating	effic.(%)	SOC(0)
2	28	Li-Ion	3000	300000	99.5	0.8
3	29	Li-Ion	3000	300000	99.5	0.8
4	30	Li-Ion	3000	300000	99.5	0.8
5	31	Li-Ion	3000	300000	99.5	0.8
6	32	Li-Ion	3000	300000	99.5	0.8
7	33	Li-Ion	3000	300000	99.5	0.8
8	34	Li-Ion	3000	300000	99.5	0.8
9	35	Li-Ion	3000	300000	99.5	0.8
10		Lead-Acid				
11		Li-Ion				
12		NiCd				
		NiMH				

Navigation: Battery Parameters ... (+) < >

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
1	ac bus	P(poles)	J	Bm(Nm.s)	Rs(ohms)	K	T1	T2	T3	T4	T5	T6	Tmin	Tmax	Td	Pm0	rated kW	kDelta
2	1	4	256.38	0.1	0.087	1	0.01	0.02	0.2	0.25	0.009	0.0384	-0.1	1.1	0.024	0.25	150000	-0.1
3	2	4	256.38	0.1	0.087	1	0.01	0.02	0.2	0.25	0.009	0.0384	-0.1	1.1	0.024	0.25	150000	-0.1
4	3	4	256.38	0.1	0.087	1	0.01	0.02	0.2	0.25	0.009	0.0384	-0.1	1.1	0.024	0.25	150000	-0.1
5	4	4	256.38	0.1	0.087	1	0.01	0.02	0.2	0.25	0.009	0.0384	-0.1	1.1	0.024	0.25	150000	-0.1
6	5	4	256.38	0.1	0.087	1	0.01	0.02	0.2	0.25	0.009	0.0384	-0.1	1.1	0.024	0.25	150000	-0.1

Navigation: Model Parameters | Bus Data | Line Connections | Diesel Generator Parameters | Gas Turb ... (+) < >

LOAD DEFINITIONS

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	A	B	C	D	E	F	G	H	I	J
1	time(s) bus									
2	1	0	29.99	30	59.99	60	89.99	90	119.99	120
3	2	0	0	0	0	0	0	0	0	0
4	3	0	0	0	0	0	0	0	0	0
5	4	0	0	0	0	0	0	0	0	0
6	5	0	0	0	0	0	0	0	0	0
7	6	1000	1000	1000	1000	1000	1000	1000	1000	1000
8	7	1000	1000	1000	1000	1000	1000	1000	1000	1000
9	8	1000	1000	1000	1000	1000	1000	1000	1000	1000
10	9	1000	1000	1000	1000	1000	1000	1000	1000	1000
11	10	18000	18000	18000	18000	18000	18000	18000	18000	18000
12	11	18000	18000	18000	18000	18000	18000	18000	18000	18000
13	12	1000	1000	1000	1000	1000	1000	1000	1000	1000
14	13	1000	1000	1000	1000	1000	1000	1000	1000	1000
15	14	1000	1000	1000	1000	1000	1000	1000	1000	1000
16	15	1000	1000	1000	1000	1000	1000	1000	1000	1000
17	16	1000	1000	1000	1000	1000	1000	1000	1000	1000
18	17	1000	1000	1000	1000	1000	1000	1000	1000	1000
19	18	1000	1000	1000	1000	1000	1000	1000	1000	1000
20	19	1000	1000	1000	1000	1000	1000	1000	1000	1000

	A	B	C	D	E	F	G	H	I	J
1	time(s) bus									
2	1	0	29.99	30	59.99	60	89.99	90	119.99	120
3	2	0	0	0	0	0	0	0	0	0
4	3	0	0	0	0	0	0	0	0	0
5	4	0	0	0	0	0	0	0	0	0
6	5	0	0	0	0	0	0	0	0	0
7	6	0	0	0	0	0	0	0	0	0
8	7	0	0	0	0	0	0	0	0	0
9	8	0	0	0	0	0	0	0	0	0
10	9	0	0	0	0	0	0	0	0	0
11	10	0	0	0	0	0	0	0	0	0
12	11	0	0	0	0	0	0	0	0	0
13	12	0	0	0	0	0	0	0	0	0
14	13	0	0	0	0	0	0	0	0	0
15	14	0	0	0	0	0	0	0	0	0
16	15	0	0	0	0	0	0	0	0	0
17	16	0	0	0	0	0	0	0	0	0
18	17	0	0	0	0	0	0	0	0	0
19	18	0	0	0	0	0	0	0	0	0
20	19	0	0	0	0	0	0	0	0	0

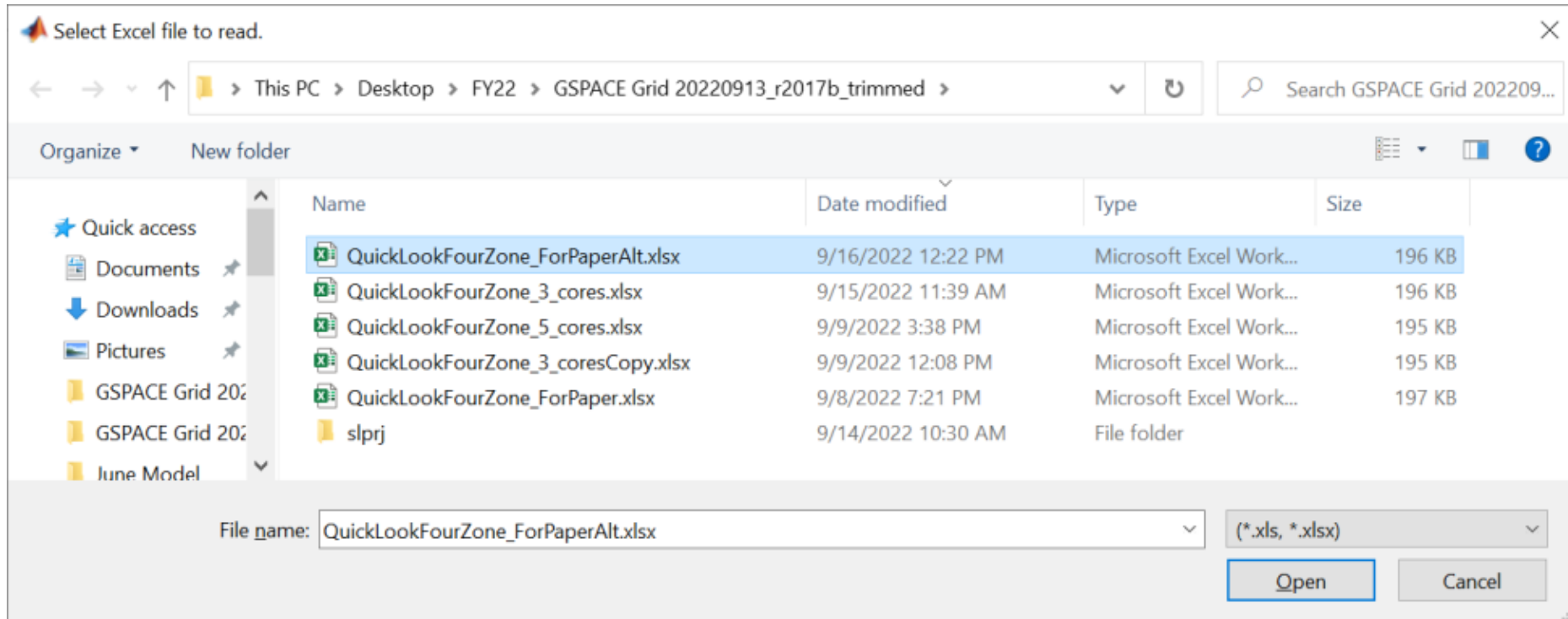
- Load Profiles
 - Active loads
 - Reactive loads
 - DC loads

	A	B	C	D	E	F	G	H
1	time(s) bus							
2	20	1000	1000	1000	1000	1000	1000	1000
3	21	1000	1000	1000	1000	1000	1000	1000
4	22	1000	1000	1000	1000	1000	1000	1000
5	23	1000	1000	1000	1000	1000	1000	1000
6	24	1000	1000	1000	1000	1000	1000	1000
7	25	1000	1000	1000	1000	1000	1000	1000
8	26	1000	1000	1000	1000	1000	1000	1000
9	27	1000	1000	1000	1000	1000	1000	1000
10	28	1000	1000	1000	1000	1000	1000	1000
11	29	0	0	0	0	0	0	0
12	30	0	0	0	0	0	0	0
13	31	0	0	0	0	0	0	0
14	32	0	0	0	0	0	0	0
15	33	0	0	0	0	0	0	0
16	34	0	0	0	0	0	0	0
17	35	0	0	0	0	0	0	0

GENERATING THE MODEL

Once Spreadsheet edits are saved

- Run script currently called 'main.m' to generate the model
- Choose the desired excel file



OPTIMAL POWER FLOW (OPF) RESULT DISPLAYED

Once file is chosen

- File read time is tracked
- AC/DC Optimal power flow is computed
- OPF results is used to initialize model state variables
- After OPF completes, new Simulink model is automatically opened and populated

```
Reading data from Excel file ...  
File read complete!  
Elapsed time is 12.439287 seconds.
```

acBus	VacLN	delDeg
1	3988	0
2	3988	-1.8447e-13
3	3914.4	0.66615
4	3872.5	0.28609
5	3877.3	1.0019
6	3921.9	-0.35788
7	3871.8	0.43243
8	3829.4	0.047519
9	3834.2	0.76358
10	3896.3	-2.9287
11	3800.5	-2.5423
12	3845.1	-2.8045
13	3862.7	-2.8017
14	3859.9	-2.8007
15	3865.8	-2.7989
16	3845.1	-2.8045
17	3862.7	-2.8017
18	3859.9	-2.8007
19	3865.8	-2.7989

OPTIMAL POWER FLOW RESULT DISPLAYED

dcBus	Vdc
20	12460
21	12603
22	12565
23	12604
24	12460
25	12603
26	12565
27	12604
28	3297
29	3297
30	3297
31	3297
32	3297
33	3297
34	3297
35	3297

acdcConvNo	dutyMag	dutyAngDeg
1	0.25789	-0.61599
2	0.25265	0.13673
3	0.24781	-0.25811
4	0.25487	0.44002
5	0.25789	-0.61599
6	0.25265	0.13673
7	0.24781	-0.25811
8	0.25487	0.44002
9	0.26478	-2.269
10	0.26298	-2.2687
11	0.26358	-2.2674
12	0.26315	-2.2664
13	0.26478	-2.269
14	0.26298	-2.2687
15	0.26358	-2.2674
16	0.26315	-2.2664

dcdcConvNo	mu
1	0.26454
2	0.26156
3	0.26235
4	0.26153
5	0.26454
6	0.26156
7	0.26235
8	0.26153

bus_no	MWgen	MVARgen	charging
1	15.793	0	false
2	15.793	0	false
3	10.009	0	false
4	10	0	false
5	10	0	false
28	0.25818	0	false
29	0.19181	0	false
30	0.17561	0	false
31	0.17631	0	false
32	0.25818	0	false
33	0.19181	0	false
34	0.17561	0	false
35	0.17631	0	false

0.071991 per-unit loss (Pgen - Pload)
11.3912 % loss
3.847s to solve.
41 iterations.
f=0.000835

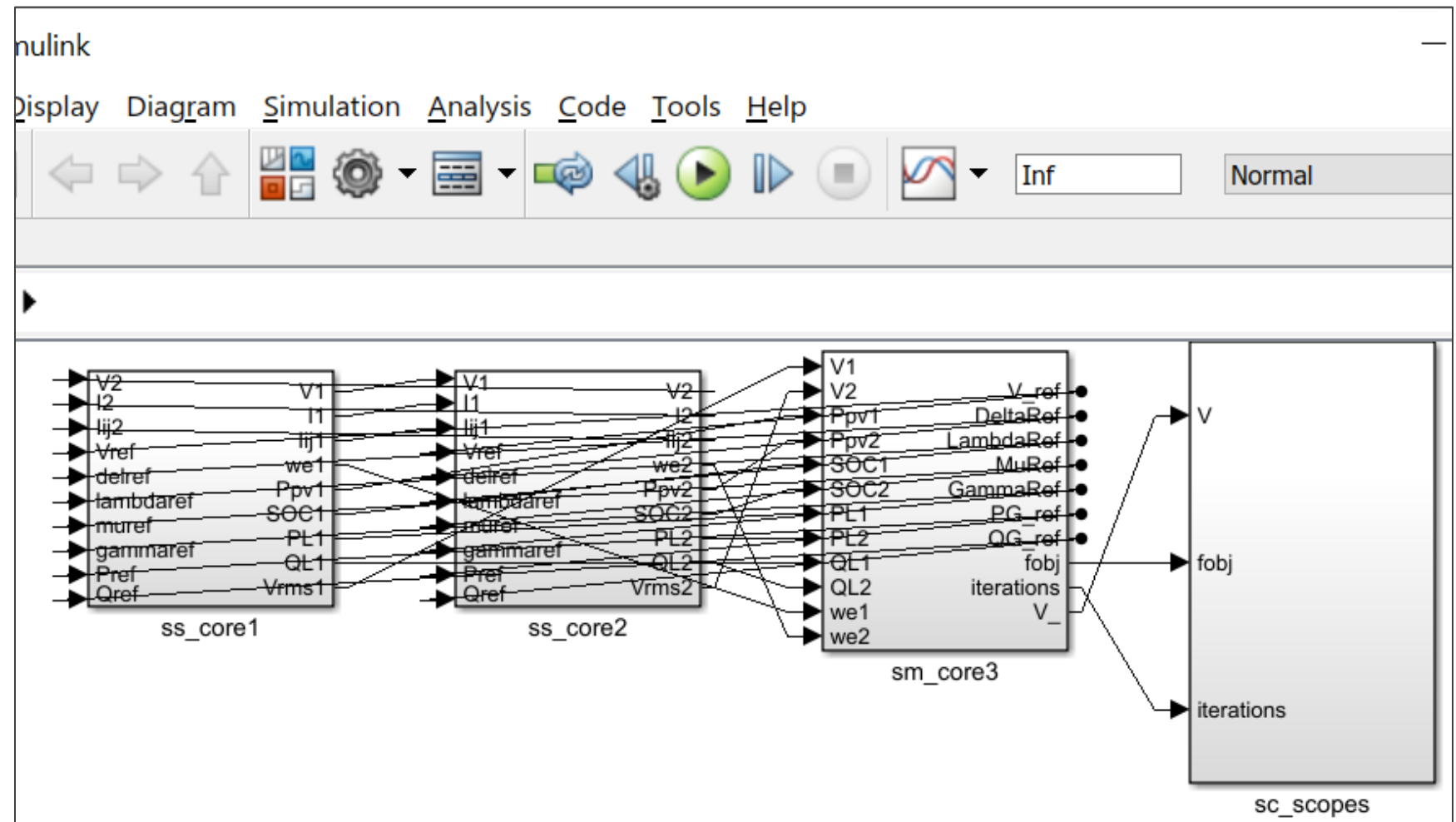
AC/DC converter duty cycles are displayed as phasor quantities

OPAL-RT MODEL AUTOMATICALLY GENERATED

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Automatically split
across the
specified number
of cores

- 1-2 are plant
cores
- 3 is the OPF
core
 - Periodic OPF
computation

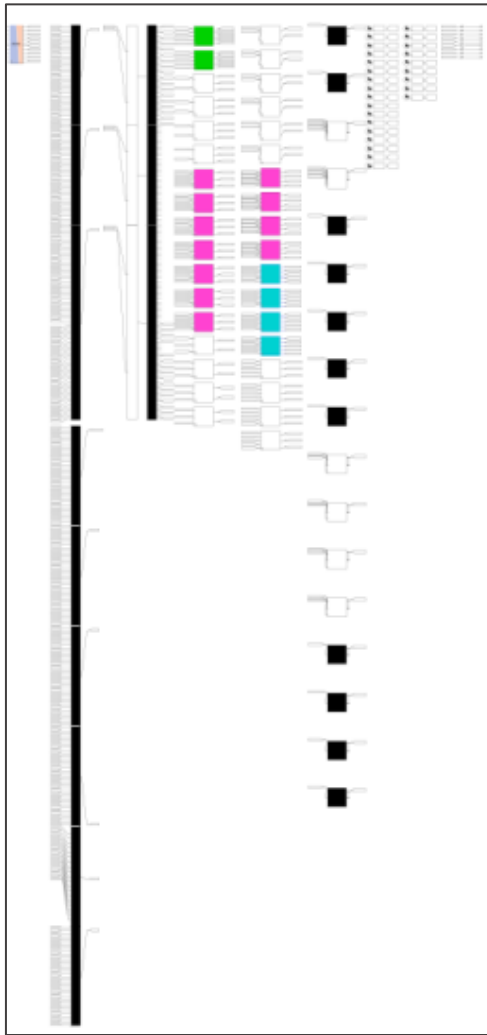


UNDER THE HOOD

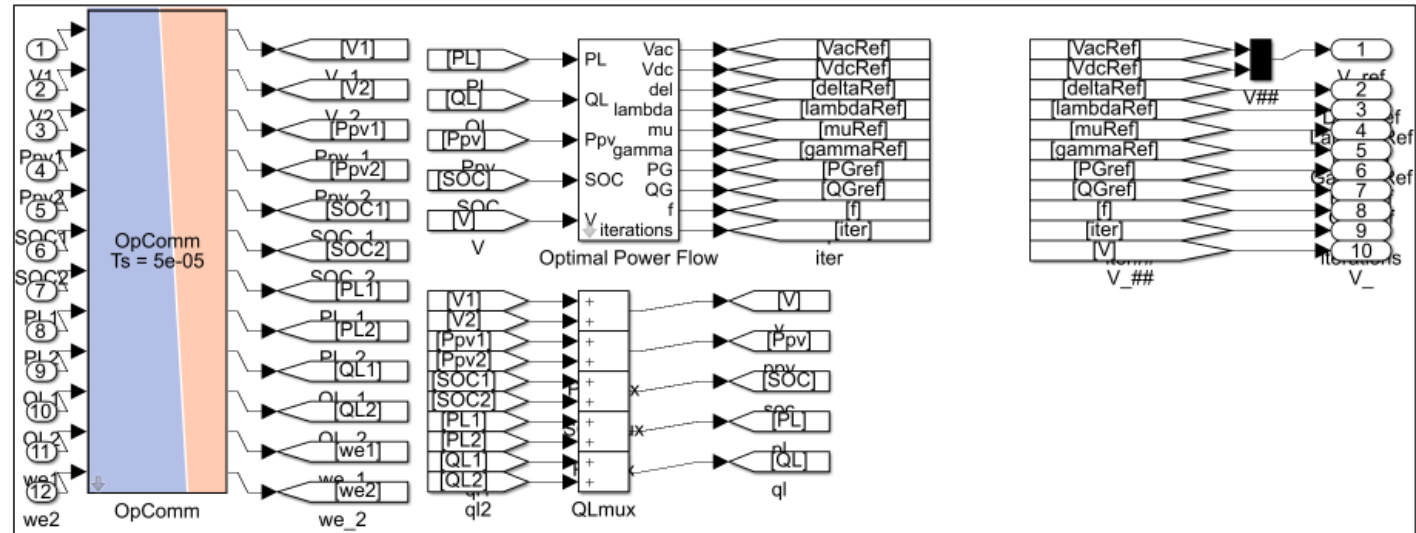
ss_core1



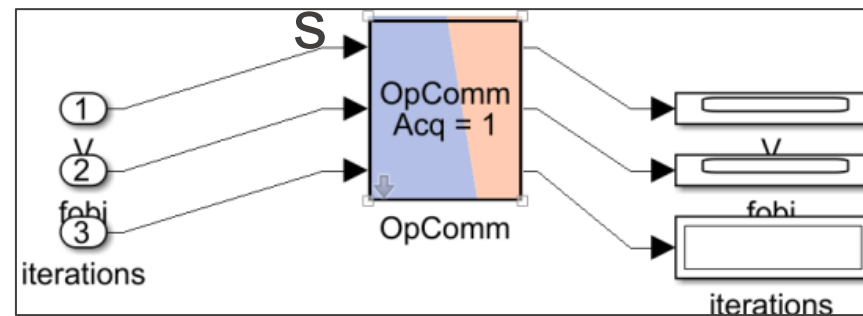
ss_core2



sm_core3



sc_scope



UNDER THE HOOD

- Hundreds of Simulink blocks are automatically placed throughout the model
- OPAL-RT OpComm blocks are automatically placed

OPAL-RT SIMULATION

- Simply save model and load to OPAL-RT as normal
- **'IGNORE CRITICAL WARNINGS'** must be chosen in the 'Variable' tab in OPAL-RT before loading

OPAL-RT SIMULATION (BUILD MODEL)

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The screenshot displays the RT-LAB v2020.1.0.327 software interface. The 'Project Explorer' on the left shows a tree structure with 'Targets' (RTServer, localhost), 'Untitled' (untitled21), and 'Models' (SEP12_6WEC_4chan_vect_deg_opal, SEP15_6WEC_4chan_vect_deg_opal, untitled -> RTServer, untitled1 -> RTServer, untitled21 [Compiling], untitled4 -> RTServer). The 'Overview' window shows 'General Information' (Name: untitled21) and 'Preparing and Compiling' (Edit the model). A 'Building model' dialog box is open, showing 'Building untitled21' with a progress bar and the option 'Always run in background' (unchecked). The 'Progress' window shows 'Building model' and 'Building untitled21: Model separation'. The console window displays the following text:

```
----- Starting compilation -----  
Start at : Friday, September 16, 2022, 13:13:00  
  
The current RT-LAB version is: v2020.1.0.327  
The current model is: C:\Users\rcmatth\Desktop\RTLAB_Files_2022_August\Untitled\models\untitled21\untitled21  
The current host platform is: Windows  
The current target platform is: OPAL-RT Linux (x86-based)  
The current compiler is: Automatic  
Separating model because it has never been built
```

The Windows taskbar at the bottom shows the search bar, task view, and several open applications (PowerPoint, RT-LAB, Paint, Word). The system tray shows the date and time (1:13 PM, 9/16/2022).

OPAL-RT SIMULATION (BUILD MODEL)

21

The screenshot displays the RT-LAB v2020.1.0.327 software interface. The main window shows the 'Overview' tab for a model named 'untitled21'. A 'Building model' dialog box is open, indicating the progress of building 'untitled21'. The dialog box includes a progress bar, the text 'Code generation: untitled21_1_sm_core3', and a checkbox for 'Always run in background'. Below the dialog box, the 'Progress' window shows the status of the build process, including 'Building model', 'Building untitled21: Code generation: untitled21_1_sm_core3', and 'Refreshing workspace'. The main window also shows the 'Project Explorer' on the left, listing various models and targets. The bottom status bar indicates 'Building model: (30%)'.

RT-LAB v2020.1.0.327

File Edit Navigate Search Simulation Tools Window Help

Project Explorer

- Targets
 - RTServer
 - localhost
- Untitled
 - Models
 - SEP12_6WEC_4chan_vect_deg_opal <Not compiled for C>
 - SEP15_6WEC_4chan_vect_deg_opal -> RTServer
 - untitled -> RTServer
 - untitled1 -> RTServer
 - untitled21 [Compiling]
 - untitled4 -> RTServer
 - I/O Interfaces
 - Panels
 - Recorders
 - Configuration (Default*)
 - data

Create a new project...

Overview

General Information

Name: untitled21

Preparing and Compiling

Edit the model.

Building model

Building untitled21

Code generation: untitled21_1_sm_core3

☐ Always run in background

Run in Background Cancel Details >>

Progress

- Building model
- Building untitled21: Code generation: untitled21_1_sm_core3
- Refreshing workspace
- Refreshing '/Untitled/models/u..._self/rtw/rtlab_rtmodel/src'.

Building model: (30%)

1:16 PM 9/16/2022

OPAL-RT SIMULATION (BUILD MODEL)

22

The screenshot displays the RT-LAB v2020.1.0.327 software interface. The main window shows the 'Overview' tab for a model named 'untitled21'. A 'Building model' dialog box is open, indicating the progress of building the model. The dialog box has a green progress bar and a checkbox for 'Always run in background'. Below the dialog box, the 'Progress' window shows the status of the build process, including 'Building model', 'Building untitled21: File transfer', 'Building workspace (Finished)', and 'Refreshing \'/Untitled/models...2_6WEC_4chan_vect_deg_opal''. The bottom status bar indicates 'Building model: (60%)'.

RT-LAB v2020.1.0.327

File Edit Navigate Search Simulation Tools Window Help

Project Explorer

- Targets
 - RTServer
 - localhost
- Untitled
 - Models
 - SEP12_6WEC_4chan_vect_deg_opal <Not compiled for C
 - SEP15_6WEC_4chan_vect_deg_opal -> RTServer
 - untitled -> RTServer
 - untitled1 -> RTServer
 - untitled21 [Compiling]
 - untitled4 -> RTServer
 - I/O Interfaces
 - Panels
 - Recorders
 - Configuration (Default*)
 - data

Create a new project...

Overview

General Information

Name: untitled21

Preparing and Compiling

Edit the model.

Building model

Building untitled21

File transfer

☐ Always run in background

Run in Background Cancel Details >>

Progress

- Building model
- Building untitled21: File transfer
- Building workspace (Finished)
- Refreshing \'/Untitled/models...2_6WEC_4chan_vect_deg_opal'.

OK

OK

Building model: (60%)

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\zero_crossing_types*.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\builtin_typeid_types*.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\multiword_types*.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\rtwtypes.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\rtmodel.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\drive_untitled21_1_sm_core3*.c (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\drive_untitled21_1_sm_core3*.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\Opal*.c (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\OpREDHAWKtarget\ssc_ml_fun*.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\slprj\rtlab_rtmodel_sharedutils*.c (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\slprj\rtlab_rtmodel_sharedutils*.h (sm_core3) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_sm_core3\slprj\rtlab_rtmodel_sharedutils*.mk (sm_core3) ... OK.

link/rtw/c/common/linux32.opt ... OK.

link/rtw/c/common/posix.rules ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_ss_core1\OpREDHAWKtarget\settings.json (ss_core1) ... OK.

les_2022_August\Untitled\models\untitled21\untitled21_ss_core1\OpREDHAWKtarget\untitled21_3_ss_core1*.c (ss_core1) ... OK.

OPAL-RT SIMULATION (BUILD MODEL)

23

The screenshot displays the RT-LAB v2020.1.0.327 software interface. The top menu bar includes File, Edit, Navigate, Search, Simulation, Tools, Window, and Help. The Project Explorer on the left shows a tree structure with Targets (RTServer, localhost), Untitled, and Models (SEP12_6WEC_4chan_vect_deg_opal, SEP15_6WEC_4chan_vect_deg_opal, untitled, untitled1, untitled21, untitled4). The main window is titled 'Overview' and shows the 'General Information' tab for the model 'untitled21'. The path is 'C:/Users/rcmatth/Desktop/RTLAB_Files_2022_August/Untitled/mc', MATLAB is 'R2017B', and the state is 'Loadable'. The 'Preparing and Compiling' section lists actions: Edit the model, Set the development properties, Build the model, Consult result in the Compilation View, and Assign targets to subsystems. The 'Executing' section lists: Set the execution properties and Load the model. The 'Console' tab at the bottom shows the build process output, including file transfer and compilation details.

RT-LAB v2020.1.0.327

File Edit Navigate Search Simulation Tools Window Help

Project Explorer

- Targets
 - RTServer
 - localhost
- Untitled
 - Models
 - SEP12_6WEC_4chan_vect_deg_opal <Not compiled for OPAL>
 - SEP15_6WEC_4chan_vect_deg_opal -> RTServer
 - untitled -> RTServer
 - untitled1 -> RTServer
 - untitled21 -> RTServer
 - untitled4 -> RTServer
 - I/O Interfaces
 - Panels
 - Recorders
 - Configuration (Default*)
 - data
 - Create a new project...

Overview

General Information

Name: untitled21

Path: C:/Users/rcmatth/Desktop/RTLAB_Files_2022_August/Untitled/mc

MATLAB: R2017B

State: Loadable

Description:

Preparing and Compiling

- Edit the model.
- Set the development properties.
- Build the model.
- Consult result in the [Compilation View](#)
- Assign targets to subsystems.

Executing

- Set the execution properties.
- Load the model.

Overview | Development | Execution | Variables | Files | Assignment | Diagnostic | Hardware | Simulation Tools

Display | Properties | **Compilation** | Console | Variables Table | Variable Viewer | Monitoring

Model: untitled21

----- Transferring the built model -----

Connecting to 192.168.10.101 ... OK.

Transferring in binary mode /home/s1034412/users/rcmatth/desktop/rtlab_files_2022_august/untitled/models/untitled21/un

Transferring in ascii mode /home/s1034412/users/rcmatth/desktop/rtlab_files_2022_august/untitled/models/untitled21/com

Transferring in binary mode /home/s1034412/users/rcmatth/desktop/rtlab_files_2022_august/untitled/models/untitled21/un

File transfer duration : 00h:00m:06s

----- Completed successfully -----

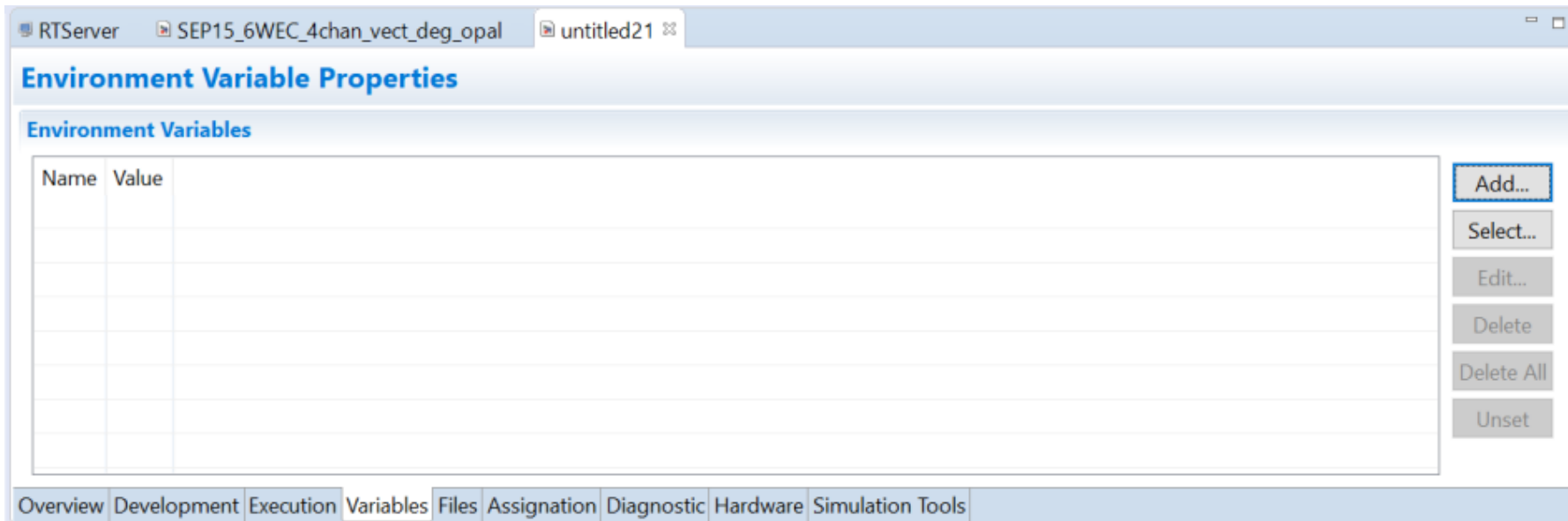
End at : Friday, September 16, 2022, 13:21:48

Compilation duration : 00h:08m:48s

Updating status for next build...OK

OPAL-RT SIMULATION (LOAD MODEL)

24



First select 'IGNORE CRITICAL WARNINGS' from 'Variables' Tab in RT-LAB

OPAL-RT SIMULATION (LOAD MODEL)

Environment Variable Properties

RT-LAB variable Custom variable

Name	Description
AFTER_LOAD_DELAY	Adds a delay after load but before execution.
DISABLE_FLASH_UPDATE	Disables the bitstream flash process at load.
FPGA_BITSTREAM_FORCE_OPTION	Forces the bitstream flash process at load, even if the bitstream is already up-to-date.
IGNORE_CRITICAL_WARNINGS	Ignores critical warnings at load. Be careful: ignoring these warnings can cause undefined behaviour.
OHCI_MAX_REC_BYTES	Defines the maximum number of bytes to be received by Firewire.
OP5142_DUMPBUFFER	Provides additional debug information from the OP5142 during execution.
OP61850_TRACE	Enables IEC61850 Trace. Needed to use the IEC61850 protocol.
OPA429MXIP_RX_LOOPBACK	Activates the software loopback on the MaxTechnologies ARINC card.
PARAM_VECTOR_SIZE_LIMIT	Maximum size of vector or matrix parameters that will be made accessible in real-time.
RTLAB_INTEL_COMPILER	Set to 0 to force RT-LAB to use GCC (GNU Compiler) instead of the Intel(c) compiler on OPAL-RT Linux targets.
SIGNALS_VECTOR_SIZE_LIMIT	Maximum size of vector or matrix signals that will be made accessible in real-time.
SNAPSHOT	Set to OFF to disable the snapshot feature.
TRACE_1553	Provides exhaustive debug information from the MIL1553 driver.

Value: ON

OK Cancel

OPAL-RT SIMULATION (LOAD MODEL)

Environment Variable Properties

RT-LAB variable Custom variable

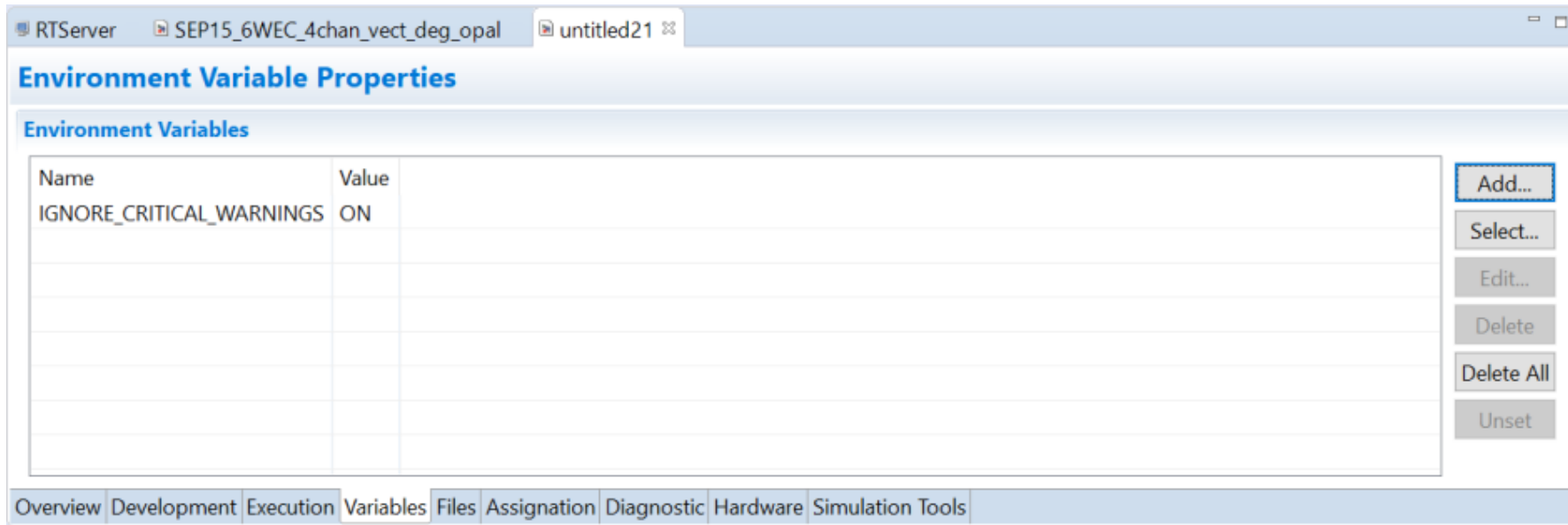
Name	Description
AFTER_LOAD_DELAY	Adds a delay after load but before execution.
DISABLE_FLASH_UPDATE	Disables the bitstream flash process at load.
FPGA_BITSTREAM_FORCE_OPTION	Forces the bitstream flash process at load, even if the bitstream is already up-to-date.
IGNORE_CRITICAL_WARNINGS	Ignores critical warnings at load. Be careful: ignoring these warnings can cause undefined behaviour.
OHCI_MAX_REC_BYTES	Defines the maximum number of bytes to be received by Firewire.
OP5142_DUMPBUFFER	Provides additional debug information from the OP5142 during execution.
OP61850_TRACE	Enables IEC61850 Trace. Needed to use the IEC61850 protocol.
OPA429MXIP_RX_LOOPBACK	Activates the software loopback on the MaxTechnologies ARINC card.
PARAM_VECTOR_SIZE_LIMIT	Maximum size of vector or matrix parameters that will be made accessible in real-time.
RTLAB_INTEL_COMPILER	Set to 0 to force RT-LAB to use GCC (GNU Compiler) instead of the Intel(c) compiler on OPAL-RT Linux targets.
SIGNALS_VECTOR_SIZE_LIMIT	Maximum size of vector or matrix signals that will be made accessible in real-time.
SNAPSHOT	Set to OFF to disable the snapshot feature.
TRACE_1553	Provides exhaustive debug information from the MIL1553 driver.

Value: ON

OK Cancel

OPAL-RT SIMULATION (LOAD MODEL)

27



- If done correctly, the 'Variables' tab will be populated as shown
- Next, the model can be loaded to OPAL-RT as normal

OPAL-RT SIMULATION (LOAD MODEL)

28

RT-LAB v2020.1.0.327

File Edit Navigate Search Simulation Tools Window Help

Project Explorer

- Targets
 - RTServer
 - localhost
- Untitled
 - Models
 - SEP12_6WEC_4chan_vect_deg_opal <Not compiled for OPAL-
 - SEP15_6WEC_4chan_vect_deg_opal -> RTServer
 - untitled -> RTServer
 - untitled1 -> RTServer
 - untitled21 [Paused]
 - untitled4 -> RTServer
 - I/O Interfaces
 - Panels
 - Recorders
 - Configuration (Default*)
 - data

Create a new project...

RTServer SEP15_6WEC_4chan_vect_deg_opal untitled21

Name: untitled21

Path: C:/Users/rcmatth/Desktop/RTLAB_Files_2022_August/Untitled/mc

MATLAB: R2017B

State: Paused

Description:

Overview Development Execution Variables Files Assignment Diagnostic Hardware Simulation Tools

Display Properties Compilation Console Variables Table Variable Viewer Monitoring

untitled21 / sm core3

A Unit delay is applied on status

Display of standard output will be

Monitoring: start time = 0.000 ms,

SubSystem step size = 0.000050 sec

Synchronized with software timer.

Real-time SingleTasking mode.

RT-LAB license ok. Unlimited time

Snapshot taken (opuntitled21_sm_co

[0]: PAUSE mode, IO set to pause

Total of 0 Overrun detected

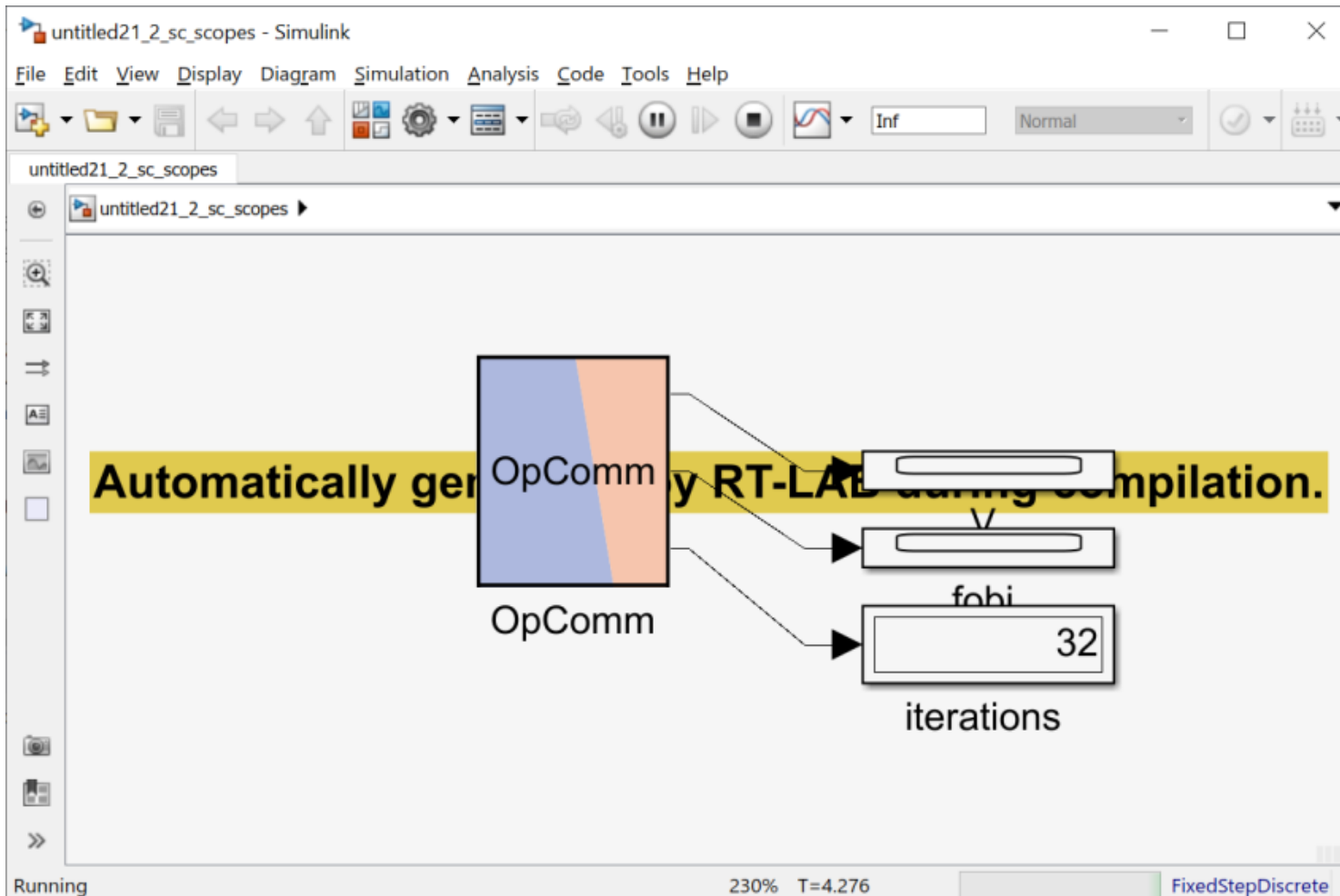
Fri Sep 16 13:32:33 2022

Starting transfer of /home/s103441

Transfer of /home/s1034412/users/r

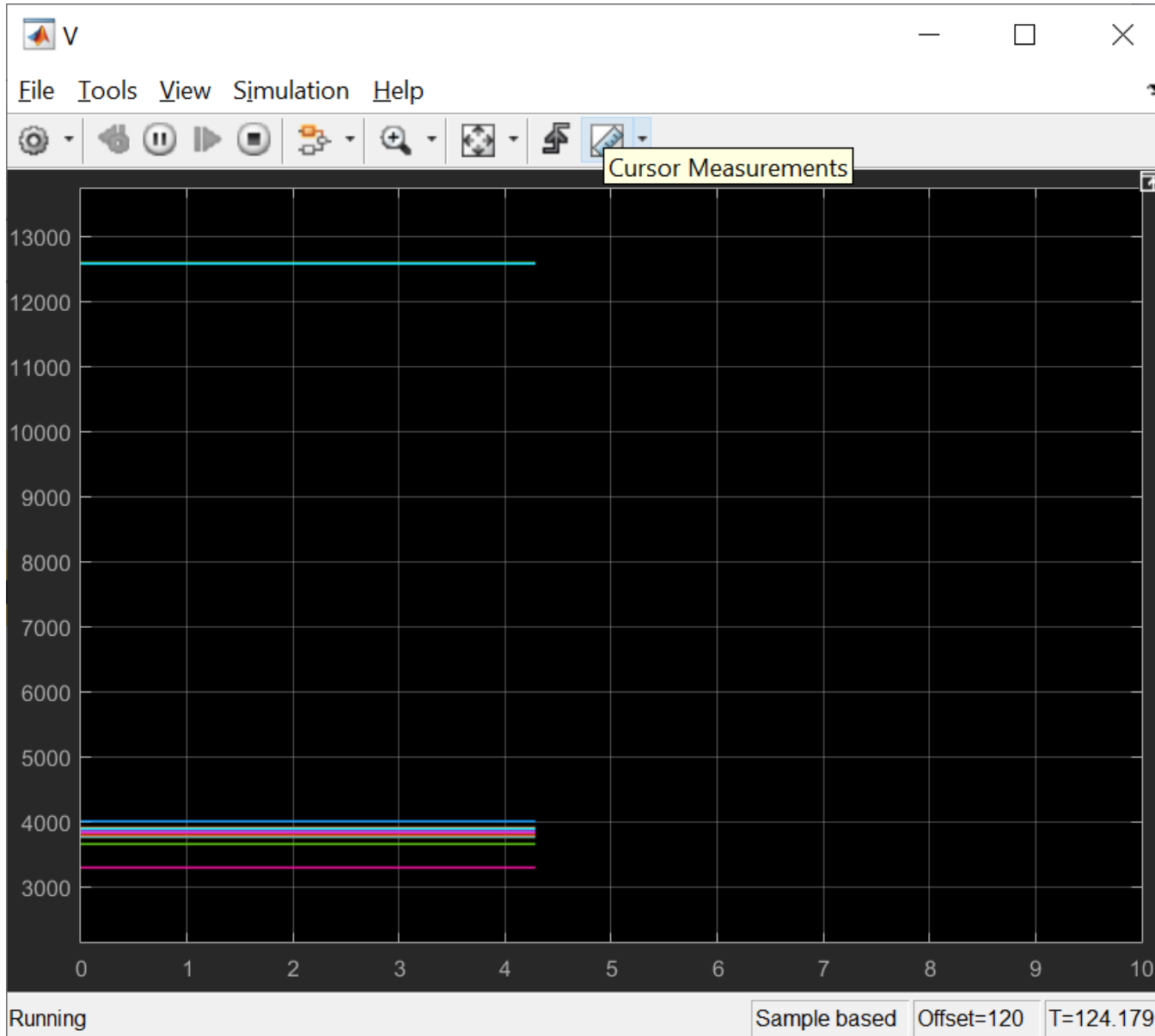
OPAL-RT SIMULATION (EXECUTE MODEL)

29



- RMS and dc voltages are plotted on scope
- Objective function value for OPF is displayed on scope
- Number of OPF iteration is displayed

OPAL-RT SIMULATION



- Voltages are as earlier defined by OPF

CHANGING NUMBER OF CORES

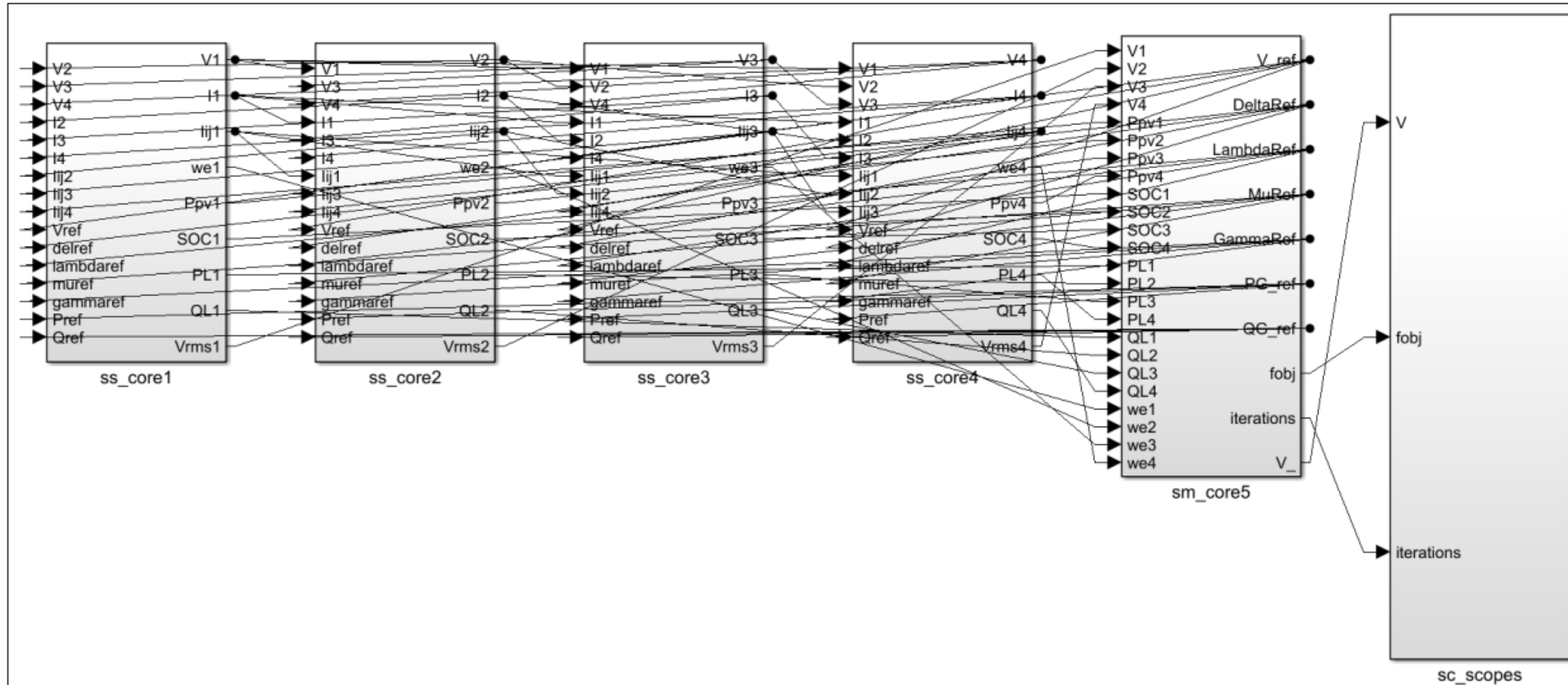
By simply modifying column A of the 'Bus Parameters Sheet, the model can be instead divided across 5 cores on-the fly.

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	core	bus	ac or dc	C(uF)	active (W)	reactive (VAr)	Vbase	Vmin	Vmax	Pmin	Pmax	Qmin	Qmax	objective	type
1	1	1	ac	0	0	0	3983.717	3784.531	4182.903	0	50000000	-50000000	50000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generato
2	2	2	ac	0	0	0	3983.717	3784.531	4182.903	0	50000000	-50000000	50000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generato
3	3	3	ac	0	0	0	3983.717	3784.531	4182.903	0	10000000	-10000000	10000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generato
4	4	4	ac	0	0	0	3983.717	3784.531	4182.903	0	10000000	-10000000	10000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generato
5	5	5	ac	0	0	0	3983.717	3784.531	4182.903	0	10000000	-10000000	10000000	$0.01 \cdot P^2 + 1.0 \cdot Q^2$	3-phase ac generato
6	1	6	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
7	2	7	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
8	3	8	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
9	4	9	ac	2000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
10	1	10	ac	1000	18000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
11	2	11	ac	1000	18000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
12	3	12	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
13	4	13	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
14	1	14	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
15	2	15	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
16	3	16	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
17	4	17	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
18	1	18	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
19	2	19	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
20	3	20	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
21	4	21	ac	1000	1000000	0	3983.717	3784.531	4182.903	0	0	0	0	0	capacitor
22	1	22	dc	16000	1000000	0	12000	11400	12600	0	0	0	0	0	capacitor
23	2	23	dc	16000	1000000	0	12000	11400	12600	0	0	0	0	0	capacitor
24	3	24	dc	16000	1000000	0	12000	11400	12600	0	0	0	0	0	capacitor
25	4	25	dc	16000	1000000	0	12000	11400	12600	0	0	0	0	0	capacitor
26	1	26	dc	16000	1000000	0	12000	11400	12600	0	0	0	0	0	capacitor
27	2	27	dc	16000	1000000	0	12000	11400	12600	0	0	0	0	0	capacitor
28	3	28	dc	16000	1000000	0	12000	11400	12600	0	0	0	0	0	capacitor
29	4	29	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
30	1	30	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
31	2	31	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
32	3	32	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
33	4	33	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
34	1	34	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
35	2	35	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
36	3	36	dc	0	0	0	3297	3297	3297	-10000000	10000000	0	0	$1 \cdot P^2$	battery
37															

OPAL-RT MODEL AUTOMATICALLY GENERATED

32

Exact same model split across 5 cores



LIMITATIONS

There is a limit to how many subsystems the model can be divided across

- Memory blocks/delays required for algebraic signal
 - Such additions slightly alter model dynamics
 - Adding more subsystems adds more delays
- There is no interpolation for signals passed among blocks
 - Smoothness of derivatives may suffer

MODEL PARTITIONING

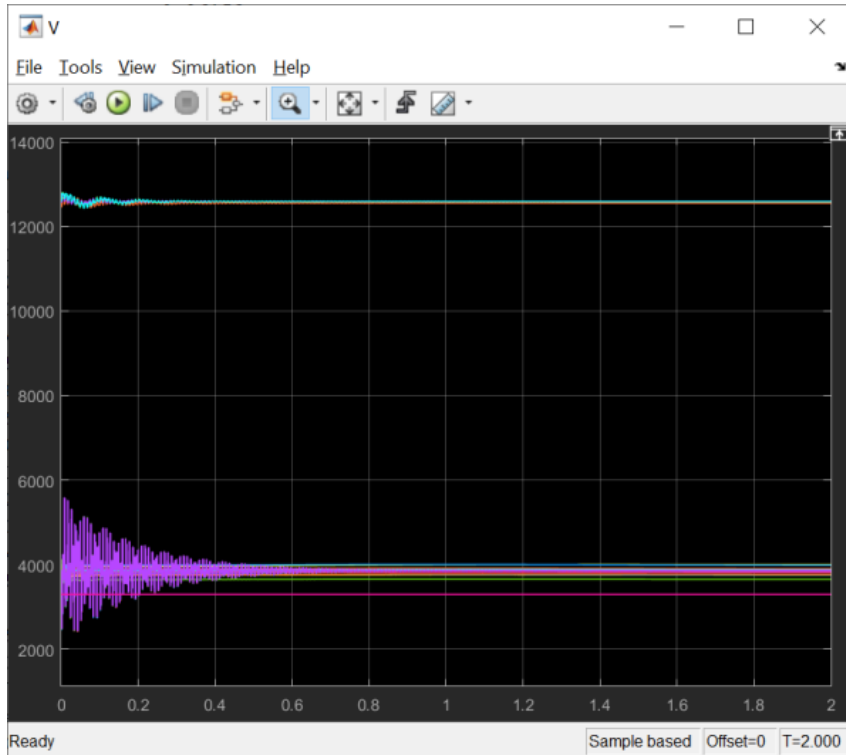
Up until now “core” and “subsystem” have been assumed to be interchangeable.

Now we make a distinction between the 2 with some more precise language.

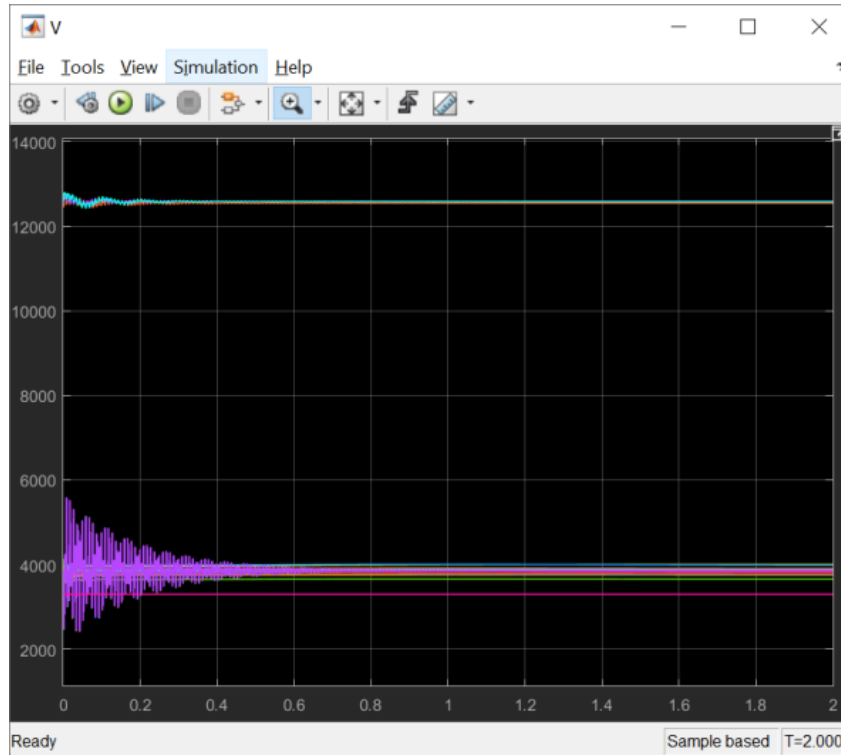
- **Logical core** = logical core on physical processor
- **Simulation core** = subsystem over which model is parallelized by OPAL-RT
- An increased number of subsystems can adversely effect model stability as will be seen shortly
- Experimentally: Exceeding 5 subsystems seems to cause instability
- If model has overruns when spit across 5 cores, multiple logical cores may be assigned to a single simulation core

SAME MODEL ACROSS 3, 5, AND 8 SUBSYSTEMS

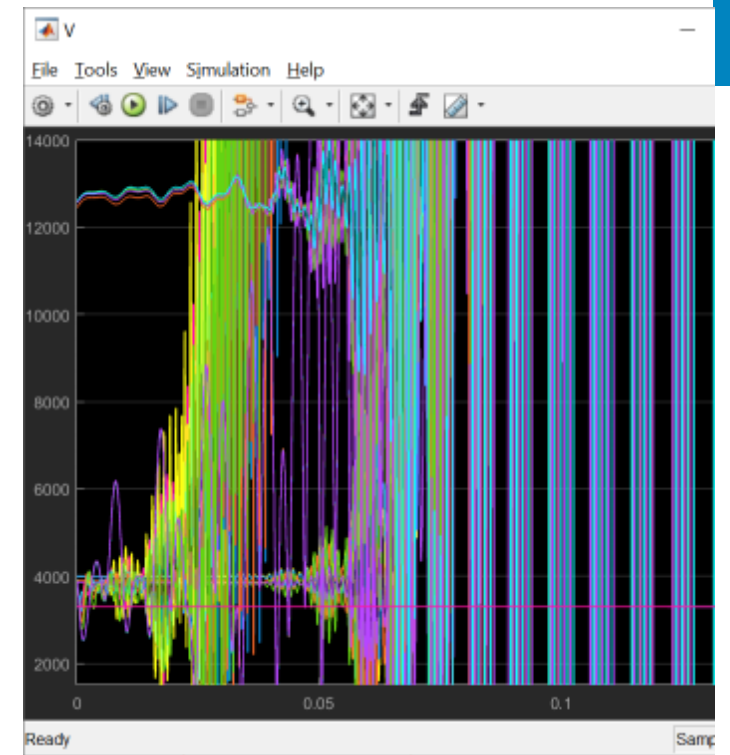
35



3 "cores"
stable



5 "cores"
stable



6 "cores"
unstable

CONCLUSIONS

SwAGSM:

- Allows for rapid model development
- Eliminates the debugging process
- Allow for number of cores to be changed without manually reconstructing model
- Streamlines the process of real-time simulation on the OPAL-RT platform

Availability:

- Not yet available for public release

For further details, contact:

- Ronald Matthews
- rcamtth@sandia.gov
- Sandia National Laboratories

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