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Sandia National Laboratories

A 67 GHz 23 mW Receiver Utilizing Complementary Current Reuse Techniques

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The 52nd European Microwave Conference

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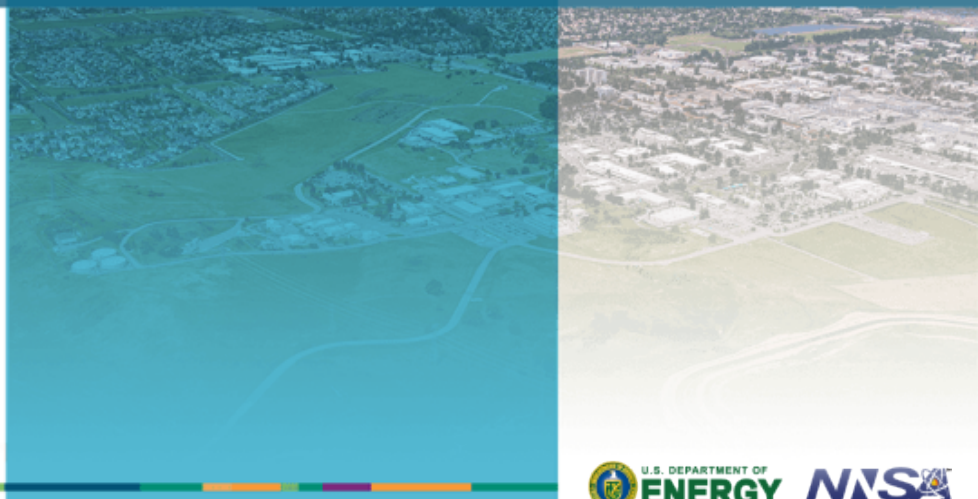

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Outline

- Motivation and prior art
- Bias scaling and current reuse
- Circuit implementation
- Measurement Results
- Conclusion

Phased array transceiver architecture

Scalable phased arrays are a driving technology behind 5/6G systems and emerging radar applications

Array performance scales w.r.t number of elements

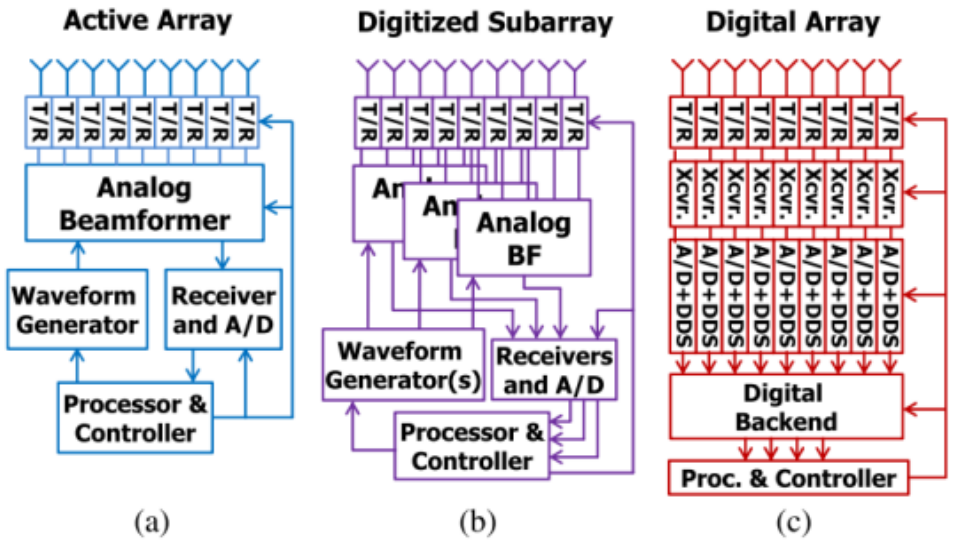
- **More elements equals more effective gain, better link margins!**
- **Array power consumption also scales w.r.t number of elements!**

Power savings cannot come at the cost of RF performance

- Every dB is precious at mmW!

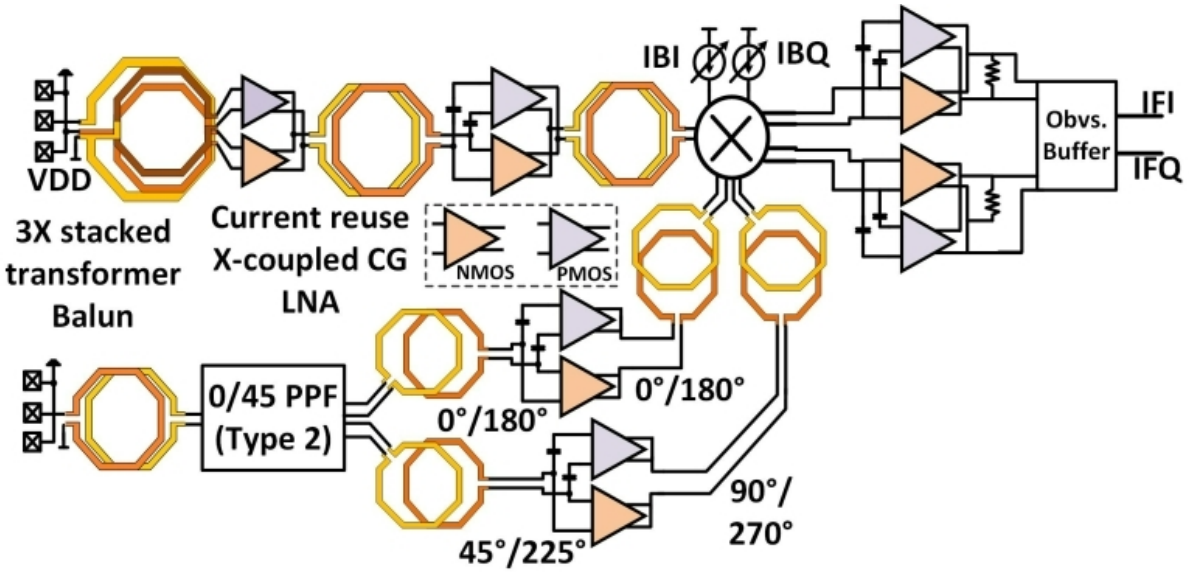
$EIS \propto N_{elements} + NF_{Element}$

- For a given EIS spec, lower NF decreases power consumption (smaller $N_{elements}$)



"Digital Phased Arrays: Challenges and Opportunities" Fulton et. al

Receiver architecture



Low IF receiver, exploiting complementary current reuse, moderate inversion biasing

- Two stage 6mW LNA provides <5dB NF across band
  - Complementary current reuse structure
- Quadrature gilbert down converts with low NF
  - Current source helpers calibrate IQ gain mismatch
- Power efficient doublers enable subharmonic LO
  - Tunable IQ phase balance by PPF
- Low power and high linearity BB enabled through CRCS amps with CMFB biasing

Power efficient bias points used to minimize all blocks PDC

Power efficient biasing for mmW systems

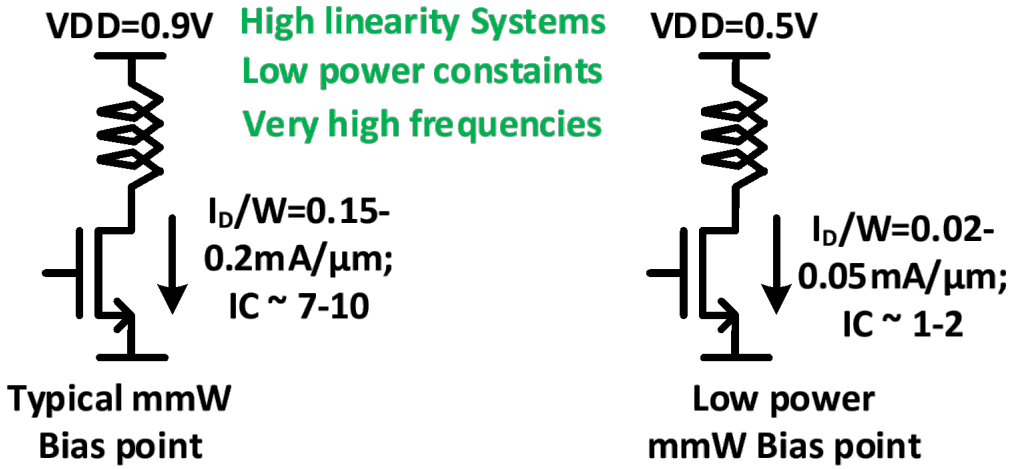
Typical mmW bias points

- 150µA/µm for minimum NF_{Min} @VDD=1V
  - IC=7 and g_m/ID=7.8
- 250µA/µm for maximum F_{max} @VDD=1V
  - IC=9 and **g_m/ID=5.8**

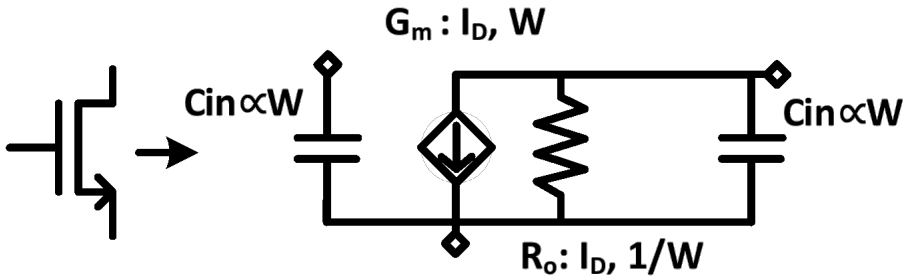
In modern CMOS technologies F_{max}>100GHz can be achieved at low current densities

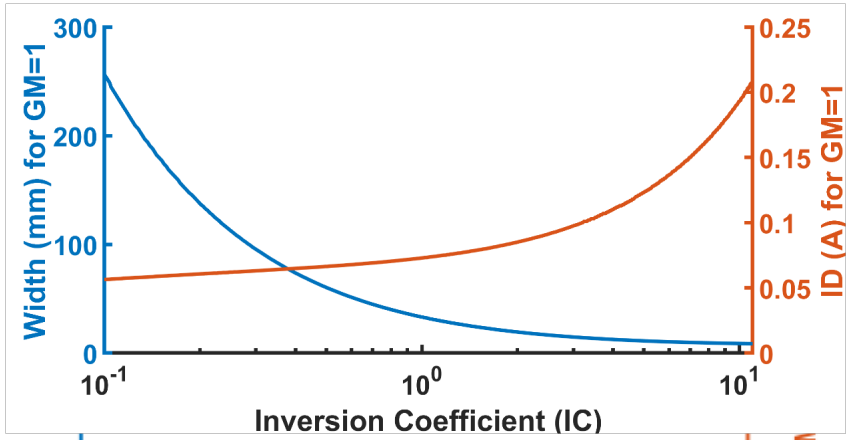
@IC=2 (43µA/µm) F_{max}~250GHz w/ **g_m/ID=11.8**

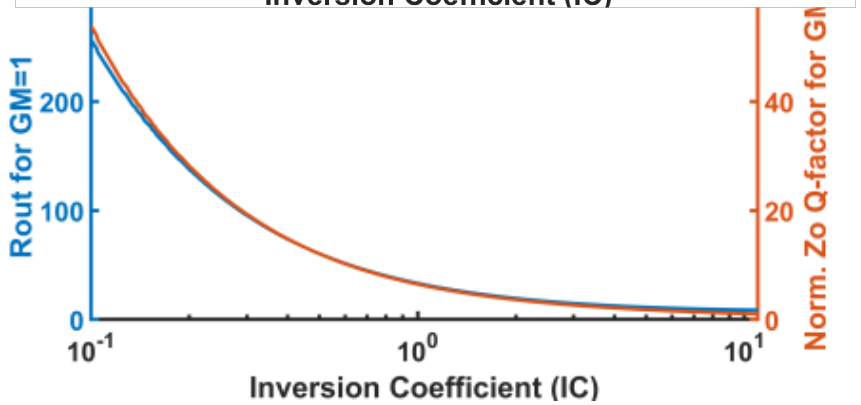
Twice as current efficient as traditional mmW bias



Current scaling versus device impedance







Lowering IC **increases** transconductance per unit current (g_m/I_D)

Lowering IC **decreases** transconductance per unit width (g_m/W)

- Power efficient bias points are both low current density, and high transistor area
- Therefore for a given g_m lower power consumption increases device capacitance
  - F_T is decreases at low IC
  - Q_{in}, and Q_{out} for a given device therefore **increase** with decreased IC
- Fano limit says higher Q-factor decreases bandwidth!

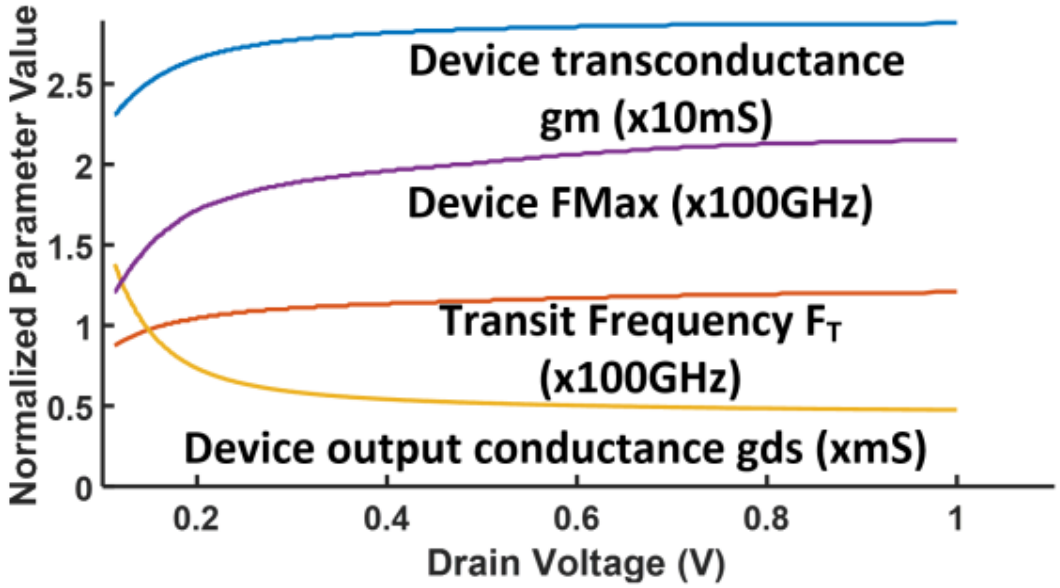
Voltage Scaling on small signal performance

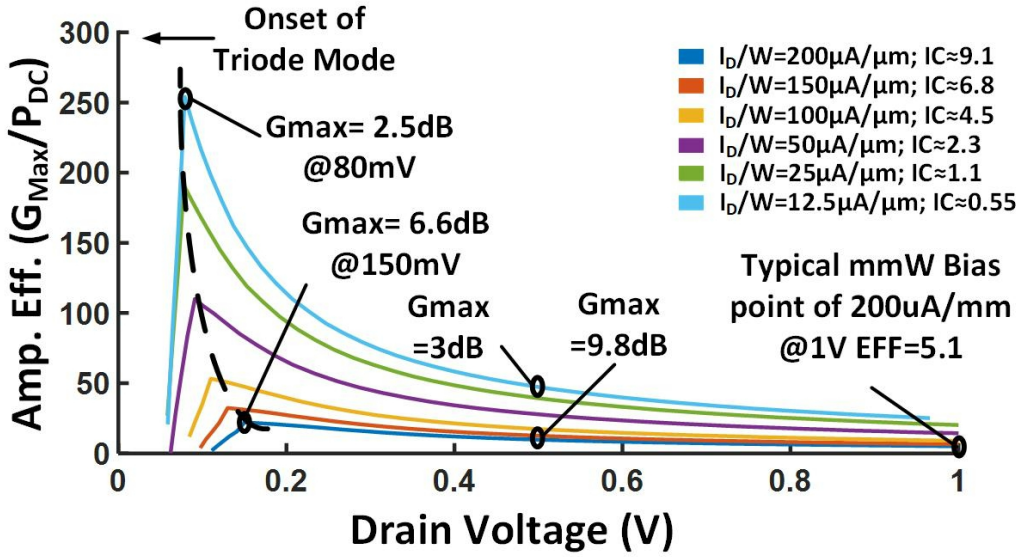
Scaling drain source voltage down moderately impacts device performance

- If VDS>VDS_{Sat} then device parameters only moderately degrade
- When VDS<VDS_{Sat} performance quickly degrade

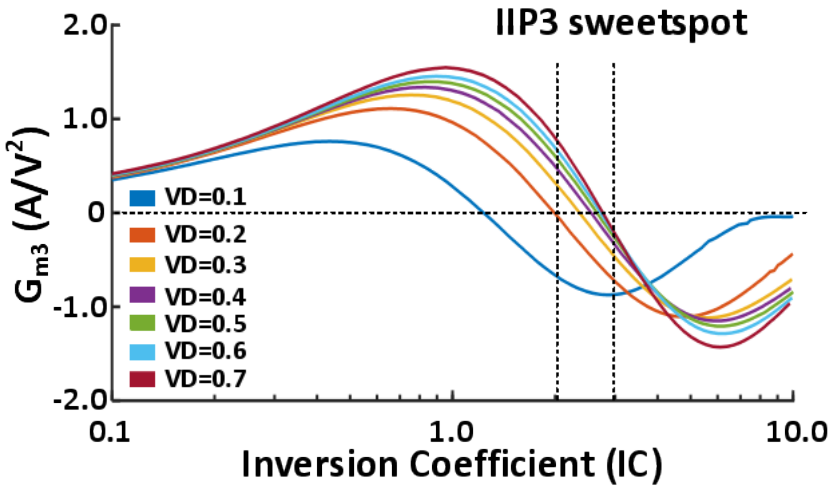
Amplifier efficiency (G_{max}/P_{DC}) monotonically increases until triode mode onset

- IC=1 @0.2V ~40X better efficiency compared IC=10 @1.0V





Bias scaling on linearity



Current scaling does not inherently reduce small signal nonlinearities (TOI)

- G_{M3} of MOS devices typically finds its minimum between IC =2 and 3 (IIP3 Sweet spot 0 crossing)
- Does not reduce IP1dB for devices driving high Z loads
  - For devices driving low Z loads OP1dB is typically reduced

Moderate voltage scaling slightly reduces TOI but linearly reduces compression point

- As devices enter triode mode, both G_{M3} and G_{D3} become significant
- Effect is more pronounced than expected as G_{D3} is driven by larger voltage levels than G_{M3} in amplifiers

Voltage scaling and current reuse

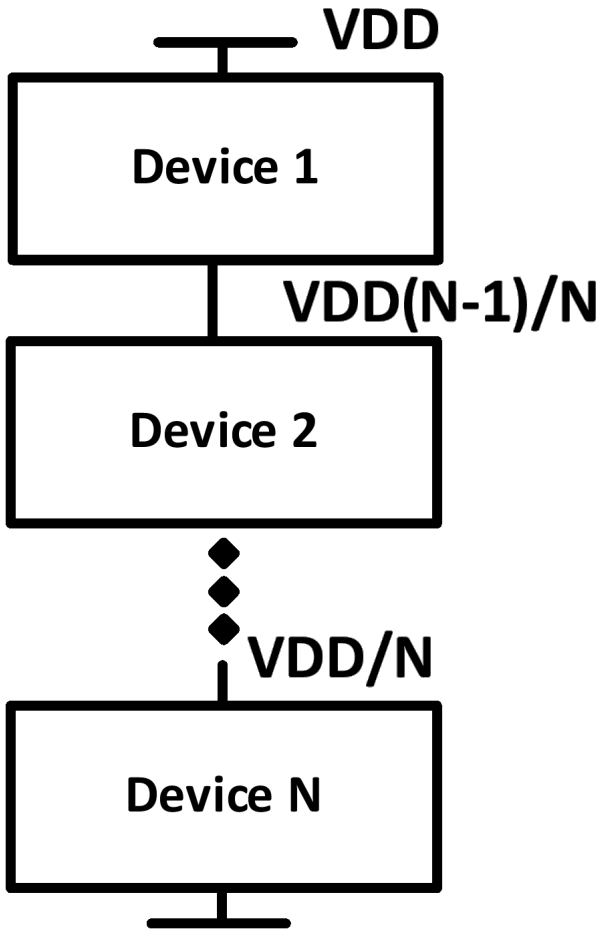
Voltage scaling directly reduces the power consumed by devices

Unfortunately in modern CMOS VDD's of <1V are uncommon

- Voltage is typically set by digital logic requirements
- Producing additional supplies increases complexity and power consumption

Current reuse is a technique which enables voltage scaling with no additional regulators required

- Multiple devices are power from the same rail, sharing the current



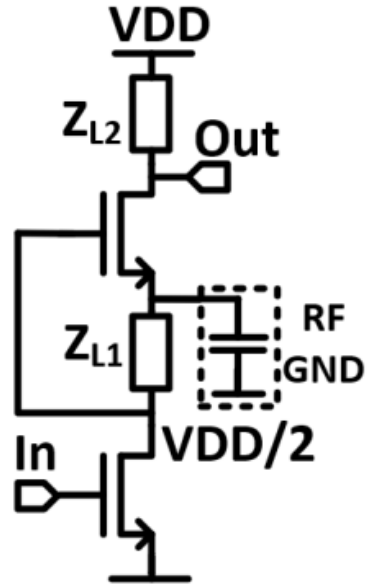
Current reuse variations

Two basic variations of current reuse are possible:

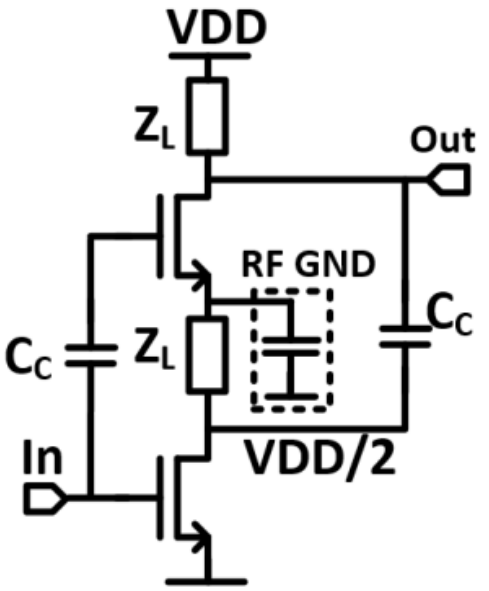
1. Cascading devices utilizing the same power supply
2. Splitting a single transconductor into multiple all sharing the same supply
    1. Combine in current domain at the output, this effectively multiples g_m/I_D enabling division of bias current

Cascaded current reuse has several drawbacks:

1. Differing blocks forced to utilize same currents
2. Differing stages share same bias current but different signal levels
    1. Nonlinearity induced current offset forces current into previous stage



Cascaded current reuse



Transconductor current reuse

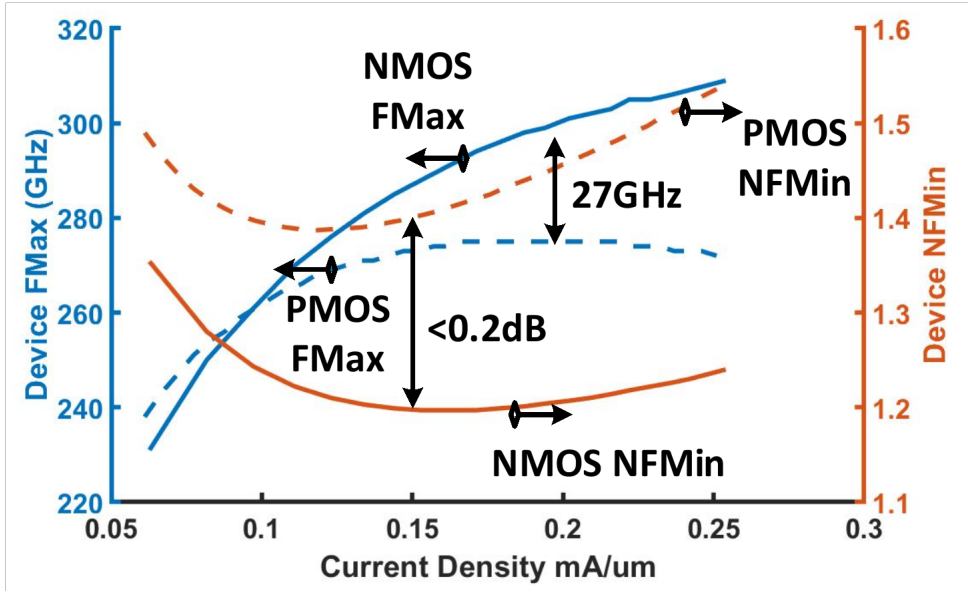
Complementary FET design

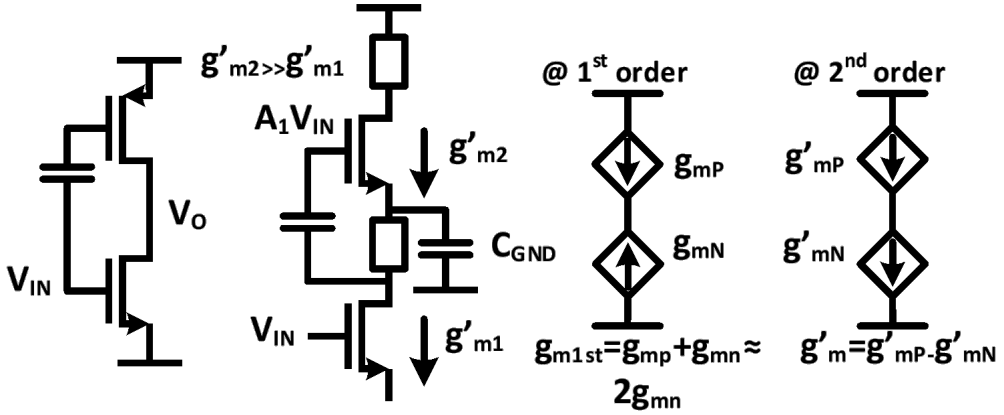
In many modern CMOS nodes NMOS and PMOS devices have similar mobilities

- Device small signal parameters are symmetric between NMOS and PMOS
  - F_{max} ~10%; NF_{Min} <0.2dB

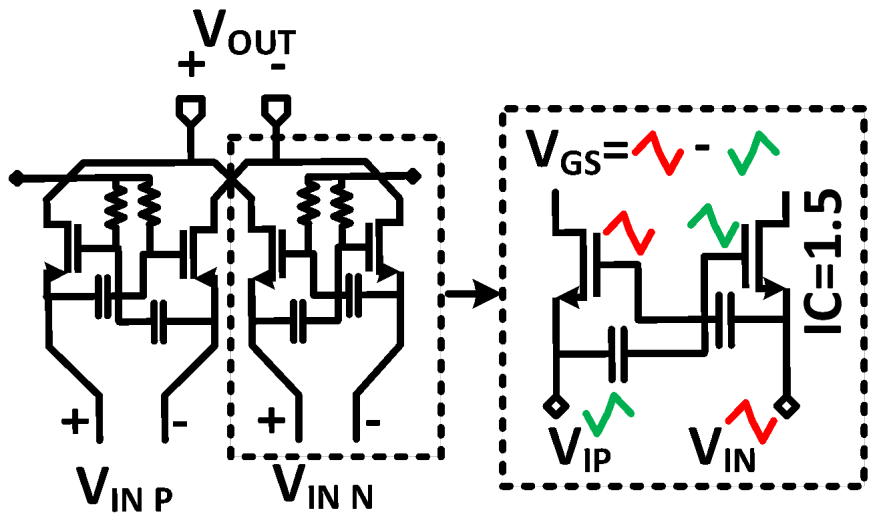
Complementary current reuse (CCR) utilizes both NMOS and PMOS as transconductors

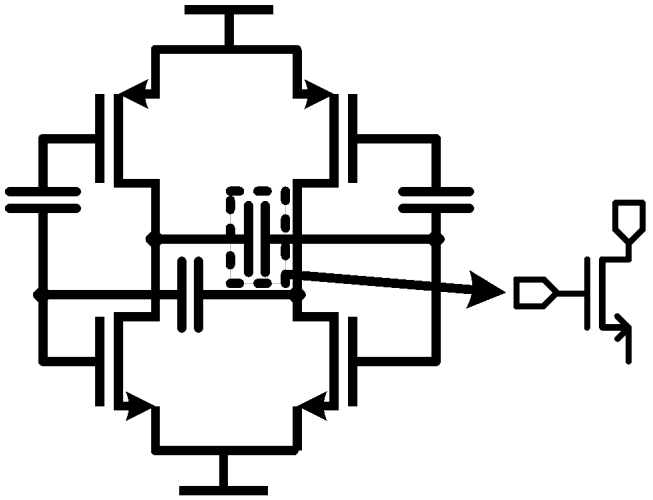
- No AC grounding node needed
- Inherent 2nd order nonlinearity cancellation
  - Opposite phases on even harmonics and identical phases on odd harmonics for signals
- No DC coupling issues from cascaded current reuse
  - Comparing CCR vs cascaded current reuse with 1V VDD and IC=2.5 P1dB improves ~6dB

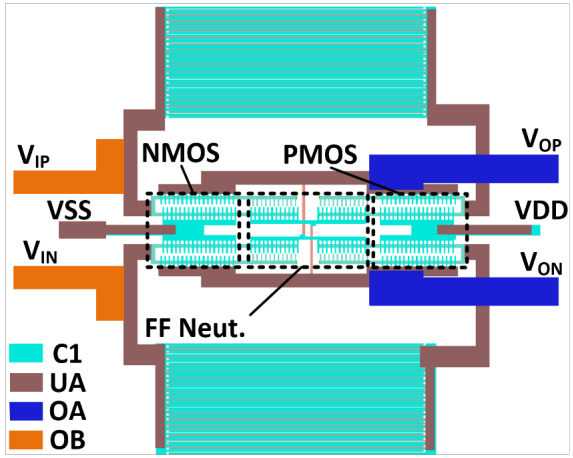




LNA Design





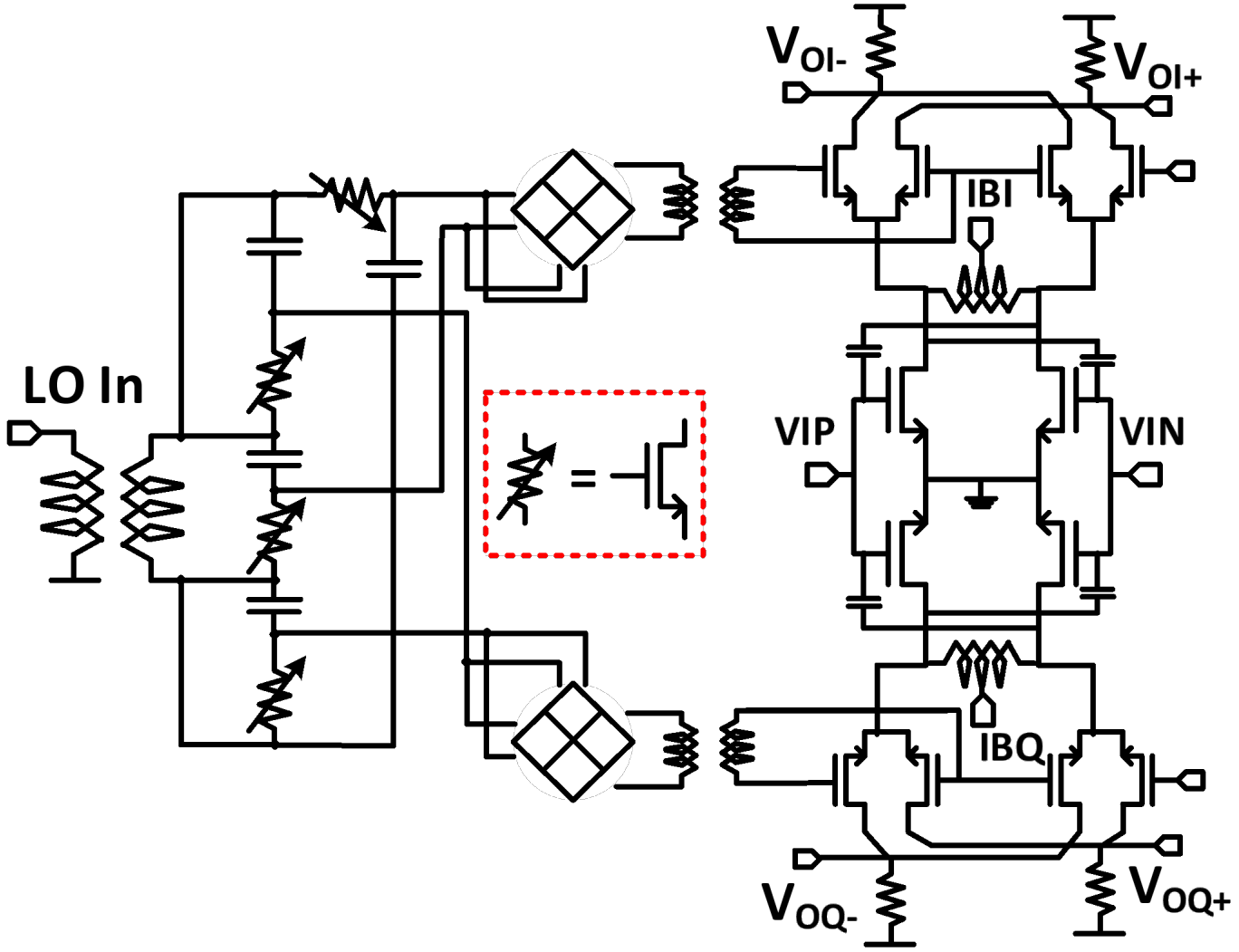


Two stage design utilizing CCR

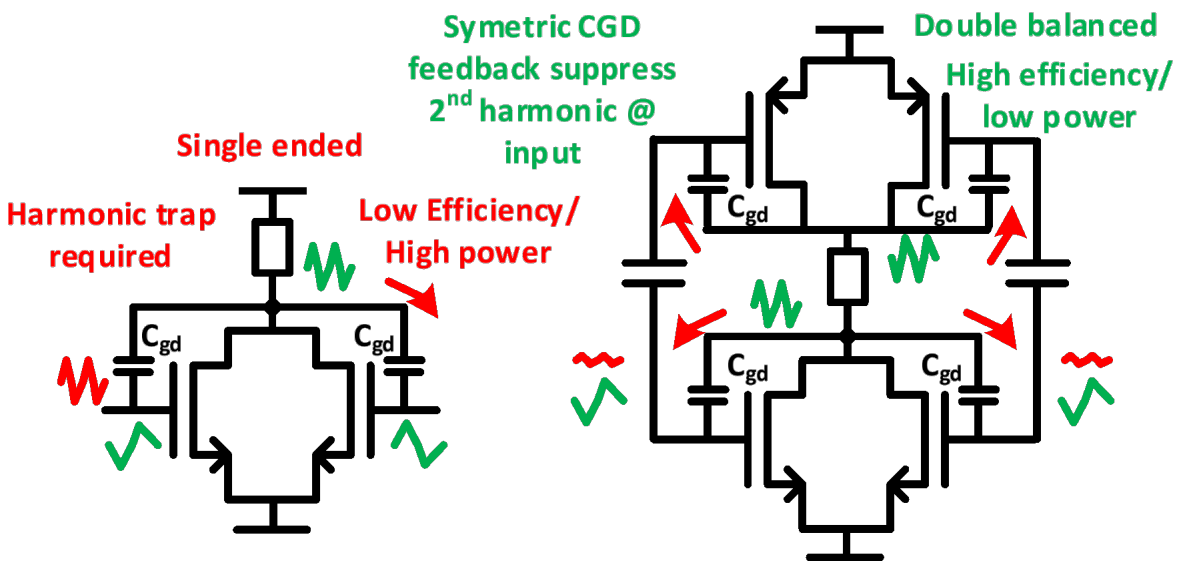
- G_M boosted common gate input stage
- Neutralized common source second stage
- Fourth order resonant matching networks for bandwidth extension
- 6mW DC power consumption

LO Chain and Mixer design

- Tunable type 2 PPF for IQ correction
  - 45 degree phase shift
- Pair of power efficient frequency doublers
- Quadrature gilbert cell mixer
- Inductive resonant out of GM cell for improved gain and IQ gain correction
- Fourth order resonator interstage coupling



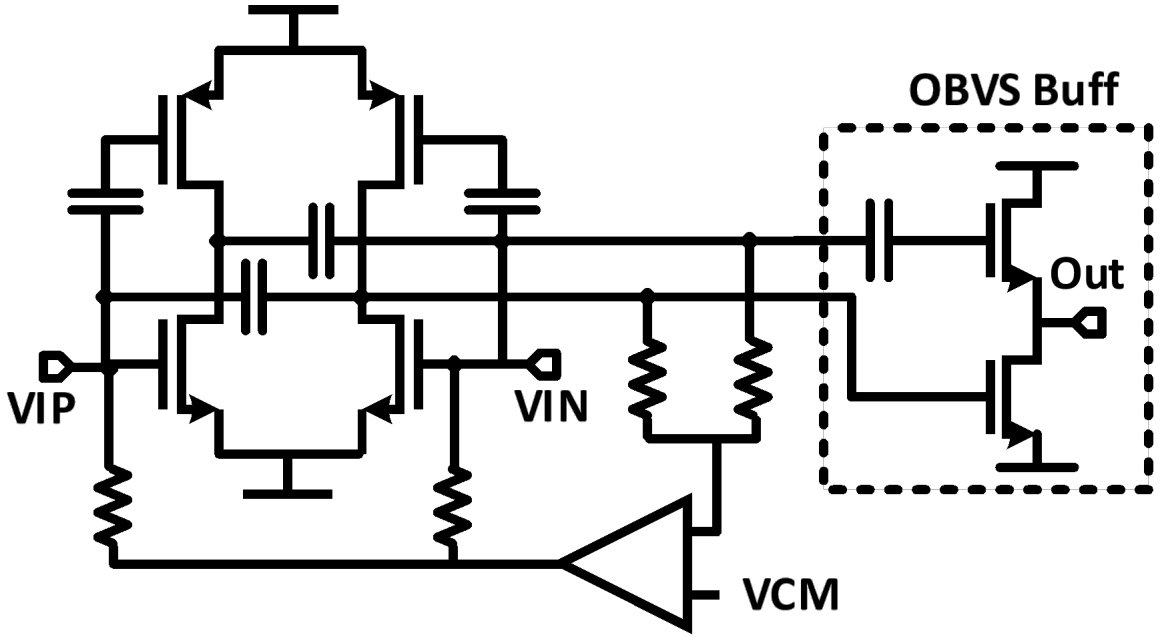
Frequency Doubler



Complementary frequency doubler provides double balanced operation

- Inherent second order cancellation at input
- Current reuse and voltage scaling for low power operation
- Odd order terms from complementary devices cancel, even order terms add
- Deep class C operation for power efficiency improvement

Baseband gain



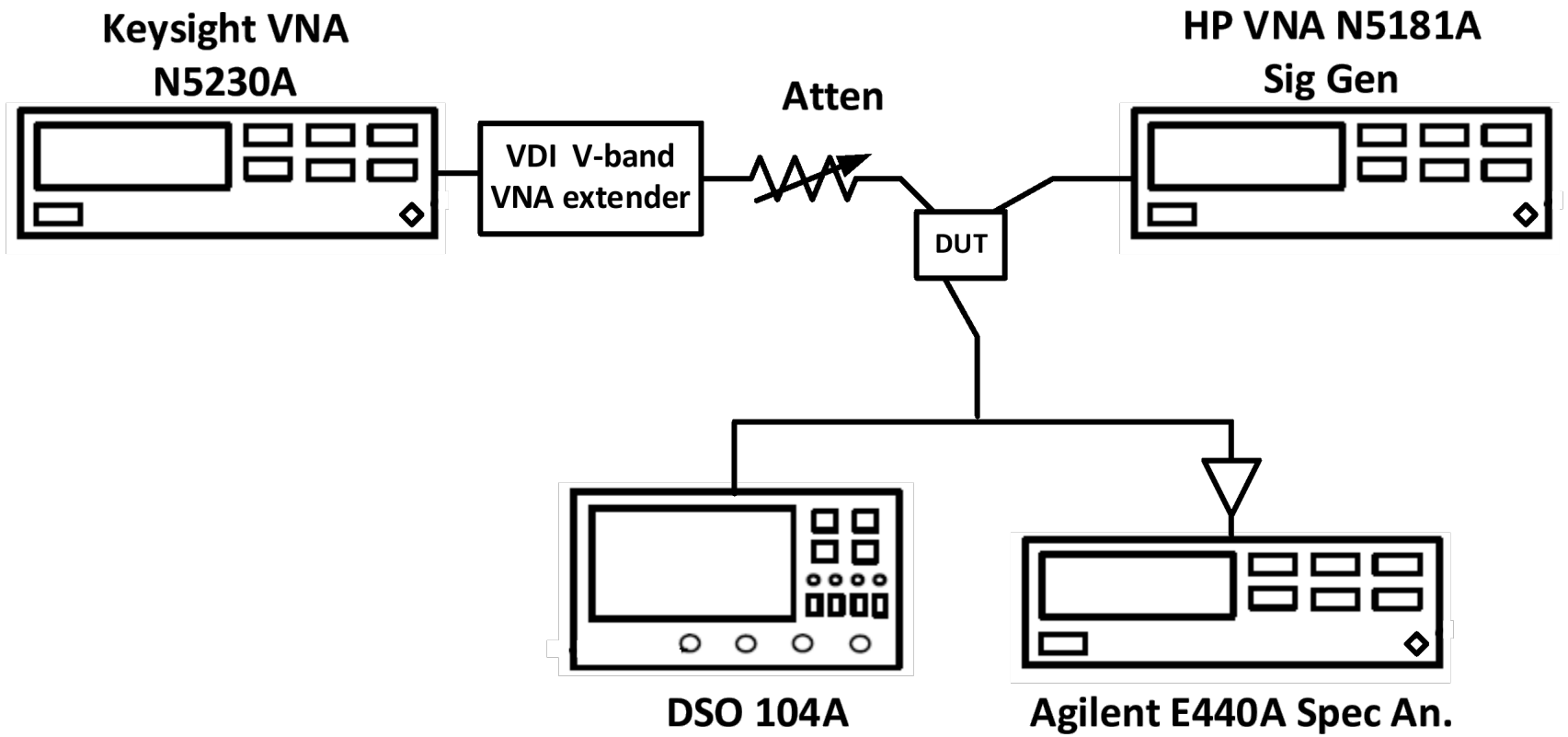
CCR-CS BB amplifier with CMFB loop for maximum OP1dB and TOI

- IC=0.5 for low power operation
- Neutralization for BW extension

Totem pole output buffer for single to diff and 50 ohm output

50MHz-8GHz BW, limited by mixer output BW

Measurement setup



RF probed and DC bias taken out through wirebonds

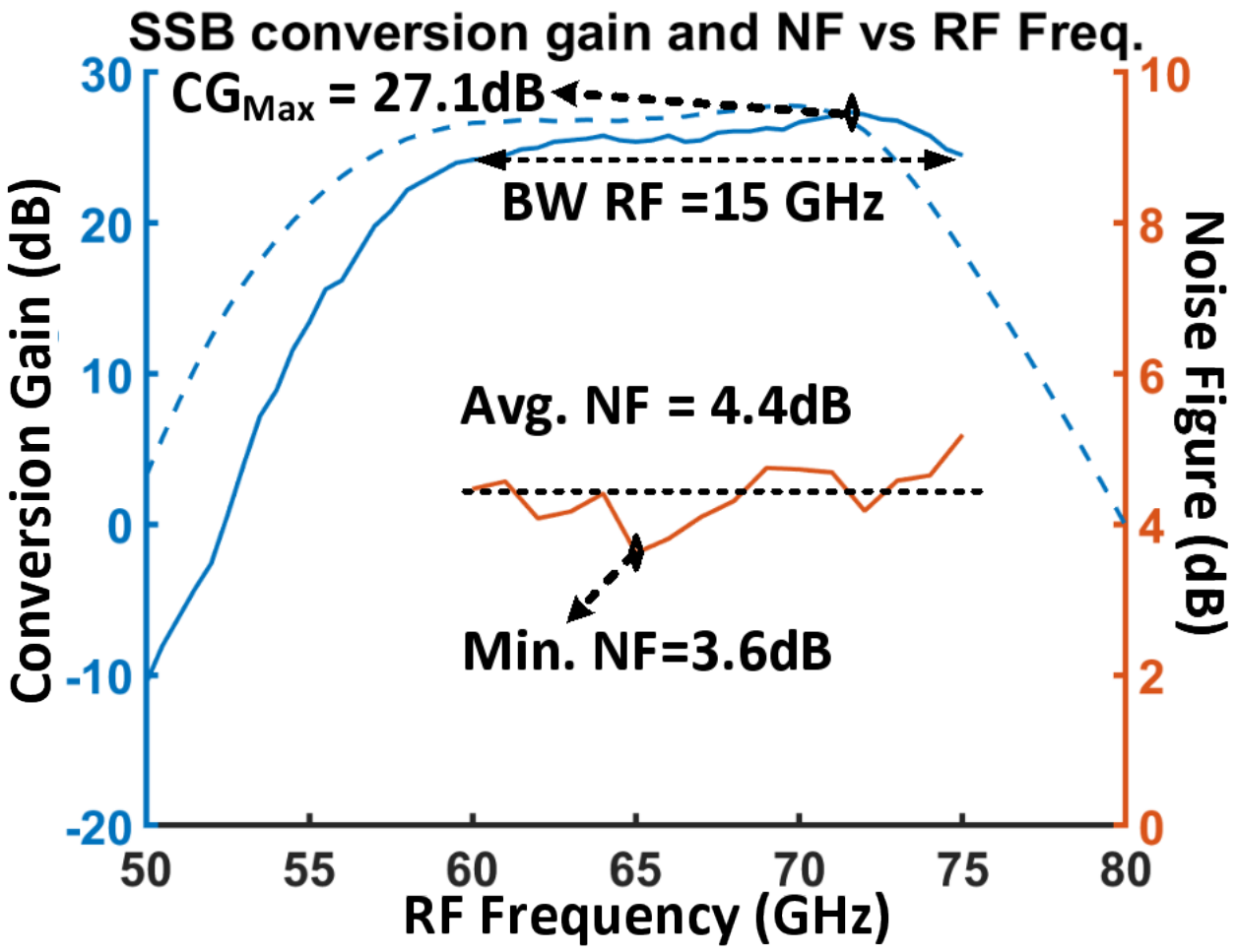
VDI extenders are used to generate V-band frequencies

Conversion gain and noise figure

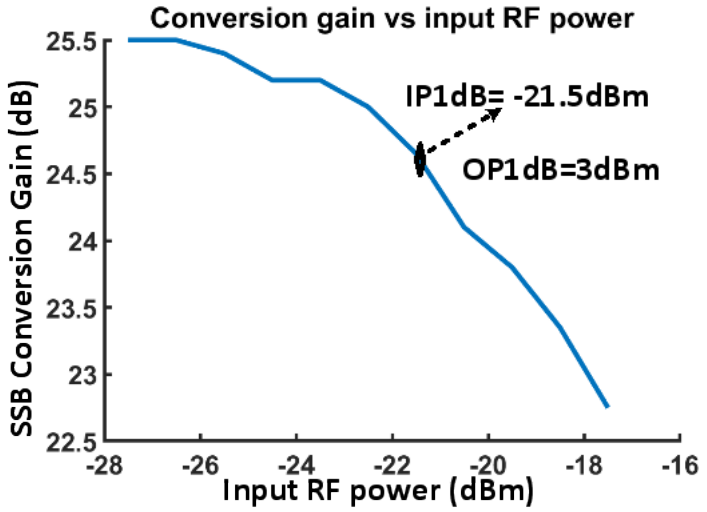
15GHz RF BW, with low ripple

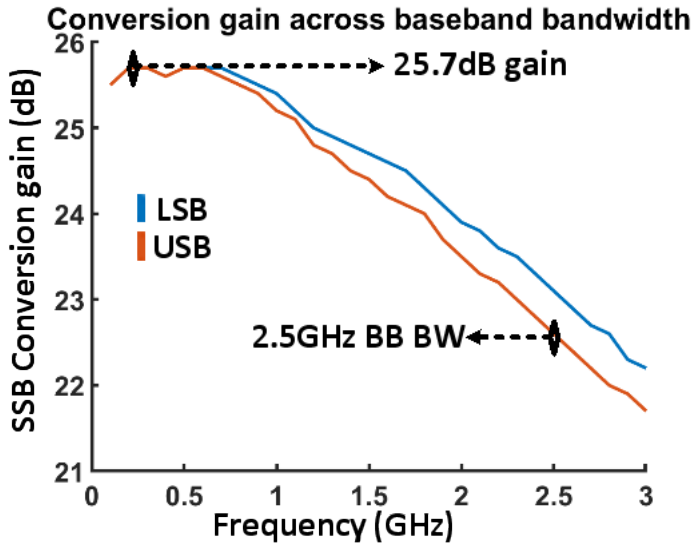
Average NF=4.4dB, 3.6dB min NF

SSB CG=27.1dB



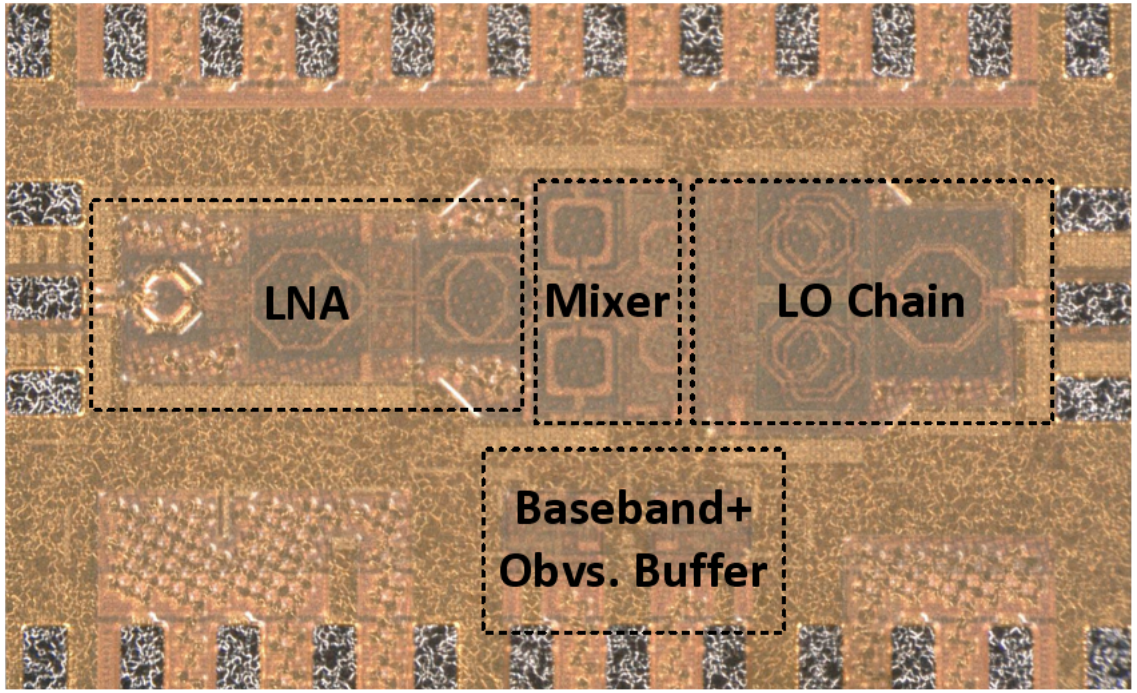
Linearity and BB Bandwidth





- 2.5GHz of BB BW, <0.5dB amplitude mismatch
- 6 degrees of uncalibrated phase mismatch, tunable to <1degree
- IP1dB limited by mixer GM-cell of -21.5dBm IP1dB

Die photo



0.47mm [] active area

Comparison with Prior Art

	This work	M. Vigilante JSSC 17	L. Iotti, ISSCC 18	D. Cai TMTT 13	T. Jang JSSC 2021	A. Kankuppe ESSCIRC 22
P_{DC} [mW]	23	57	12	8	153.4	67
Min. NF [dB]	3.6	9.5	8	4.9	10.8	8
Conv Gain [dB]	27.1	23.6	25.1	55	28.2	55
F_C [GHz]	67	75	85	60	120	147
RF BW [GHz]	15	21.7	10*	3.5	26	18
IP1dB [dBm]	-21.5	-25.3	-20.4^{x}	-51	-26.7	NA
Area [mm^2]	0.47	0.675	0.085	0.56	1.52	3.6

*Estimated from plot, S11 BW 30GHz ^{x}Estimated average from plot

Conclusions

- Bias point scaling and complementary current reuse are powerful tools for receiver power reduction
- Introduces new doubler structure showing excellent efficiency in small area

Acknowledgements

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- Christopher Nordquist for helpful technical discussions and measurement support
- Laboratory Directed Research and Development program at Sandia National Laboratories for the funding support