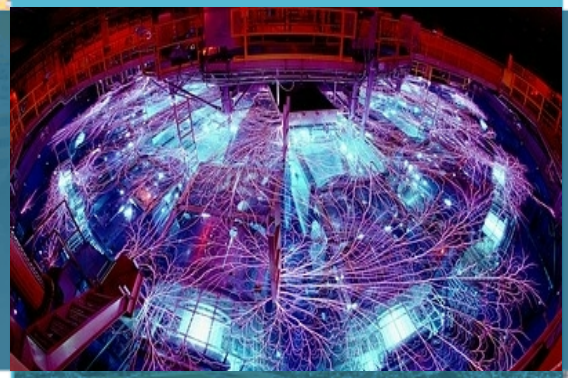
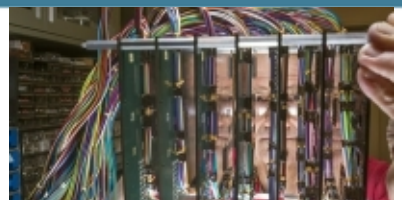
SAND2022-11384C

Sandia National Laboratories

Reliability of GaN power devices: Current status and Future challenges





Ozgur Aktas, Gregory Pickrell, Robert Kaplar

2022-08-24

Power Electronics & Energy Conversion Workshop, Albuquerque, NM.

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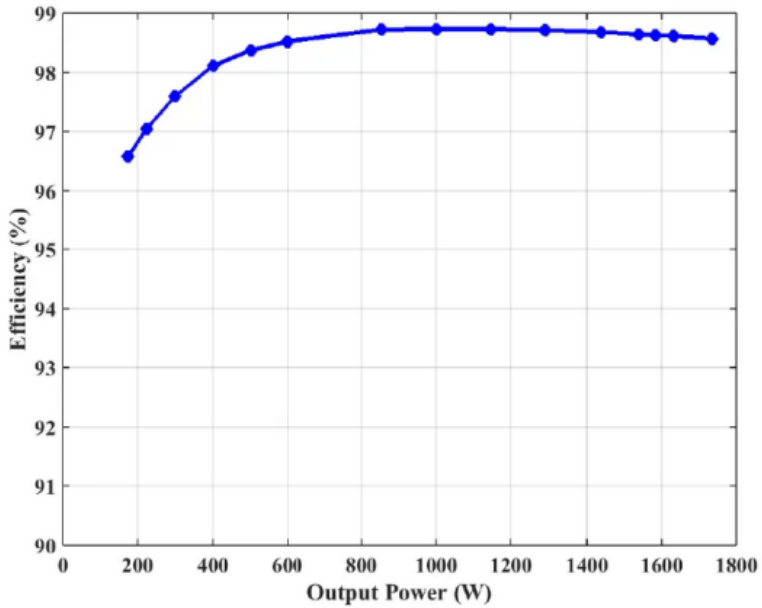
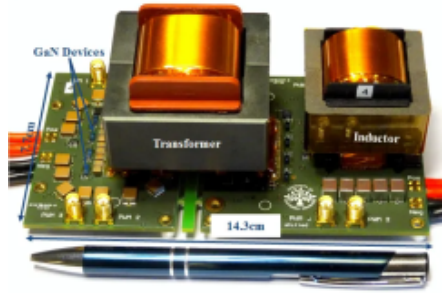
GaN IMPACT

GaN has changed the world !

- Blue and White LEDs
- RF HEMT transistor
- HEMT power switch
- Vertical power rectifiers and switches
- Micro-LEDs



R. Ramachandran, M. Nymand, "A 98.8% Efficient Bidirectional Full-Bridge Isolated DC-DC GaN Converter," 31th Annual APEC Conference Proceedings 2016, Mar 2016



Under development:

- New and improved GaN RF and Power devices
- Integrated logic and power
- Optically triggered switches

Fraunhofer IAF

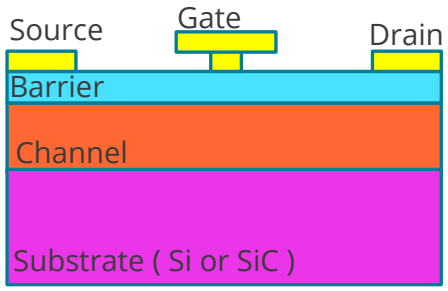
86% driver efficiency
22W power consumption
2680 lm
120 lm/W
Fraunhofer press release

Critical Aspects of GaN Devices

LED	RF HEMT	HEMT power switch	Vertical Power Rectifier and Switch
Grown on sapphire Vertical current flow InGaN QW High IF, low VR	Grown on SiC Lateral current flow High current 2DEG High IF, low VR	Grown on Si Lateral current flow Medium current 2DEG High IF, high VR	Grown on fs-GaN and Si Vertical current flow No 2DEG High IF, high VR
Huge volumes High yield Good reliability	High volumes High yield High reliability	Ongoing adoption Yield optimizations Established reliability	Under development Performance optimizations Reliability under study

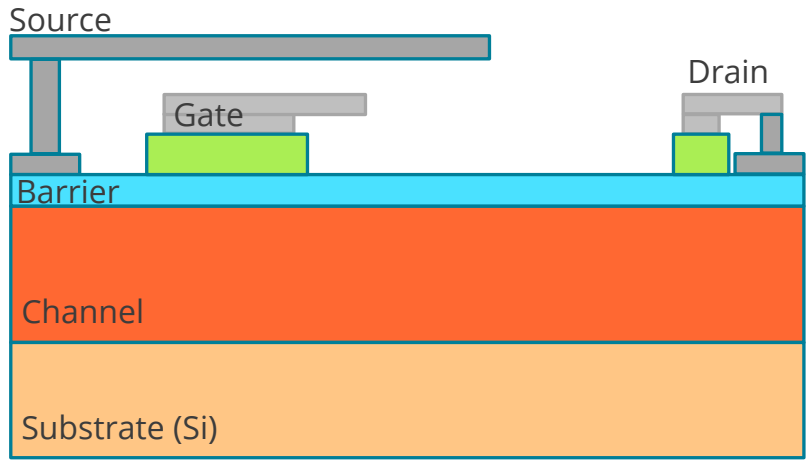
RF-HEMT vs Power-HEMT

RF-HEMT



Higher breakdown
Lower voltage margin
Similar current density
Lower power density

Power-HEMT

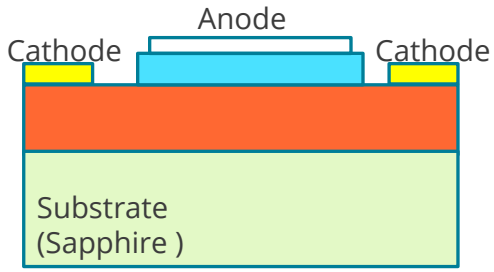


200V breakdown
50V rated
0.3 to 1 A/mm current density
Large devices ~1 to ~10 mm
Chips around 10 mm^2
Chip power density ~50W/mm^2

1200V breakdown
600V rated
~0.3 A/mm current density
Large devices 100 to 300 mm
Chips around 50 mm^2
Chip power density ~10W/mm^2

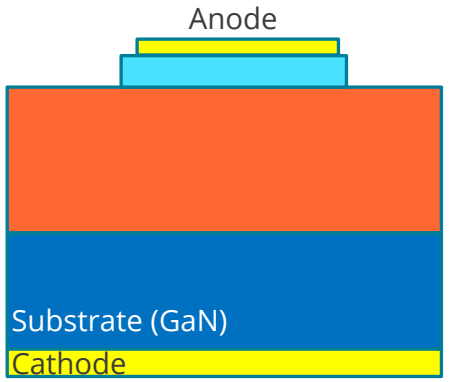
LED vs Power-diode

LED



Higher breakdown
Much lower voltage margin
Higher current density
Higher power density

Power-Diode



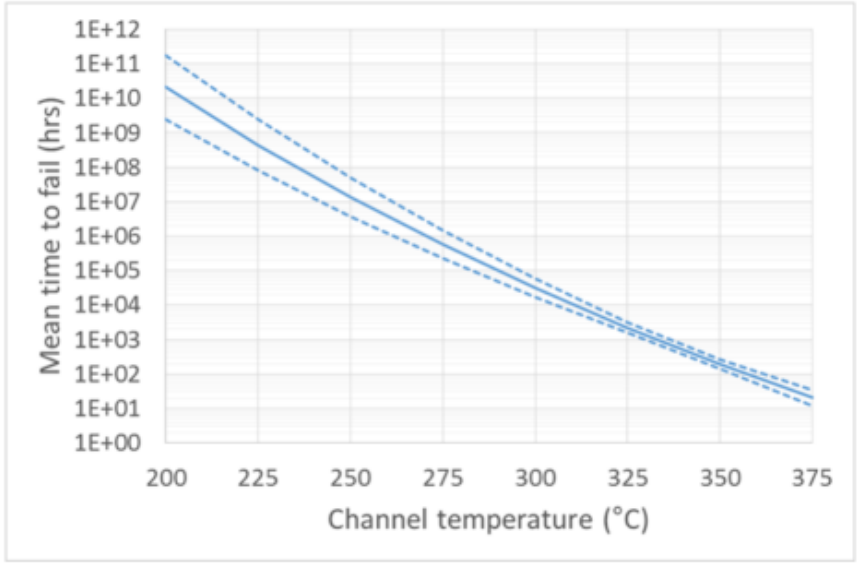
Less than 100V breakdown
Forward current operation only
~1 A/mm^2 current density
Large devices at around 1mm^2
Chip power density ~3 W/mm^2
Optical emission ~60% of power

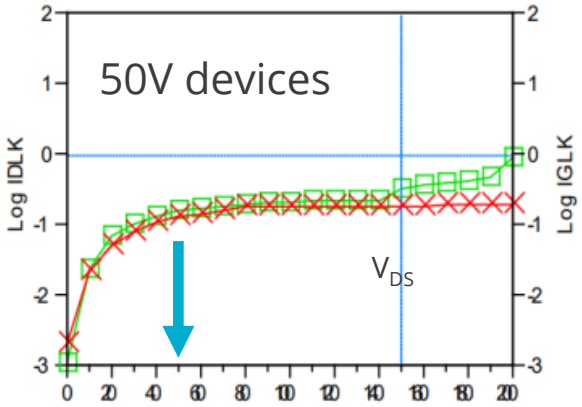
1250V breakdown
1200V rated
~10 A/mm^2 current density
Large devices at around 4mm^2
Chip power density ~30 W/mm^2
Non-radiative recombination

RF-HEMT reliability status

- Qualification Procedures in place
- 28V devices: IDON degradation under IF, ALT tests to 310 °C
- 50V devices: IDOFF increase and breakdown, ALT tests to 355 °C
- Activation energy
  - 28V devices: ~2eV
  - 50V devices: ~3.1eV
- Assumptions
  - Zero random failures
  - Single failure mechanism for random and wear-out failures
- MTTF about 1E10 hours, 0.1 FIT
- Very reliable despite the Schottky gate

Merola, et.al, Reliability of Compound Semiconductors (RoCS) 2018 Austin, Texas





Macom press release

RF-HEMT reliability status

Technology Tests for Device Intrinsic Reliability

- DC-HTOL: 30 devices each at 260, 285, 310C
- RF-HTOL: 12 devices, 500 hours, 0 fails
- Electromigration

Product Device reliability tests

- DC-HTOL: 200C, 28V, 168hrs, 45 samples
- ESD: 1020/MIL-STD-750

Assembly Tests

- THB
- Pressure, temperature, humidity,
- Thermal cycle
- Thermal shock
- Bond strength

Qualification of RF-HEMTs

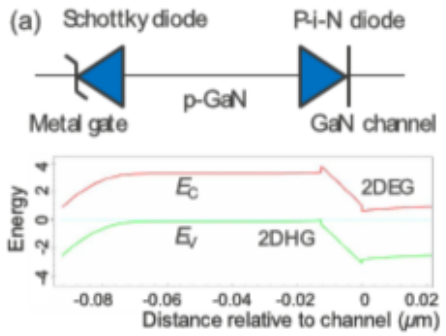
Test Name	Test Standard	Sample Set	Result
3-Temp DC	JEP118-B	30 Devices/Temp @ 260, 285, and 310°C	Ea = 2.0eV, MTTF > 10^7hours at 150°C
DC-HTOL	JESD22-A108	45 devices, 2000 hours	20-yr Imax drift <7% at 200°C 20-yr Imax drift <3% at 150°C
RF-HTOL	JESD22-A101-A	12 Devices, 500 hours	< 0.25dB drift through 500 hours
ESD-HBM	JESD22-A114	9	>1000V (class 1C) for NPT35050
ESD-MM	JESD22-A115	9	>200V (class M3) for NPT35050
Thermal Impedance	IR imaging	9	All samples meet datasheet target of 1.95°C/W for NPT35050
Autoclave	JESD22-A102	45	Minimal change in performance
VSWR	10:1 VSWR	5	Minimal change in performance
Temp. Cycling	JESD22-A104	45	Minimal change in performance
Thermal Shock	M-750-1056	15	Minimal change in performance
Solderability	JESD22-B102	4	Passed
Mech. Shock	M-883-2002	38	Passed
Vibration	M-883-2007	38	Passed
Const. Acceleration	M-883-2001	38	Passed
Moisture Res.	M-883-1004	38	Passed
Salt Atmosphere	M-883-1009	15	Passed
Solvent Res.	M-833-2015	15	Passed
Bond Strength	M-750-2037	15	Passed

Macom Application Note

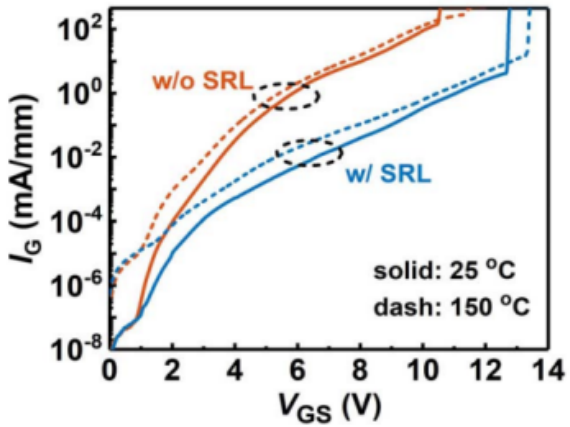
Power-HEMT reliability status

Two main types of power-HEMTs

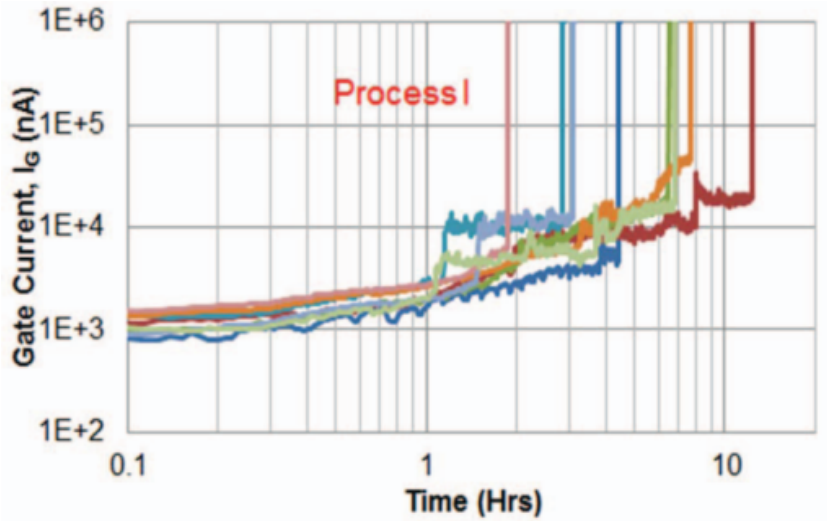
- MISHEMT : Gate breakdown
  - TDDB of gate dielectric
  - Dielectric interface state formation
- p-GaN gate HEMT: Gate breakdown
  - TDDB and defect generation in floating p-GaN layer
  - p-GaN sidewall leakage and degradation



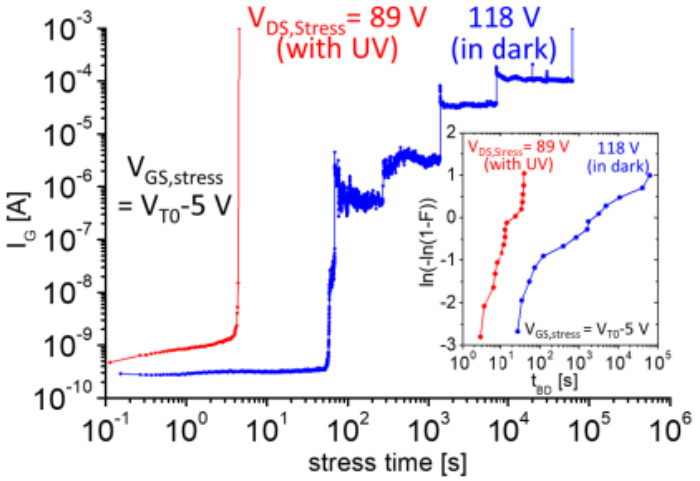
Decoutere, et.al., IEEE-TED vol 68, no 2, Nov. 2021



K.J. Chen et.al., IEEE-EDL vol 42, no 1, Jan. 2021



Veereddy, et.al, IRPS, Monterey, CA, 2017



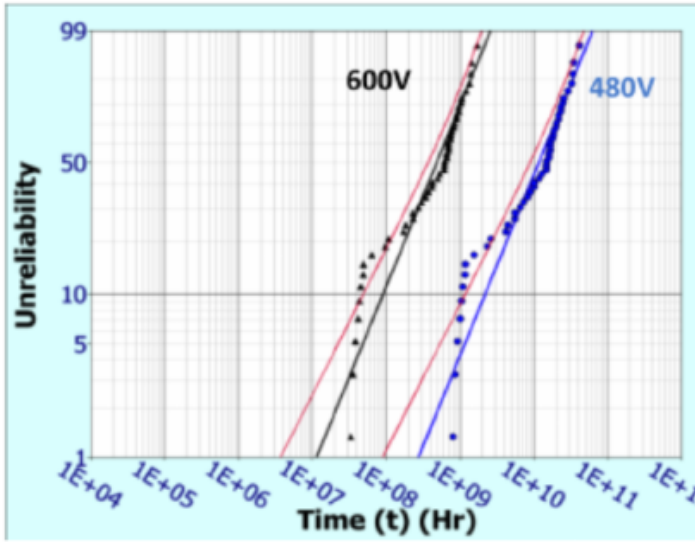
del Alamo & Lee, IEEE-TED vol 66, no 11, Nov. 2019

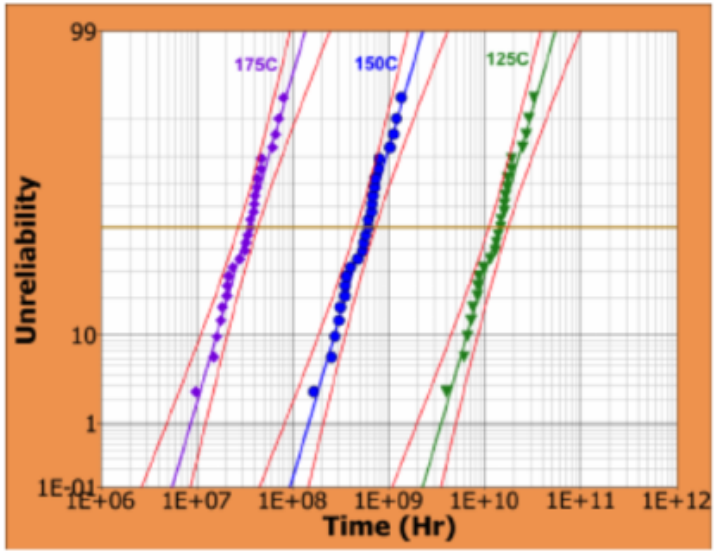
Power-HEMT reliability status

In open literature, conflicting reports of Ea from MISHEMT

- E_a from Infineon : E_a=0.7 to 0.9eV
- E_a from Transphorm : E_a=1.8eV
- V_α from Transphorm : V_α= 0.026 V^{-1}

p-GaN gate HEMT qualified with low FIT, no open data on E_a





Transphorm press release 2018

Transphorm press release 2019

MISHEMT has demonstrated high reliability
- Random failures: FIT: 3.1
- Intrinsic MTBF: 1E11 hrs

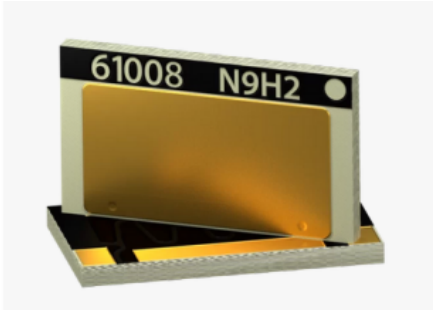
Power-HEMT reliability status

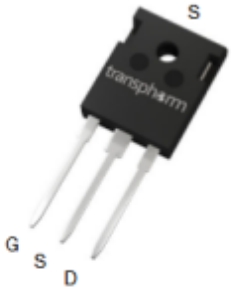
Technology still evolving fast

Baseline reliability plan established

JEDEC working on establishing and improving related standards

Packaging solutions have been developed





Electrical Stress Test Results:

Test Description	Abbr.	Condition	Duration	Lots/SS	Fail/Qty	Result
High Temperature Storage Life *JESD22-A103*	HTSL	T_a = 150 °C	1000 h	3 x 45	0 / 135	PASS
High Temperature Reverse Bias *JESD22-A108*	HTRB[1]	T_a = 150 °C V_{DS} = 600 V	1000 h	3 x 77	2^3 / 231	Cond. PASS
Positive High Temperature Gate Stress *JESD22-A108*	HTGF[1]	T_a = 150 °C I_D = 50 mA	1000 h	3 x 77	0 / 231	PASS
Negative High Temperature Gate Stress *JESD22-A108*	HTGS[1]	T_a = 150 °C V_{GS} = -10 V	1000 h	3 x 77	0 / 231	PASS
Intermittent Operational Life Test *MIL-STD 750 / Meth.1037*	IOL[1]	ΔT = 100 K	15,000x	3 x 77	0 / 231	PASS
ESD (HBM) *JESD22-A114*	HBM	Class 2 (2000 V to <4000 V)		1 x 3 (per voltage level)	0 / 3	PASS
ESD (CDM) *JESD22-C101*	CDM	Class C3 (1000 V or greater)		1 x 3 (per voltage level)	0 / 3	PASS

Environmental Stress Test Results:

Test Description	Abbr.	Condition	Duration	Lots/SS	Fail/Qty	Result
Pre-Conditioning *J-STD020 / JESD22 A113*	PC	MSL and 3 x reflow		3	0	PASS
High Humidity, High Temperature Reverse Bias *JESD22 A101*	H^{3}TRB[1]	T_a = 85 °C r.h. = 85% V_{DS} = 100 V	1000 h	3 x 77	0 / 231	PASS
Biased Highly Accelerated Stress Test *JESD22 A110*	HAST[1]	T_a = 130 °C r.h. = 85% V_{DS} = 480 V	192 h	3 x 77	0 / 231	PASS
Temperature Cycling *JESD22 A104*	TC[1]	-55 °C to +150 °C	1000x	3 x 77	0 / 231	PASS

Mechanical Stress Test Results:

Test Description	Abb	Condition	Duration	Lots	Fail/Qty	Result
Moisture Sensitivity Level *IPC / J-STD-020*	MSL	MSL 3 @ 260 °C			0 / 22	PASS

Additional, Non-Standard Reliability Test Data

Test Description	Abbr.	Condition	Duration	Lots/SS	Fail/Qty	Result
Dynamic High Temperature Reverse Bias	dynHTRB[1]	T_a = 150 °C V_{DS} = 600 V f = 100 kHz	1000 h	3 x 77	0 / 231	PASS
Dynamic Gate Current Bias	dynGCB	T_a = 150 °C f = 100 kHz	1000 h	1 x 14	0 / 14	PASS
High Voltage, High Humidity, High Temperature Reverse Bias	HV-H^{3}TRB[1]	T_a = 85 °C r.h. = 85% V_{DS} = 480 V	1000 h	3 x 77	0 / 231	PASS
Unbiased Highly Accelerated Stress Test *JESD22 A118*	uHAST[1]	T_a = 130 °C r.h. = 85%	192 h	3 x 77	0 / 231	PASS
Low Temperature Reverse Bias	LTRB[1]	T_a = 0 °C V_{DS} = 600 V	1000 h	1 x 77	0 / 77	PASS
Positive Low Temperature Gate Stress	LTGF[1]	T_a = 0 °C I_D = 50 mA	1000 h	1 x 77	0 / 77	PASS
Negative Low Temperature Gate Stress	LTGS[1]	T_a = 0 °C V_{GS} = -10 V	1000 h	1 x 77	0 / 77	PASS
Positive High Humidity, High Temperature Gate Stress	H^{3}TGF[1]	T_a = 85 °C r.h. = 85% I_D = 50 mA	1000 h	1 x 77	0 / 77	PASS
Negative High Humidity, High Temperature Gate Stress	H^{3}TGS[1]	T_a = 85 °C r.h. = 85% V_{GS} = -10 V	1000 h	1 x 77	0 / 77	PASS
High Load Test		T_a = 25 °C V_{DS} ≤ 600 V I_D = 15 A (mean) f = 100 kHz	1000 h	1 x 10	0 / 10	PASS
Autoclave JESD22 A102	AC[1]	Ta = 121 °C r.h. = 100%	192 h	3 x 77	0 / 231	PASS

Infineon Application Note

GaN LED reliability

Degradation mechanisms

- Reverse bias stress:
  - reverse leakage increase due to defect creation
- Forward bias stress:
  - reverse and forward leakage increase due to defect assisted dopant diffusion
- Forward bias stress:
  - optical power reduction due to ohmic and p-GaN degradation due to hydrogen movement and bad ohmics

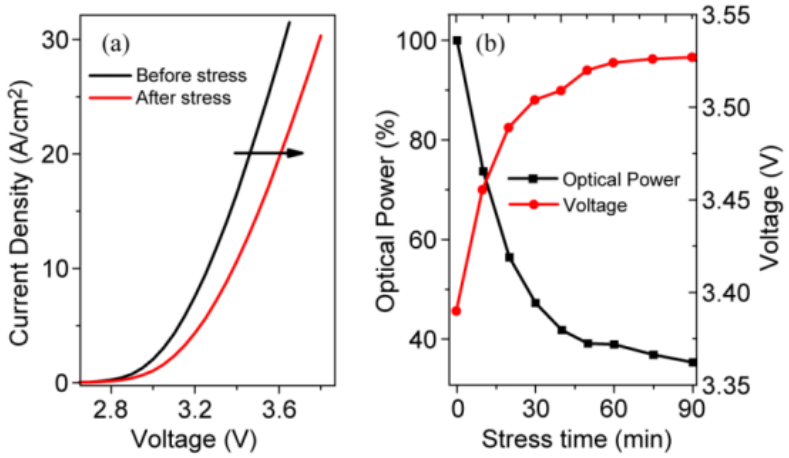


Fig. 12. (a) I–V characteristics measured before and after stress at high temperature (90 min at 250 °C) on a blue LED. (b) Optical power decrease and operating voltage increase measured (at 16 A/cm^2) during stress at high temperature (90 min at 250 °C) on a blue LED.

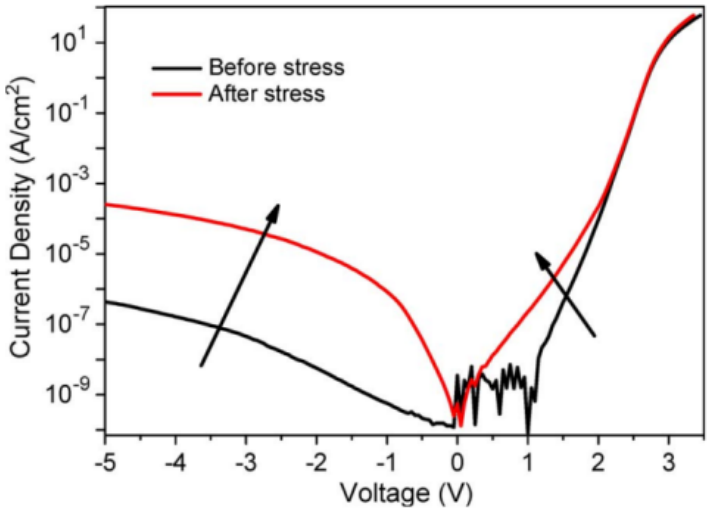


Fig. 3. I–V characteristics measured before and after stress at 85 A/cm^2 on one of the analyzed samples.

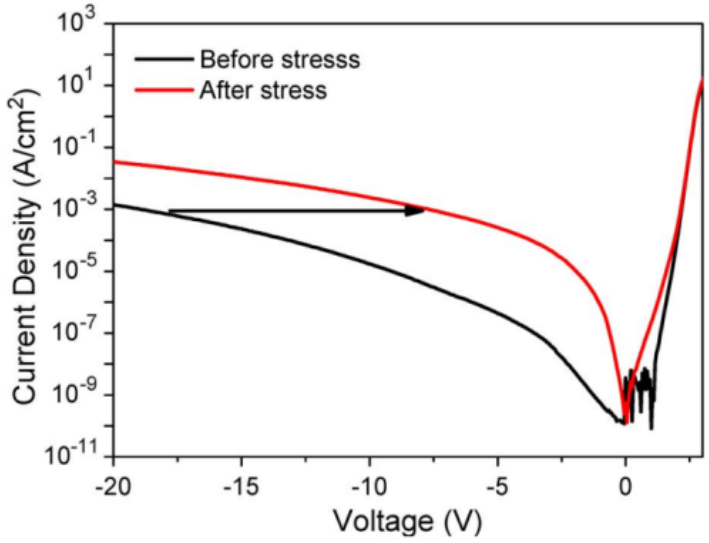


Fig. 7. I–V characteristics measured before and after reverse-bias stress on one of the analyzed samples (stress conditions are −1.2 A/cm^2, RT).

Zanoni, et.al., IEEE-TED vol 57, no 1, Jan. 2010

Vertical Diode Device Reliability Status

Observed failure mechanisms

- TDDB under reverse bias
  - JTE or defect related
  - Likely impacted by passivation
- R_{ON} , V_F and I_R increase under forward current
  - Hydrogen diffusion related
- V_{BR} increase under avalanche
  - C trap related

Improvements in device design and fabrication being developed

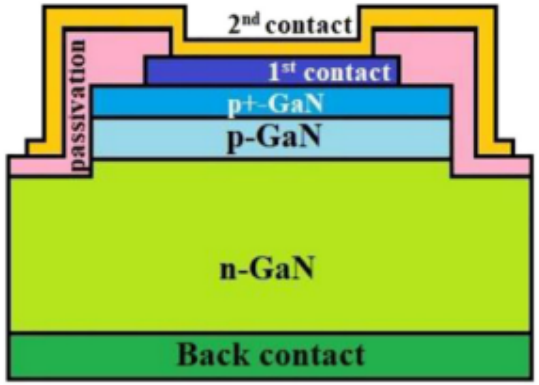
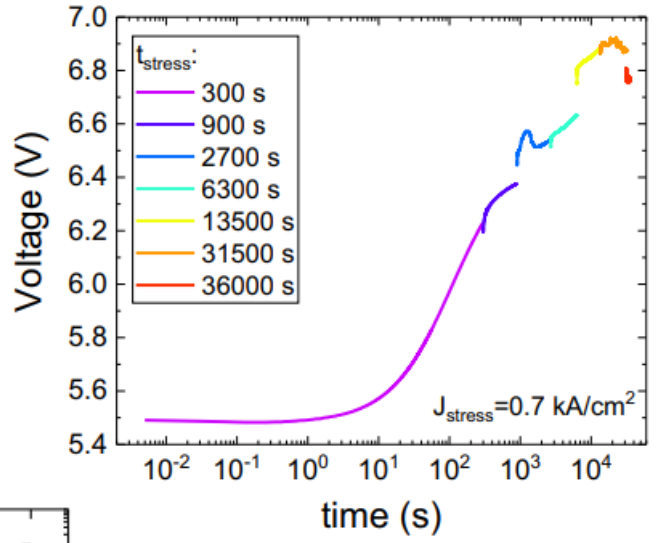
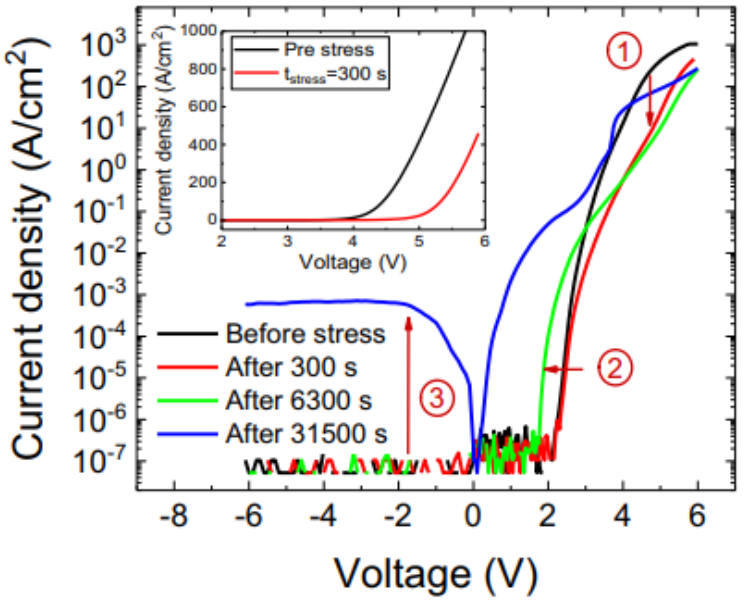


Fig. 1. Schematic cross-section of the vertical GaN pn diode.

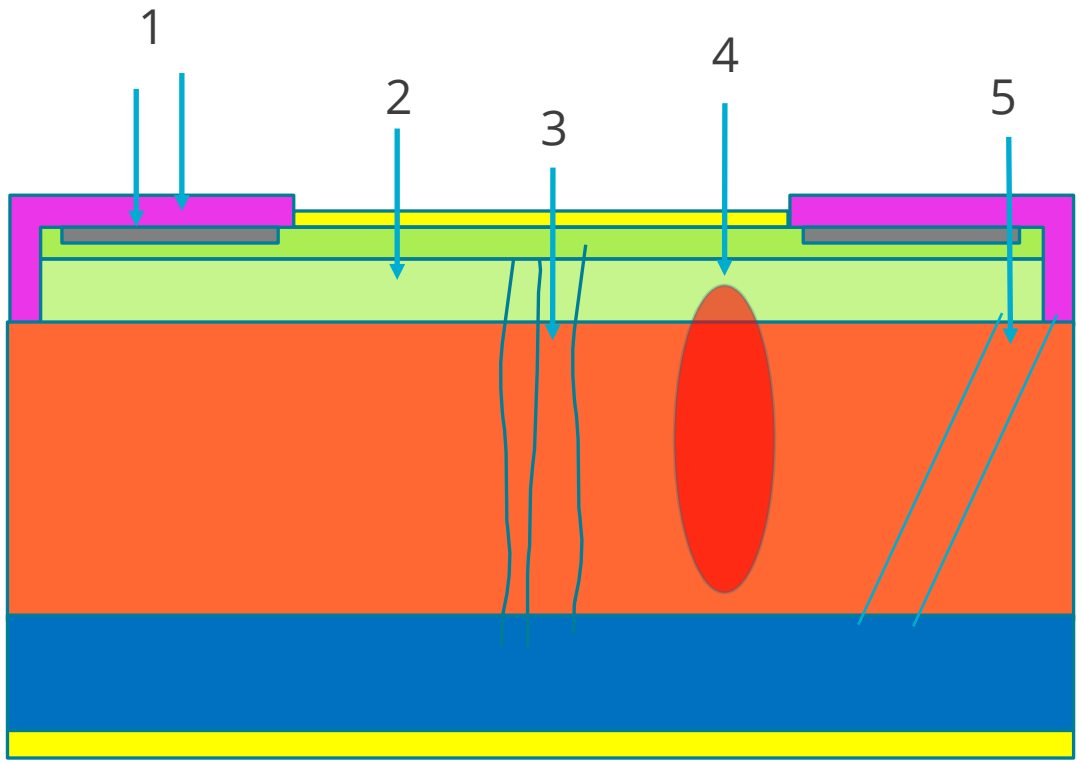




Zanoni, et.al., Microelectronics Reliability, vol 88-90, pp. 568-571, 2018.

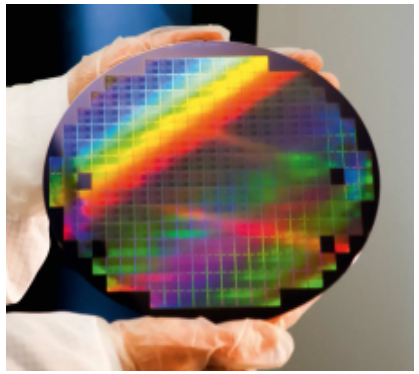
Vertical GaN Diode: Possible failure mechanisms and Path Forward

1. Dielectrics and surface leakage
   a) Research dielectrics and optimize surface
   b) Design JTE with safety margins
2. Recombination
   a) Research device design options
3. Leakage through dislocations
   a) Identify killer defects
   b) Identify corrective actions
   c) Improve wafer quality
4. Compensation
   a) Reduce impurities, defects
   b) Improve doping control
5. BPD/stacking faults
   a) Improve wafer quality

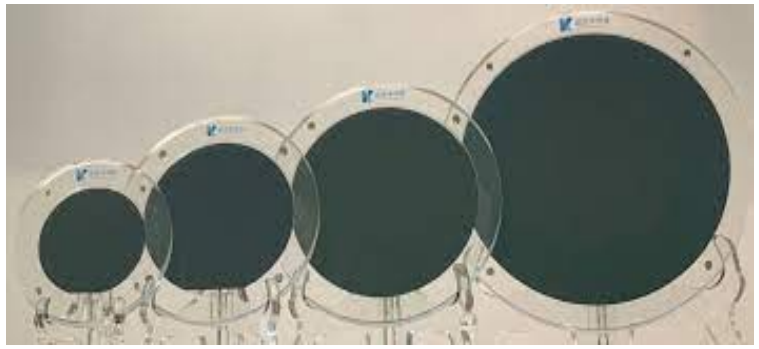


Vertical GaN: Promise

High-performance and cost-efficient power devices on large area substrates manufactured with a Si CMOS compatible technology



Aledia press release



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Thanks…

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