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Carnegie Mellon University

A Radiation Hardened by Design FPGA with Distributed Single Event Upset Sensors, Embedded Error Handler, and 8Mb Embedded MRAM Configuration Storage in 22nm Bulk FinFET CMOS

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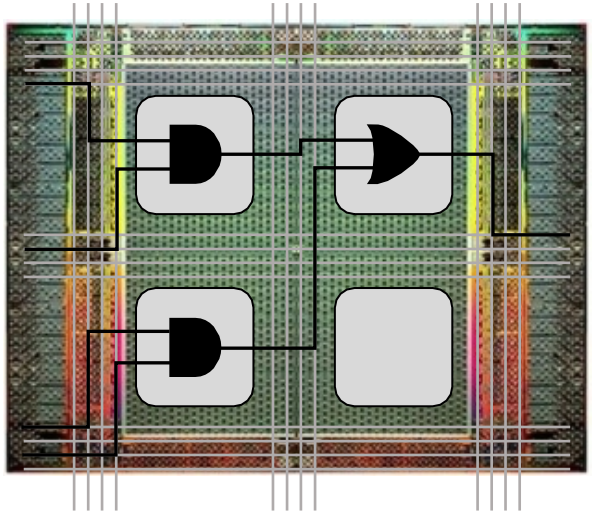
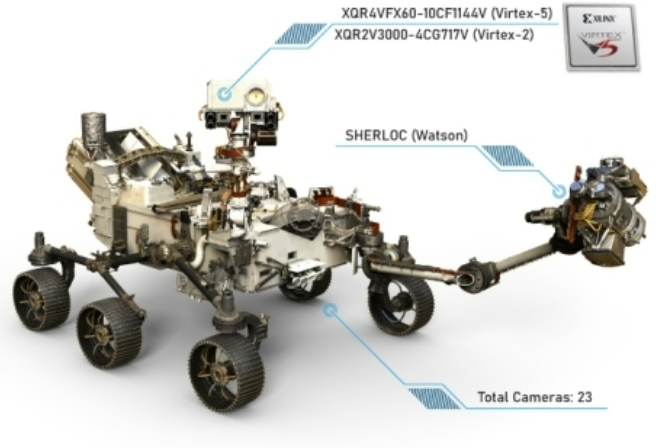
Field Programmable Gate Arrays (FPGAs)

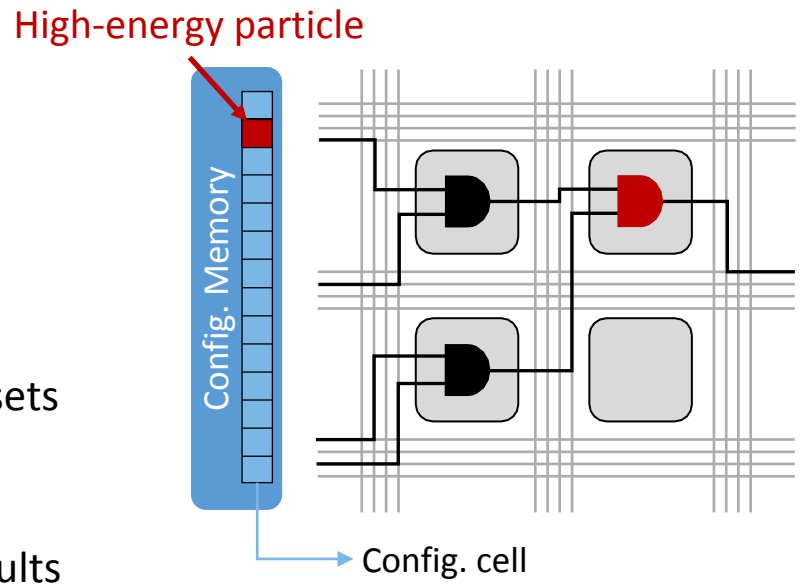
- FPGAs offer:
  - Short design times and flexibility
  - Performance and efficiency
  - (Re)programmable hardware
- Widely deployed in high-reliability applications
  - Aerospace - Image analysis, control, communication
  - Automotive – Driver assistance, autonomous cars
  - Data centers – Acceleration, glue logic
- Radiation-induced errors cause reliability concerns in these spaces





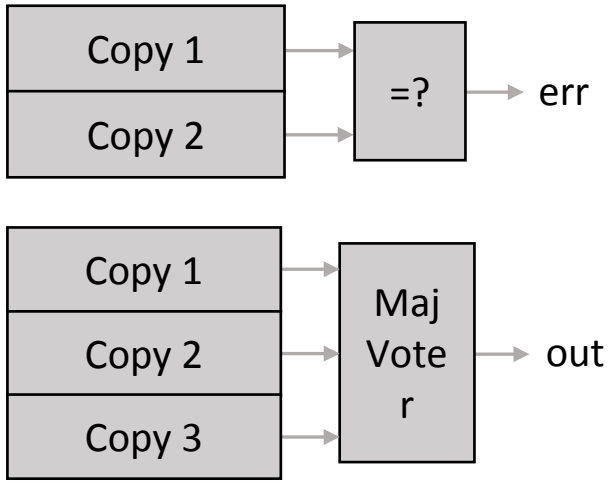
FPGA Structure and Radiation Concerns

- FPGAs contain repeated elements
  - Programmable logic (CLBs)
  - Programmable interconnect (SBs, CBs)
  - SRAM config memory
- Configuration memory is the Achilles heel
  - Configuration cells are vulnerable to radiation-induced upsets
  - Bit flips in configuration cells can break functionality
  - Vendors provide IPs to mitigate errors and publish test results
  - Multiple bit flips common in more advanced processes



Existing Radiation Hardening Approaches

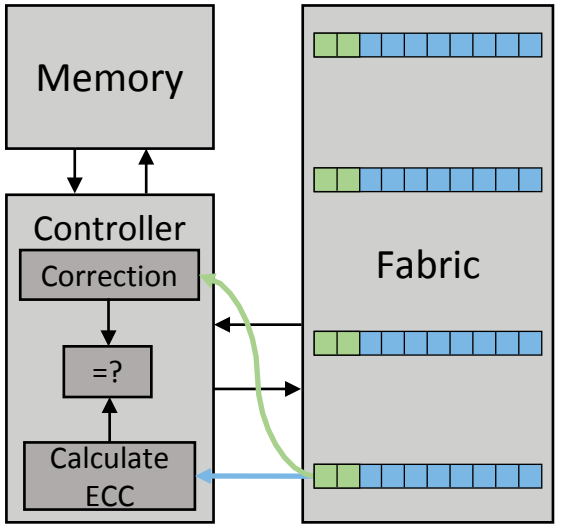
Modular Redundancy



Errors are not corrected

Needs to be paired with other approaches

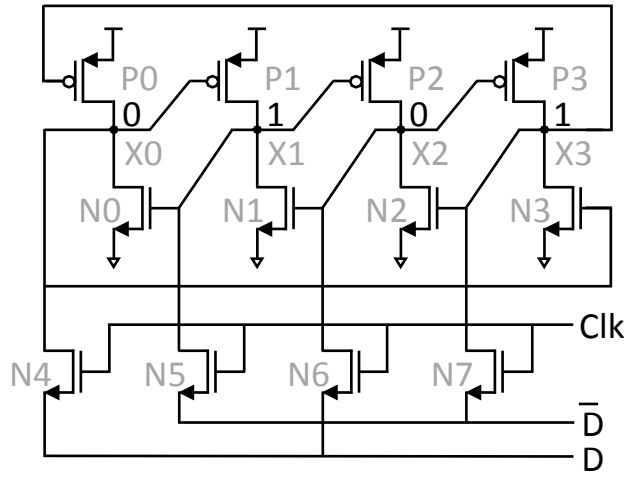
ECC / Scrubbing



High latency

Multi-bit errors on the same row cause problems

DICE



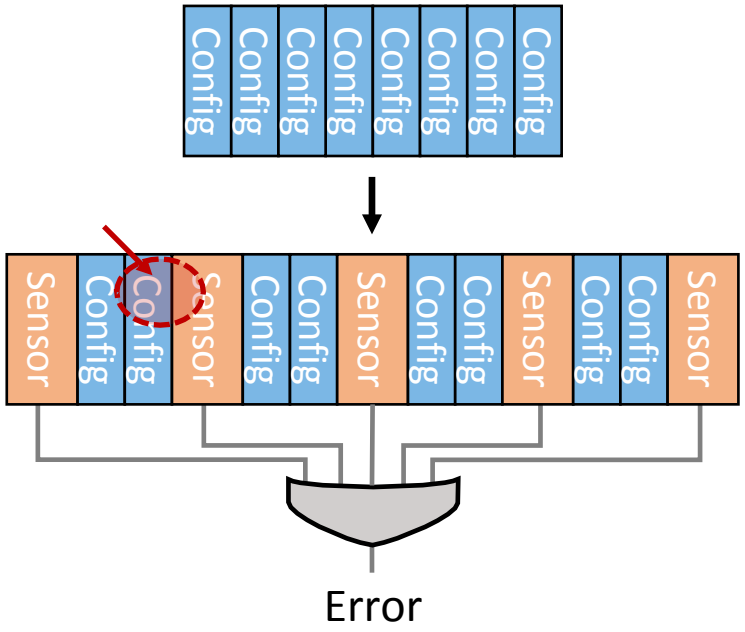
Significant area overhead

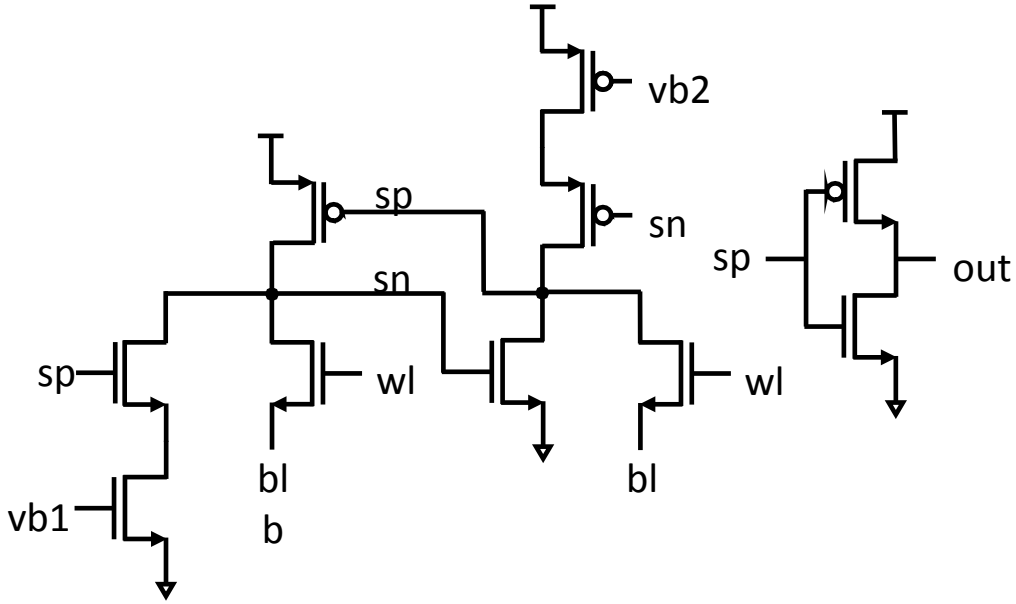
Can fail when multiple nodes collect charge

Get worse with process scaling!

SEU Sensors

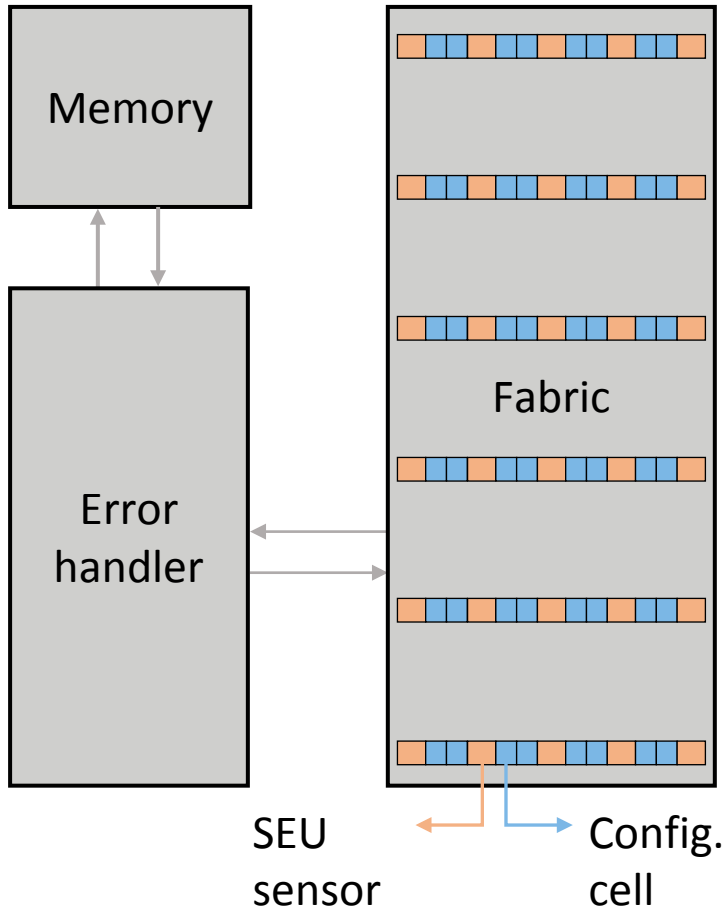
- SRAM-like, tunable sensor cells allow localized & fast error detection
- Gets more effective with process scaling



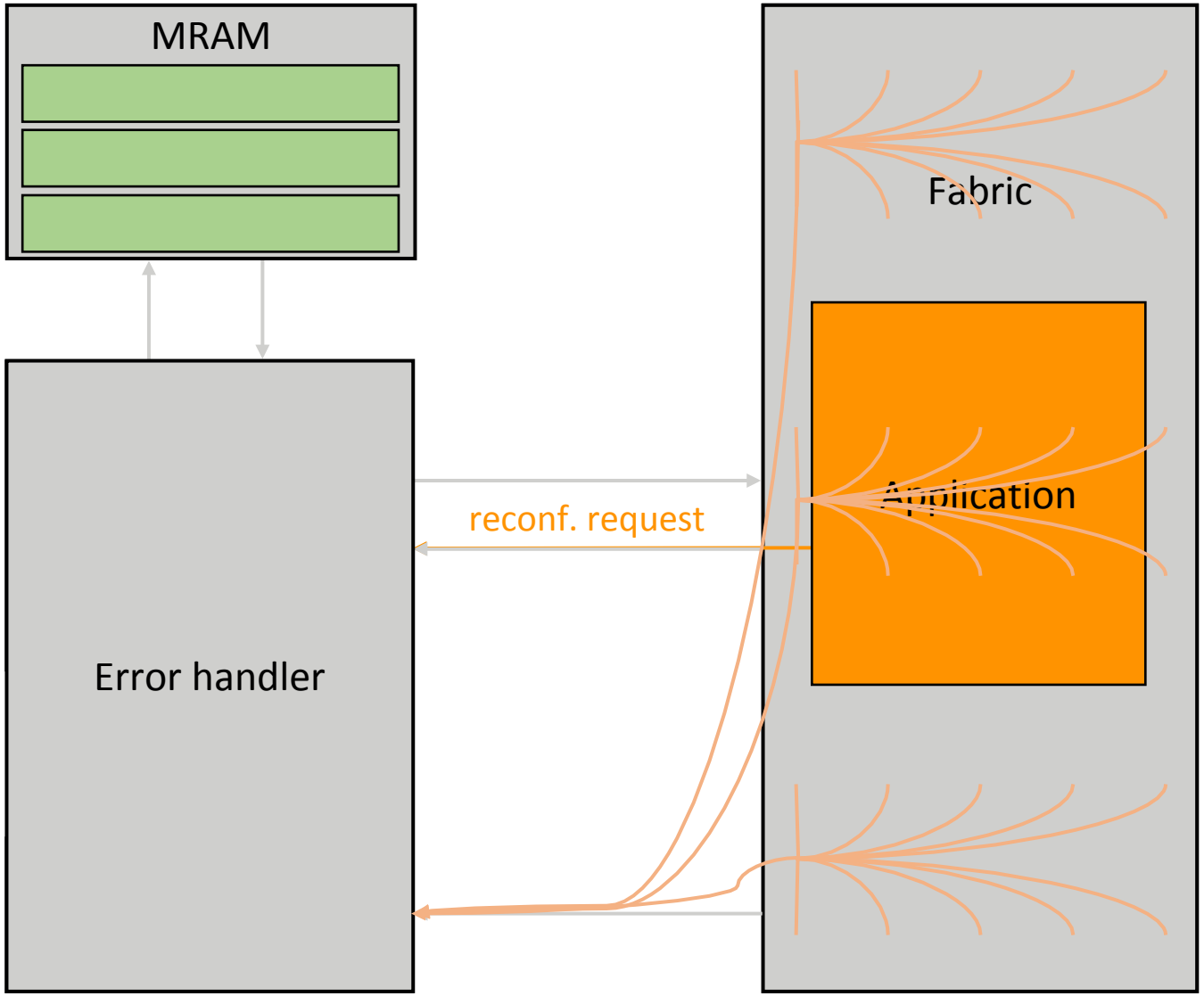


Radiation-Hardened FPGA with Sensors

- Config. memory with SEU sensors
  - Low-latency error detection
  - Localized error flags
- Memory
  - MRAM-based, non-volatile
  - Store config. data & info for handler
- Error handler
  - Interface to the memory, fabric
  - Process requests from sensors, application

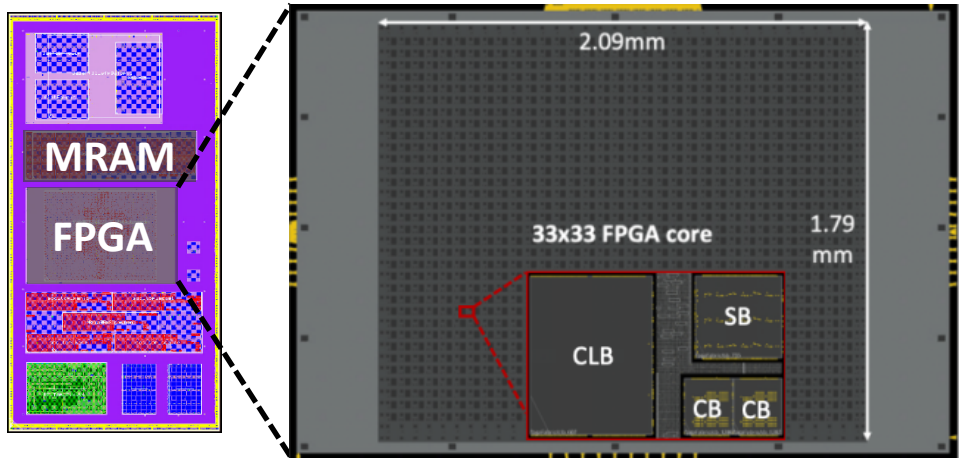


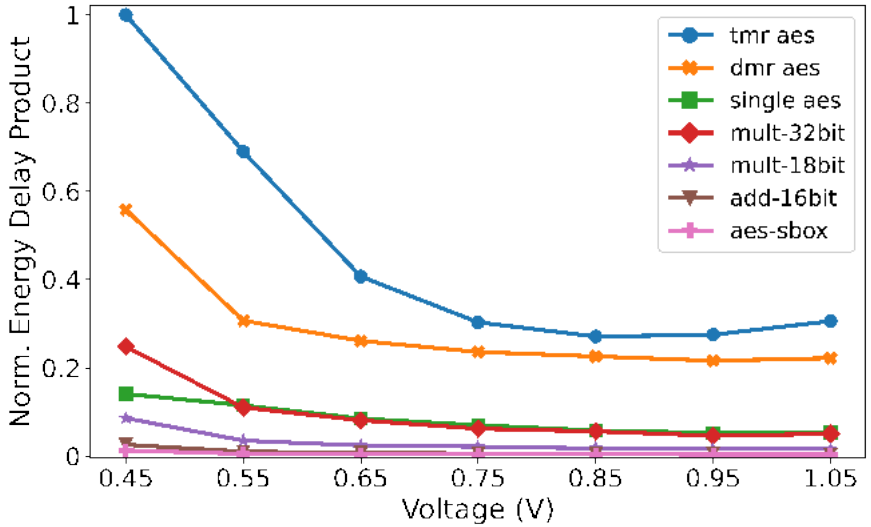
Error Handler

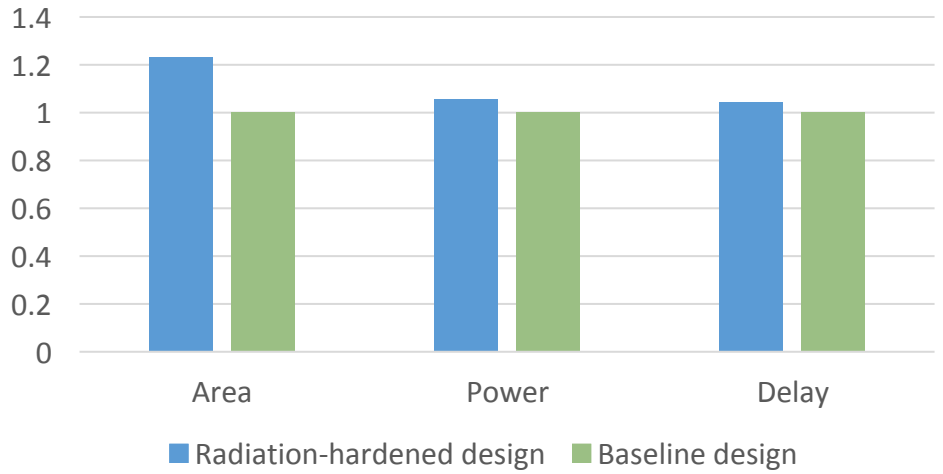


Radiation-hardened FPGA Test Chip

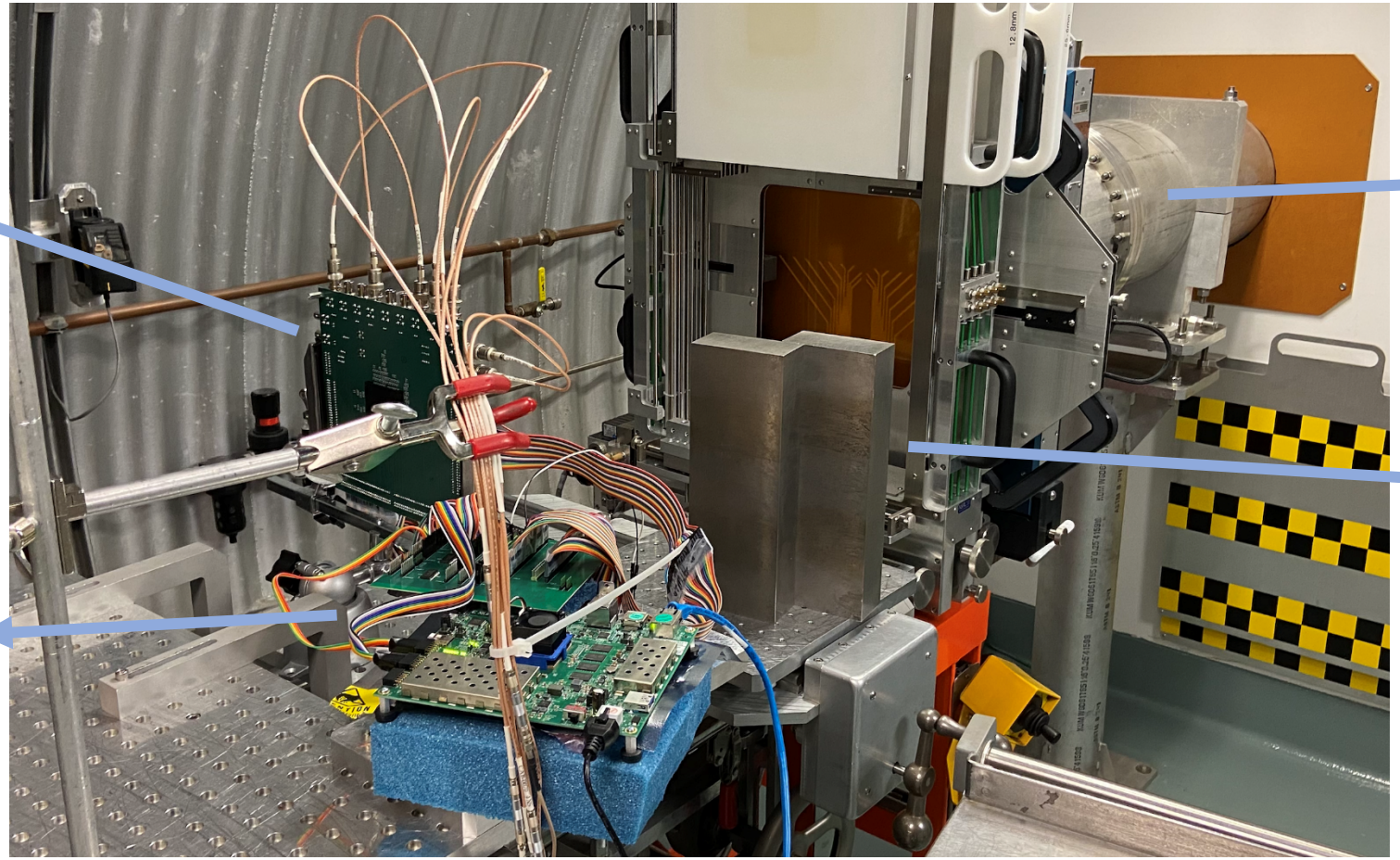
- Fabricated in 22nm FinFET process
- 33x33 tiles, 72 channels
- 6534 6-input fracturable LUTs





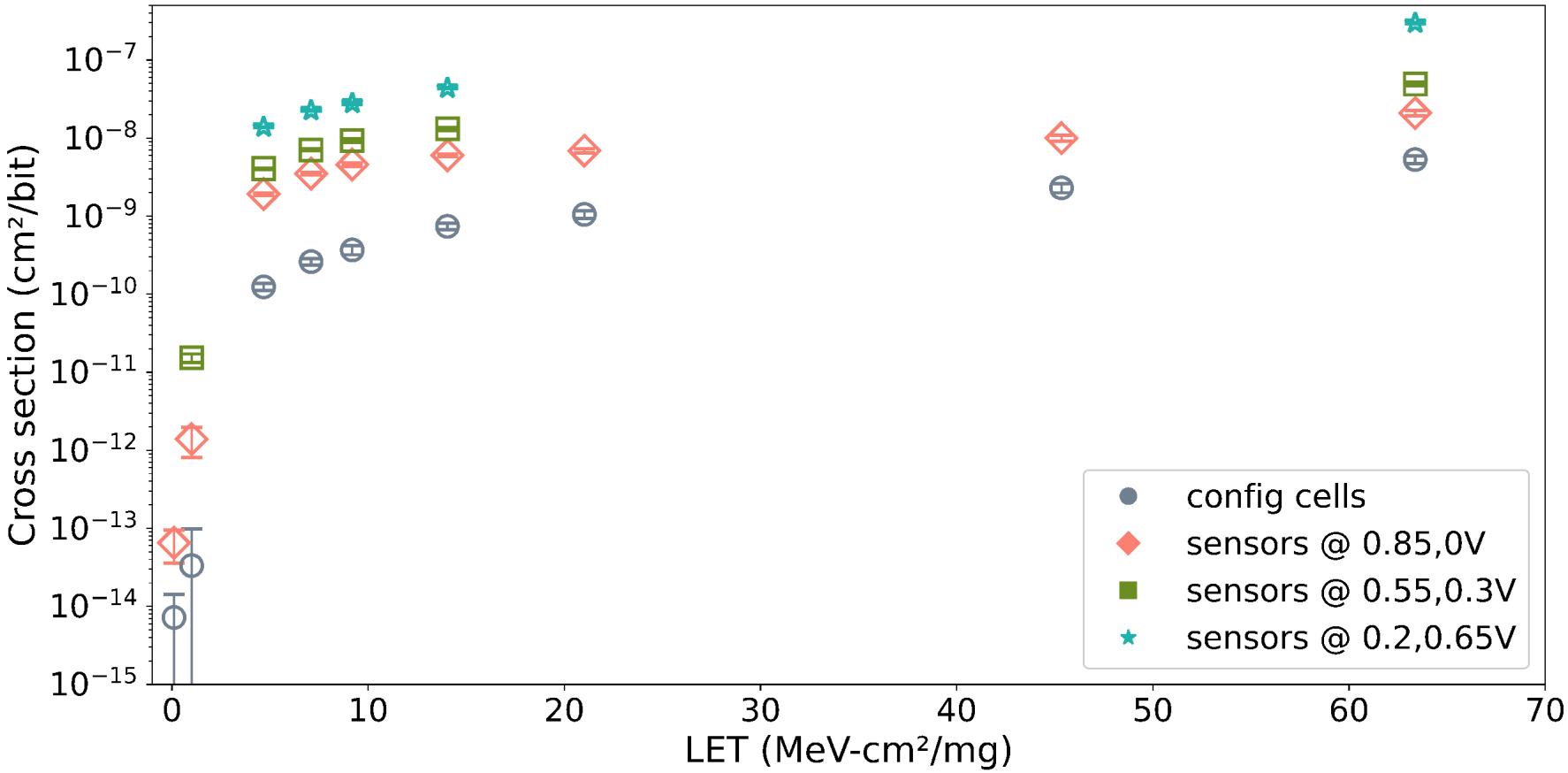


Heavy Ion Tests



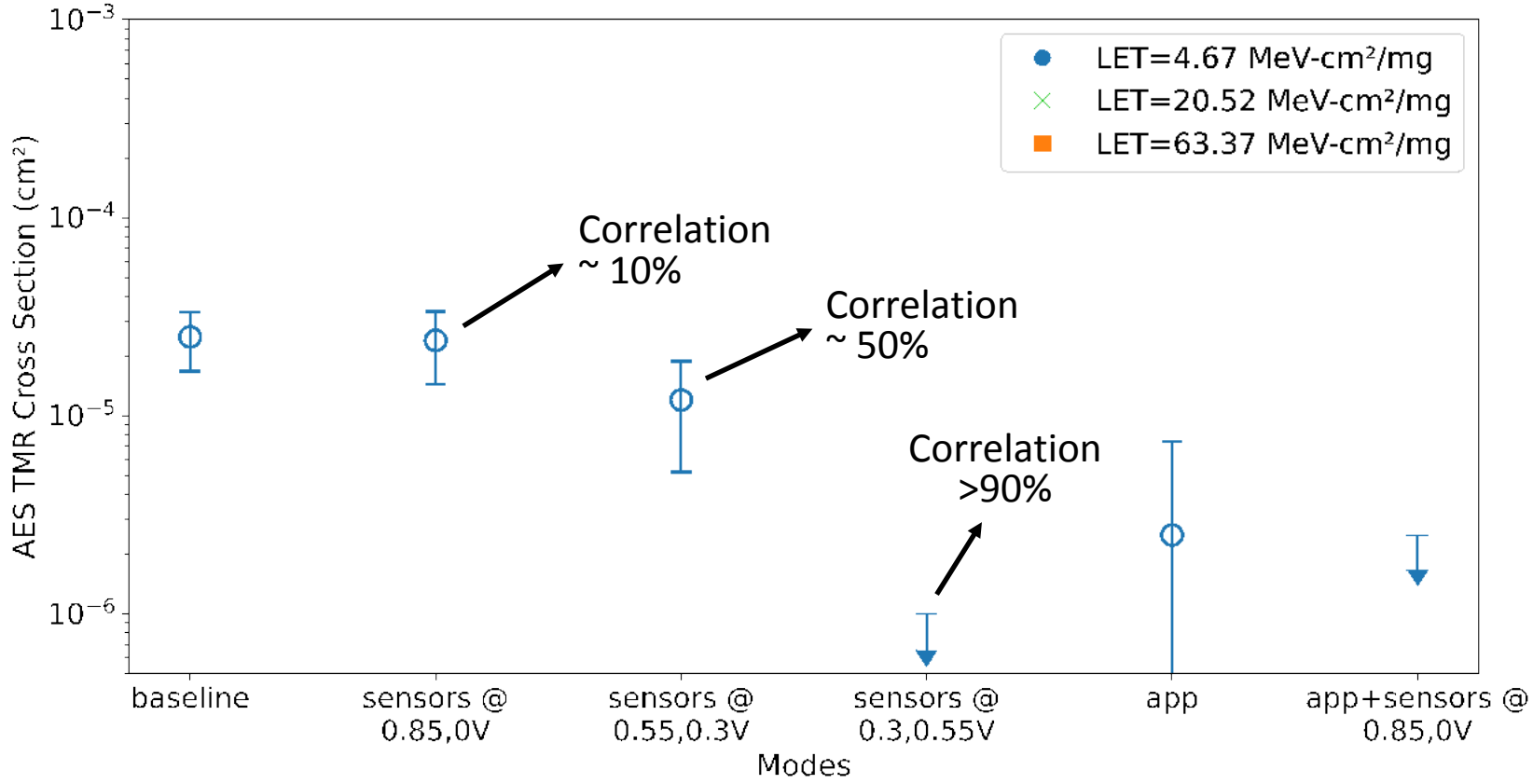
Tested @ NASA Space Radiation Lab. in Brookhaven National Laboratory

Sensor & Config. Cell Cross Sections



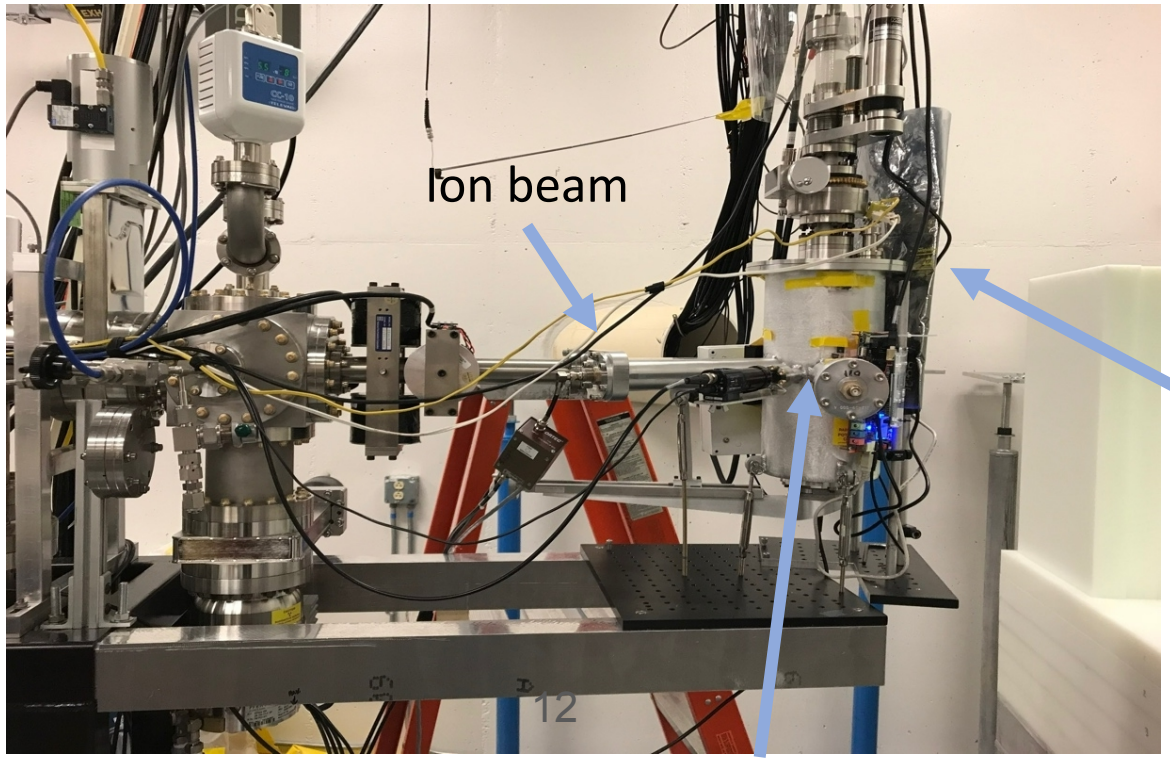
- Sensors are more vulnerable than config. cells
- Sensors become even more vulnerable when the bias voltages are tuned

TMR AES-128 with Error Handler



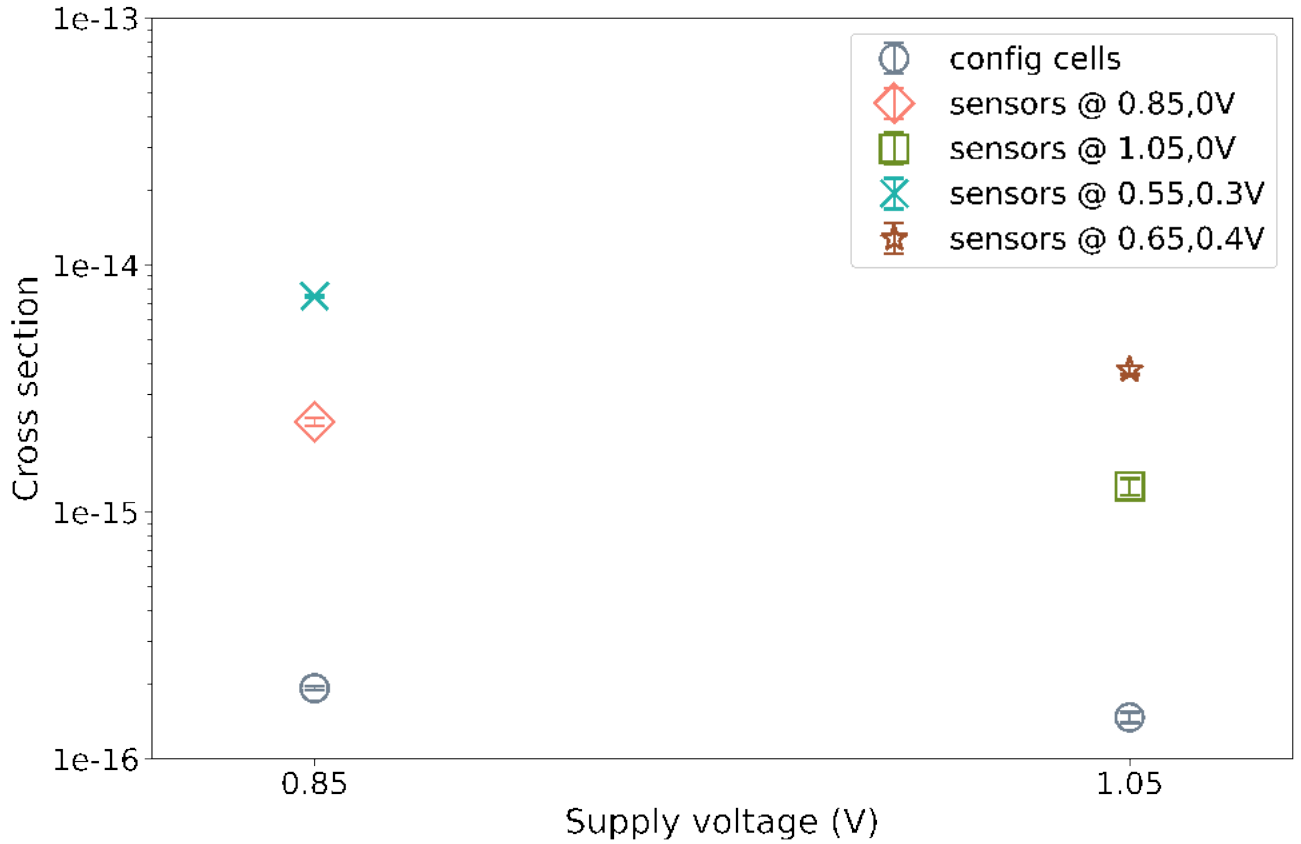
- Larger sensor correlation corresponds to less failures at the system level
- Error handling through the app. also works very well

Neutron Tests



- Tested at a government facility
- ZCU104 board in another room 100 ft away

Sensor & Config. Cell Cross Sections



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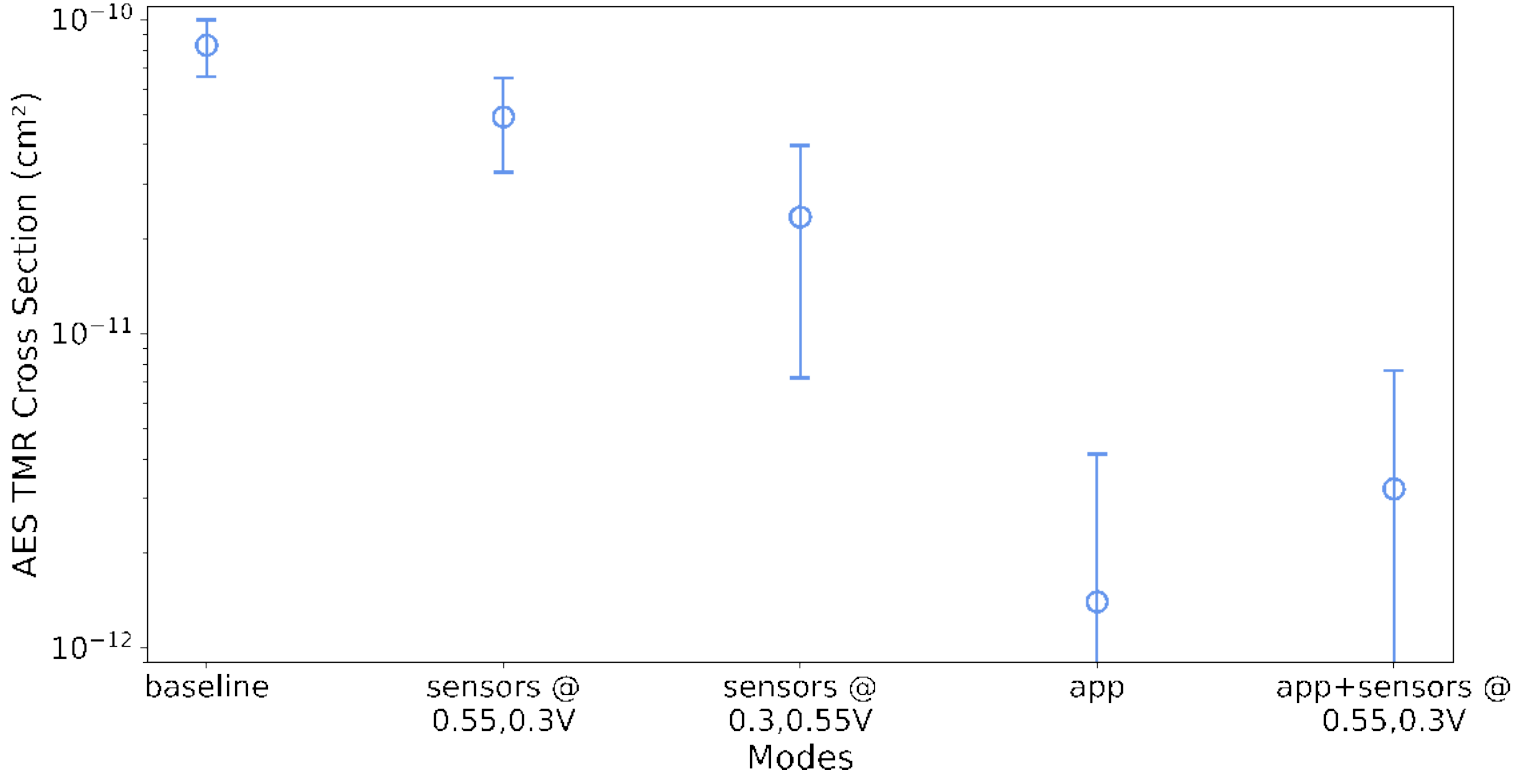
TMR AES-128 with Error Handler



- Sensors did not help as much as they did with heavy ions
- Error handling through the app. works very well

Summary and Conclusions

Our FPGA works well under radiation

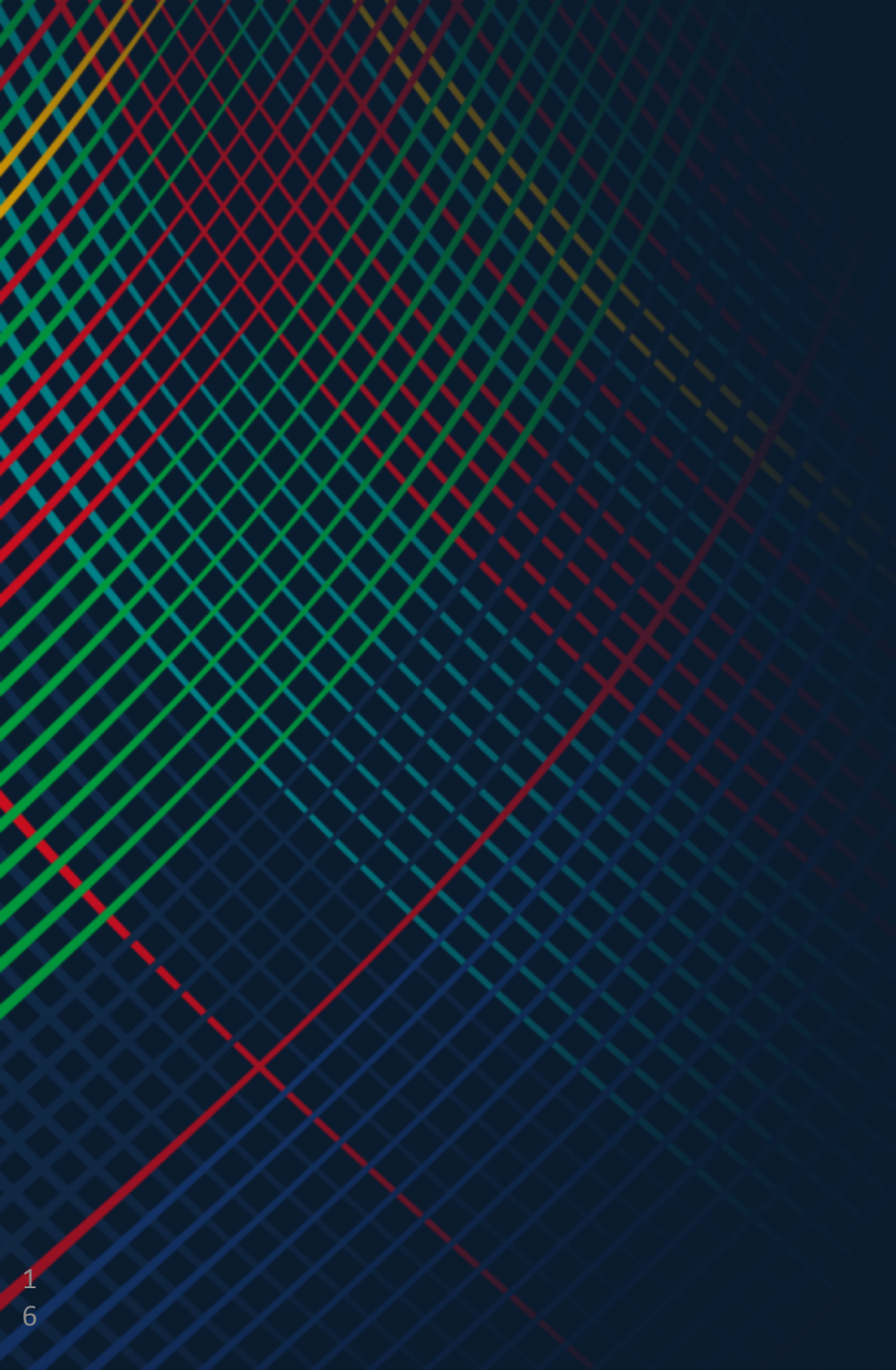
- Radiation hardening features decreased the application cross section over 10x

Sensors work better with higher LETs

- Can detect ~30% of SEUs with neutrons, >90% of SEUs with heavy ions

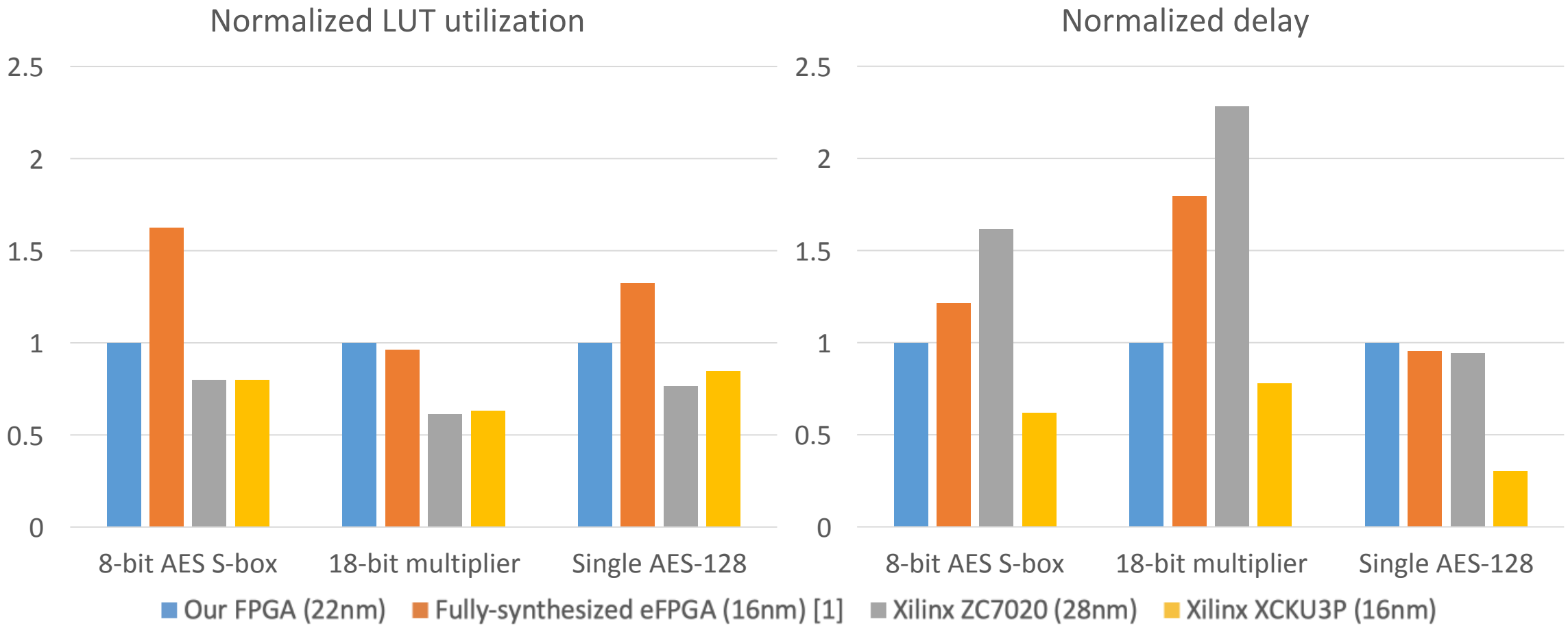
We can take advantage of scaling trends to tackle SEUs

- >90% error detection and low system down time are achievable with SEU sensors



Questions?

Benchmark Measurement Comparison

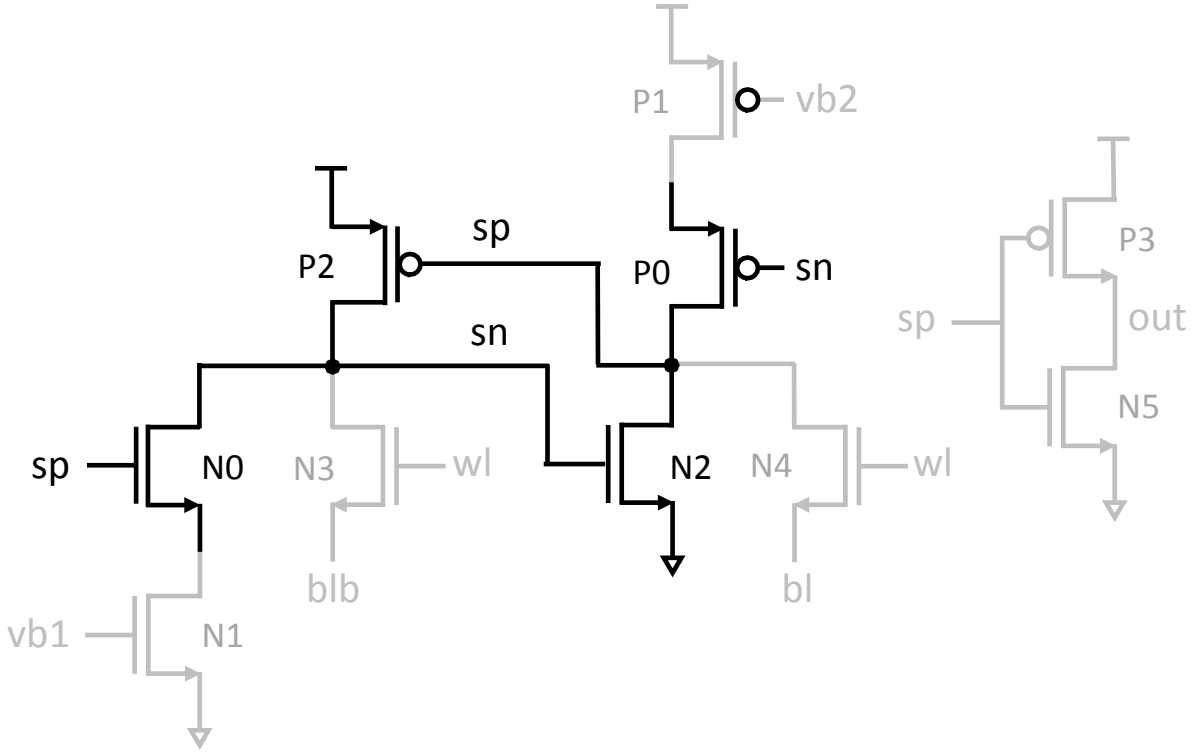


- Semi-custom advantage over the eFPGA
- Tool, architecture, and design effort disadvantages over industrial FPGAs

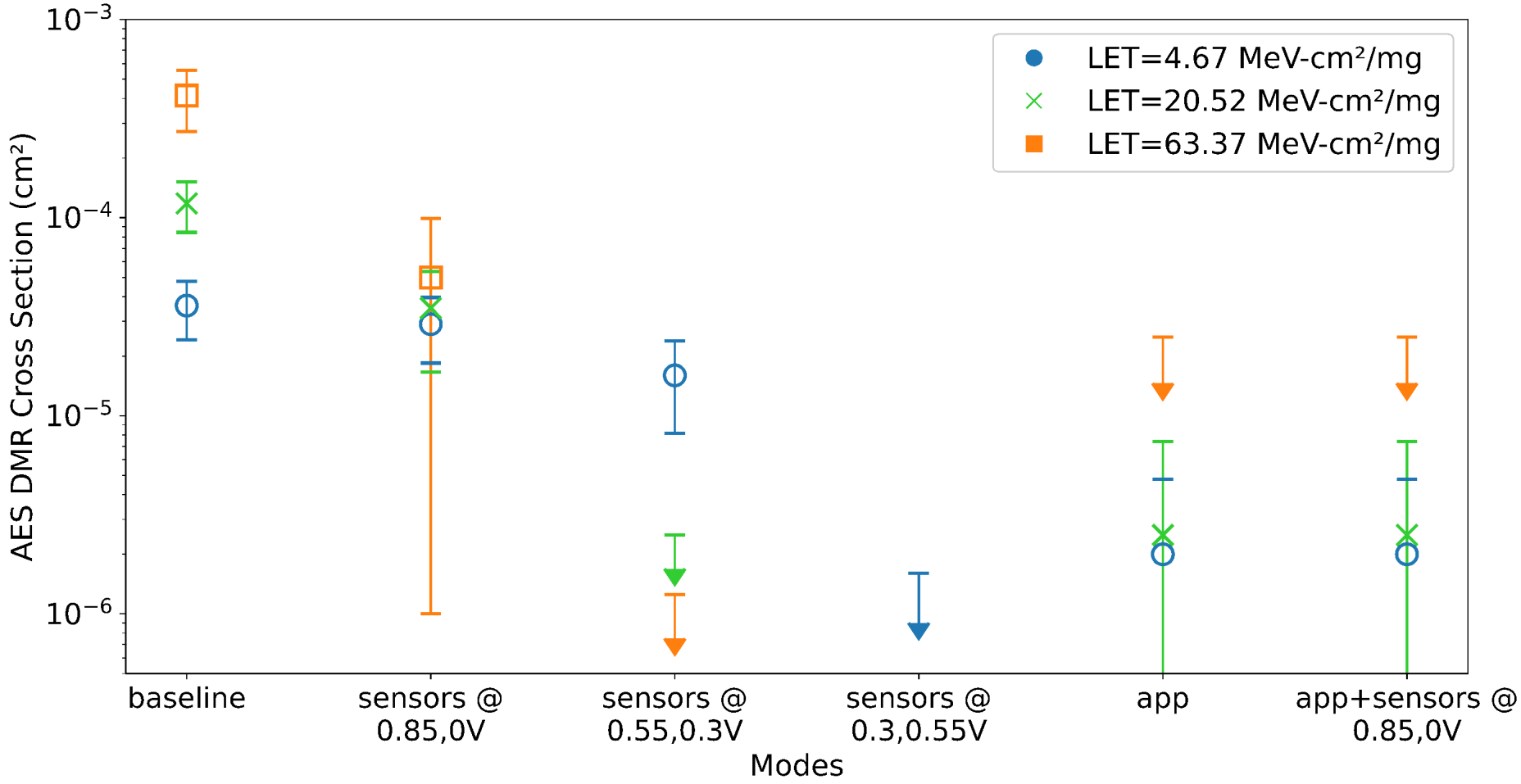
[1] P. Mohan *et al*, "Top-down Physical Design of Soft Embedded FPGA Fabrics"

SEU Sensors in FPGA Configuration Memory

- Reset and error state
- Vulnerability and tunability
- Writability and readability
- Continuous access to output

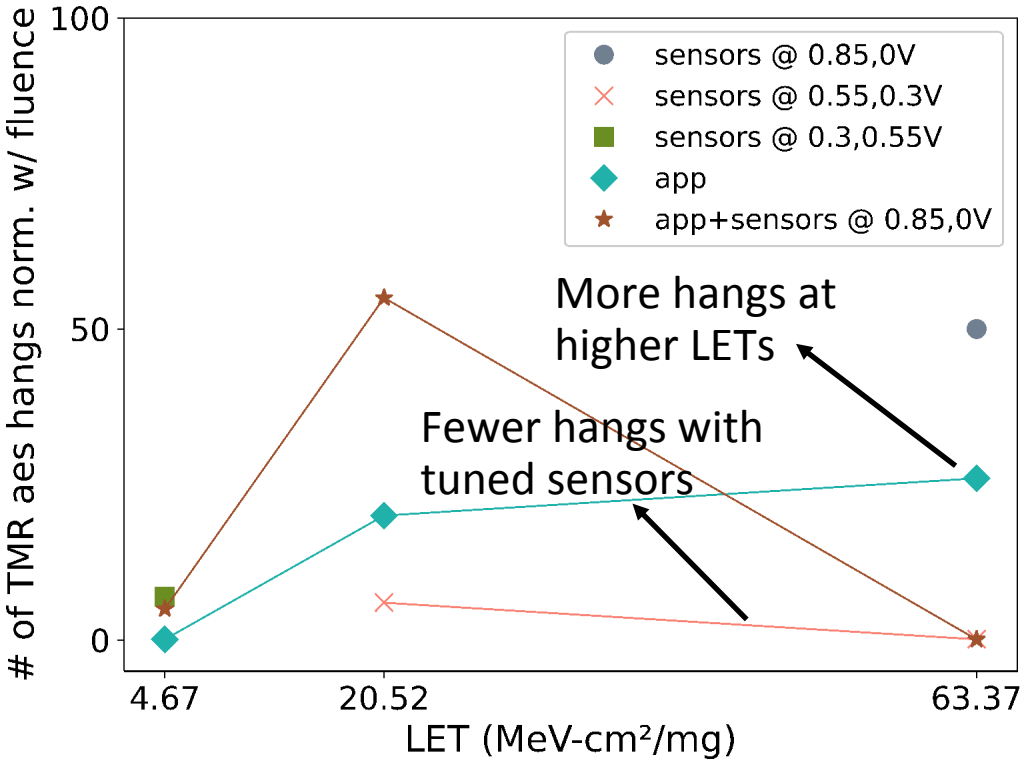


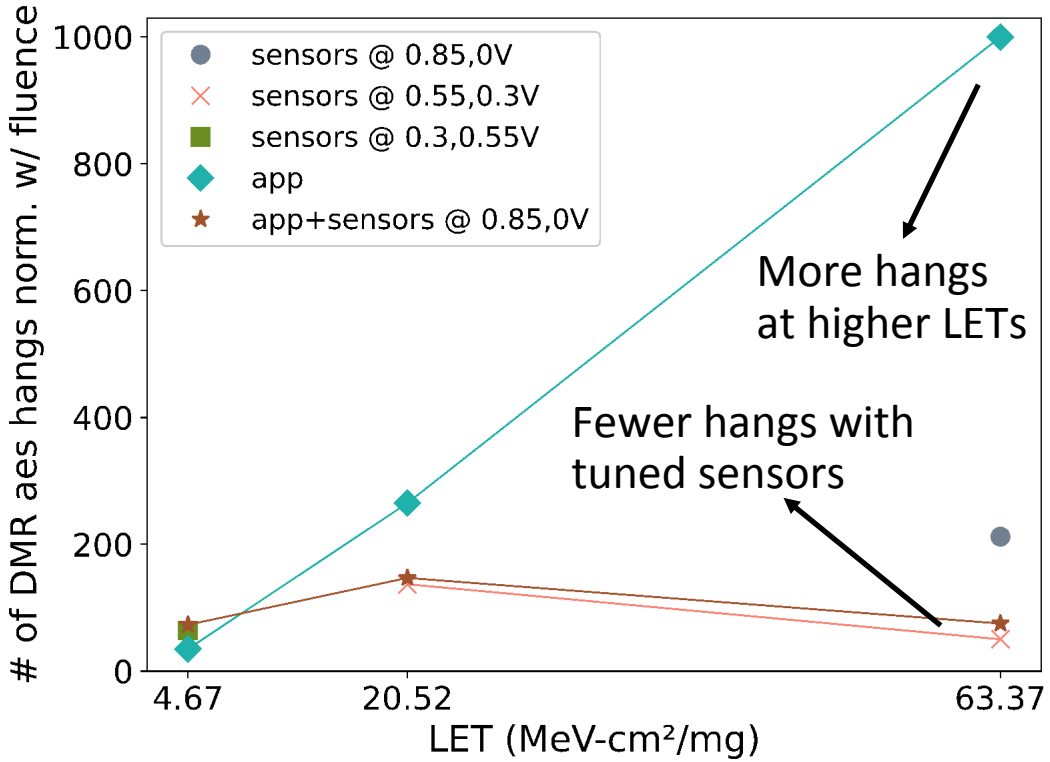
DMR AES-128 with Error Handler



- Similar results to TMR
- We can eliminate the system-level errors with our error handling methods

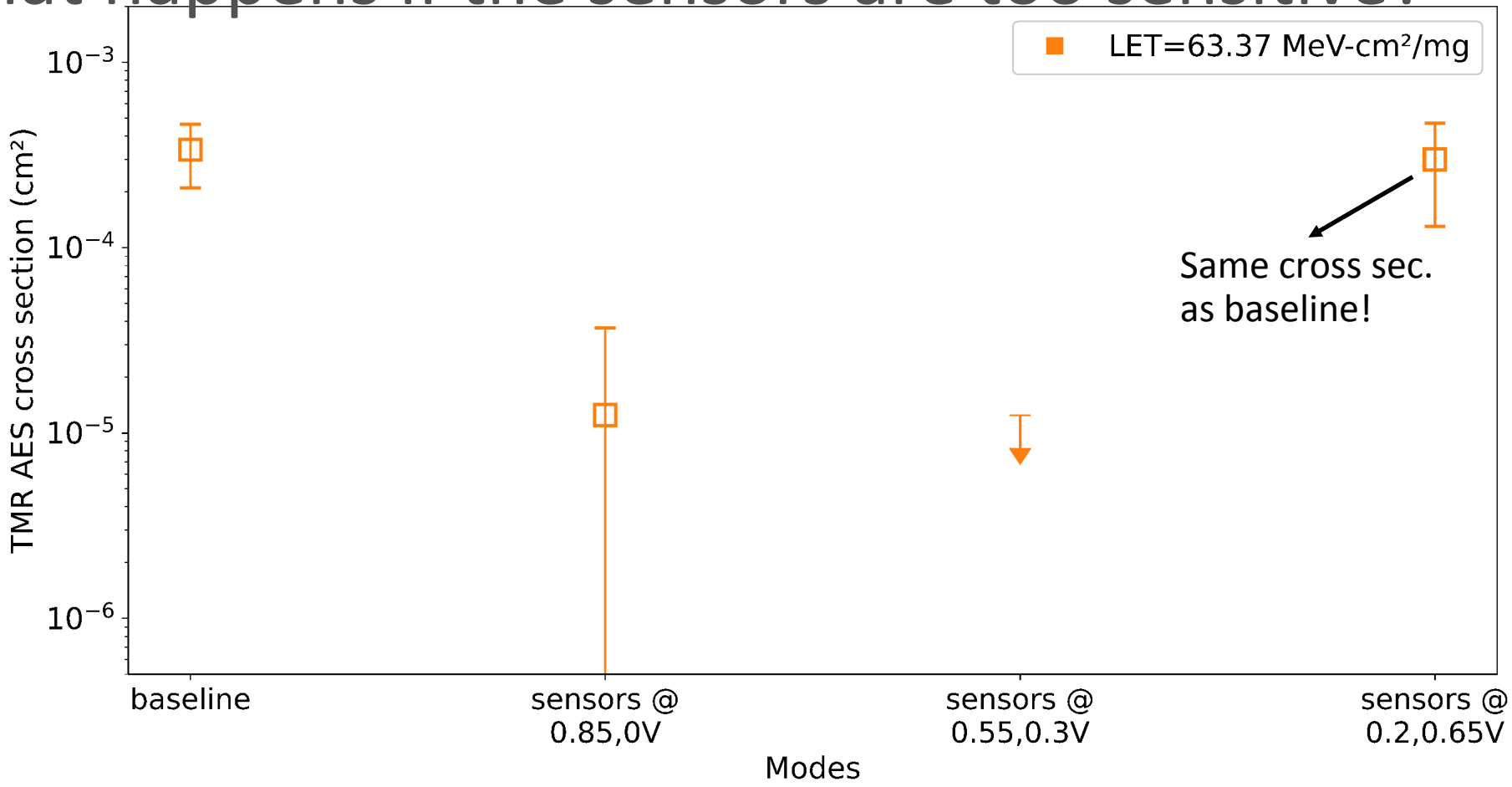
How often do the applications hang?





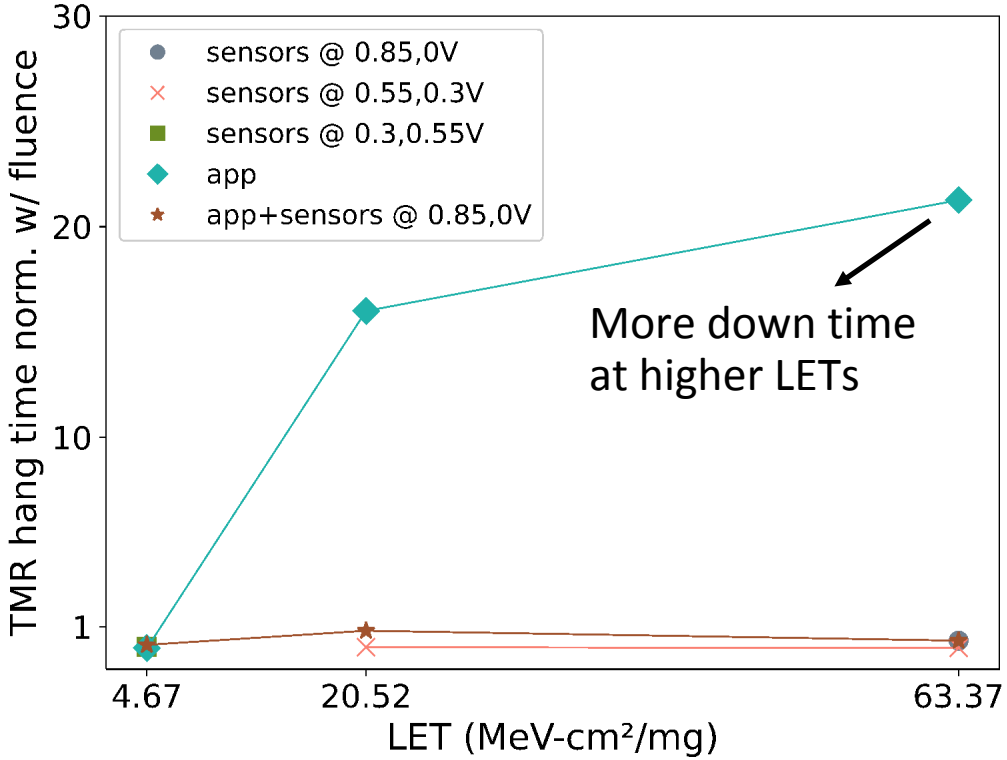
- DMR hangs more often than TMR, as expected
- More errors at higher LETs → DMR, TMR hang more often without sensors
- Fewer hangs with sensors at higher LETs (better correlation)

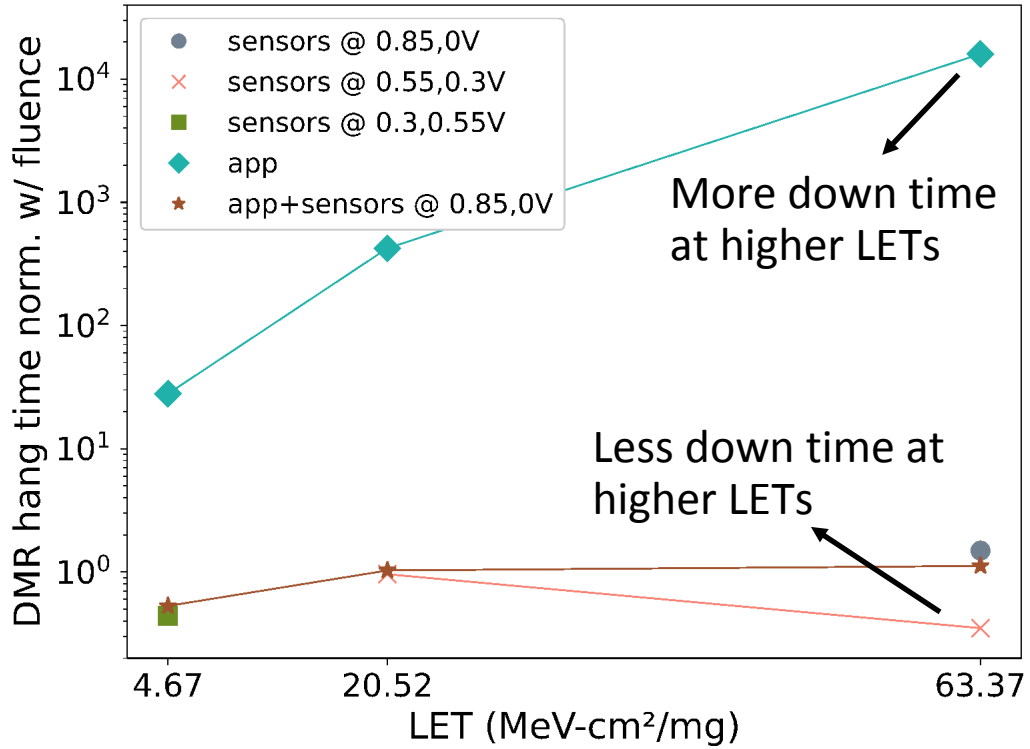
What happens if the sensors are too sensitive?



- Way too many false positives at bias voltages 0.2,0.65V. Can't get to handling the actual error
- Same cross section as plain!

How long are the applications hung?





- Much shorter hang time with sensors compared to error handling through the app.

  → Sensors can mitigate system level failures with minimum system down time