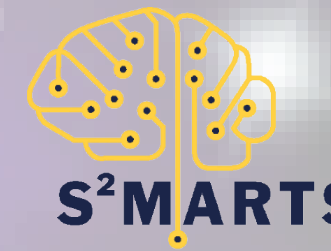
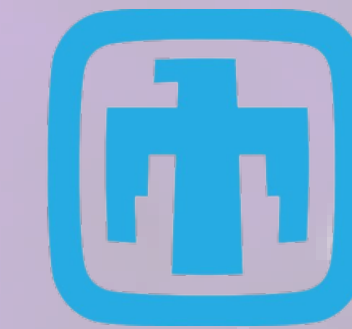


Single Event Upset and Total Ionizing Dose Response of 12LP FinFET Digital Circuits

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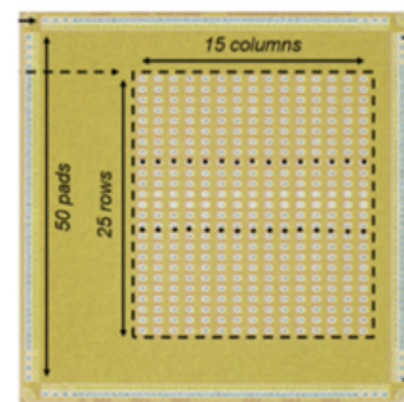
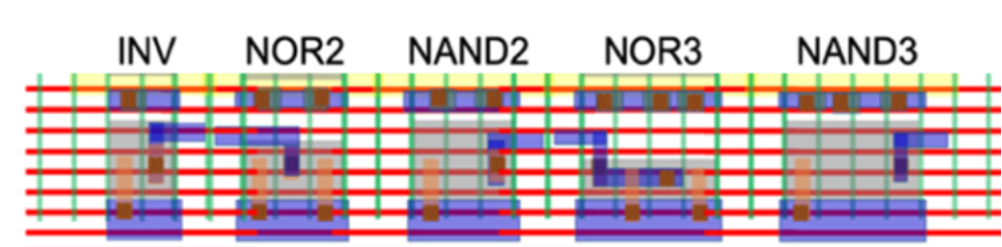
SEU Experiment Description

Single event upset (SEU) testing was performed on digital flip flops (DFF), designed with RVT transistors, on test chip 3 (TC3). Larger energy ions consisting of Carbon, Boron, and Oxygen were used in testing. Further, lighter ions consisting of three energies for Hydrogen and one energy for Helium were used. Each ion was tested at voltages of 0.4V, 0.8V, and 1.2V. At each voltage level in addition to all 1's or all 0's for the data, the clock was either fixed in a low state or a high state during beam exposure.

TID Experiment Description

Total ionizing dose (TID) testing was conducted on 9 TC1 test chips. 5 chips were exposed to an ARACOR 60 KeV X-Ray source, 1 chip was exposed to a 63.6 rad(Si)/s ⁶⁰Co Gamma-Rays, and 3 chips were used as controls. Both the NMOS and PMOS test structures, designed with RVT transistors, were irradiated with ON-state bias. For NMOS structures in ON-state bias, V_d , V_g and V_b were set to 0V, and V_g was set to 0.8V. For PMOS structures in ON-state bias, V_d , V_g and V_b were set to 1.6V and $V_g = 0.8V$ making $V_{gs} = -0.8V$. During measurement of NMOS structures V_g was swept from -0.3V to 0.8V and V_d was set to 0.8V. For PMOS structures, V_g was swept from -0.8V to 0.3V and V_d was set to -0.8V.

(Pictured: the test structure order and TC1 chip)



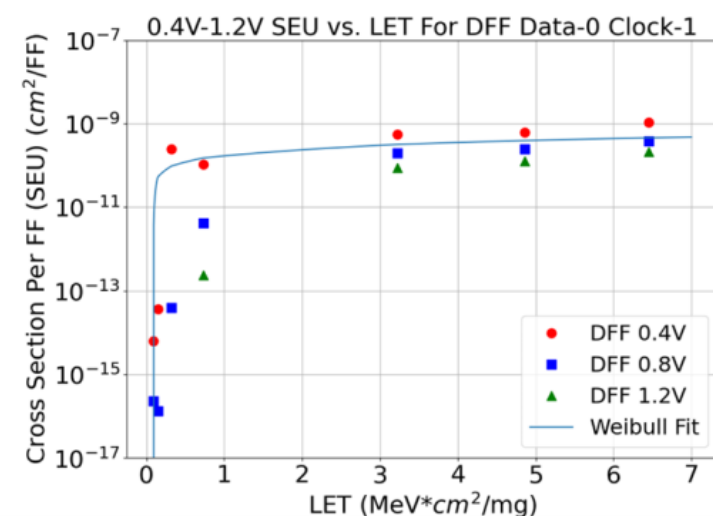
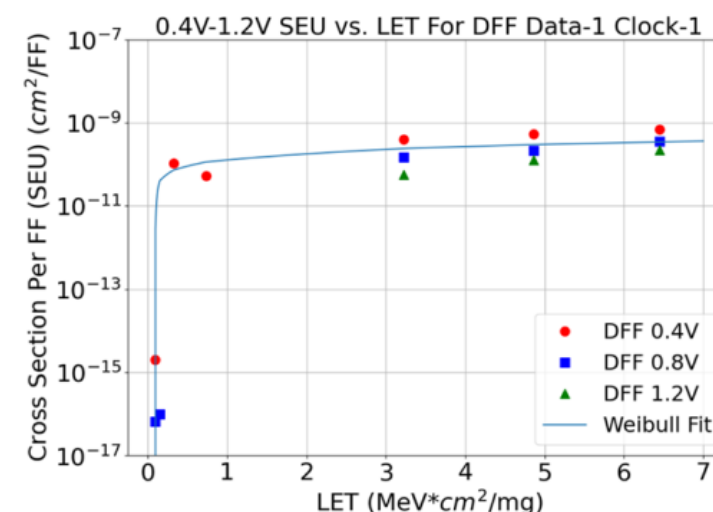
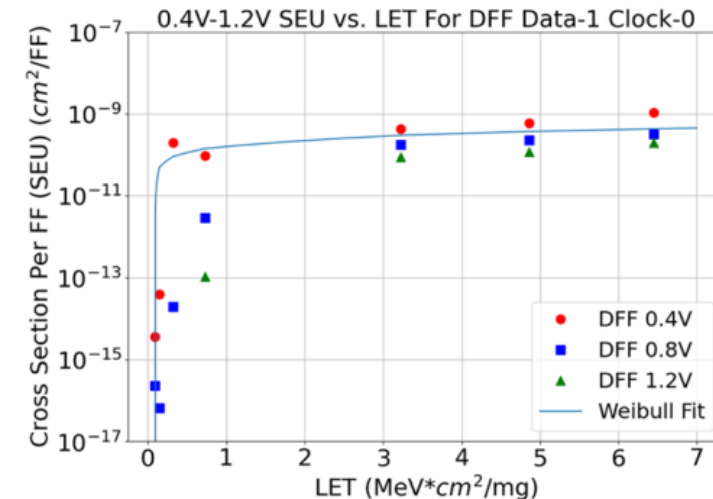
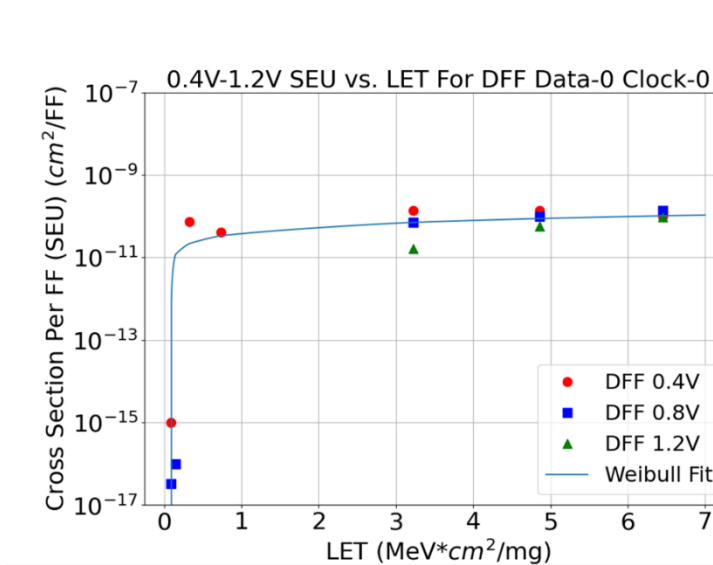
Acknowledgements

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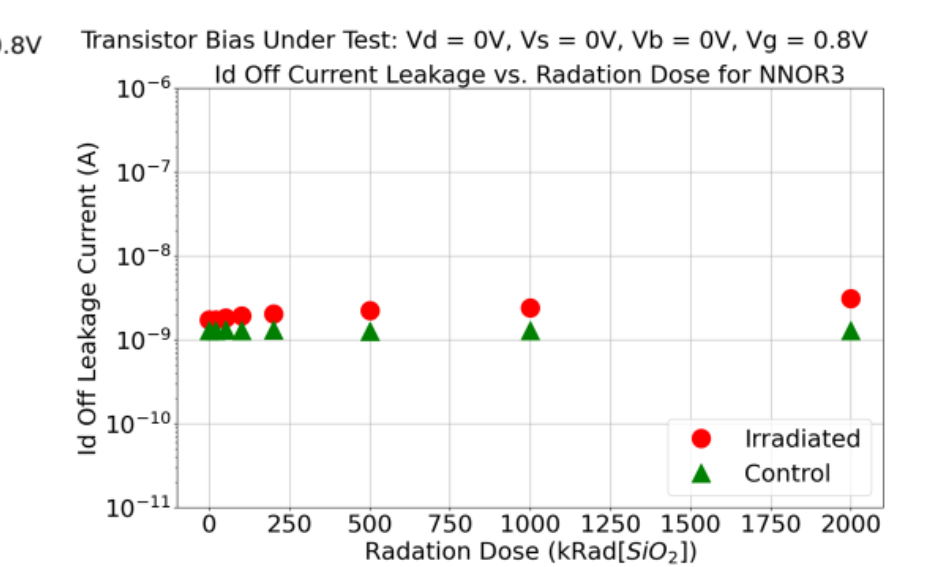
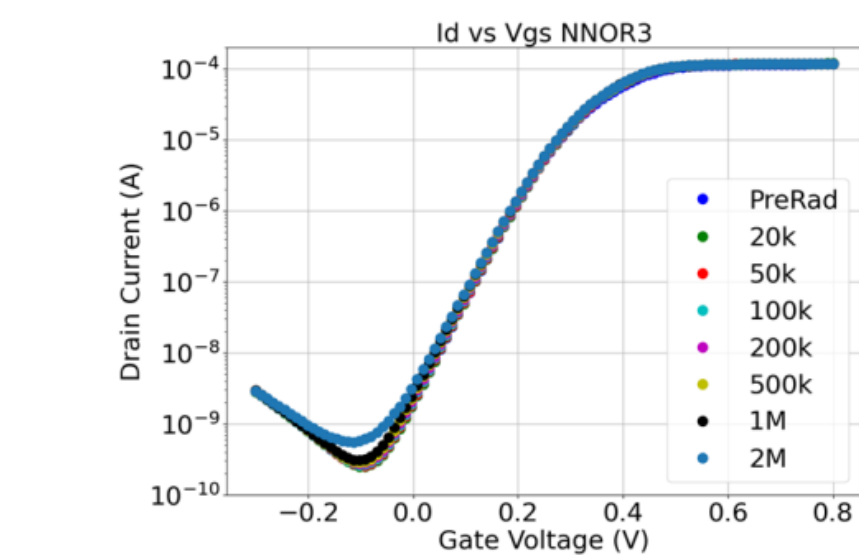
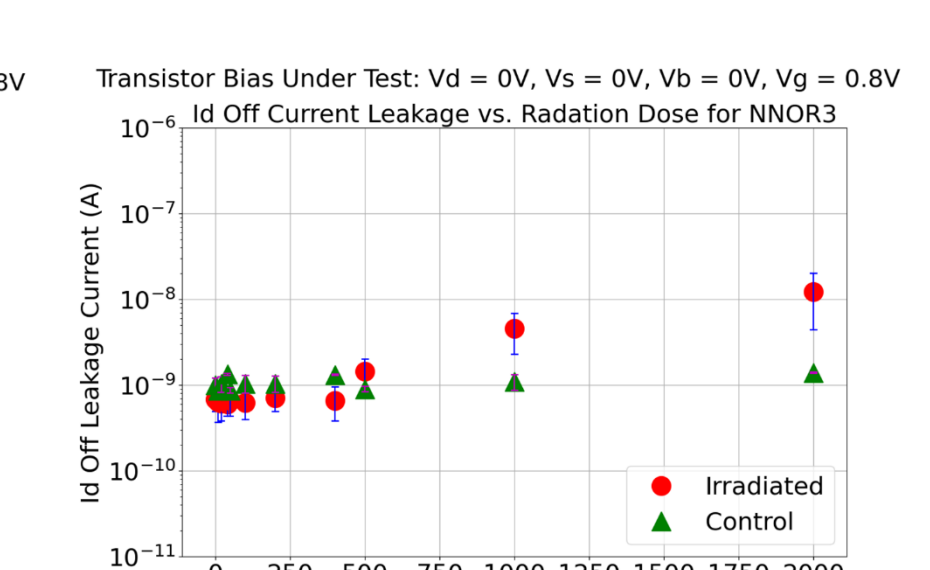
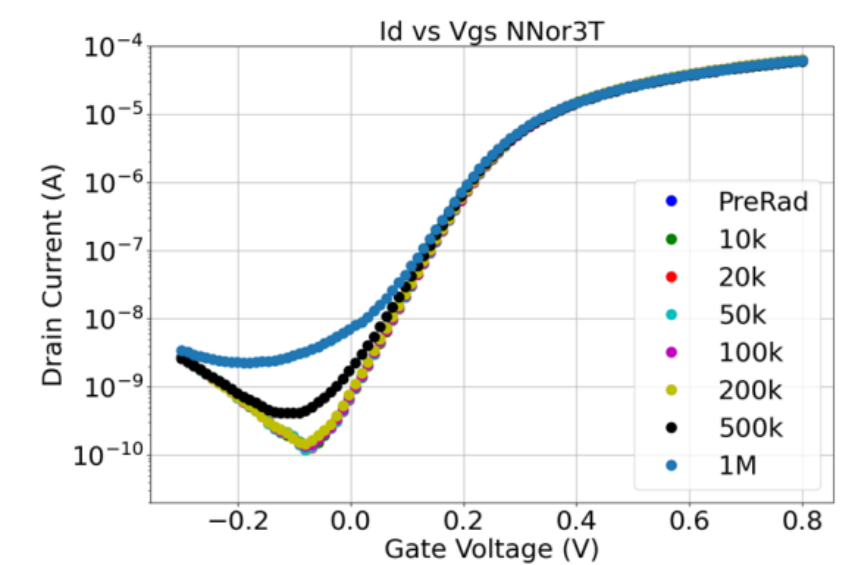
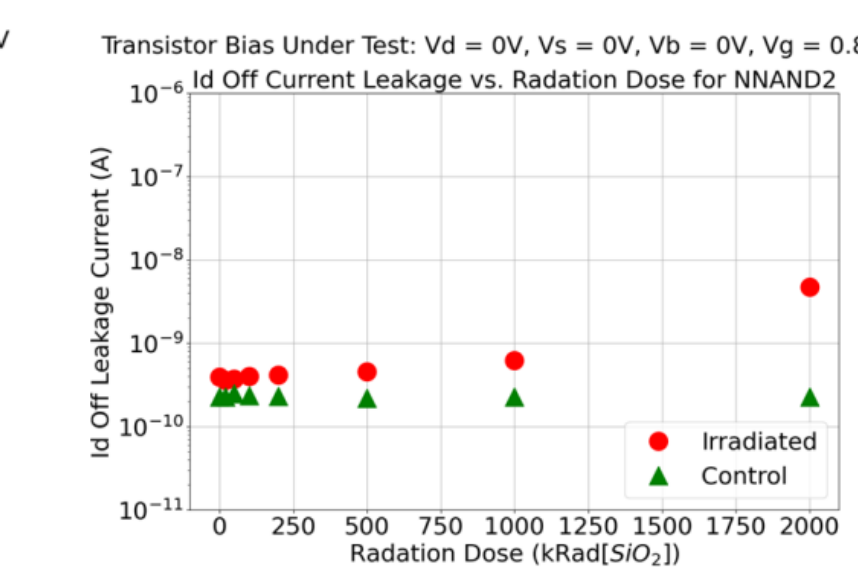
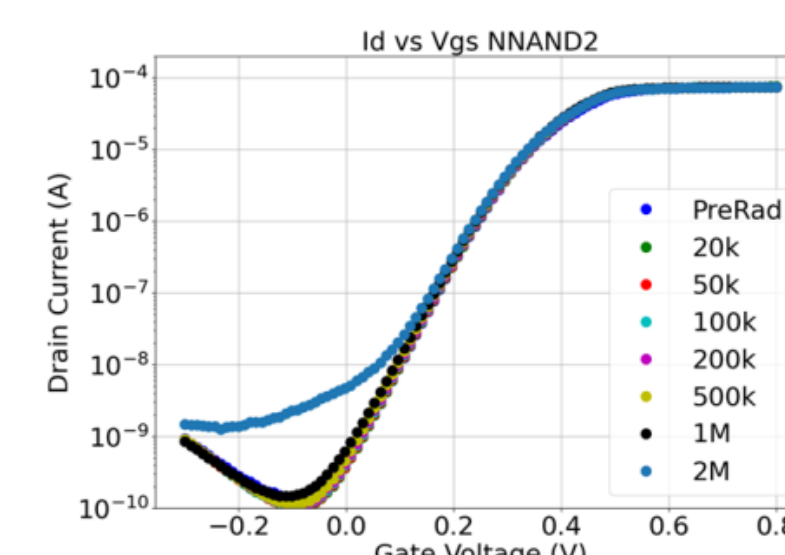
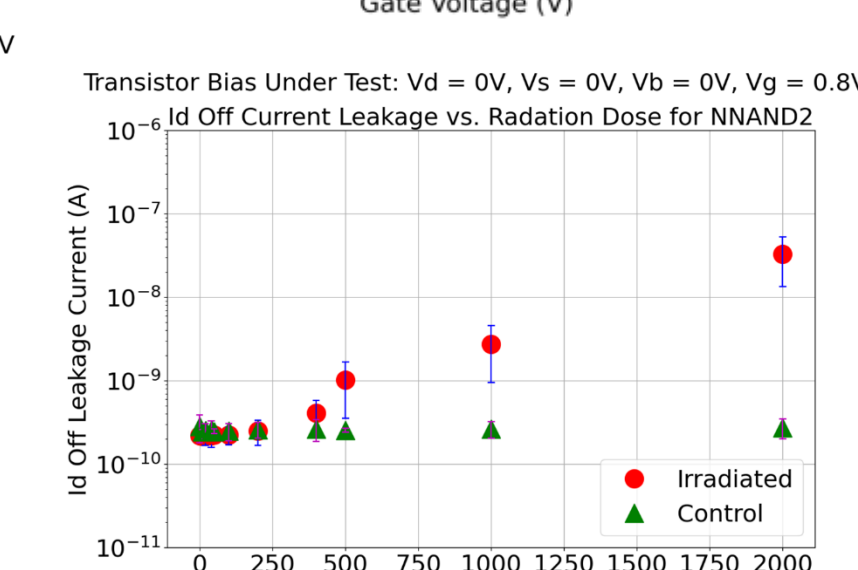
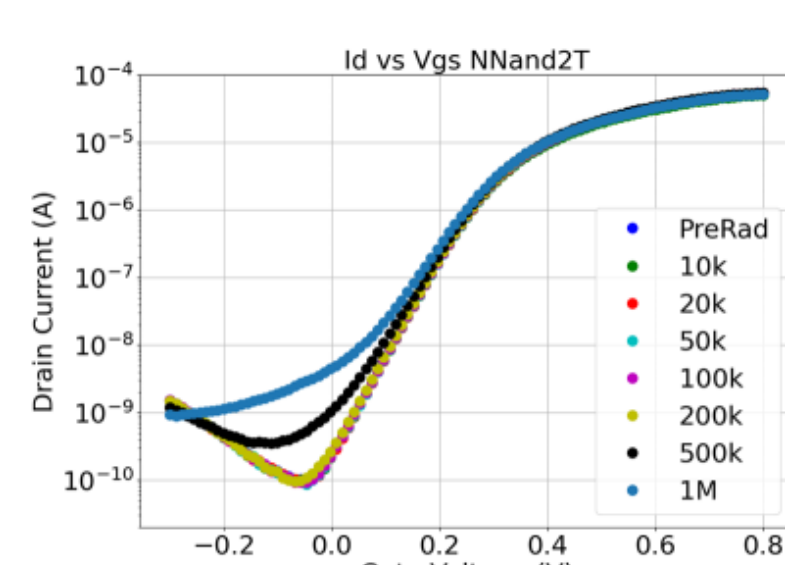
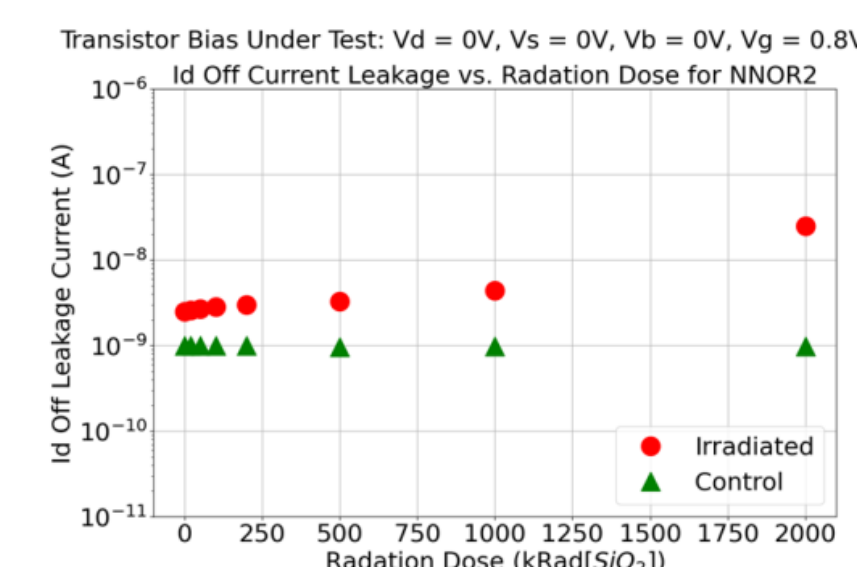
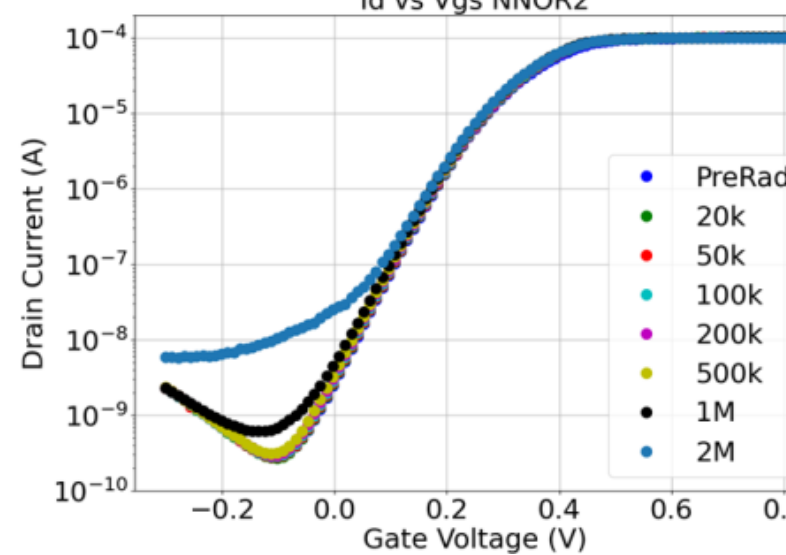
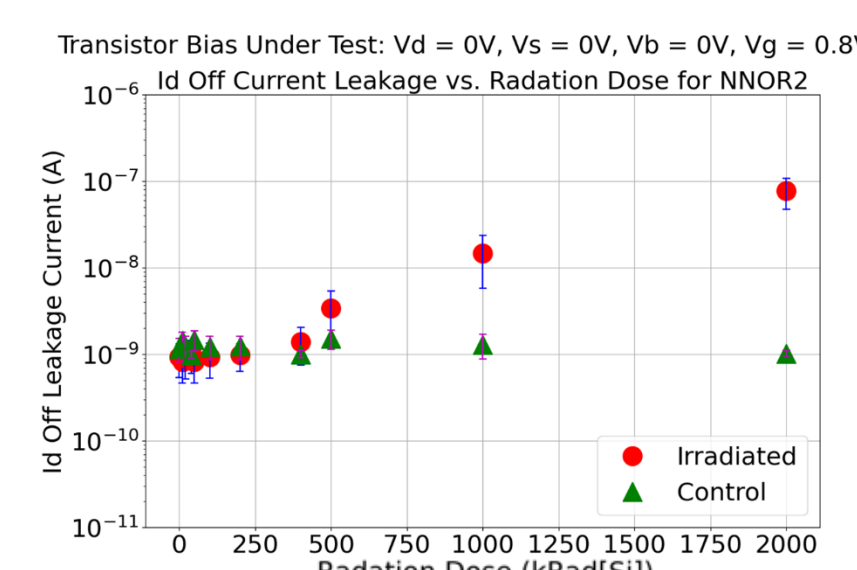
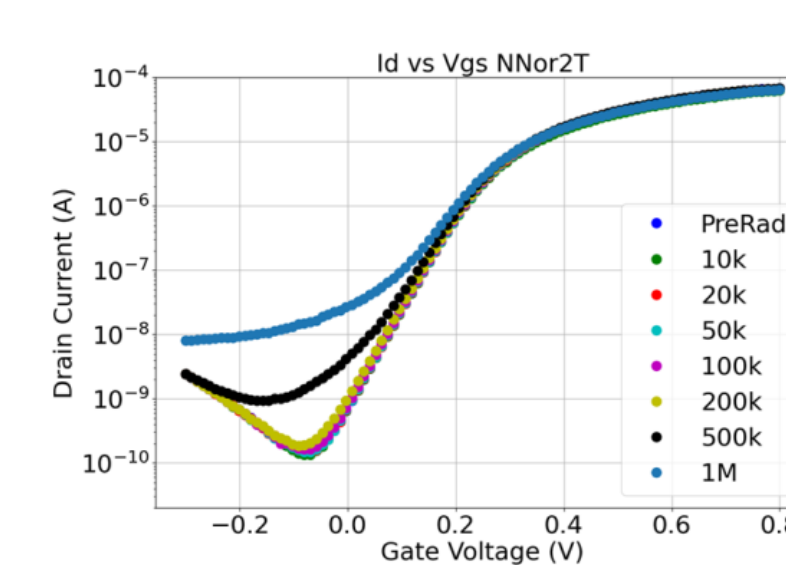
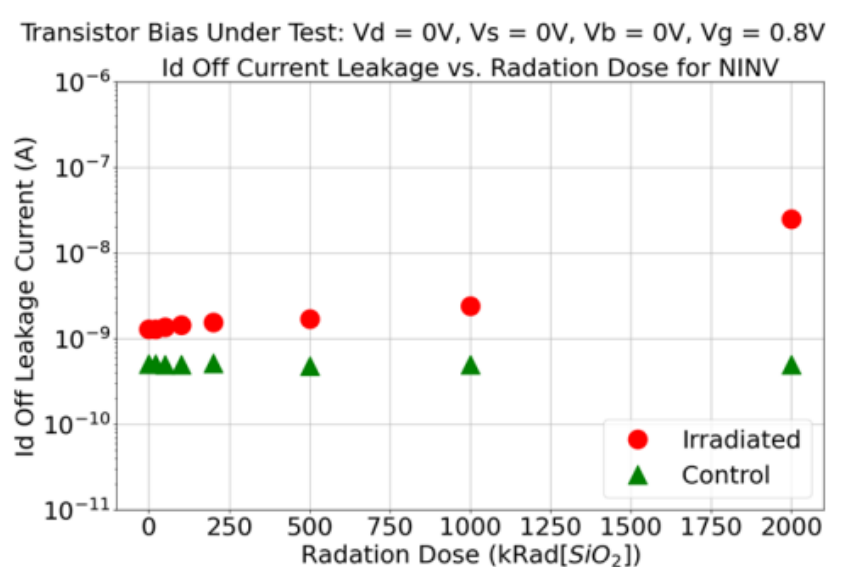
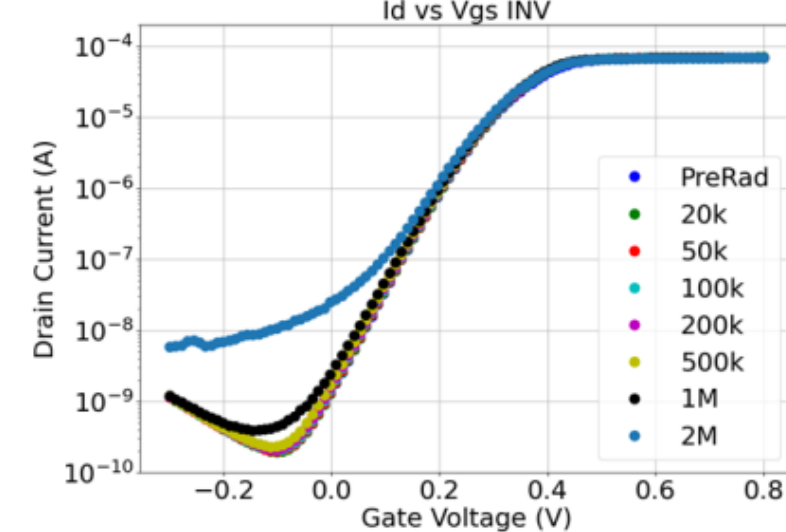
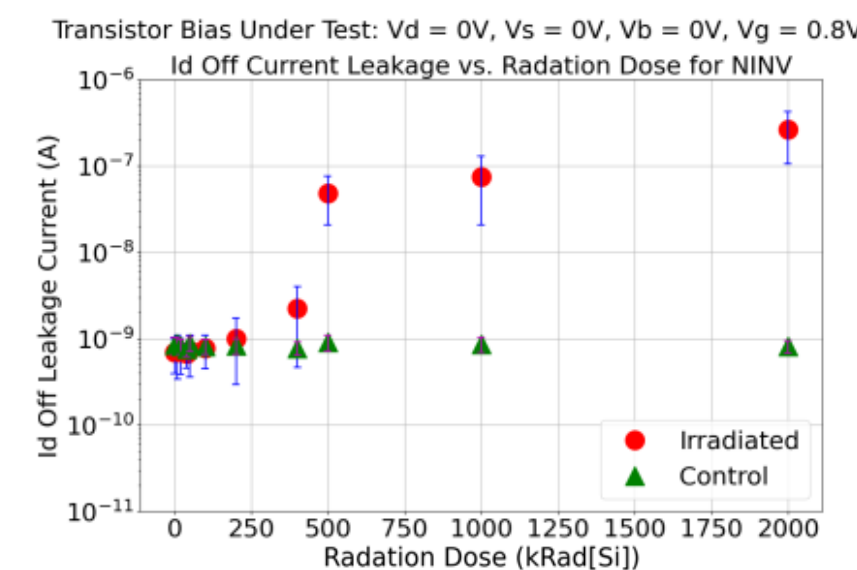
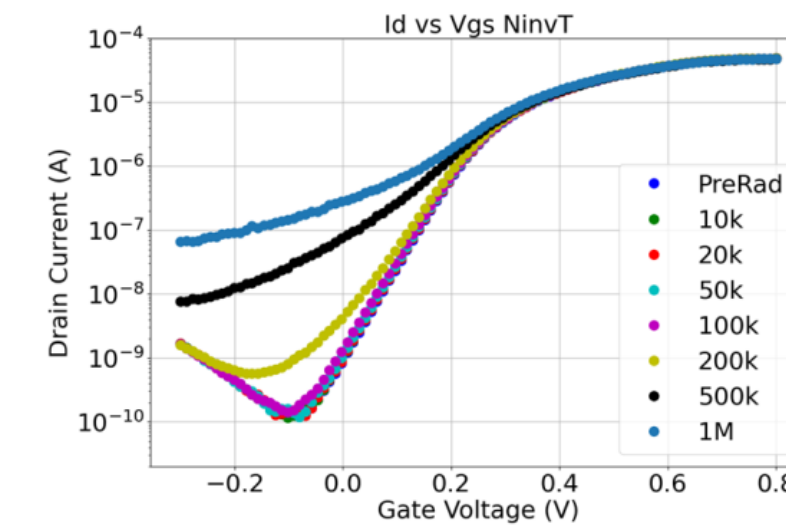
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- [2] M. P. King et al., TNS, vol. 64, 2017
- [3] D. R. Ball et al., TNS, vol. 65, 2017

TC3 SEU Results



TC1 NMOS Results



TC1 PMOS Results

