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SRAM Multi-Cell Upset Vulnerability at the 5-nm FinFET Node

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***Abstract*— Single-port and two-port SRAM designs in a 5-nm bulk FinFET node were tested for multi-cell upset (MCU) vulnerability against alpha particles, 14-MeV neutrons, thermal neutrons, and heavy ions with nominal and reduced supply voltages. Multi-cell upset contributions to single-event upset rates and observed bit-line upset ranges are presented for each particle as a function of supply voltage. Results show that MCUs account for a majority of events from high LET particles and neutrons at lower supply voltages. MCU shapes are shown for various sizes of upset clusters, showing upset reversal throughout the charge cloud.**

***Index Terms*—SRAM, Single-Event, Multi-cell Upset**

I. Introduction

STATIC random-access memory (SRAM) circuits are of particular interest for studying single-event effects because of their widespread usage in all types of electronic systems. SRAM circuits generally occupy significant area of integrated circuits (ICs). SRAM cells are generally densely packed due to area and speed constraints and have very low critical charge (Q_{crit}) values compared to other circuit types [1-5]. These factors often result in SRAM arrays experiencing high single-event upset (SEU) rates and being a large factor in determination of the overall single-event performance of application specific integrated circuits (ASICs) and electronic systems. Another effect of SRAM cell density is that the increased proximity of adjacent cells leads to an increased probability of multiple cells collecting charge from a single incident particle, potentially leading to multi-cell upsets (MCU). Designers use error-correcting codes (ECC) and interleaving in SRAM layouts to mitigate single-event effects. ECC and interleaving can mitigate both single-bit upsets (SBU) and MCU, but will decrease overall SRAM performance. Additionally, ECCs increase in complexity with the size of the MCUs they are designed to mitigate. Designers need to know the size and the shape of MCU clusters to determine ECC and interleaving parameters for optimized performance. As a result, it is important to investigate MCU cluster size at each technology node so designers can make appropriate design decisions to meet specifications.

This paper presents SBU and MCU characteristics of single-port (SP) and two-port (TP) SRAM arrays at the 5-nm bulk FinFET technology node. Custom-designed test ICs were exposed to 14-MeV neutrons, thermal neutrons, =alpha particles, and heavy-ions with varying supply voltages. Observed upset ranges for the various particle types and supply voltage conditions as well as observed probabilities of occurrence for each MCU size relative to the overall single event upset rate are presented. These results will help designers optimize error detection and correction schemes and interleaving distance in 5-nm bulk FinFET SRAM arrays.

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II. Background

MCUs are caused when multiple adjacent transistors

collect charge from the charge cloud of a single event,

called charge-sharing. Charge-sharing in cells within the

charge cloud is due to diffusion processes of the freed

charge carriers in the ion track [5-8]. Charge cloud

characteristics (size and carrier density) along the track of

an incident ion is controlled by the linear energy transfer

(LET) of that ion. The LET value is dependent on the

material on which the ion is incident, as well as the type

and energy of the incident ion. Fig. 1 [9] shows TCAD

simulations of well potential perturbations for particle

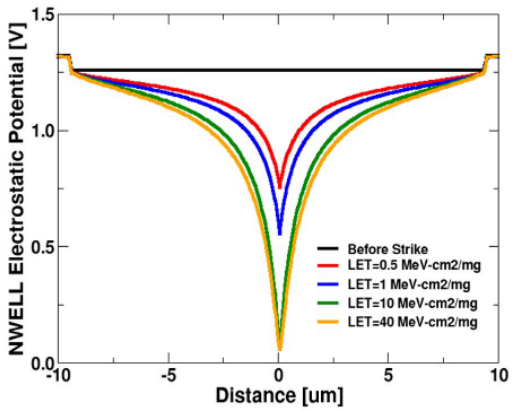

Fig. 1. Electrostatic potential perturbation ranges for various incident particle LET values for a generic 16-nm process. [9].

strikes of various LET values for a generic 16-nm technology. For bulk Si-based technologies, the same underlying silicon material means the charge cloud generated by an incident ion is expected to be similar, irrespective of the technology node. Therefore, it is expected that FinFET technology nodes would exhibit similar characteristics and well perturbation ranges as that shown in Fig. 1. For low-LET particles, most upsets are SBU because the amount of charge deposited is usually not sufficient to result in charge-sharing. Low-LET particles must strike at or near the drain region to cause an upset, as charge collected through drift processes are required to cause an upset. Particle strikes far away from the drain region may not cause an upset, as the diffusion processes do not spread significant charge to surrounding sensitive regions for low-LET particles. Supply voltage reduction is a common approach to decreasing the power consumption of a circuit. Supply voltage is also a significant factor affecting Q_{crit}. For an SRAM cell with a given capacitance, decreasing the supply voltage also decreases the stored charge on a node. Therefore, less charge must be collected by a node from a particle strike for a significant change in voltage at that node required to upset the SRAM cell, leading to increased susceptibility from SBU and MCUs.

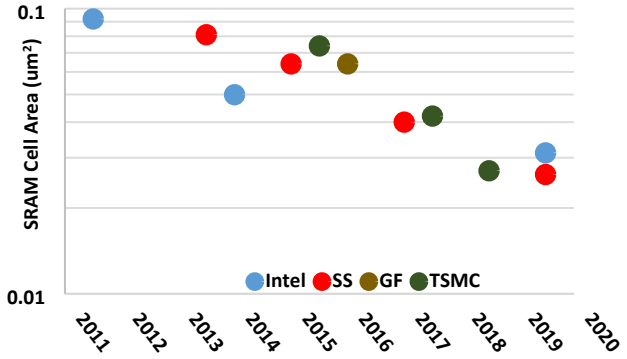

Fig. 2. SRAM cell areas for various processes over time. Decreased cell area leads to more affected cells from a given charge cloud size [11].

The evolution to FinFET nodes led to an overall reduction in drain region size, and thus a decrease in soft error rate (SER) from planar nodes [10]. Further scaling of FinFET technology nodes led to the reduction in SRAM cell sizes from various manufacturers shown in Fig. 2 [11]. Scaling-induced reduction in cell size has led to overall decreasing SER rates per SRAM cell in recent technologies [12][13], as seen for 16-nm and 7-nm nodes in Fig. 3 [13]. However, at the 5-nm node, the decreases in critical charge and collected charge have resulted in a ~2x increase in SER for low-LET particles as shown in Fig. 3 [13]. Though SBU rates increased for the 5-nm node over the 7-nm node, it is not clear how MCU rates will be affected at the 5-nm node as MCU rates may not scale directly with SBU rates for a given technology [14].

While scaling may change the transistor sizes, the area over which transistors collect charge due to charge-sharing remains similar across FinFET technology nodes due to the underlying Si lattice structure remaining the same. As a result, decreasing SRAM cell size can result in an increased MCU bit size due to more cells being within the influence of a given charge cloud. Decreasing SRAM cell size also results in reducing the Q_{crit} for an upset. Reducing Q_{crit} results in an increase in the area over which charge-sharing will be effective. With SRAM cell size changing from 0.074 um^2 at the 16-nm node, to 0.027 um^2 at the 7-nm node, and to 0.021 um^2 at the 5-nm node, the number of cells collecting charge from a given charge cloud is expected to have increased significantly.

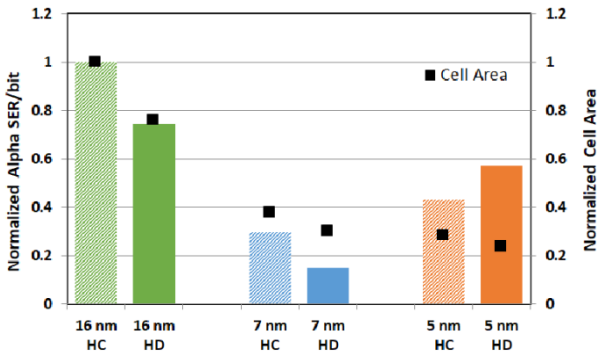

Fig. 3. 5-nm technology shows a significant increase in per-bit SER over previous technology scaling trends. [13]

III. Device and Experiment Description

Test ICs were fabricated using a 5-nm bulk FinFET technology at a commercial foundry. Both the SP and TP SRAM designs were fabricated and tested. Cell schematics for SP and TP designs are shown in Fig. 4. The TP cell has additional access transistors to accommodate additional read/write functionality with additional bit-lines. The SP SRAM array was 256Kb in size and in an

8K x 32 configuration. The TP SRAM array was 76Kb in size and in a 1K x 72 configuration. Heavy-ion experiments were conducted at the Lawrence Berkeley National Laboratory (LBNL) 88" Cyclotron in vacuum, using the 10 MeV/nucleon cocktail at normal incidence and room temperature. During heavy-ion tests, particle beam flux was adjusted to minimize possibility of the aggregation of multiple MCUs contributing to one upset cluster. Ion LETs ranged from 2 – 86 MeV-cm^2/mg. For terrestrial neutron testing at the LANSCE facility, 12 ICs, 6 of each SRAM design, were placed in a line within the neutron beam. Neutron tests were carried out to a fluence of ~10^{11} n/cm2. 14-MeV neutron experiments were conducted at Sandia National Laboratories using 2 ICs, one of each SRAM design, exposed to the beam at a time. The neutron flux varied over these tests, but the neutron fluence was in the range of 10^{13} neutrons/cm^2 for each test. Alpha particle experiments were conducted at Vanderbilt University using a 1 cm x 1 cm size 10 µCi ^{241}Am foil button source placed less than 1 mm from the top of the die. The alpha particles were approximately ~5.4 MeV at a flux of approximately 1000 particles/mm^2/sec. Thermal neutron tests were conducted at the MU Research Reactor facility at the University of Missouri.

Nominal core voltage for this technology is 750 mV and nominal I/O voltage is 1.2 V. Core supply voltage was varied at each facility. I/O voltage was not adjusted from nominal unless noted otherwise.

The SRAM was programmed using all-0 or all-1 patterns and continuously read throughout the experiment. Each SRAM array was read completely within 1 second. Upon detection of an error, the bit position and address for the word were recorded, and the correct data was rewritten back to the erroneous word location. MCUs were detected based on spatial and temporal proximity. Errors must have occurred within the same read of the SRAM array (temporal proximity). Upset bits that were within 3 cells from an existing upset belonging to the MCU (spatial proximity) were added to the cluster. In this paper, relative MCU contribution rates are shown with respect to overall events, rather than upset counts. One MCU counts as one event, regardless of size. MCU ranges are determined based on the physical greatest distance in cells along the BL or WL direction between two upset cells from a single event.

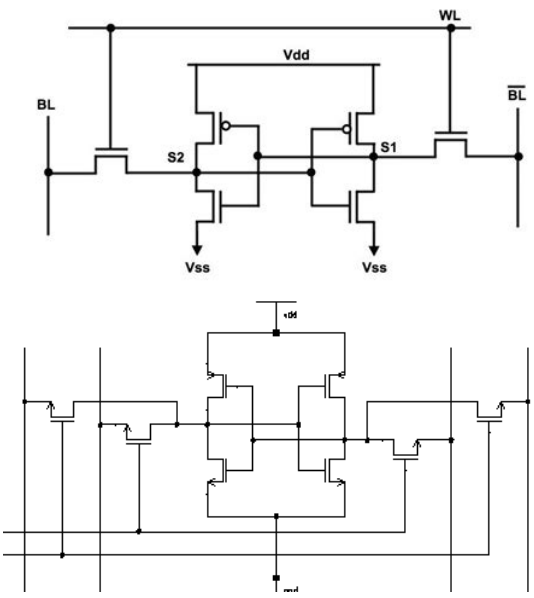

Fig. 4. SP (top) and TP (bottom) SRAM cell designs. Additional access transistors are needed in the two-port design.

IV. Data/Results and Discussion

SRAM cells are vulnerable in both the space and terrestrial environments. Experiments were performed with exposures to alpha particles, 14-MeV neutrons, thermal neutrons, and heavy ions to evaluate susceptibility across a range of incident particle LETs.

A. Alpha Particles

Alpha particles have the lowest energy and LET values of the particles considered in these experiments. Thus, a small charge cloud was expected with a small number of transistors influenced by any given particle strike. It is clear that, at the 5-nm node, alpha particles are still capable of causing SRAM MCUs even at nominal and elevated supply voltages. Fig. 5 shows the relative contributions of MCU cluster sizes for a range of supply voltages for both the SP and TP designs. The small LET values lead to significantly greater contributions of SBUs to the total number of upsets, but MBUs were observed across all supply voltages tested, and contribute to >15% of overall errors for both SRAM designs when supply voltages were decreased below 550 mV. The SP design shows slightly higher SBU contribution to overall upset rates. The number of upsets along the bit-line (BL) are shown in Fig. 6 for both the SP and TP SRAM designs under alpha particle exposure, and both designs show similar BL ranges.

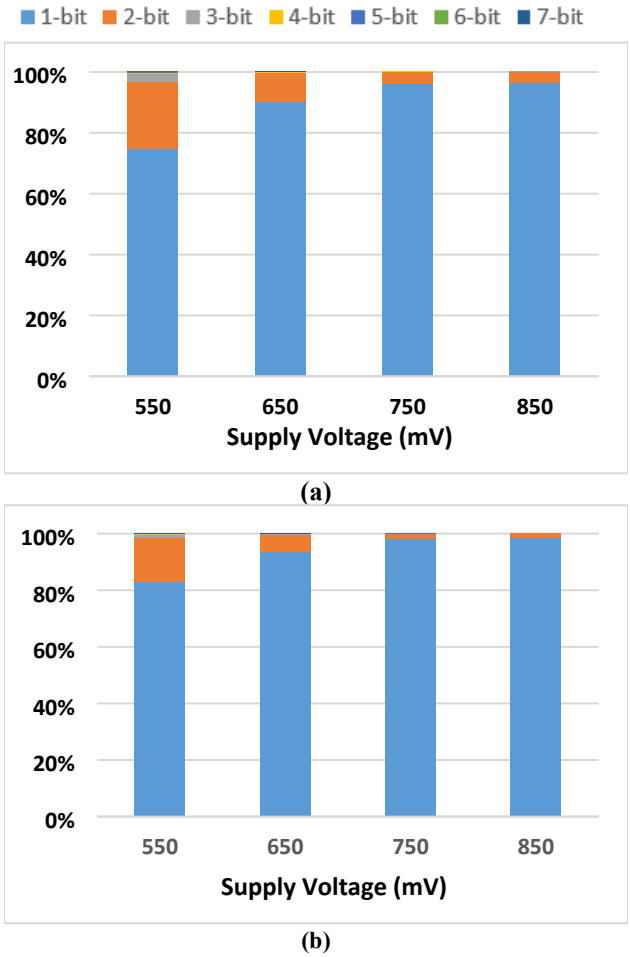

Fig. 5. MCU rate is a strong function of supply voltage for alpha particle exposures, for both (a) SP SRAM and (b) TP SRAM. Legends have been omitted due to size constraints. Total event counts were >10,000 for each experiment.

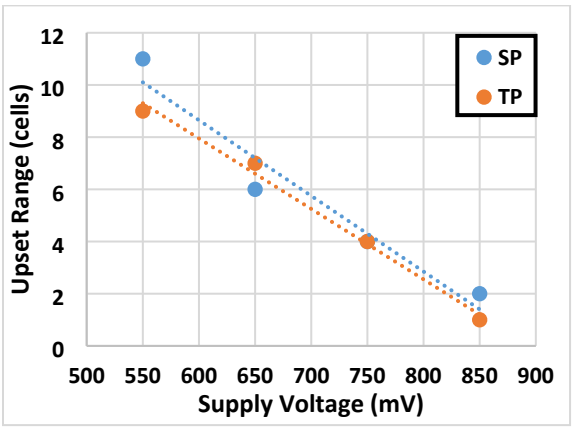

Fig. 6. Maximum observed BL upset ranges under alpha particle exposure.

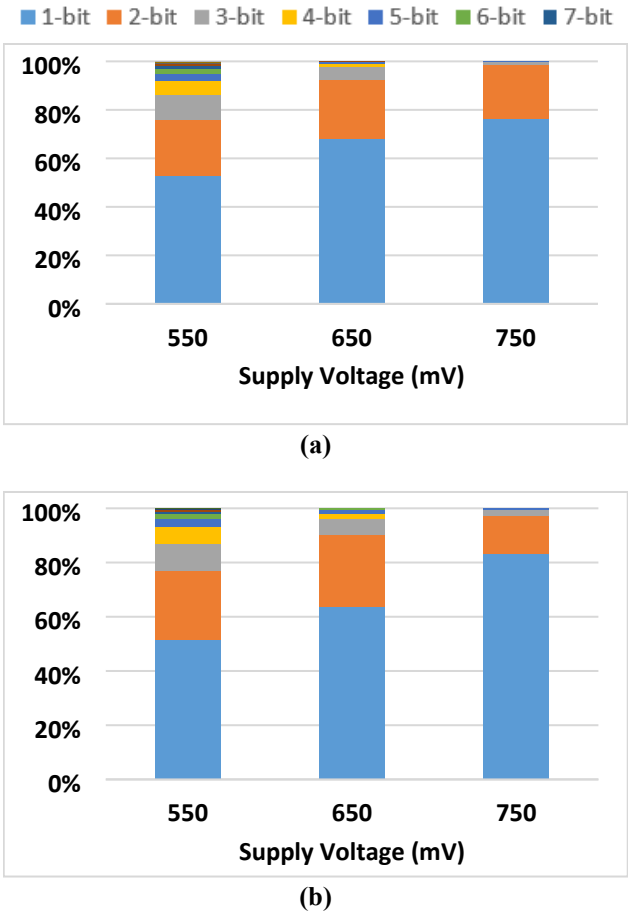

Fig. 7. (a) SP SRAM and (b) TP SRAM relative MCU size contributions under 14-MeV neutron exposure for various supply voltages. Total event counts were >100 for each experiment. The bottom blue section of each bar represents single-bit upsets, the orange represents 2-bit upsets, and so on.

B. 14-MeV Neutrons

Neutron-induced single-events comprise the greatest upset vulnerability to terrestrial electronics [15,16]. Neutrons may interact directly with lattice nuclei and produce spallation products with a wide range of particle LETs. Thus, neutrons are capable of creating larger MCUs with greater range along the word-line (WL) and BL than alpha particles. For the 14-MeV neutron exposures, relative contributions of various MCU sizes are shown in Fig. 7. It can be seen that the greatest MCU size potential is larger than that for alpha particles. Additionally, the contributions of MCUs to overall upset rates are also increased. At 550 mV supply voltage, SBUs only account for ~50% of overall events. MCU contributions to the overall event rates are similar across the two designs, as well as the overall MCU sizes themselves. This shows that the charge collection and Q_{crit} differences between the two designs conflict and compensate each other, leading to similar MCU responses from these neutrons. The maximum observed bit-line upset ranges from 14-MeV neutron induced upsets are shown in Fig. 8. These were observed to be greater than the alpha particle upset ranges, as expected, due to greater

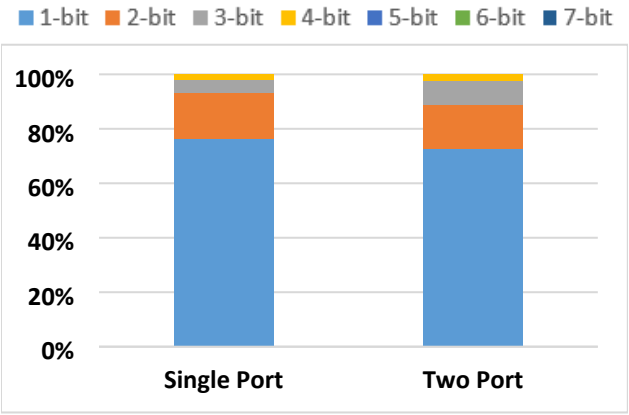

Fig. 9. MCU size contributions to the overall event rate for terrestrial neutron exposure.

LET values of nuclear interaction products.

C. *Terrestrial Neutrons*

Terrestrial neutron exposures were performed at nominal supply voltage for both SRAM designs. Like 14-MeV neutrons, terrestrial neutrons interact directly with lattice nuclei and produce spallation products with a wide range of particle LET values. Fig. 9 shows the relative contributions of various MCU sizes to overall upset event rate for both the SP and TP designs at nominal supply voltage (750 mV). Maximum bit-line upset ranges for terrestrial neutrons were 3 cells for the SP design and 2 cells for the TP design.

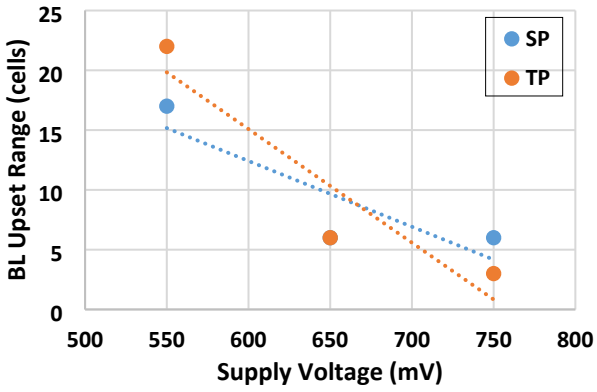

Fig. 10. Maximum observed BL upset ranges under thermal neutron exposure.

D. *Thermal Neutrons*

Thermal neutron reactions with Boron-10 produce alpha particles as well as a Lithium-7 ion. The lithium ion has a higher LET value than the alpha particle, but a significantly shorter range. Maximum observed BL upset ranges from thermal neutron exposure are shown in Fig.

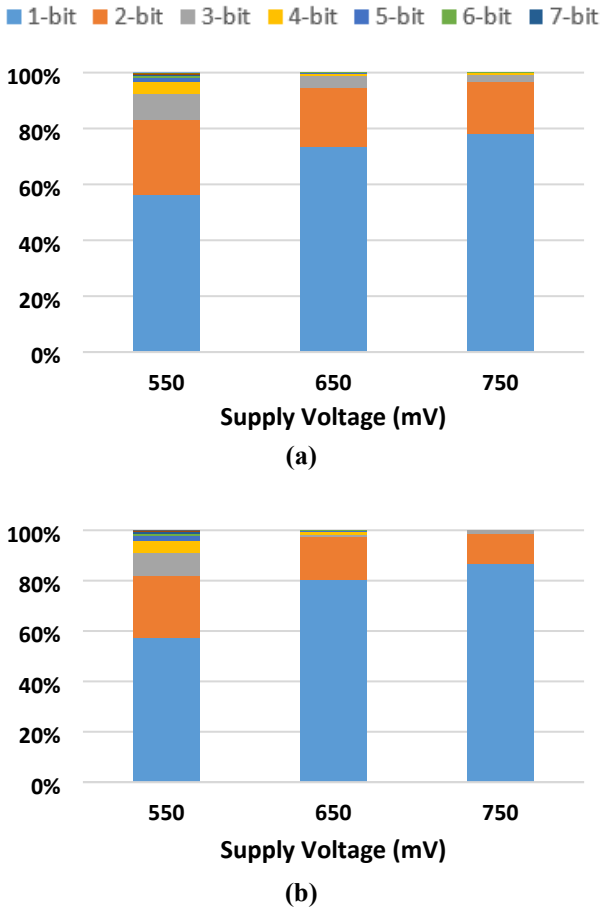

Fig. 11. (a) SP SRAM and (b) TP SRAM relative MCU size contributions under thermal neutron exposure.

10 as a function of supply voltage. Relative contributions of MCUs and SBUs for thermal neutrons are shown in Fig. 11. Results are similar to those of the 14-MeV neutron results for relative contributions. The greatest MCU size observed for the SP SRAM design at nominal voltage was 6 bits, and for TP SRAM was 3 bits.

E. Heavy Ions

Heavy ion experiments were conducted with particle LETs ranging from 2-86 MeV-cm^2/mg with a range of supply voltages. Fig. 12 shows the contributions of various size MCUs to the overall upset events for both the SP and TP SRAM designs for 10 MeV-cm^2/mg Argon ions. It is interesting to note that the probability of occurrence for MCU decreases monotonically with increasing MCU size for 750 and 650 mV supply voltages. However, with a 550 mV supply voltage, the probabilities show non-monotonic behavior. This may be attributed to upset reversal where the same SRAM cell upsets twice quickly to revert to original data [17]. In these scenarios, charge diffusion is long enough in duration and significant enough in magnitude to cause the same cell to undergo multiple logical flips. Another explanation is that the critical charge for these cells is reduced low enough at 550 mV that the majority of events cause MCUs.

As supply voltage is decreased, the maximum MCU size for the SP design increased from 7 bits at 750 mV to 29 bits at 550 mV for this LET value, as seen in Fig. 12 (a). As the diffusion currents after an ion strike are independent of the supply voltage, these increases in MCU size are caused by decreases in Q_{crit}. For the same LET particle, Fig. 12(b) shows the MCU size probabilities for the TP design. The TP design shows higher probabilities for the greater MCU sizes than the SP design for this LET value. This trend was not observed to the same degree during alpha particle testing or neutron testing. Increasing the LET increased the occurrence probability of a given MCU size and the largest overall cluster size. High LET particles were seen to cause multiple 200+ bit upsets for both SP and TP designs at 550 mV operating voltage. The biggest cluster size at nominal supply voltage for the TP design was 76 bits as opposed to 12 bits for the SP design.

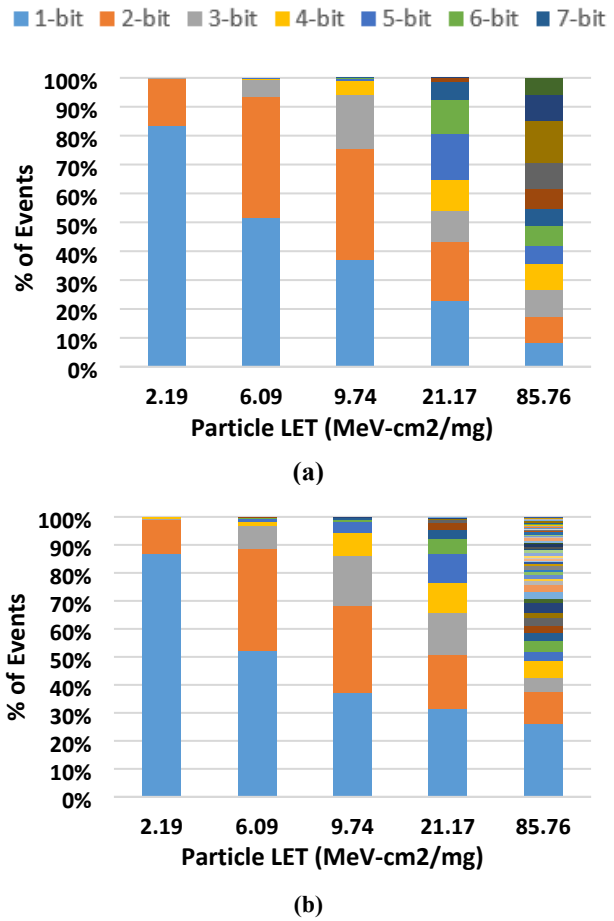

Fig. 13. MCU rate is a strong function of particle LET, shown here at nominal supply voltage for (a) SP SRAM and (b) TP SRAM. The bottom blue section of each bar represents single-bit upsets, the orange represents 2-bit upsets, and so on. Legends have been truncated due to size constraints. Total event counts were >500 for each experiment. Adjacent colors generally indicate differences of 1 upset cell per event.

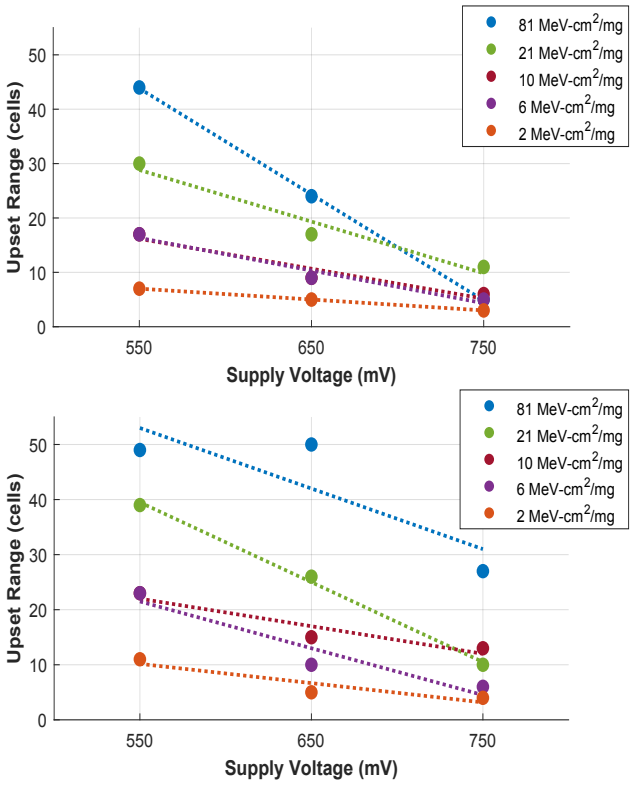

Fig. 14. Bit-line upset ranges are strongly dependent on operating voltage for SP (a) and TP (b) SRAM designs. Legend values represent particle LET in MeV-cm^2/mg.

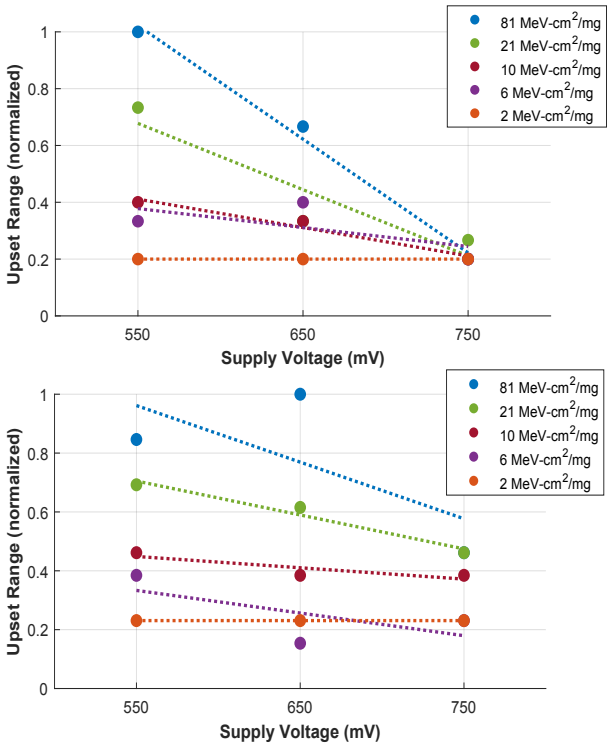

Fig. 15. Word-line upset ranges are strongly dependent on operating voltage for SP (a) and TP (b) SRAM designs. Legend values represent particle LET in MeV-cm^2/mg. Each chart is normalized by independent values.

Fig. 13 shows the occurrence probability for each MCU size as a function of particle LET for nominal supply voltage. For low LET values, the MCU event rate is similar across the two designs. However, MCUs from the highest LET particle increased in cluster size significantly more for the TP design compared to the SP design. The SP SRAM design shows greater relative MCU contributions from the 85 MeV-cm^2/mg ions (SBUs only accounted for <10% of upset events, compared to ~25% for the TP design), but the TP design shows greater susceptibility to larger MCUs, shown as more colors on the bar. These differences in susceptibility are due to the number of transistors collecting charge per cell and differences in critical charge [9] between the two designs.

Fig. 14 shows BL upset ranges for both the SP and TP designs across various supply voltages. WL upset ranges were determined for the same environments. Normalized WL upset ranges for heavy ions are shown in Fig. 15 for both the SP and TP designs for various heavy ion LETs as a function of supply voltage. Both the WL and BL ranges show a strong dependence on supply voltage and LET. The SP design shows lower upset ranges at nominal supply voltage, and the TP design shows generally greater upset ranges at higher LET values.

F. MCU Cluster Analysis

Analysis of cluster shape shows an elliptical shape for MCU clusters with the elongated axis along the BL direction. Bit-line upset ranges are generally larger than word-line ranges, as adjacent cells in the bit-line direction are in the same well. Charge clouds causing upset in the word-line direction must diffuse charge through multiple substrate/well junctions, and thus the ranges are greatly reduced. Word-line upset distance is more important in the design of SRAM circuits, as it helps to determine the interleaving distance and parameters for ECC.

Elliptical MCU shapes can be seen in Fig. 16, for three small MCUs with word-line upset ranges of 1, 2, and 3 cells. It is clear that upset range is increased in the BL

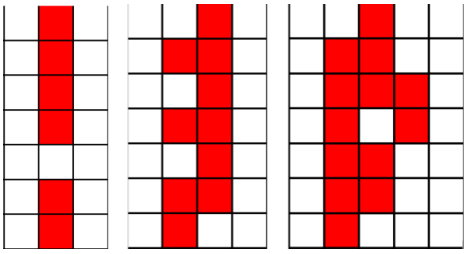

Fig. 16. Upset cells from MCUs with WL range of 1 cell (left), 2 cells (middle) and 3 cells (right). Upset range along the BL (vertical) is larger than WL range for each of these upsets.

(vertical in these figures) direction over the WL direction due to cells being in the same well. Examples of larger upset clusters observed from heavy ion exposures at reduced supply voltage are shown in Fig. 17. In these figures, the range of the charge cloud is expected to be bound by the outermost flipped cells from the center of the upset region, approximated by the black elliptical outlines on each figure. However, it is observed that not all of the cells within this region were observed to be upset. It is speculated that this masking of upsets is due to upset reversal. This is caused when the deposited charge is collected with significant magnitude over an extended period of time, greater than the feedback time of the SRAM cell. With continuing collection after an upset is reinforced by feedback, another bit-flip returns the cell to the original data.

All of the MCU upset-size results presented here do not correct for this possible upset reversal and depend directly on the upset cells that differ from the input data. Therefore, the number of affected cells is greater than the number of cells observed to be upset. Additionally, since this masking of errors is dependent on charge cloud collection characteristics, a reduction in charge collection may not necessarily lead to a direct reduction in MCU size or upset rate.

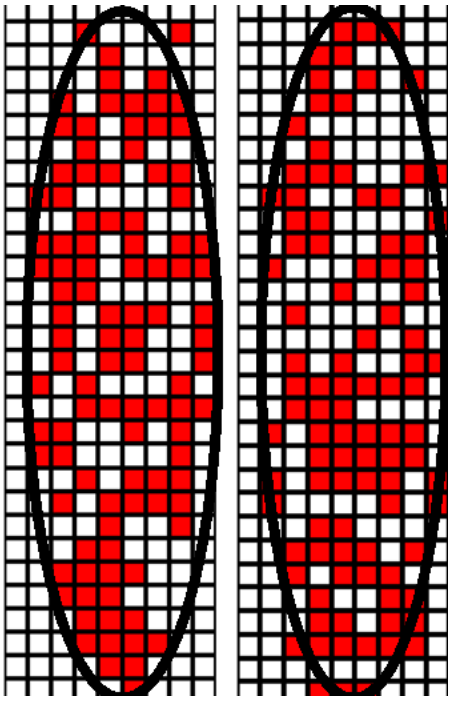

Fig. 17. Upset cells from MCUs with WL range of 1 cell (left), 2 cells (middle) and 3 cells (right). Upset range along the BL (vertical) is larger than WL range for each of these upsets.

V. Conclusion

This 5-nm bulk FinFET technology is susceptible to multi-cell upsets in both the terrestrial and space environment. Overall single bit and multi-bit upset relative event rates were presented for various heavy ion LETs, thermal neutrons, 14-MeV neutrons, and alpha particles. Increasing LET and decreasing operating supply voltage led to increased MCU contributions and increased multi-cell upset sizes and ranges along both the word line and the bit line. Single-port and two-port SRAMs show similar MCU relative contribution rates for the terrestrial environment but have significantly different responses to high LET heavy ions. Not all cells within an upset region are observed to be flipped from their original data, potentially caused by upset reversal. The information presented here will help designers understand the full extent of MCU to determine critical SRAM design parameters, such as error-correction circuit complexity and interleaving distance.

References

[1] E. Ibe, K. -i. Shimbo, T. Toba, Y. Taniguchi and H. Taniguchi, "Novel SER standards: Backgrounds and methodologies," 2010 IEEE International Conference on Integrated Circuit Design and Technology, 2010, pp. 203-207, doi: 10.1109/ICICDT.2010.5510259.

[2] M. A. Clemens, B. D. Sierawski, K. M. Warren, M. H. Mendenhall, N. A. Dodds, R. A. Weller, R. A. Reed, P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, S. A. Wender, and R. C. Baumann, "The effects of neutron energy and high-z materials on single event upsets and multiple cell upsets," IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 2591–98, Dec. 2011.

[3] A. D. Tipton, X. Zhu, H. Weng, J. A. Pellish, P. R. Fleming, R. D. Schrimpf, R. A. Reed, R. A. Weller, and M. H. Mendenhall, Increased rate of neutron induced multiple-bit upset at large angles of incidence," IEEE Trans. Dev. Mater. Rel., vol. 8, no. 3, pp. 565–570, Sep. 2008.

[4] T. Mérelle, F. Saigné, B. Sagnes, G. Gasiot, P. Roche, T. Carriére, M.-C. Palau, F. Wrobel, and J.-M. Palau, "Monte-Carlo simulations to quantify neutron-induced multiple bit upsets in advanced SRAMs," IEEE Trans. Nucl. Sci., vol. 52, no. 5, pp. 1538–1544, Oct. 2005.

[5] R. Baumann, "The impact of technology scaling on performance and limits to the efficacy of error correction," in Proc. IEDM Tech. Dig., Dec. 2002, pp. 329–333.

[6] B. L. Bhuva et al., "Multi-Cell Soft Errors at Advanced Technology Nodes," in IEEE Transactions on Nuclear Science, vol. 62, no. 6, pp. 2585-2591, Dec. 2015, doi: 10.1109/TNS.2015.2488630.

[7] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf "Charge collection and sharing in a 130 nm CMOS technology," IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3253–3258, Dec. 2006.

[8] K. Foley, N. Seifert, J. B. Velamala, W. G. Bennett, and S. Gupta, "IRT: A modeling system for single event upset analysis that captures charge sharing effects," in Proc. 2014 IEEE Int. Reliability Physics Symp. (IRPS), Jun. 2014, pp. 5F.1.1–5F.1.9.

[9] N. Tam, B. L. Bhuva, L. W. Massengill, D. Ball, M. McCurdy, M. L.Alles, and I. Chatterjee, "Multi-cell soft errors at the 16-nm

FinFET technology node," in Proc. 2015 IEEE Int. Reliability Physics Symp. (IRPS), May 2015, pp. 4B.3.1–4B.3.5

[10] N. Seifert et al., "Soft Error Susceptibilities of 22 nm Tri-Gate Devices," in IEEE Transactions on Nuclear Science, vol. 59, no. 6, pp. 2666-2673, Dec. 2012, doi: 10.1109/TNS.2012.2218128.

[11] Schor, D. "TSMC Details 5 nm". WikiChip Fuse. 21 Mar 2020.

[12] R. Grover et al., "A Reliability Overview of Intel's 10+ Logic Technology," 2020 IEEE International Reliability Physics Symposium (IRPS), 2020, pp. 1-6, doi: 10.1109/IRPS45951.2020.9128345.

[13] B. Narasimham, V. Chaudhary, M. Smith, L. Tsau, D. Ball and B. Bhuva, "Scaling Trends in the Soft Error Rate of SRAMs from Planar to 5-nm FinFET," 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, pp. 1-5, doi: 10.1109/IRPS46558.2021.9405216.

[14] Y. -P. Fang and A. S. Oates, "Characterization of Single Bit and Multiple Cell Soft Error Events in Planar and FinFET SRAMs," in IEEE Transactions on Device and Materials Reliability, vol. 16, no. 2, pp. 132-137, June 2016, doi: 10.1109/TDMR.2016.2535663.

[15] R.C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies", *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 305-316, 2005.

[16] E. Ibe et al., "Spreading Diversity in Multi-cell Neutron-Induced Upsets with Device Scaling," IEEE Custom Integrated Circuits Conference 2006, 2006, pp. 437-444, doi: 10.1109/CICC.2006.321010.

[17] I. Chatterjee et al., "Impact of Technology Scaling on SRAM Soft Error Rates," in IEEE Transactions on Nuclear Science, vol. 61, no. 6, pp. 3512-3518, Dec. 2014, doi: 10.1109/TNS.2014.2365546.