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# RF Performance and TID Hardness Trade-offs in Annular 45-nm RF SOI CMOS Devices

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***Abstract*—The operability and TID response of 45-nm annular RF SOI nFETs are evaluated and compared with standard layouts. All devices were exposed to 10-keV X-rays, up to a dose of 1 Mrad($SiO_2$), at both high-gate/low-drain and low-gate/high-drain irradiation conditions. Differences in damage response to DC and small-signal performance between samples are observed, as a result of TID-sensitive oxides and their proximity to key transport regions of the devices. Annular FETs are more TID tolerant than standard nFETs, while showing small RF performance tradeoffs for lower drive current and higher threshold voltage. TCAD is used to isolate critical oxides and damage mechanisms in annular and standard layouts to help confirm experimental data and observed damage trends. Taken together, these results suggest that Annular FETs represent a valid TID-hardening approach in small-lithography RF SOI CMOS technology platforms, for both DC and RF applications.**

***Index Terms*—Total Ionizing Dose, Silicon-On-Insulator (SOI), Silicon, nFET, Radiation, X-ray, Shallow Trench Isolation (STI), Buried Oxide Layer (BOX), TCAD, RF, Radiation-Hardening By Design, RHBD.**

## I. Introduction

SINCE its emergence over 10 years ago, 45-nm silicon-on-insulator (SOI) CMOS technology has been utilized heavily for both digital and RF circuit applications. Decreased body leakage and parasitic capacitance at high frequencies compared to similarly sized bulk CMOS has made SOI CMOS an especially desirable choice for many RF circuits [1]. Emerging RF applications in the space community have sparked interest in the technology's RF performance when subjected to high radiation environments [2].

45-nm SOI CMOS technology has previously been demonstrated to possess an improved resilience to total-ionizing-dose (TID) when compared with larger-node alternatives [3]. This TID tolerance is partially a result of its comparably thin gate oxide, which in turn reduces the density of traps generated during TID exposure [4]. This advantage, however, does not exclude it from degradation entirely. The inevitable damage experienced by these devices during TID exposure has led to various radiation-hardening by design (RHBD) techniques aimed at mitigation of these degradation effects [5].

One such RHBD technique involves changing CMOS gate layouts to an annular geometry [6]. In the presence of ionizing radiation, electron-hole pairs are generated in the oxides near the exposed device, creating oxide and interface traps [7]. As seen in Fig. 1, traps generated in the shallow-trench-isolation (STI) oxide of a standard FET will reside in close proximity to the channel of the device, which exists under the gate between the source and drain [3]. This phenomenon can cause increased off-state leakage current, among other degradations in performance [7]. This concern is ideally mitigated using annular FETs, which have no STI edge in the transport

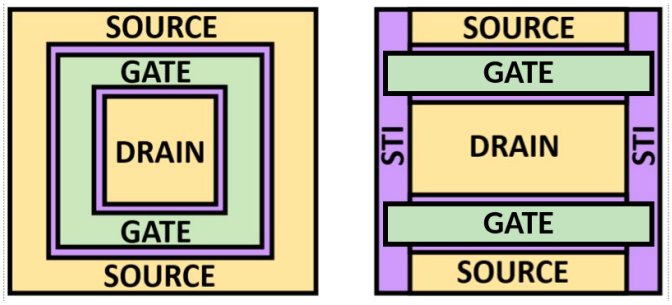


Fig. 1. A top-down view of both an annular MOSFET (left) and a standard layout MOSFET (right). Note that for the annular FET the gate does not overlap the STI, unlike the standard FET.

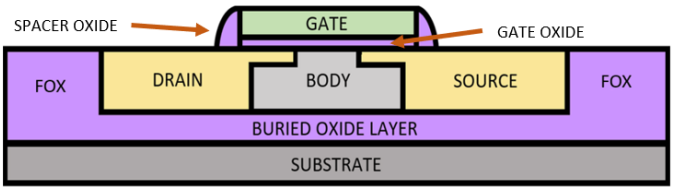


Fig. 2. Cross-section of a 45-nm SOI CMOS device. Note the thin source and drain extensions that reach under the gate oxide, as well as the spacer oxides on either side of the gate. The structure is built on a buried oxide (BOX) layer, insulating it from the substrate to reduce capacitance and improve isolation.

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This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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path [6], [8]. While such layouts are advantageous from a TID perspective, other vulnerable oxides still exist in the device, such as the self-alignment spacer oxides, gate oxide, and buried oxide (BOX).

Although the general benefits of annular FETs in a high TID environment have been previously demonstrated, this approach is yet to be adequately characterized in a 45-nm SOI CMOS technology targeting RF performance. Such devices utilize source and drain extensions vital to their high-quality RF performance, which can only be fabricated with the use of angled source/drain ion implantation [9]. These extensions run from the highly doped source and drain regions underneath the gate, as seen in Fig. 2 [10]. This approach limits the ability to fabricate devices in more than one layout orientation, since the angled implants would be incorrectly oriented, resulting in sub-optimal or even inoperable MOSFETs.

In the present investigation, various nFET layouts were fabricated, regardless of their anticipated feasibility, in order to better establish damage mechanisms and trade-offs in advanced-node RF CMOS-on-SOI technology. Horizontally oriented "on-axis", vertically oriented, "off-axis" horizontally oriented, and annular nFETs, consisting of two horizontal and two vertical gates, were designed, layed-out, and fabricated. The on-axis device was fabricated with implant angles aligned as intended by the foundry (i.e., optimally, the process-of-record control), while off-axis devices had incorrectly oriented implants. The differences in layout can be observed in Fig. 1. Note that the off-axis case is simply a 90°-rotated on-axis device of identical gate width and length (W/L). The present work assesses the feasibility of using annular MOSFETs in a commercial 45-nm SOI CMOS process for radiation intense RF applications, while illuminating the benefits and drawbacks of this RHBD approach in nanoscale SOI CMOS technology, in both the DC and RF domains. These devices were analyzed to evaluate how their performance changes with respect to increasing TID from a 10-keV X-ray source. In addition to experimentally collected data, TCAD models were created to isolate the damage mechanisms expected in specific oxide regions present in the annular and standard layouts. The effects of TID damage in the spacer oxides, BOX, and STI were isolated and analyzed to characterize their effects on nFET RF performance. Specifically these models were created to confirm TID damage mechanism trends and changes for each layout orientation.

## II. Experimental Setup

Devices were fabricated in the GlobalFoundries 45RFSOI CMOS process technology [11]. On-axis and off-axis devices were optimized for RF performance, which require larger W/L ratios, and had 40 fingers of 1 $\mu$m each to give a total width of 40 $\mu$m. Meanwhile, the annular FETs were composed of 4 "devices" with 10 $\mu$m width each, connected in a square configuration. Thus, the total gate areas were comparable across all three variants.

Experiments were performed using the ARACOR Model 4100 Semiconductor Irradiation System at Vanderbilt University, at a dose rate of 30.3 krad($SiO_2$)/min [12]. Two different

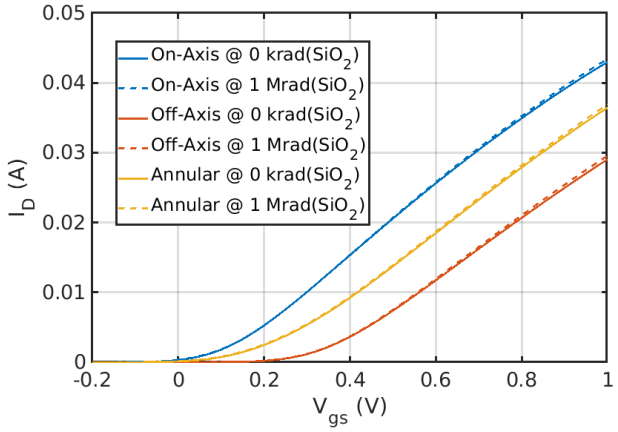


Fig. 3. Transfer curves for the 3 different layouts, observed pre-irradiation and after 1 Mrad($SiO_2$) with a gate-high, drain-low irradiation condition. Curves are taken at $V_{ds}$ = 1.0 V on a linear scale.

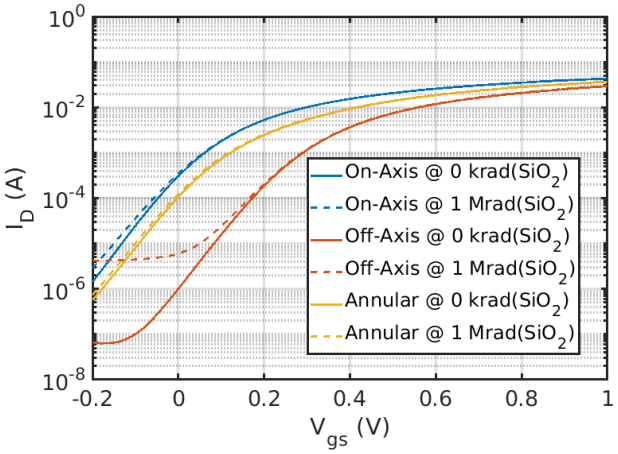


Fig. 4. The data in Fig. 3, shown on a semi-log scale to accentuate the drain leakage at low $V_{GS}$.

bias conditions were used during exposure to ensure the worst case was being observed, as well as to evaluate potential differences due to bias conditions. In one condition, samples were biased with a drain voltage of 0 V and a gate voltage of 1 V ("gate-high, drain-low") during exposure. A second sample set had a gate voltage of 0 V and a drain voltage of 1 V ("gate-low, drain-high") during exposure. Both RF and DC data were taken at 0, 30, 100, 300, and 1000 krad($SiO_2$) to assess the effects of TID on device RF performance [13].

An Agilent 4155 Semiconductor Parameter Analyzer was used for DC measurements, with a minimum current resolution of 100 fA. Transfer curves ($I_D$ vs. $V_{gs}$) were collected for each device tested, at multiple $V_{ds}$ values. For all $V_{ds}$ values, S-parameters were measured from DC to 26 GHz using a Keysight P5004A vector network analyzer. Anritsu K251 bias tees were used to provide DC bias during S-parameter measurements. These transfer curves and S-parameters were used in post-processing to determine metrics such as device unity current gain cutoff frequency ($f_T$) and dose-dependent

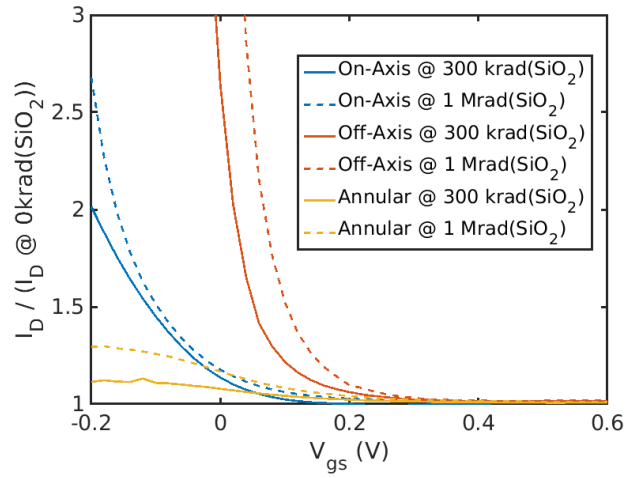


Fig. 5. Transfer curves for all 3 layout geometries at 300-1000 krad($SiO_2$) with gate high, drain low irradiation condition, normalized to their respective $I_D$ values at pre-irradiation.

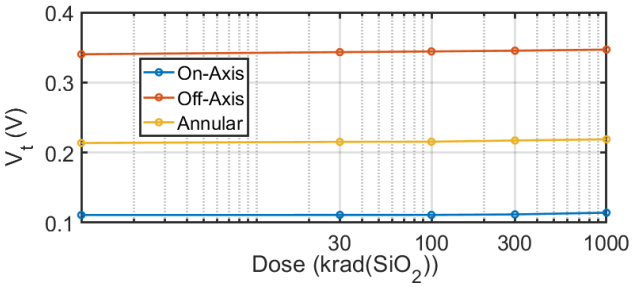


Fig. 6. $V_T$ for the 3 different layouts as a function of a gate high, drain low irradiation condition.

threshold voltage ($V_T$).

## III. Measurement Results

### A. DC Characterization

The pre-irradiation and 1 Mrad($SiO_2$) cases for the three samples in the gate-high, drain-low irradiation condition can be seen on a linear scale in Fig. 3, and with logarithmic Y-axis in Fig. 4. At a gate voltage of -0.2 V, the three device types exhibit different levels of increased leakage with respect to their pre-irradiation values. These changes are best visualized in Fig. 5. At $V_{gs}$ = -0.2 V, the annular case exhibits the least degradation with increasing TID, as expected, since these leakages primarily come from traps along the STI/channel interface. Indeed, at 1 Mrad($SiO_2$), the annular FET's off-state leakage changes by less than 30%, compared to the on-axis case of over 150% change. These differences in leakages are especially relevant for digital circuits and exhibit one of the main benefits of annular FETs for digital applications that holds even down to 45 nm CMOS. For RF circuits, these leakages correspond to changes in small-signal drain-source resistance ($R_{ds}$), which is analyzed below.

$V_T$ values were extracted using using X-intercept extrapolation from peak-transconductance bias [14], [15]. The values can be seen in Fig. 6. Minimal changes were observed as a function of dose. The largest percent change was below 2%, for the off-axis case. This negligible change is expected, given the very thin gate of the device [1] [3].

Together, these DC data demonstrate two trends: First, regardless of the layout topology chosen, $I_D$ at high $V_{gs}$ will be affected similarly, suggesting this increase in $I_D$ is not caused by the STI/channel interface. The cause of this increase is examined in Sec. IV. Second, the off-state leakage varies significantly depending on topology, as expected. The annular device exhibited the highest resilience to TID damage, meaning if off-state leakage is critical to system performance (e.g., memory circuits), annular gate geometries represent a valid RHBD approach, and can operate as useful MOSFETs even in nano-scale RF-focused platforms utilizing angled source/drain implantations.

### B. RF Characterization: Amplifier Applications

In addition to the transfer characteristics, the AC S-parameters for each sample were measured as a function of dose, up to 26 GHz. $f_T$ was obtained from extrapolation of RF current gain. SOLT calibration was used to shift the RF reference plane to the pads of the tested die, and open-short de-embedding was applied to remove the effects of parasitic layout components. Fig. 7 shows $f_T$ vs. gate overdrive voltage ($V_{gs} - V_T$) of the three layouts, at 0 and 1 Mrad($SiO_2$). For all layouts, $f_T$ increase slightly with exposure. Similar to the DC results for the three layouts, the pre-irradiation peak $f_T$ performance of the annular FETs lies between that of the on-axis and off-axis cases. Thus, annular FETs in this technology may be thought of as a combination of on-axis and off-axis devices. The $f_T$'s of all three geometries exhibit similar changes in both direction and magnitude as a function of TID.

A simple equation for the $f_T$ of a CMOS transistor is

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1}$$

where $g_m$ is the transconductance, $C_{gs}$ is the parasitic gate-source capacitance and $C_{gd}$ is the parasitic gate-drain capacitance. To determine why $f_T$ increases with dose, $g_m$, $C_{gs}$, and $C_{gd}$ were extracted as well, according to the equations below.

$$g_m = \Re(Y_{21}) \tag{2}$$

None of the layouts exhibited noticeable changes in their parasitic capacitances as a function of dose. Meanwhile, Fig. 8 shows an increase in $g_m$ vs. dose for all layouts. Since the capacitances were fixed, the increase in $g_m$, which is expected given the increase in drive current in Fig. 3, can explain the observed increase in $f_T$. The change in $f_T$ could have a minor effect on most RF applications. Amplifiers and circuits less dependant on constant $f_T$ should not be impacted by these slight shifts. This would also be the case for matching circuits which are designed for frequency ranges typically larger than the shifts observed. That is to say, if only amplifier performance was observed, all three devices would look comparable with respect to TID. To test an RF application that may better separate the individual performance of each device, RF switches are considered.

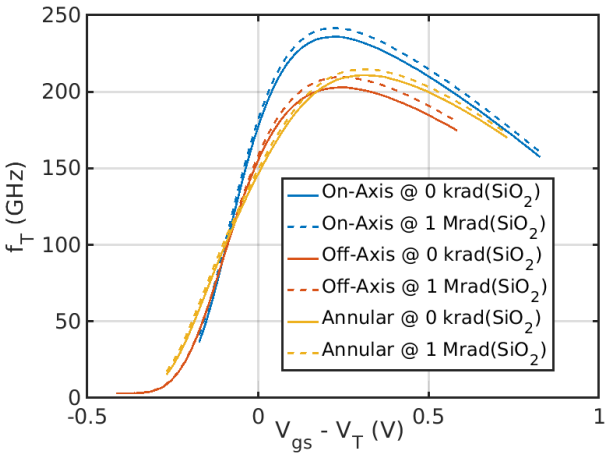


Fig. 7. $f_T$ vs. overdrive voltage ($V_{gs}$ - $V_T$) for the three layouts discussed. Values are shown at 0 and 1 Mrad($SiO_2$). Gate high, drain low irradiation condition.

### C. RF Characterization: Switch Applications

Although $f_T$ changes are similar for all three layouts, deviations can be seen in each layout's drain-source resistance ($R_{ds}$), which is critical to the performance of RF switches. This AC parameter can be extracted [16] using (3).

$$R_{ds} = \frac{1}{\Re(Y_{22})} \tag{3}$$

where $\Re\{\cdot\}$ is the "real-part" operation. $R_{ds}$ was observed to be constant across frequency, so the average value from DC to 26 GHz was used.

$R_{ds}$ in two different biasing conditions can be observed in Fig. 9. The first case shows $R_{ds}$ in the "on"-state ($R_{ds,on}$) at $V_{gs}$ = 1 V and $V_{ds}$ = 0 V. In an RF switch, a lower value of $R_{ds,on}$ is desired to decrease insertion loss [17], according to

$$\text{Insertion Loss} = 1 + \frac{R_{ds,on}}{Z_0} \tag{4}$$

where $Z_0$ is the reference impedance of the system (e.g., 50 Ω). The second case seen in Fig. 9 is biased in the "off"-state at $V_{gs}$ = $V_{ds}$ = 0 V ($R_{ds,off}$). $R_{ds,off}$ is important for determining how well an open switch isolates its input from its output, given by

$$\text{Isolation} = 1 + \frac{R_{ds,off}}{Z_0} \tag{5}$$

No data points are shown for $R_{ds,off}$ for the off-axis device, as values were too large ($>$ 10 kΩ) to extract accurately.

There are noticeable differences in both $R_{ds}$ magnitude and percent change with dose in both the on-state and off-state, when comparing the three layouts. This manifests itself as insertion loss and isolation changes, which are important to RF switches. Changes in insertion loss and isolation over dose are shown in Tables I and II.

The annular profile has an increased value of $R_{ds}$ at both biasing conditions, when compared to the on-axis case. This equates to an improvement in isolation and a degradation in insertion loss, which is intrinsic to the gate geometry. The

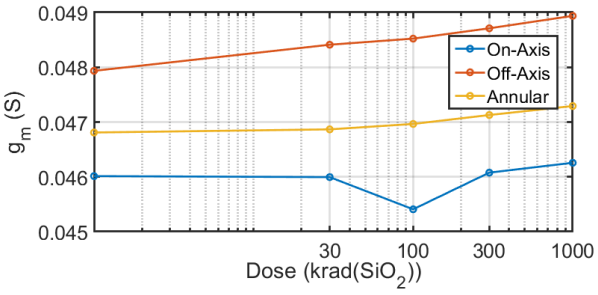


Fig. 8. Calculated $g_m$ for the three observed layouts from 0 to 1 Mrad($SiO_2$) with gate high, drain low irradiation configuration.

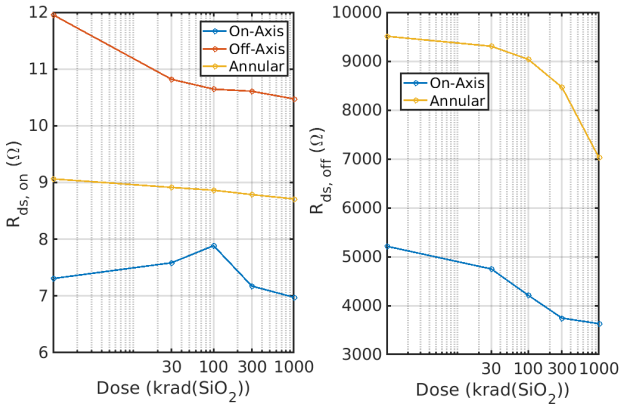


Fig. 9. $R_{ds}$ with $V_{gs}$ = 1 V and $V_{ds}$ = 0 V ($R_{ds,on}$) to detect insertion loss (left). $R_{ds}$ with $V_{gs}$ = $V_{ds}$ = 0 V ($R_{ds,off}$) to determine isolation (right). Gate high, drain low irradiation condition.

second noteworthy difference lies in the performance changes for each layout as a function of dose. The annular FET isolation changes less than the standard FET as a function of dose, and is notably larger. In fact, the annular device offers better isolation performance, regardless of TID, and may be considered an important advantage for RF applications requiring high signal isolation. In the case of insertion loss, however, the magnitudes of changes are similar between the standard and annular FET, with the on-axis FET demonstrating a slightly better insertion loss.

TABLE I
INSERTION LOSS ($IL$) AT 0 AND 1MRAD($SiO_2$)

| Layout | $IL$ @ 0 rad($SiO_2$) | $IL$ @ 1 Mrad($SiO_2$) | Change |
|---|---|---|---|
| On-Axis | 1.185 dB | 1.135 dB | -0.050 dB |
| Off-Axis | 1.862 dB | 1.652 dB | -0.210 dB |
| Annular | 1.442 dB | 1.395 dB | -0.047 dB |

TABLE II
ISOLATION AT 0 AND 1MRAD($SiO_2$)

| Layout | Iso. @ 0 rad($SiO_2$) | Iso. @ 1 Mrad($SiO_2$) | Change |
|---|---|---|---|
| On-Axis | 40.445 dB | 37.336 dB | -3.109 dB |
| Annular | 45.629 dB | 43.017 dB | -2.612 dB |

These $R_{ds}$ values further demonstrate the efficacy of using

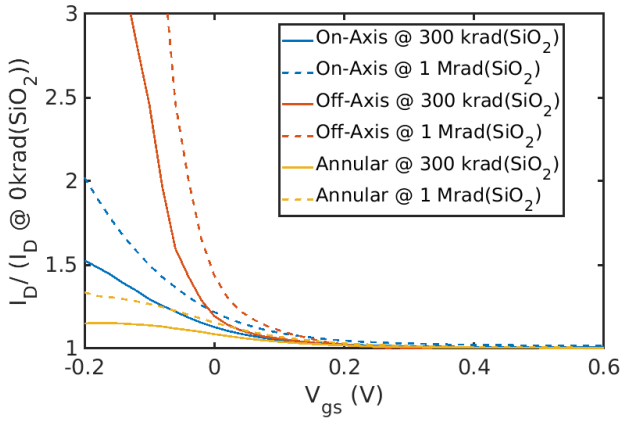


Fig. 10. Transfer curves for all 3 layout geometries at 300-1000 krad($SiO_2$) with gate low, drain high irradiation condition, normalized to their respective $I_D$ values at pre-irradiation.

annular gate FETs in small node RF technologies. In addition to these devices exhibiting excellent DC and AC performance, they could feasibly prove to be especially useful in RF circuits applications requiring high RF isolation.

### D. Bias Dependence

Differences in performance were observed based on biasing conditions during irradiation. For the purposes of demonstrating worst case, data collected in the gate high, drain low was used to evaluate the operability and effectiveness of annular gate FETs compared to the on-axis cases. After analysis, this bias was found to be the case that exhibited more damage; however, there are comparisons between the conditions still worth noting. Viewing Fig. 10, it can be seen compared to Fig. 5, that regardless of condition, the annular FET off-state leakage increased in very similar magnitudes with a roughly 30% change. This is not the case when viewing the on-axis case, which showed a smaller increase in off-state leakage current, 150% compared to 100% at the 1 Mrad($SiO_2$). This could be a result of the way the design was layed out, or may be intrinsic to the differences in annular and standard gate geometries. The difference in field between the two biasing conditions may only affect standard layouts, further supporting the consistency of annular; however, more analysis is needed to both discern the mechanisms causing this discrepancy and assess the validity of this statement.

## IV. TCAD Analysis

The feasibility of using an annular layouts as a viable RF device has been explored for the 45-nm CMOS SOI technology. The combined TID response and RF performance offer a highly encouraging picture for RF applications. The annular layout improves TID resiliency when compared to the on-axis device regardless of irradiation configuration.

The benefits of the annular topology are clearly seen when viewing the off-state leakage and $R_{ds,off}$. Although the annular geometry has no STI edge, there are still other oxides that can potentially exhibit TID sensitivity, such as the gate oxide, spacer oxides, and BOX [3]. Therefore, it is possible that observed changes in $g_m$ and drive current may result from traps existing in these other oxides, while the differences in leakage increases between geometries and $R_{ds}$ shifts may result from effects of charge trapping in the STI [15].

### A. TCAD Simulations

To better understand the results underlying these layout-dependent changes in RF performance and TID response, calibrated Sentaurus TCAD models were created to assess the impact of radiation-induced trapped charge in the spacer oxides, buried oxide, and STI. These models were created to determine why annular FETs exhibit off-state leakage with no STI, and why drive current increases in all devices.

### B. BOX/Spacer Effects

2-D models were first created to assess the changes in performance trends expected by the addition of traps into sensitive oxides induced by radiation. Fig. 11 shows one of the model cases created and used for TID induced trend extraction. The initial use of 2-D was imperative to preserve time and reduce complexity, before eventually creating 3-D models, which are ultimately needed. This model can explore the effects of BOX traps as well as spacer-oxide traps which can exist at the spacer/SOI interface, or the gate oxide itself, and how they affect performance. Notably, the STI could not be included in these simulations, considering the STI exists in the dimension not expressed in this model. For this model, two cases involving the addition of oxide trap densities ($N_t$) in only the spacer and only the buried oxide layers were explored. Only interface trap cases, only oxide trap cases, and interface with oxide trap cases were explored, in order to help understand the effects of each trap species. The ability to isolate the oxides and trap types helps to deconvolve the operative mechanisms that may or may not be influencing data trends seen experimentally.

Changes in transfer curves were observed as a function of various trapped-charge concentrations, for both oxides, which were assessed independently. These changes can be seen in Fig. 13 and Fig. 12, which shows the transfer curves as trapped charge was added, normalized to the 'no trap' case. Note that these figures show the addition of oxide traps. Adding large concentrations of interface traps alone did not align with experimental data, implying this assumption was incorrect for the mechanisms that occurred during exposure. For cases where both interface and oxide traps were added in various concentrations, differences in oxide trap densities better matched experimental data, implying the dominance of oxide trap mechanisms over interface trap mechanisms when looking specifically at the distinctions between the geometries in their leakage and DC performance trends.

The addition of trapped charge in the BOX causes increases in drive current at higher $V_{gs}$, similar to that seen in the experimental data. This similarity can be seen in Fig. 12. This may be a result of an increased back gate effect, where current is able to flow between the source and drain. Note that this back gate is noticeably weaker than the main current pathway

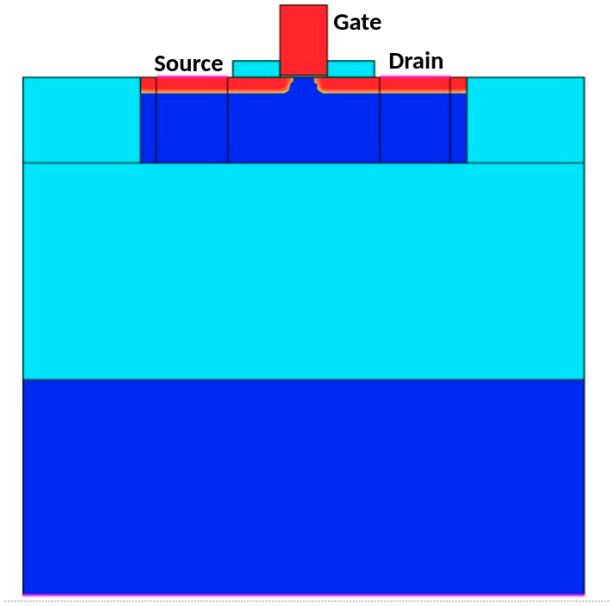


Fig. 11. 2D TCAD model of nFET. Oxides are light blue. Silicon is dark blue. Trap states added to the two spacer oxides next to gate above the drain and source as well as the BOX between SOI and substrate to assess degradation trends.

in the channel even with large concentrations of traps added. The relative magnitude of these two current pathways could explain the very slight increases in drain current observed experimentally. This in turn, provides a plausible explanation for the similarity in responses of the different devices layouts, which all saw increases in drain current at high $V_{gs}$.

Spacer oxide trap transfer curves display different degradation mechanisms. Normalized off-state leakage trends can be seen in Fig. 13, with minimal changes to drive current at high $V_{gs}$, but increases in off-state leakage. This follows the experimental data, which showed increases in leakage for all devices, with marginally less leakage in the annular case. These results indicate how the annular FET, which has no STI/channel interface, can still experience changes in off-state leakage. To better assess distinctions in off-state leakage between spacer and STI effects, a 3-D analysis is presented next.

### C. STI Effects

The off-state leakage seen in the experimental data is partially explained by traps in the spacer oxide. To understand the differences in off-state leakage between the on-axis and annular cases, a 3-D nFET model was constructed. The calibrated model is shown in Fig. 14, and has the same doping concentrations and geometries as the calibrated 2-D model. With this 3-D model, the effects of traps in the STI can be assessed, as seen in Fig. 15.

Similar to spacer traps, STI traps degrade off-state leakage. However, the effects of traps in either oxide are not equivalent. First, the STI traps cause leakage on a much larger scale with the same trap densities. This contrast is seen in the $N_t$ = $10^{13}$ cm$^{-2}$ cases in Fig. 13 and Fig. 15. The same trap

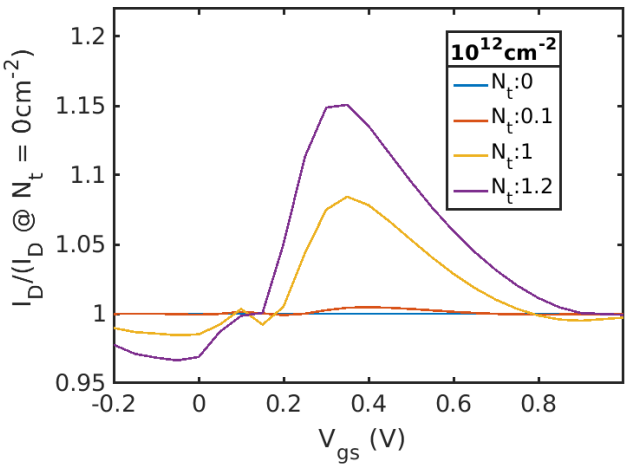


Fig. 12. Normalized transfer curves for a standard orientation nFET with varying oxide trap densities ($N_t$) only in the buried oxide (BOX).

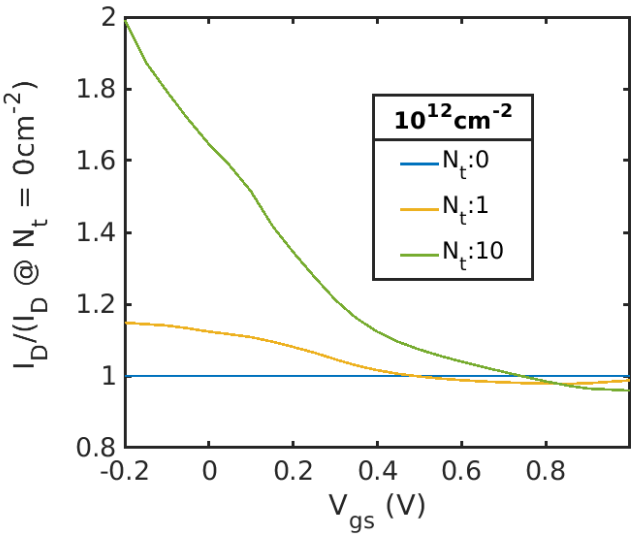


Fig. 13. Normalized transfer curves for a standard orientation nFET with varying oxide trap densities ($N_t$) only in the spacer oxides.

density in the STI causes an over four times increase in off-state leakage at $V_{gs} = -0.2$ V when compared to the spacer oxide case. The second distinction is the bias at which each degradation mechanism affects off-state leakage. In the case of spacer oxide traps, degradation can be seen in biases as high as $V_{gs} = 0.5$ V. STI damage begins increasing drastically at lower biases with current leakage values above $V_{gs} = 0.4$ V staying relatively negligible compared to its $V_{gs} = -0.2$ V values.

With the differences in the three sensitive oxides trap-induced degradation mechanisms known, DC leakage trends can be better separated according to the most sensitive oxide, a seen in Fig. 16. Small increases in drive currents can likely be attributed to BOX traps. Increases in leakage at positive $V_{gs}$ are likely a result of spacer-trap-induced degradation, which appears at higher $V_{gs}$ than STI trap induced degradation. Lastly, off-state leakage degradation at low $V_{gs}$ is dominated

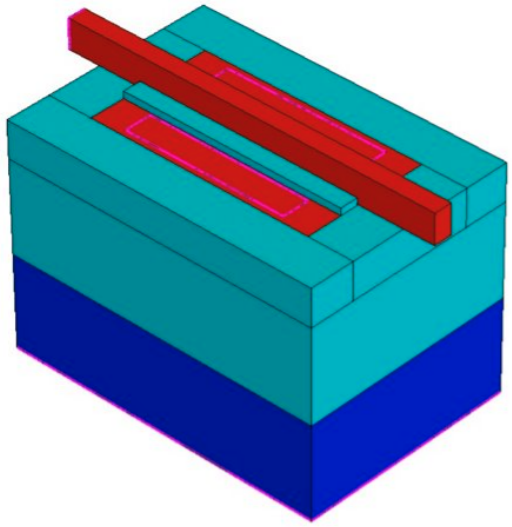

Fig. 14. 3D TCAD model of nFET. Trap states added to spacer oxides next to gate, BOX between SOI and substrate, and STI under gate next to SOI to assess degradation trends.

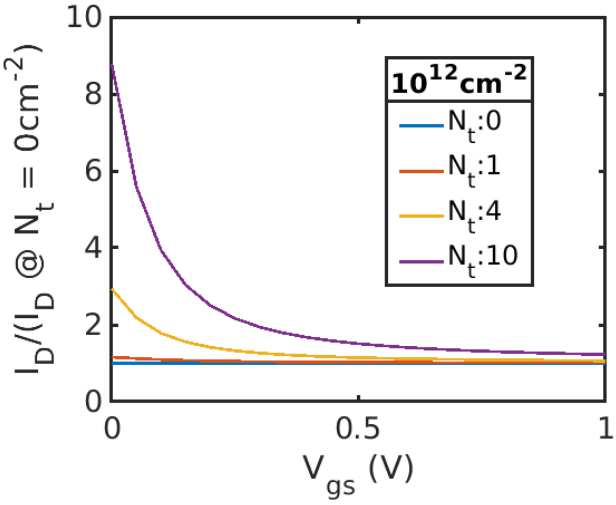


Fig. 15. Normalized transfer curves for a standard orientation nFET with varying oxide trap densities ($N_t$) only in the STI.

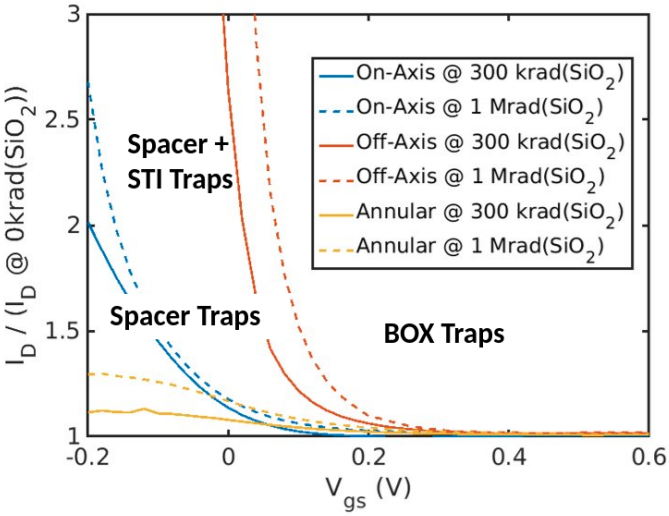


Fig. 16. Normalized $I_D$ for each device at various doses as a function of $V_{gs}$. leakage trends labeled by the sensitive oxide with traps likely causing the effect seen.

by STI trap mechanisms, accounting for the sharp increases in off-state leakages for both the on-axis and off-axis devices. Because of the annular FETs lack of STI to channel interface, its leakage stays noticeably much lower than the other two cases, and its leakage is likely only the result of comparably less oxide traps in the spacer oxide.

We conclude that removing the STI-channel interface reduces but does not eliminate effects of radiation-induced charge trapping in these 45-nm RF CMOS devices. Removing this degradation mechanism does still greatly improve off-state leakage performance and TID resiliency, confirming the main application for annular FETs in integrated circuit design as radiation-hardened alternatives to conventional FET layouts. The remaining leakage seen in annular FETs after exposure is likely the result of spacer oxide damage, while the increases in drive current for all devices, and as a result $f_T$, are likely due to BOX traps.

## V. Summary

Three different nFET layouts were created in a 45-nm CMOS on SOI RF process to investigate the TID-hardness and performance trade-offs of annular designs as well as their general operability in a high speed nano-scale RF SOI technology platform. Annular nFET designs were confirmed to operate as functional nFETs for DC and RF purposes. TID-hardness was improved in the annular layouts, but some degradation was still observed. This degradation was smaller than standard nFET layouts. The annular devices suffer slightly worse drive current, $f_T$, and switch insertion loss, but exhibit improved TID tolerance, especially in the case of off-state leakage, $R_{ds}$ shifts with dose, and isolation. These results were observed in the worst case irradiation condition.

With these trade-offs in mind, annular nFETs represent a viable alternative in systems not requiring the higher drive current capabilities, or which do not operate near the upper limit of $f_T$. The TID resiliency and lower yet substantial performance of annular devices make them well-suited as potential replacements to standard nFETs in 45-nm SOI CMOS integrated circuit applicants for high-radiation environments. A mixure of both classical and annular layouts may ultimately prove optimal for many RF applications.

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