SAND2022-9556C

Single Event Upset and Total Ionizing Dose Response of 12LP FinFET Digital Circuits

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***Abstract*— Experimental results show the response of Global Foundries (GF) 12-nm bulk FinFET digital structures to 60 keV x-ray, ^{60}Co gamma rays, and heavy ions. Among the structures are circuits of 19 scan chains each made up of 15840 digital flip-flops (DFF). Other test structures include digital cells including modified inverters, two input NOR, three input NOR, two input NAND, and three input NAND. Heavy ion sources and 63.6 rad(SiO_2)/s gamma rays were provided by Sandia National Laboratories in Albuquerque, New Mexico. The x-ray source was provided by the SES facility at AFRL in Albuquerque, New Mexico. Single event upset (SEU) cross-sections vs. ion linear energy transfer (LET) for the digital flip-flop chains are extracted. Total ionizing dose (TID) experimental results for both the modified digital cells and DFF circuits are reported.**

***Index Terms*—FinFET, total ionizing dose, single event upset, digital flip-flop.**

I. Introduction

THIS paper reports on the total ionizing dose (TID) and single event upset (SEU) response of digital circuits and modified cell structures fabricated in the Global Foundries 12LP FinFET technology. The test circuitry was designed at Arizona State University for the Navy S2MARTS and Sandia National Laboratories SEEEC Grand Challenge program to support the evaluation of radiation susceptibilities in advanced non-planar CMOS processes. Test circuits were D flip-flop (DFF) cells arranged into long shift registers. A gate level schematic of one shift register with clock circuitry is shown in Fig. 1. The clock and data lines run in opposite directions to alleviate any timing race-through. TID effects data were collected on transistor test structures made by modifying digital cells from the same FinFET technology. The TID transistor data show a similar trend to what King *et al.* reported; that is, a significant increase in off-state and sub-threshold current with increasing ionizing radiation exposure [1-2].

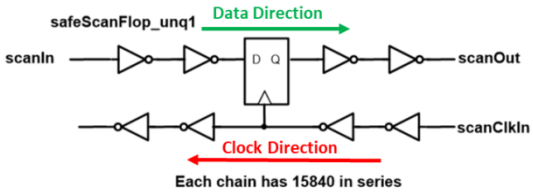


Fig. 1. Schematic of DFF cell in scan chain on digital circuit test chip (TC3).

The TC3 microchip (third test chip) was manufactured for the S2MARTS and SEEEC programs. The standard cell library DFF was used. SEU and TID testing were performed at the Ion Beam Laboratory (IBL) at Sandia National Laboratories and the SES facility at AFRL in Albuquerque, New Mexico. The transistor test structures were included on test chip one (TC1). TC1 consists of a 25x15 pad array. Each column in the array has two modified gate cell structures, making a total of thirty. The structures consist of the standard digital library cells: inverter logic gate, two-input NAND logic gate, three-input NAND logic gate, two-input NOR logic gate, and three-input NOR logic gate. On TC1, each logic gate in a structure is split to isolate the PMOS pull-up network (PUN) and the NMOS pull-down network (PDN). Isolating the PUN and PDN network allows for individual measurements to be taken on the transistors that make up the respective logic gate networks. In this paper we go over the experimental details and present the responses these test chips had to various types of radiation.

II. Experimental Details

The single event upset (SEU) response of the DFFs on TC3 was characterized at the IBL. The ions used in the testing were produced by either the IBL's Tandem or Pelletron beam lines. The Tandem beam (setup shown in Fig. 2a) provided data on strikes by larger energy ions consisting of Carbon, Boron,

Manuscript received February 2, 2022; accepted June 15, 2022. Date of publication TBD; date of current version July 7, 2022 This work was supported by the Navy Strategic & Spectrum Missions Advanced Resilient Trusted Systems (S2MARTS) program, Project No. S2MARTS 19-03 and the SEEEC Grand Challenge, part of the Laboratory Directed Research and Development program at Sandia National Laboratories. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government. The authors would like to thank Matthew Gadlage of Navy, Crane for his support of this work.

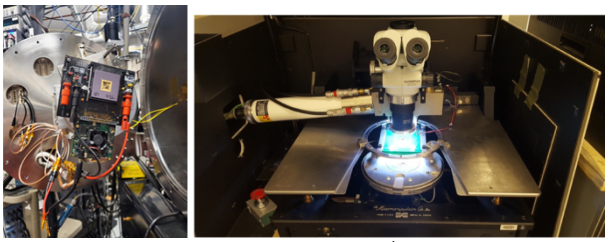
Oxygen and Silicon. The Silicon results are not reported as the tests produced negligible SEUs due to the ion having too low of linear energy transfer (LET) in the sensitive region. The Pelletron Beam was used to source the lighter ions, three energies for Hydrogen and one energy for Helium.

Table 1
Test conditions for radiation testing performed on the TC3 12nm LP chip.

Ion Used	Average Fluence (ions/cm²)	Linear Energy Transfer (MeV*cm²/mg)	Bias Voltage (V)
O	$4.84x10^7$	6.45	0.4
C	$4.95x10^7$	4.859	0.4
B	$4.88x10^7$	3.225	0.4
He	$1.0x10^9$	0.731	0.4
1.0 MeV H	$1.0x10^9$	0.3225	0.4
1.8 MeV H	$1.0x10^9$	0.1462	0.4
2.8 MeV H	$1.0x10^{10}$	0.0903	0.4
O	$4.88x10^7$	6.45	0.8
C	$4.88x10^7$	4.859	0.8
B	$5.06x10^7$	3.225	0.8
He	$1.0x10^7$	0.731	0.8
1.0 MeV H	$1.0x10^7$	0.3225	0.8
1.8 MeV H	$1.0x10^7$	0.1462	0.8
2.8 MeV H	$1.0x10^7$	0.0903	0.8
O	$4.83x10^7$	6.45	1.2
C	$4.91x10^7$	4.859	1.2
B	$5.0x10^7$	3.225	1.2
He	$1.0x10^9$	0.731	1.2
1.0 MeV H	$1.0x10^9$	0.3225	1.2
1.8 MeV H	$1.0x10^9$	0.1462	1.2

Each SEU test was conducted at voltage levels of 0.4V, 0.8V, and 1.2V. Furthermore, each test had either a low fixed clock state or a high fixed clock state during beam exposure. The different clock states were used to investigate if the static input clock state impacted the SEU rate. The data loaded into the scan chains during beam exposure consisted of all binary 1s, all binary 0s, or checkerboard (4 zeros followed by 4 ones). An Opal Kelly FPGA (field programmable gate array) board was used to send and receive data between TC3 and the PC after irradiation.

TID tests were performed on TC1. The TC1 structures were exposed in the ARACOR 60 keV x-ray source housed in the AFRL Space Electronics Branch laboratory on Kirtland AFB, NM (setup shown in Fig 2b). Seven TC1 chips were tested with two devices used as a control while the other five were exposed in the x-ray source. Probe cards were designed to bias two adjacent columns on the TC1 chip while the transistors were exposed to x-rays up to 2 Mrad(Si). The column design of TC1 is presented in Fig. 3. TID tests were also preformed using a ^{60}Co 63.6 rad(SiO_2)/s gamma ray source at Sandia. For these tests, two TC1 chips were tested, one was used as control the other was exposed to the ^{60}Co gamma rays up to 2 Mrad(SiO_2). The NMOS logic networks had 0.8V applied to the gate and 0V applied to the source, drain, and body making it biased in the ON state during exposure. The PMOS logic networks had 0.8V applied to the gate and 1.6V applied to the source, drain, and body, making V_{gs} = -0.8V thus making the PMOS transistors ON biased for radiation tests. Only NMOS cells were tested for the gamma ray experiments at Sandia. Drain current vs gate voltage (I_d vs. V_g) sweeps were performed after each exposure using the Keysight B1500A semiconductor parameter analyzer. Five repeated I_d vs. V_g sweeps were run on each device under test (DUT) after each irradiation step to ensure consistency among the respective data sets. During each sweep, the NMOS V_{ds} was biased to 0.8V and the PMOS V_{ds} was biased to -0.8V. It should be noted that for series NMOS (modified NAND) and PMOS (modified NOR), the V_d corresponds to the top (NMOS) or bottom (PMOS) terminal in the cascaded stack (see Fig. 3).



a. b.

Fig. 2. a) Tandem heavy ion beam setup for TC3. b) ARACOR 60 KeV X-Ray beam setup for TC1.

TID effects in the DFF circuits were also characterized through measurements of supply current to the shift registers after stepped ionizing radiation exposure stress. These data were taken in both the Pelletron Ion Beam in the IBL and the ARACOR X-ray source at the AFRL SES facility. The TID response of the supply current on the DFF circuits showed a measurable increase consistent with what was observed in the TC1 transistor data. These results are shown in Fig. 38.

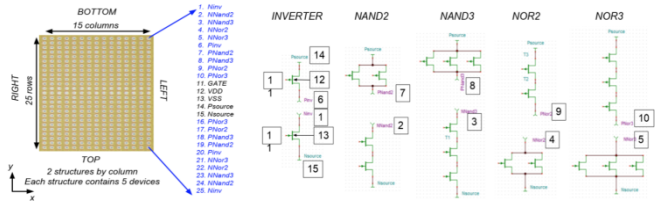


Fig. 3. Transistor design of the devices on TC1 that were used for TID data

III. Experimental Results

A. SEU Experimental Data

The SEU data are shown in Figs. 4-7. The SEU vs. LET cross sections are similar to the cross sections that *Ball et al.* observed in their paper in 2018 [3]. When the input data are the same as the clock state under test state the number of observed errors is typically less. That is, when the data are all 0s and the clock state is low under test the error rate is typically lower when compared to the high clock state under test. Similarly, when the data are all 1s and the clock state under test is high, generally less errors are observed when compared to the same data input with the clock state under test being low. Overall, the data 0 and low clock under test showed the least amount of SEUs across all the voltages. For each test, the supply voltages were 0.4V, 0.8V, and 1.2V.

Fig. 4 shows the SEU cross-section (cm²/FF) vs. LET (MeVcm²/mg) when the data was all zeros and the clock was

low when under test. Fig. 5 plots the SEU (cm^2/FF) vs. LET (MeV*m^2/mg) obtained when the data was all zeros and the was clock high when under test.

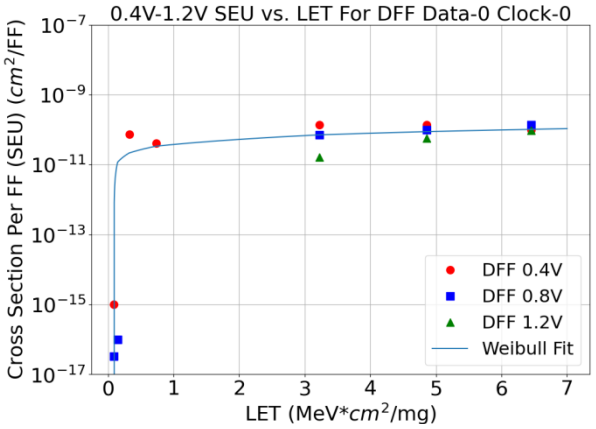


Fig. 4. SEU cross-section/FF vs. LET (data 0s, clk_test lo).

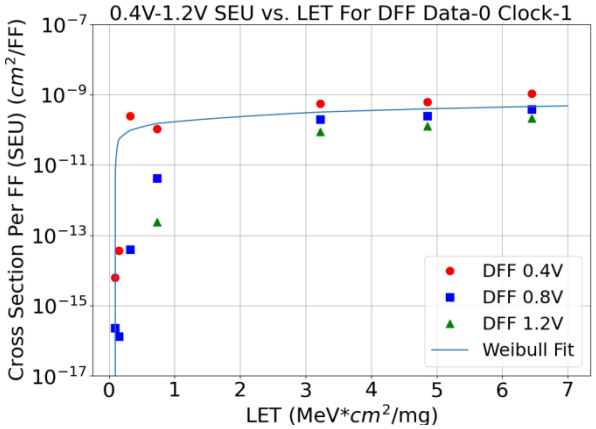


Fig. 5. SEU cross-section/FF vs. LET (data 0s, clk_test hi).

Fig. 6 plots the SEU cross-section per FF vs. LET response obtained when the data was all ones and the clock was fixed as low when under test. Fig. 7 plots the SEU cross-section per FF vs. LET response obtained when the data was all ones and the clock was fixed as high when under test.

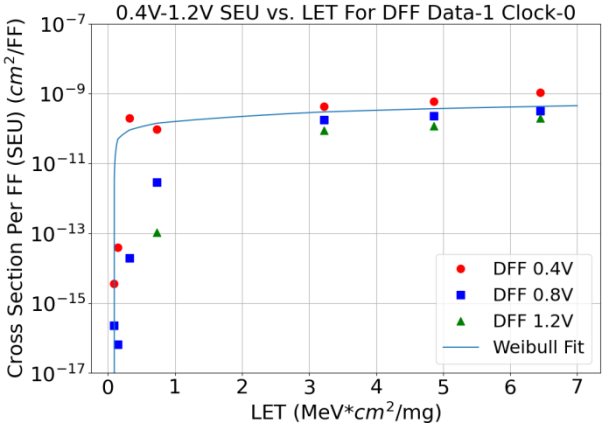


Fig. 6. SEU cross-section/FF vs. LET (data 1s, clk_test lo).

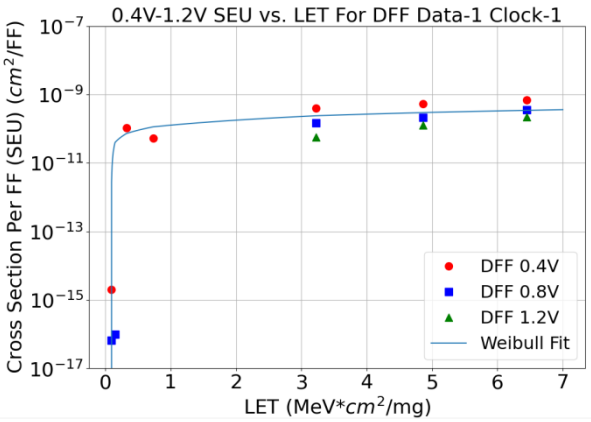


Fig. 7. SEU cross-section/FF vs. LET (data 1s, clk_test hi).

B. TID Experimental Data

The TID data on TC1 transistor structures are summarized on Figs. 8-37. The data collected present similar trends. NMOS devices exhibit increased I_d when V_g = 0V, that is off-state current leakage increased with radiation dose. PMOS devices exhibited no significant changes to I_d with dose. Between the ARACOR and gamma-ray sources, data was collected from 9 TC1 chips biased in the ON state; 6 chips were irradiated, and 3 chips served as control data. For NMOS devices, the ON state bias indicates V_d, V_s, and V_b were set to 0V, and V_g was set to 0.8V. For PMOS devices, the ON state bias indicates V_d, V_s, and V_b were set to 1.6V and V_g = 0.8V making V_{gs} = -0.8V. After exposure to NMOS devices, V_g was swept from -0.3V – 0.8V and V_d was set to 0.8V, for PMOS devices V_g was swept from --0.8V – 0.3V and V_d was set to -0.8V. The symbols in Figs. 10-11, 16-17, 22-23, 28-29, and 34-35 represent the average and error bars the standard deviations of the yielding data. Plots in the before mentioned figures were generated using over 300 data points taken from 7 TC1 chips. In total, 28 of each NINV, PINV, NNAND2, PNAND2, NNAND3, PNAND3, NNOR2, PNOR2, NNOR3, and PNOR3 transistor logic gates were tested for a total of 280 cell configurations tested between the 60KeV x-ray source and control data. The I_d vs V_{gs} curves presented from the ARACOR data are representative of all the TC1 devices that were exposed to that source. The TC1 chips for x-ray tests were irradiated in doses up to 2 Mrad(Si). The data shown in Figs. 12-13, 18-19, 24-25, 30-31, and 36-37 were collected from the 63.6 rad(SiO_2)/s gamma ray source, one chip was exposed while the other chip served as a control. For that test one of each NINV, NNAND2, NNAND3, NNOR2, and NNOR3 transistor structure was tested. The before mentioned figures were generated from over 100 data points for each test. The TCI chips used in the ^{60}Co gamma-ray tests were irradiated up to a dose of 2 Mrad(SiO_2).

1) INV (inverter) Devices

The test yield for irradiated NMOS inverter devices was 87.81% and the control yield was 100%. For the irradiated PMOS inverters, the yield was 87.5% and the control was 84.95%.

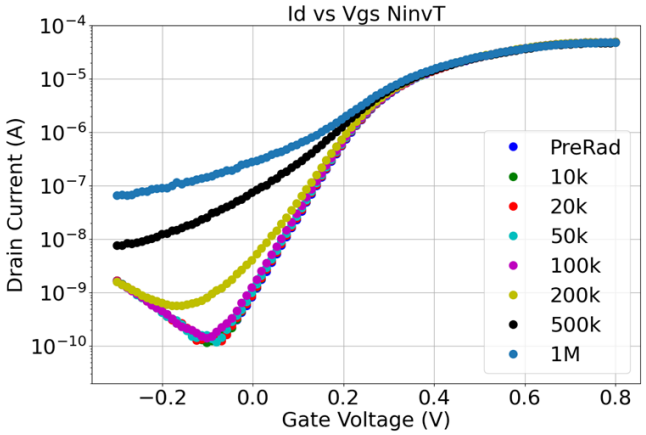


Fig. 8. Representative I_d vs V_{gs} curve NMOS network of INV on after exposure to the ARACOR x-ray. V_d = 0.8V during measurement.

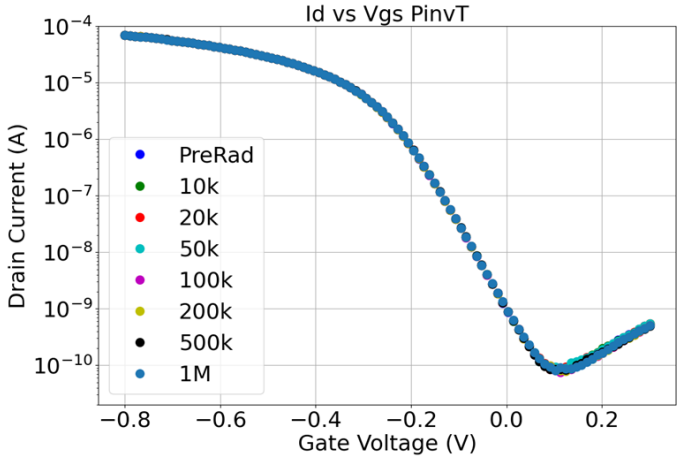


Fig. 9. Representative I_d vs V_{gs} curve PMOS network of INV on after exposure to the ARACOR x-ray. V_d = -0.8V

Fig. 10. Plot showing the off-state leakage vs. dose for NMOS network of INV gates exposed to the ARACOR x-ray in the ON state. V_d = 0.8V during measurement.

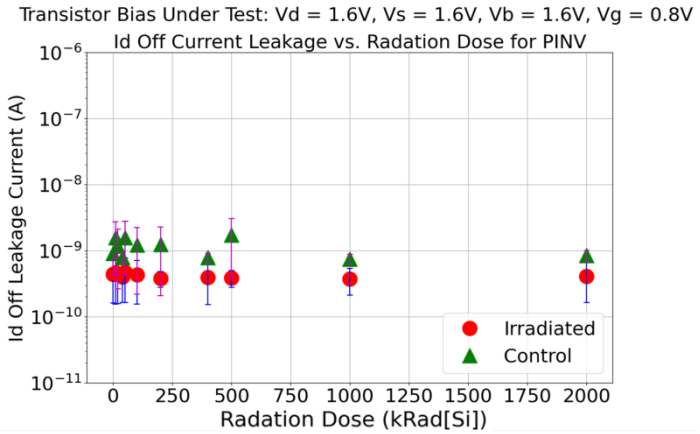


Fig. 11. Plot showing the off-state leakage current vs. dose for PMOS network of INV gates exposed to the ARACOR x-ray in the ON state. V_d = -0.8V during measurement.

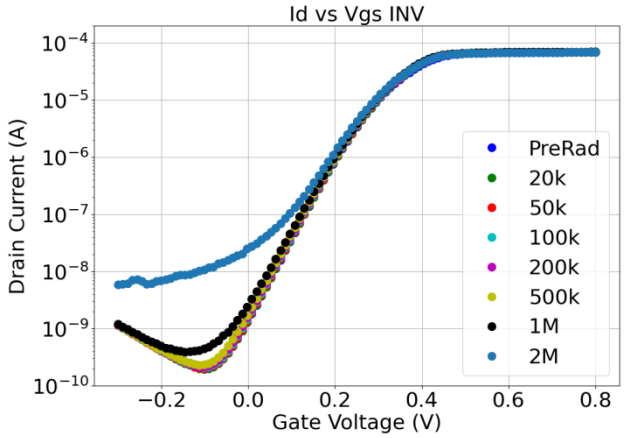


Fig. 12. I_d vs V_{gs} curve NMOS network of INV on TC1 after exposure to the ^{60}Co gamma ray source. V_d = 0.8V during measurement.

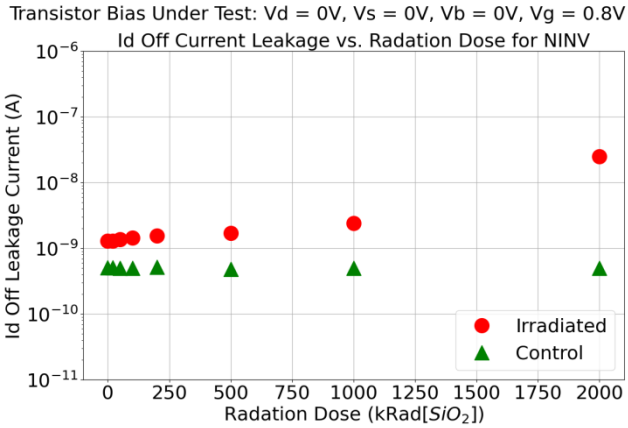


Fig. 13. Plot showing the off-state leakage current vs. dose for NMOS network of INV gates exposed to the ^{60}Co gamma-ray in the ON state. V_d = 0.8V during measurement.

2) NAND2 Devices

The test yield for irradiated NMOS NAND2 devices was 85.94% and the control yield was 88.17%. For the irradiated PMOS NAND2 devices, the yield was 96.67% and the control was 86.84%.

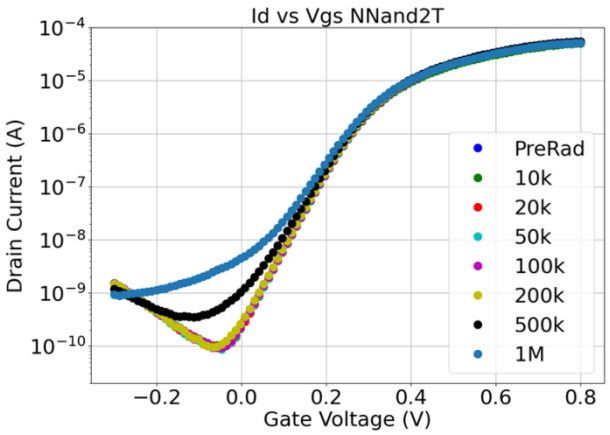


Fig. 14. Representative I_d vs V_{gs} curve NMOS network of NAND2 on after exposure to the ARACOR x-ray. V_d = 0.8V during measurement.

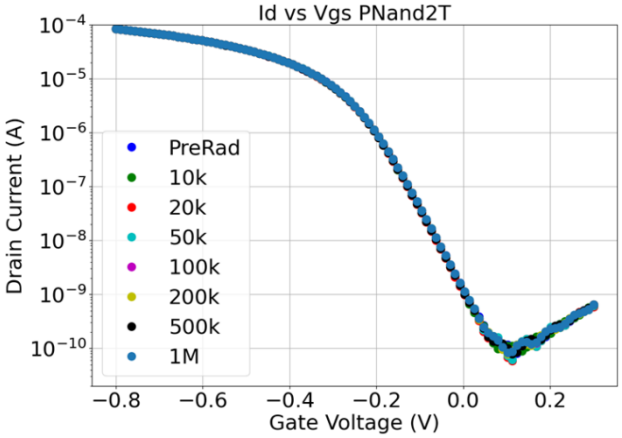


Fig. 15. Representative I_d vs V_{gs} curve PMOS network of NAND2 on after exposure to the ARACOR x-ray. V_d = -0.8V during measurement.

Fig. 16. Plot showing the off-state leakage vs. dose for NMOS network of NAND2 gates exposed to the ARACOR x-ray in the ON state. V_d = 0.8V during measurement.

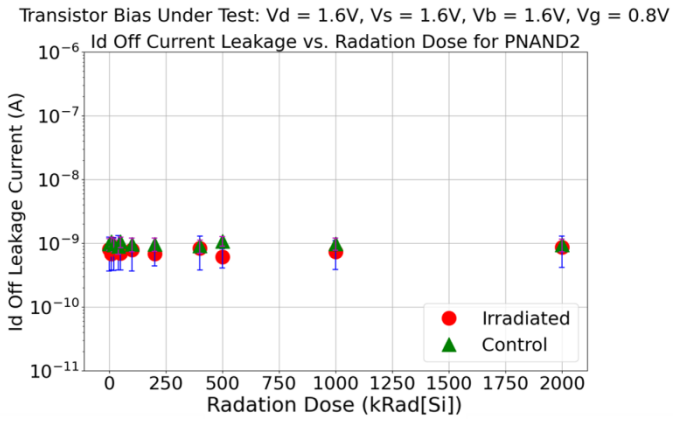


Fig. 17. Plot showing the off-state leakage vs. dose for PMOS network of NAND2 gates exposed to the ARACOR x-ray in the ON state. V_d = -0.8V during measurement.

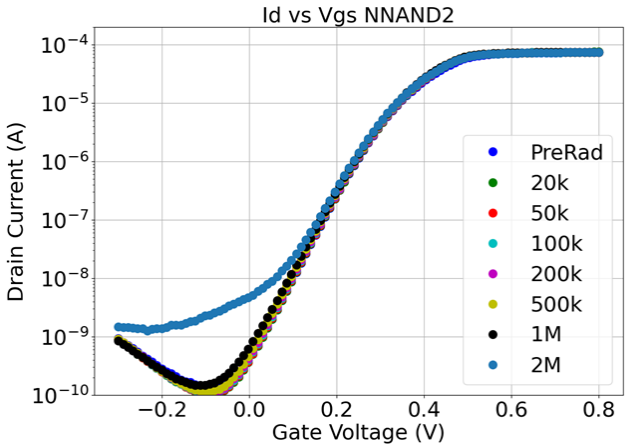


Fig. 18. I_d vs V_{gs} curve NMOS network of the NAND2 gates on TC1 after exposure to the gamma ray source. V_d = 0.8V during measurement.

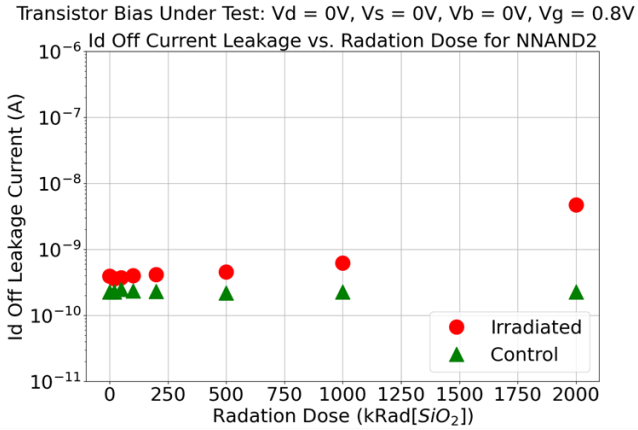


Fig. 19. Plot showing the off-state leakage current vs. dose for NMOS network of NAND2 gates exposed to the gamma-ray in the ON state. V_d = 0.8V during measurement.

3) NAND3 Devices

The test yield for irradiated NMOS NAND3 devices was 91.25% and the control yield was 89.25%. For the irradiated PMOS NAND3 devices, the yield was 95.63% and the control was 89.25%.

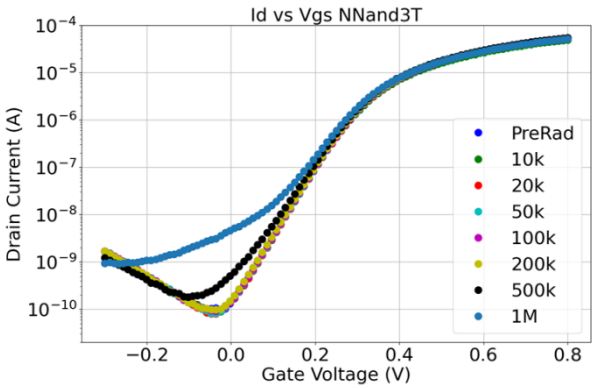


Fig. 20. Representative I_d vs V_{gs} curve NMOS network of NAND3 on after exposure to the ARACOR x-ray. V_d = 0.8V during measurement.

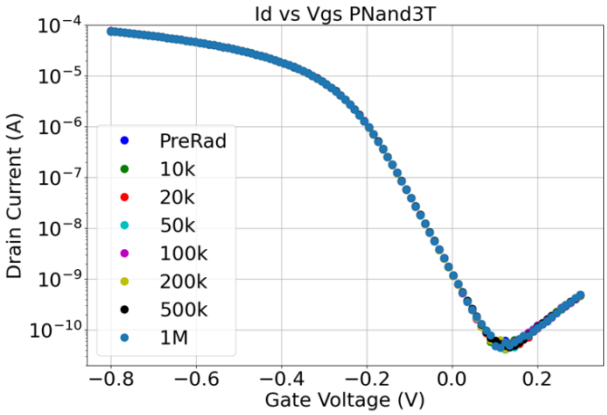


Fig. 21. Representative I_d vs V_{gs} curve PMOS network of NAND3 on after exposure to the ARACOR x-ray. V_d = -0.8V during measurement.

Fig. 22. Plot showing the off-state leakage vs. dose for NMOS network of NAND3 gates exposed to the ARACOR x-ray in the ON state. V_d = 0.8V during measurement.

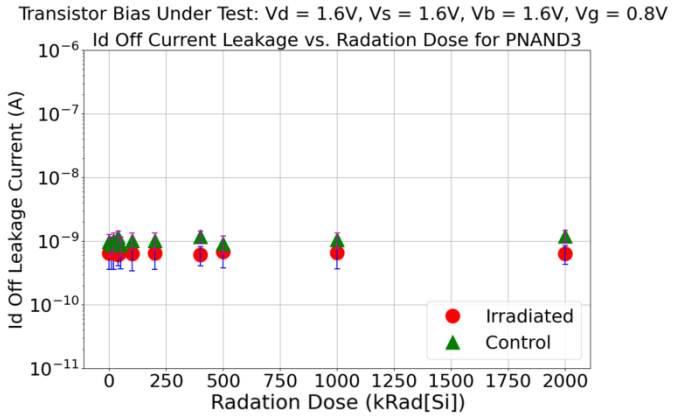


Fig. 23. Plot showing the off-state leakage vs. dose for PMOS network of NAND3 gates exposed to the ARACOR x-ray in the ON state. V_d = -0.8V during measurement.

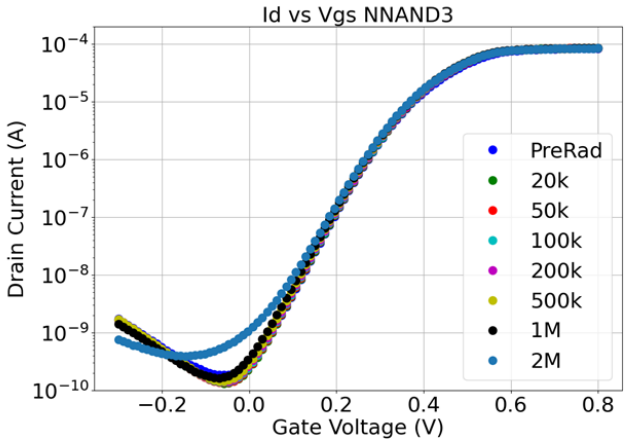


Fig. 24. I_d vs V_{gs} curve NMOS network of the NAND3 gates on TC1 after exposure to the gamma ray source. V_d = 0.8V during measurement.

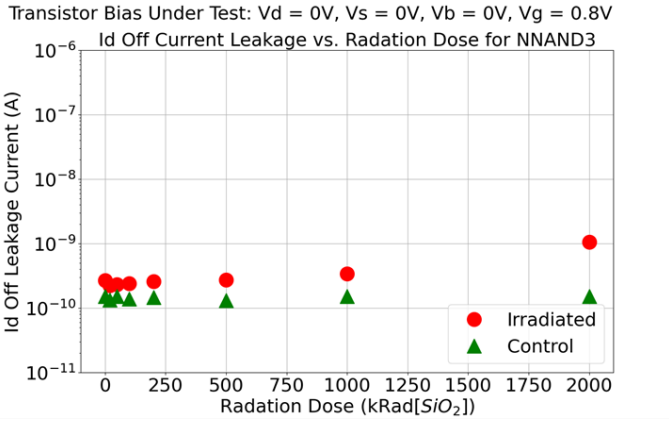


Fig. 25. Plot showing the off-state leakage current vs. dose for NMOS network of NAND3 gates exposed to the gamma-ray in the ON state. V_d = 0.8V during measurement.

4) NOR2 Devices

The test yield for irradiated NMOS NOR2 devices was 88.44% and the control yield was 89.25%. For the irradiated PMOS NOR2 devices, the yield was 95.83% and the control was 85.51%.

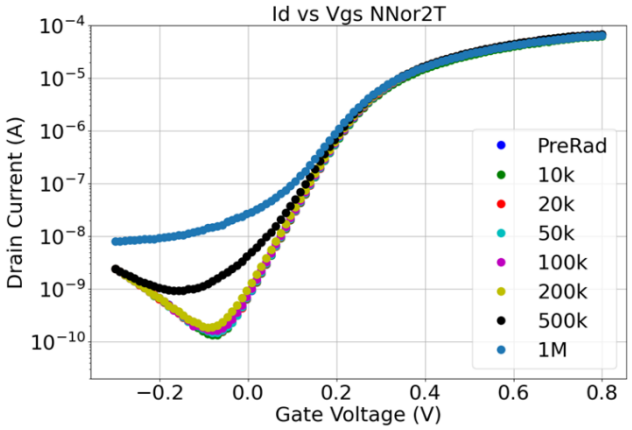


Fig. 26. Representative I_d vs V_{gs} curve NMOS network of NOR2 on after exposure to the ARACOR x-ray. V_d = 0.8V during measurement.

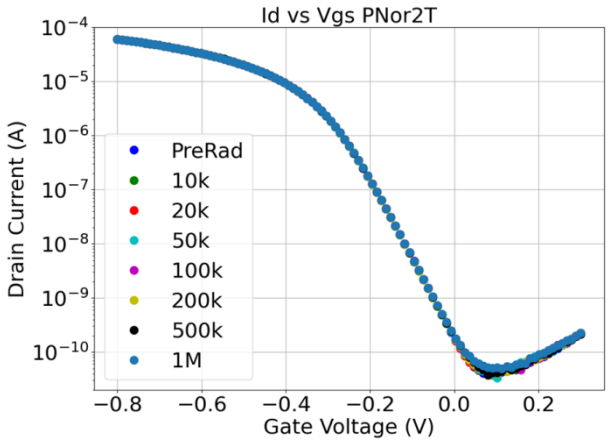


Fig. 27. Representative I_d vs V_{gs} curve PMOS network of NOR2 on after exposure to the ARACOR x-ray. V_d = -0.8V during measurement.

Fig. 28. Plot showing the off-state leakage vs. dose for NMOS network of NOR2 gates exposed to the ARACOR x-ray in the ON state. V_d = 0.8V during measurement.

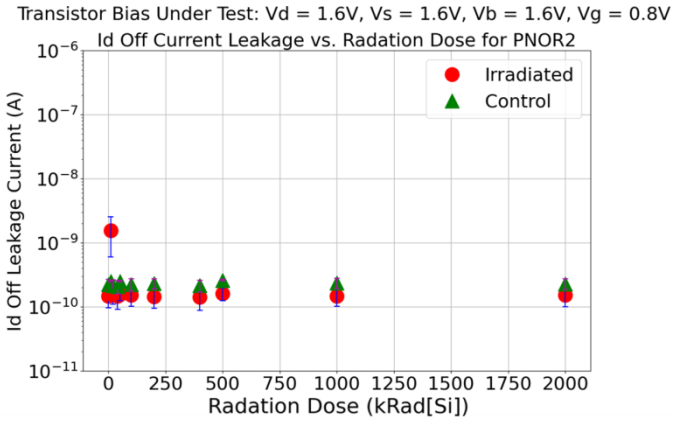


Fig. 29. Plot showing the off-state leakage vs. dose for PMOS network of NOR2 gates exposed to the ARACOR x-ray in the ON state. V_d = -0.8V during measurement.

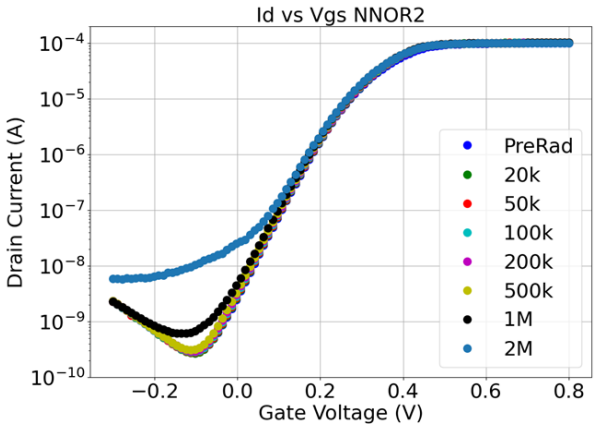


Fig. 30. I_d vs V_{gs} curve NMOS network of the NOR2 gates on TC1 after exposure to the gamma ray source. V_d = 0.8V during measurement.

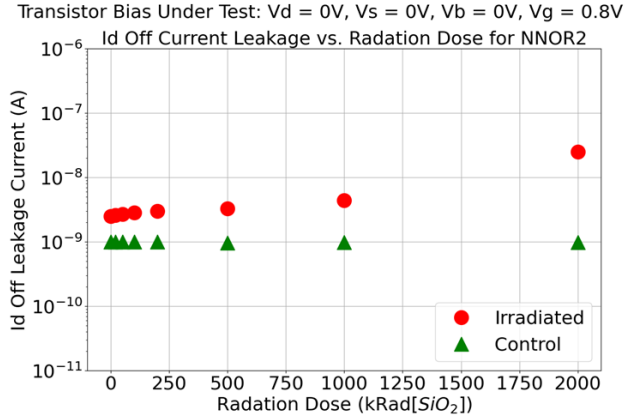


Fig. 31. Plot showing the off-state leakage current vs. dose for NMOS network of NOR2 gates exposed to the gamma-ray in the ON state. V_d = 0.8V during measurement.

5) NOR3 Devices

The test yield for irradiated NMOS NOR3 devices was 82.50% and the control yield was 87.01%. For the irradiated PMOS NOR3 devices, the yield was 99.38% and the control was 89.25%.

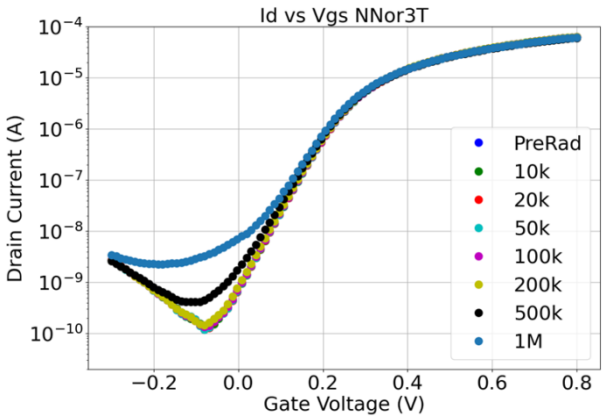


Fig. 32. Representative I_d vs V_{gs} curve NMOS network of NOR3 on after exposure to the ARACOR x-ray. V_d = 0.8V during measurement.

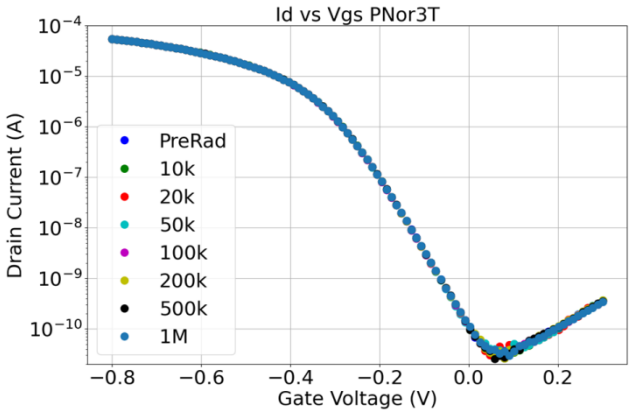


Fig. 33. Representative I_d vs V_{gs} curve PMOS network of NOR3 on after exposure to the ARACOR x-ray. V_d = -0.8V during measurement.

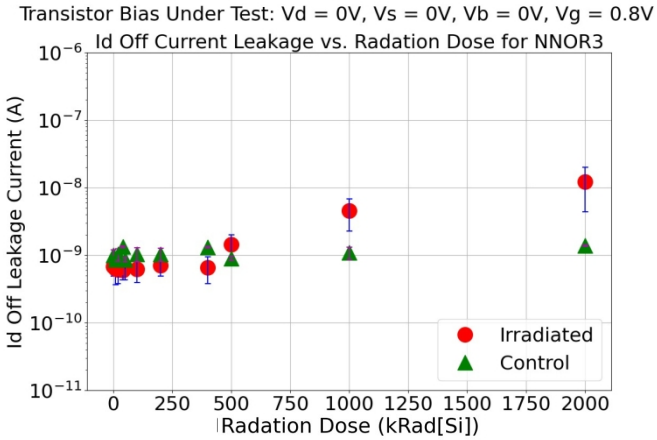


Fig. 34. Plot showing the off-state leakage vs. dose for NMOS network of NOR3 gates exposed to the ARACOR x-ray in the ON state. V_d = 0.8V during measurement.

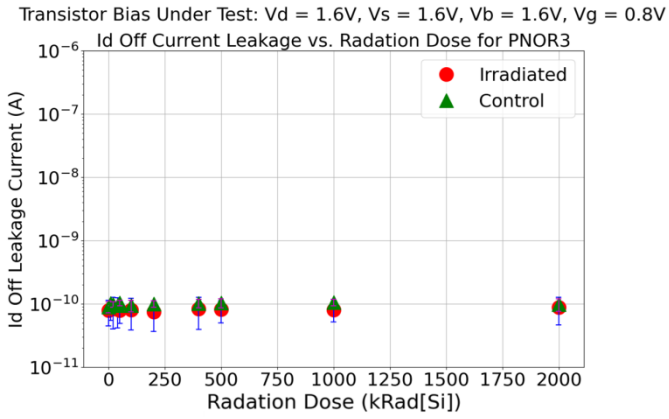


Fig. 35. Plot showing the off-state leakage vs. dose for PMOS network of NOR3 gates exposed to the ARACOR x-ray in the ON state. V_d = -0.8V during measurement.

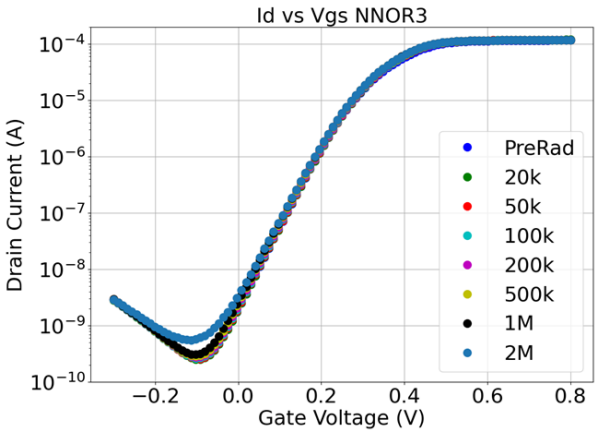


Fig. 36. I_d vs V_{gs} curve NMOS network of the NOR3 gates on TC1 after exposure to the gamma ray source. V_d = 0.8V during measurement.

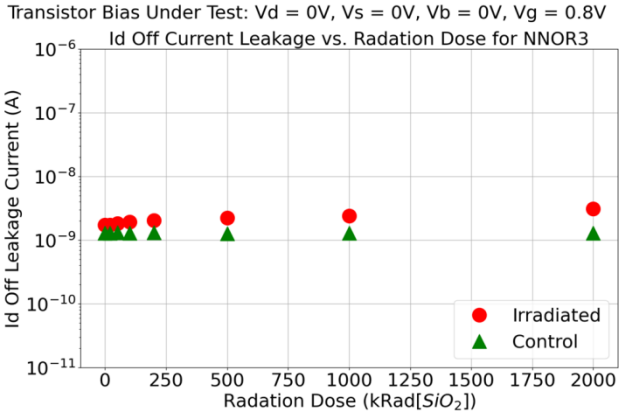


Fig. 37. Plot showing the off-state leakage current vs. dose for NMOS network of NOR3 gates exposed to the gamma-ray in the ON state. V_d = 0.8V during measurement.

6) TC3 Digital Circuits

Fig. 38 plots the TID response of the DFF digital circuits that were on TC3. The DDFs were tested on the Pelletron Beam exposed to radiation up to 10 Mrad(SiO_2) and the DFFs exposed to the ARACOR were exposed to radiation up to 1 Mrad(S_i). The data from the Pelletron and ARACOR are consistent with each other.

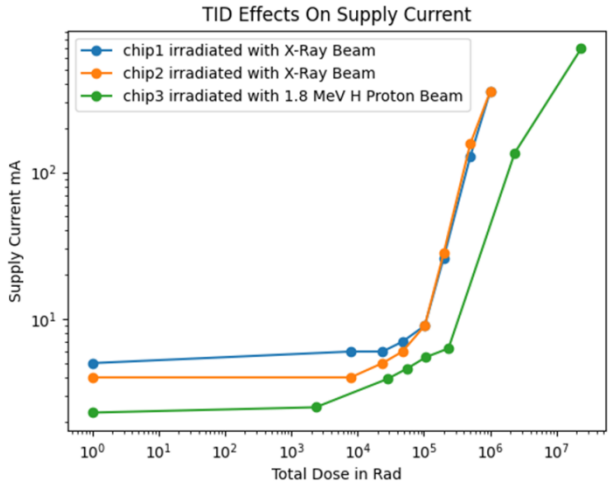


Fig. 38. Graph showing the current increase on the DFF devices after they were exposed to TID radiation from two different sources.

IV. Conclusion

These new data sets on 12LP FinFETs show that this technology is suspectable to both SEU and TID effects. The NMOS devices appear to have measurable increases in off-state current as irradiation dose increases. The PMOS devices appear to not exhibit any TID effects. The 12nm LP digital structures tested (DFF) were suspectable to SEU effects with a threshold LET of less than 1 MeVcm^2/mg and a saturated cross section of less than 10^{-9} cm^2/FF. The DFF devices were also susceptible to TID effects at doses around 10^5 -10^6 rad (Si).

References

[1] M. P. King *et al.*, "TID-Induced Leakage and Drive Characteristics of Planar 22-nm Partially-Depleted Silicon-on-Insulator and 14-nm Bulk and Quasi-Silicon-on-Insulator FinFET Devices," presented at the IEEE Nuclear and Space Radiation Effecxt Conference, Kona, HI, 2018.

[2] M. P. King *et al.*, "Analysis of TID Process, Geometry, and Bias Condition Dependence in 14-nm FinFETs and Implications for RF and SRAM Performance," IEEE Transactions on Nuclear Science, vol. 64, no. 1, pp. 285-292, 2017.

[3] D. R. Ball et al., "The Impact of Charge Collection Volume and Parasitic Capacitance on SEUs in SOI- and Bulk-FinFET D Flip-Flops," IEEE Transactions on Nuclear Science, vol. 65, no. 1, pp. 326-330, 2018.