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Study of Avalanche Behavior in 3 kV GaN Vertical P-N Diode Under UIS Stress for Edge-termination Optimization

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***Abstract*— This work investigates both avalanche behavior and failure mechanism of 3 kV GaN-on-GaN vertical P-N diodes, that were fabricated and later tested under unclamped inductive switching (UIS) stress. The goal of this study is to use the particular avalanche characteristics and the failure mechanism to identify issues with the field termination and then provide feedback to improve the device design. DC breakdown is measured at the different temperatures to confirm the avalanche breakdown. Diode's avalanche robustness is measured on-wafer using a UIS test set-up which was integrated with a wafer chuck and CCD camera. Post failure analysis of the diode is done using SEM and optical microscopy to gain insight into the device failure physics.**

Index Terms-- ***Gallium Nitride, GaN, Reliability, Vertical PN Diode, Avalanche, Robustness, Unclamped Inductive Switching.***

I. INTRODUCTION

GaN-based power semiconductor devices promise superior switching performance and higher power efficiency than the Si, and possibly SiC-based power devices [1], [2]. Particularly, GaN-based vertical semiconductor devices are an attractive choice for the power electronic applications, as they can handle higher current density and offer better thermal management, and area efficiency [3], [4]. Hence, there is a growing interest in GaN-based vertical power devices and their robustness under circuit-level stress conditions. Semiconductor devices in the power electronic converters, usually experience a voltage overshoot in the off state due to a series line or load inductor and they may fail if not robust [5]-[7]. Hence, ruggedness in the device's breakdown is very critical for the power switching applications [6], [7]. Fortunately, the intrinsic P-N junction in GaN-based vertical devices possesses an avalanche capability and offers robustness against breakdown [4], [8]-[10]. GaN-based vertical P-N diodes with avalanche breakdown voltage up to ~5 kV under DC condition, are already reported in the literature [9]. However, most of these works are limited to studying positive temperature coefficient of device's breakdown voltage to confirm presence of avalanche. Very few studies discuss device's avalanche robustness under circuit conditions [10], [11]. Non-uniform or unstable avalanche severely hampers the device's reliability and can limit its safe operation [12]. Therefore, it is crucial to achieve a robust avalanche. Robustness in avalanche is determined by how uniformly the device avalanches during breakdown. A uniform field distribution is indispensable to achieve uniform avalanche. Therefore, an effective edge termination [13]-[15] and optimized doping [15] are very crucial to achieve uniform field distribution hence, avalanche uniformity in a device. Recently, we reported repeatable avalanche in a bevel terminated GaN-based vertical P-N diode, achieved by optimizing the p-type doing and bevel angle [15]. The 1.3 kV rated GaN diode demonstrated a uniform avalanche under the inductive switching stress [11]. The bevel terminated diode sustained more than 5000 UIS stress pulses before facing thermal failure. This study advances our previous work [15], where a field plate is also added to the GaN-based P-N diode besides the 5° bevel, to improve the avalanche breakdown voltage. In this report, we extended our evaluation to study the avalanche behavior and robustness of 3 kV GaN-on-GaN vertical P-N diode, fabricated in-house, under repetitive UIS stress and probe the diode's failure mechanism. This manuscript is structured as follows. Diode design, and its DC characteristics are presented in Section II. Experimental setup for the on-wafer avalanche characterization, is described in section III and the results from the diode's avalanche characterization are discussed. Physical insights into the diode's degradation during avalanche are derived and a failure mechanism is proposed in Section IV. Finally, conclusive remarks are drawn in Section V.

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II. Device Design and DC Characteristics

Circular P-N diodes of 300 µm anode diameter were fabricated on a GaN epi-stack, which was realized on a highly doped 2-inch n^+ GaN substrate, using MOCVD. Figure 1(a) shows the device schematic depicting different layers of the device stack. A 20 µm n-drift region is grown with Si-doping of 6-9E15 cm^{-3}, followed by a 500 nm thin p-GaN layer with 5E17 cm^{-3} Mg doping to form the P-N junction. Ni/Au/Ti/Au metal stack was used as anode on top while Ti/Au stack is used as cathode on backside. All devices possess field plate with 5° bevel at anode for edge termination. 300 nm thick spin-on-glass (SOG) was used as the field plate dielectric and for surface passivation. Figure 1(b) shows the top view SEM image of the fabricated diode with the bevel and field plate termination as shown in the figure inset. DC characterization of the diodes was done using Keysight's B1505A power device analyzer. Figure 2(a) shows the I-V characterisitics of the diode. Pulse I-V characterisition was done in the forward mode for the current above 100 mA. The particular diode studied offered a turn-on voltage of around 4 V as seen in Fig. 2(a). This is due to an extra voltage drop at the p-type contact. The diode showed an ON-current of up to 2.2 A at 13 V and a remarkably low reverse leakage of 10 pA. The reverse breakdown voltage of the diode was measured at different temperatures as shown

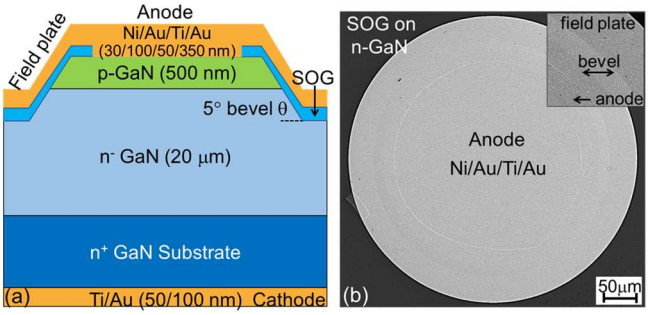

Figure 1. (a) Cross-sectional schematic of 3 kV GaN vertical P-N diode depicting different layers of the device stack. **(b)** Top view SEM image of diode, with magnified view of field plate and bevel shown in the inset.

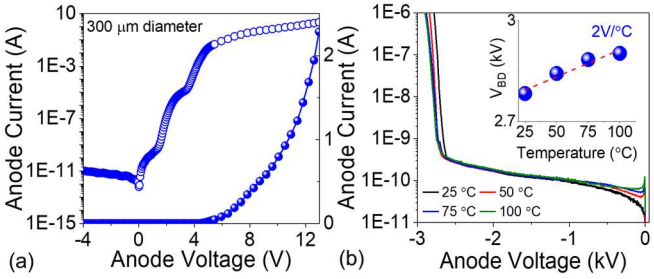

Figure 2. (a) I-V characteristics of 3 kV GaN-based vertical P-N diode. **(b)** Reverse breakdown voltage (V_{BD}) of diode measured at different temperatures. Inset shows V_{BD} increases with temperature exhibiting a positive temperature coefficient which confirms presence of avalanche breakdown.

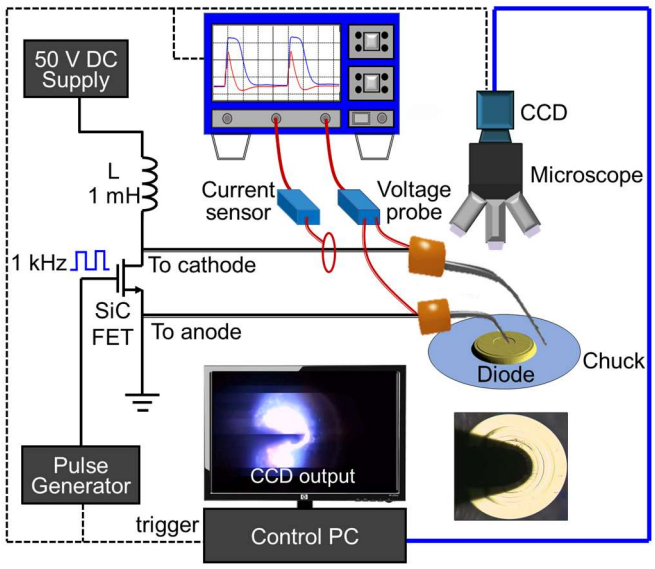

Figure 3. Experimental set-up with integrated CCD for on-wafer UIS testing and avalanche study in GaN-based vertical P-N diode. The diode is probed on chuck using thick needle probes and connected in antiparallel to the MOSFET.

in the Fig. 2(b). Fluorinert was used during the breakdown measurements and the current compliance was set to 1 µA. The diode showed a reverse breakdown voltage (V_{BD}) of ~2.8 kV@1 µA with a positive temperature coefficient of 2 V / °C, as depicted in inset of Fig. 2(b), confirming the presence of the avalanche breakdown.

III. Avalanche Characterization

As, discussed above, the diode shows the avalanche breakdown. Next, the uniformity and ruggedness of the avalanche is evaluated. The avalanche behavior of diode is investigated under an inductive switching stress. Here, the avalanche characterization is done at the wafer-level, on a prober, for a quick estimation of the avalanche robustness of the fabricated diodes to provide quick feedback to the design/ fabrication team. For this, an unclamped inductive switching (UIS) test circuit is integrated with wafer chuck under a high-speed CCD camera as shown in Fig. 3. The diode under test, is probed on the chuck using thick needle probes and connected in antiparallel to a SiC MOSFET, which has a higher breakdown voltage (3.3 kV) than the diode itself. The MOSFET

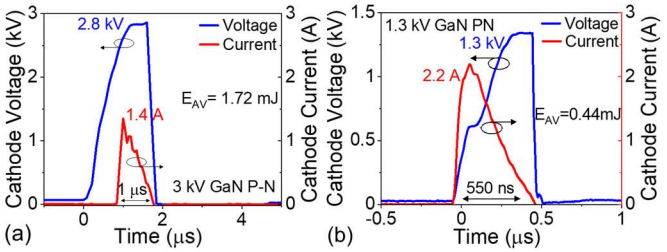

Figure 4. (a) Cathode voltage and current waveforms recorded in (a) 3 kV GaN vertical P-N diode and (b) 1.3 kV GaN vertical P-N diode, in a UIS cycle [11].

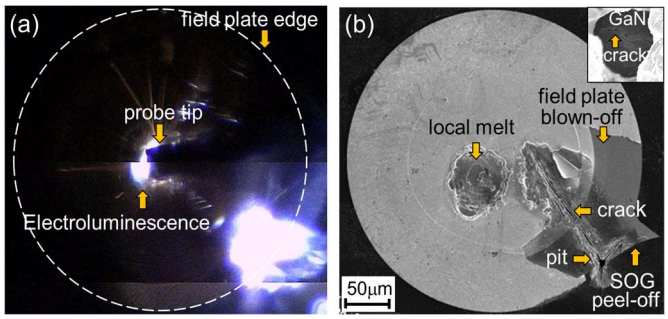

Figure 5. (a) Optical image of 3 kV GaN vertical P-N diode captured during the avalanche in the UIS test circuit. **(b)** Post failure SEM image of 3 kV GaN vertical P-N diode shows evidence of field dominated failure. A closer look at the pit reveals cracks in underlying GaN layer, as shown in the inset.

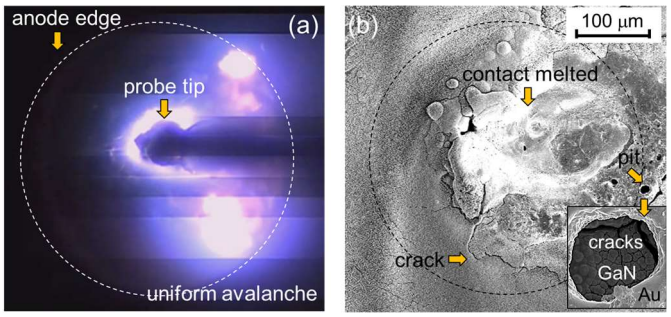

Figure 6. (a) Optical image of 1.3 kV GaN P-N diode exhibiting uniform avalanche operation under UIS stress [11]. **(b)** SEM image of 1.3 kV GaN vertical diode which failed after uniform avalanche [11]. Pit revealed cracks in underlying GaN as seen in the inset.

is turned on to energize the inductor and later it is turned off to interrupt the current flowing through it. Interruption to the inductor current generates a voltage overshoot at the diode's cathode terminal which pushes the diode into the avalanche. Cathode voltage and current waveforms are recorded using a high bandwidth voltage and current probes, respectively, on a Tektronix Mixed Signal Oscilloscope. During the avalanche breakdown, the cathode voltage clamps to 2.9 kV, and a peak current of 1.4 A flows through the GaN diode for a duration of t_{AV} = 1 μs as shown in the Fig. 4a. The avalanche robustness (E_{AV}) is determined using the following relation.

$$E_{AV} = \int_0^{t_{AV}} V \times I \, dt$$

The diode shows avalanche robustness of E_{AV} = 1.72 mJ/pulse. In contrast, a bevel terminated 1.3 kV GaN vertical P-N diode without field plate, avalanched at 1.3 kV with a higher current of 2.2 A flowing through the diode, for a duration, t_{AV} = 550 ns as seen in the Fig. 4(b) [11]. The higher current in the 1.3 kV diode resulted from diode's uniform avalanche behavior which possibly distributed the generated heat and associated thermal stress uniformly across the device. On the other hand, the 3 kV diode showed lower current (1.4 A) which can be attributed to non-uniform avalanche as discussed in next section. Uniform avalanche is a sign of superior edge termination which was achieved in the 1.3 kV diode. While the 3 kV diode although demonstrated avalanche, based on the positive temperature coefficient of breakdown, the UIS stress test indicates that the avalanche was not uniform.

IV. Degradation During Avalanche

To gain physical insight into the device breakdown, optical images of the GaN diode were captured using the high-speed CCD, during the UIS test. Figure 5(a) shows an optical image of the 3 kV GaN vertical P-N diode captured during the avalanche in the UIS test. The diode undergoes a non-uniform avalanche as evident from the localized electroluminescence (EL) seen in the anode center and at the anode edge. Post failure, a SEM image of the diode is taken as shown in Fig. 5(b). It shows that the contact metal melted, and got removed from the anode center, which earlier showed EL and a massive pit and crack developed at the anode edge. Localized metal melting indicates a localized heating [16]-[18]. A part of the field plate and SOG was also peeled off. Material layers (here metal and SOG) peel-off under mechanical stress [19]-[24]. A closer look inside the pit unveiled cracks in the underlying GaN layer as well, as shown in the inset of Fig. 5(b). Cracks and pits in GaN are strong signature of field driven failure mechanism i.e., inverse piezoelectric effect [25]-[29]. Whereas the 3 kV GaN P-N diode showed more localized EL and avalanche, the 1.3 kV diode showed a more uniform avalanche as shown in Fig. 6(a) [11]. As evident, most of the anode contact region including the edges, showed EL. The 1.3 kV diode failed after 5000 UIS pulses and Fig. 6(b) shows its post-failure SEM image. As seen, most of the anode contact melted uniformly due to the intense heat and developed multiple cracks and pits all over the contact region due to the associated thermal stress [11].

Based on the above observations, the following failure mechanism is proposed for 3 kV GaN P-N diode; thermal stress during avalanche expands SOG more due to its higher coefficient of thermal expansion (CTE) than the underlying GaN layer [30]. Consequently, this peels off the SOG and damages the field plate lying on top of it as seen in Fig. 5(b). Once a portion of the field plate is blown-off, the peak field returns from the bulk to the anode edge. The peak field at the anode edge enhances piezoelectric tensile strain in the underlying GaN layer which develops cracks/ pits, eventually causing failure in 3 kV GaN diode.

V. Conclusion

Avalanche behavior of our in-house fabricated 3 kV GaN-on-GaN vertical P-N diode was studied. Reverse breakdown voltage showed a positive temperature coefficient, confirming avalanche. Under UIS stress the diodes avalanched at 2.9 kV with 1.4 A of peak current, with an energy of 1.72 mJ/pulse. Localized EL was seen at the anode center and its edge. Thermal stress damaged the SOG & field plate followed by piezoelectric strain-induced cracking in GaN eventually failed the diode. This study shows how the UIS stress test and EL features can be used to determine the efficacy of edge termination.

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