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Interface Trap Density Characterization of ALD Gate Dielectrics for GaN Power MOSFETs

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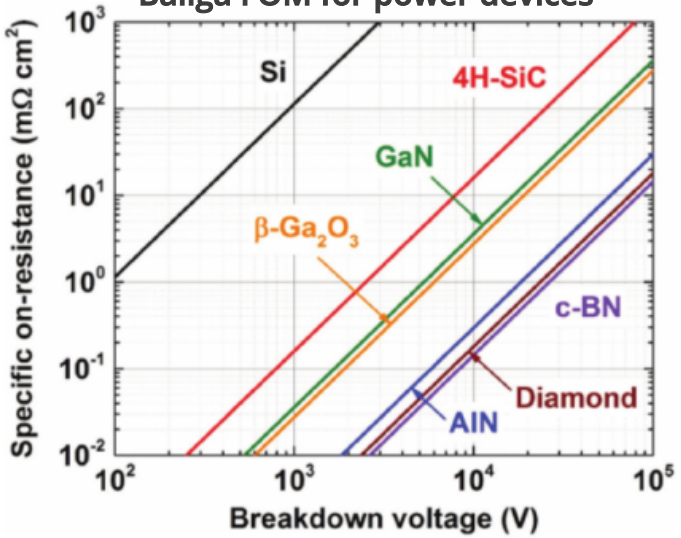
Challenges for wide bandgap power devices

- WBG materials such as GaN improve Si/SiC power devices from material properties
  - Utilize material properties to enhance performance

$$BFOM = \varepsilon m_n E_{crit}^3$$

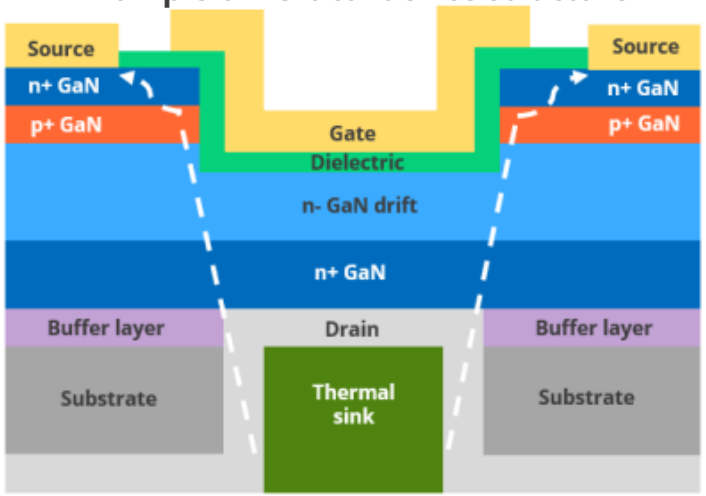
- Vertical architectures for high-power applications
- Challenges to design must be addressed before implementation
  - p-dopant activation
  - Mitigation of sidewall damage
  - Improved gate dielectric interface ←

Baliga FOM for power devices



[1] Tsao *et al.*, *"Ultrawide-bandgap semiconductors: research opportunities and challenges," Advanced Electronic Materials, 2018.*

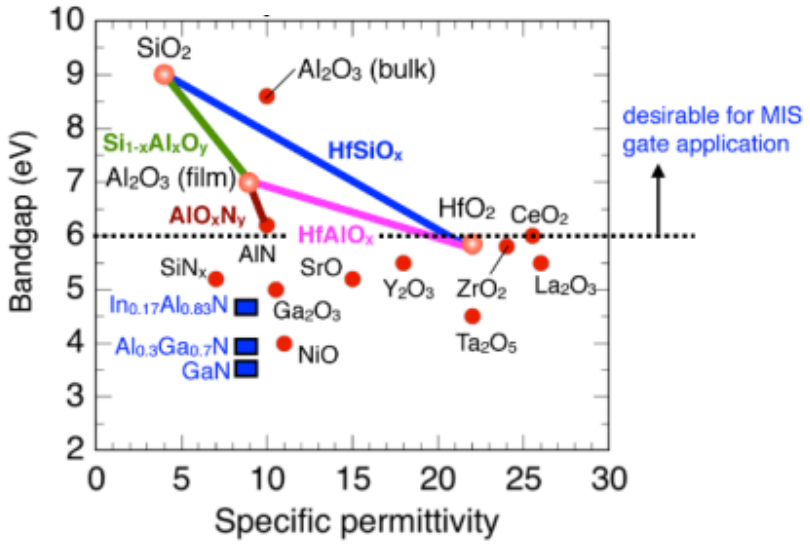
Example of vertical device structure



Dielectric material properties directly related to device performance

- Properties vary with thickness and deposition methods
- SiO_2 most commonly used for MOSFET gates
  - Other materials may be preferred with larger k and breakdown
- ALD preferred to other deposition techniques
  - Conformal coatings
  - High aspect ratio
  - Low temperature deposition

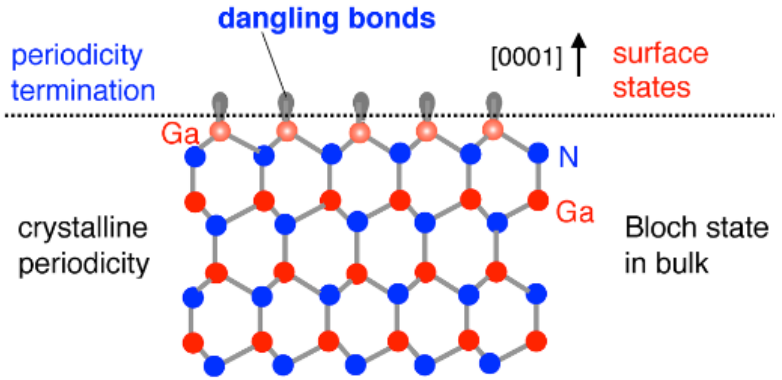
Material	Dielectric constant	Bandgap (eV)	Breakdown Strength (MV/cm)
SiO_2	3.9	8.8	7.5
Si_3N_4	7.5	5.3	11.9
Al_2O_3	9.8	9	8.2
ZrO_2	25	5.8	0.4
HfO_2	25	5.8	5.6
La_2O_3	30	5.8	13.5
Ta_2O_5	46	4.4	3.5
TiO_2	80	3.5	0.3



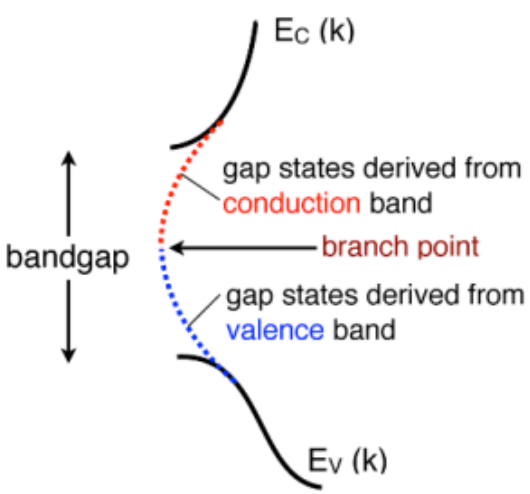
[2] Asubar, et al., "Controlling surface/interface states in GaN-based transistors: Surface model, insulated gate, and surface passivation," Journal of Applied Physics, 2021.

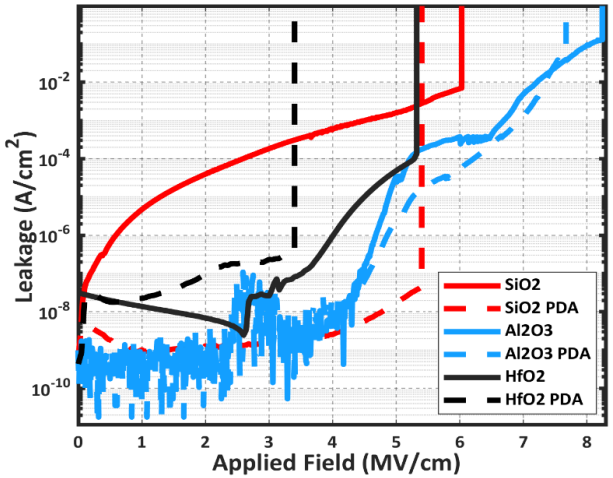
Defects at interface reduce device functionality

- Optimization of interface crucial to device performance
  - Reduce threshold voltage, leakage, and D_{IT}
- Surface/interface states add excess charges
  - Additional available states in energy bands
  - Reduced gate control, decreases carrier mobility, and increases R_{on}
  - Trapped charges cause large V_{th} fluctuation
- Previous work on D_{IT}/leakage reduction
  - Chemical surface treatments
  - Post deposition anneals (PDAs) to dielectric



[2] Asubar, et al., "Controlling surface/interface states in GaN-based transistors: Surface model, insulated gate, and surface passivation," Journal of Applied Physics, 2021.

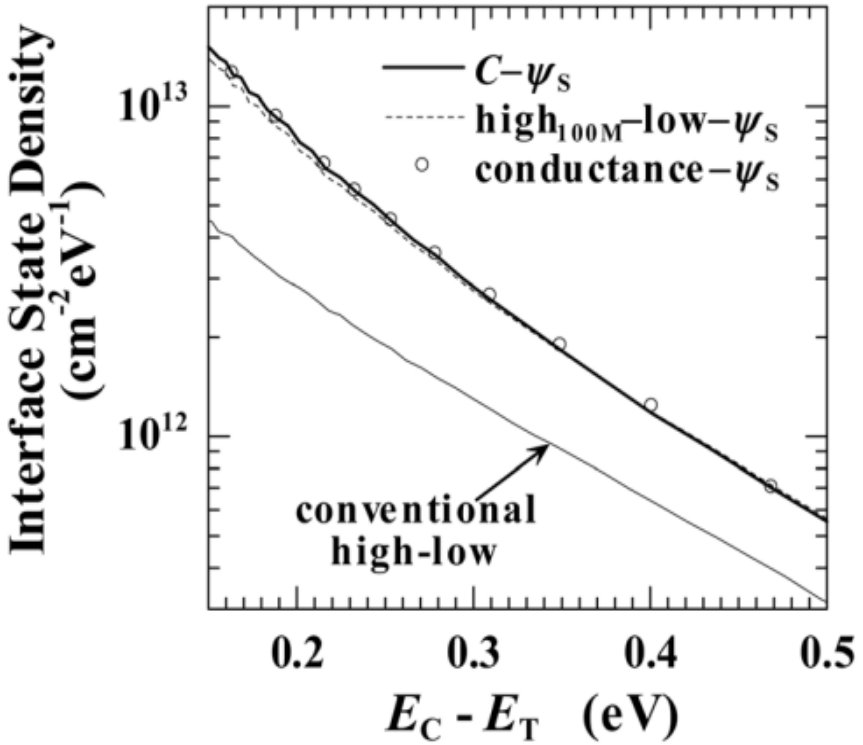




[3] Glaser et al., "Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices, WiPDA, 2021.

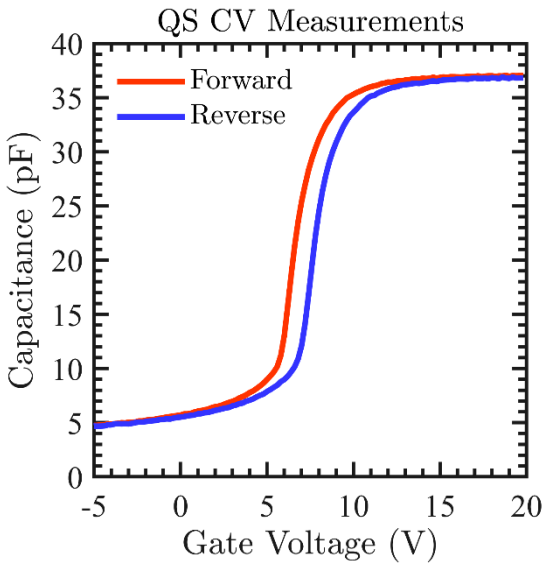
Routine D_{IT} analysis is difficult for wide-bandgap materials

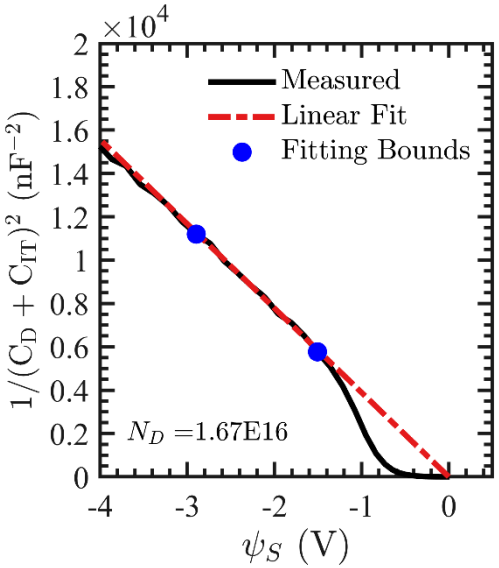
- High-Low
  - Conventional high-frequency CV measurements underestimates D_{IT} in wide bandgap semiconductor
- Conductance
  - Despite its accuracy, the conductance technique is often time consuming and impractical for routine device analysis
- C-Ψ_s
  - A relatively simple and fast technique
  - Shown to account for fast interface traps and reports accurate interface trap distributions

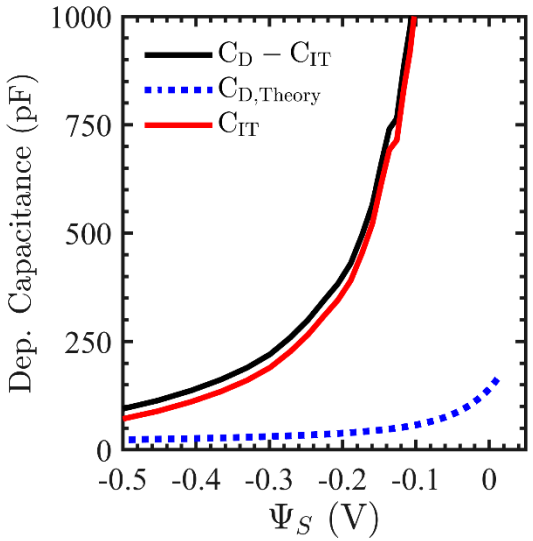


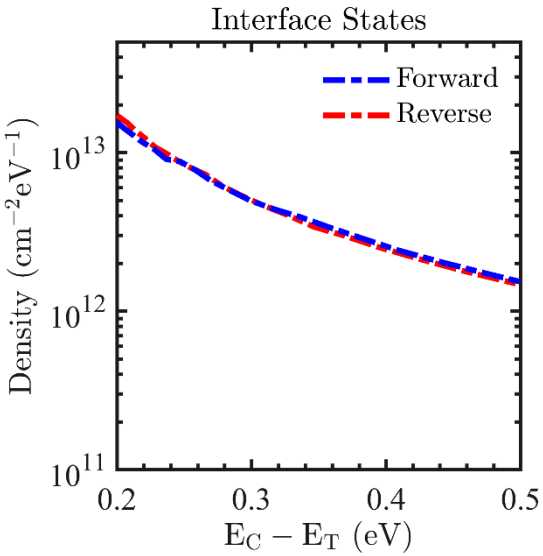
[4] Yoshioka et al.,"Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures using surface potential based on depletion capacitance," Journal of Applied Physics, 2012.

Steps in C-Ψ_s method analysis









Quasi-Static C-V Measurements → **Determine Surface Potential Constant** → **Comparing Theoretical & Experimental Depletion Capacitance** → **D_{IT} Extraction**

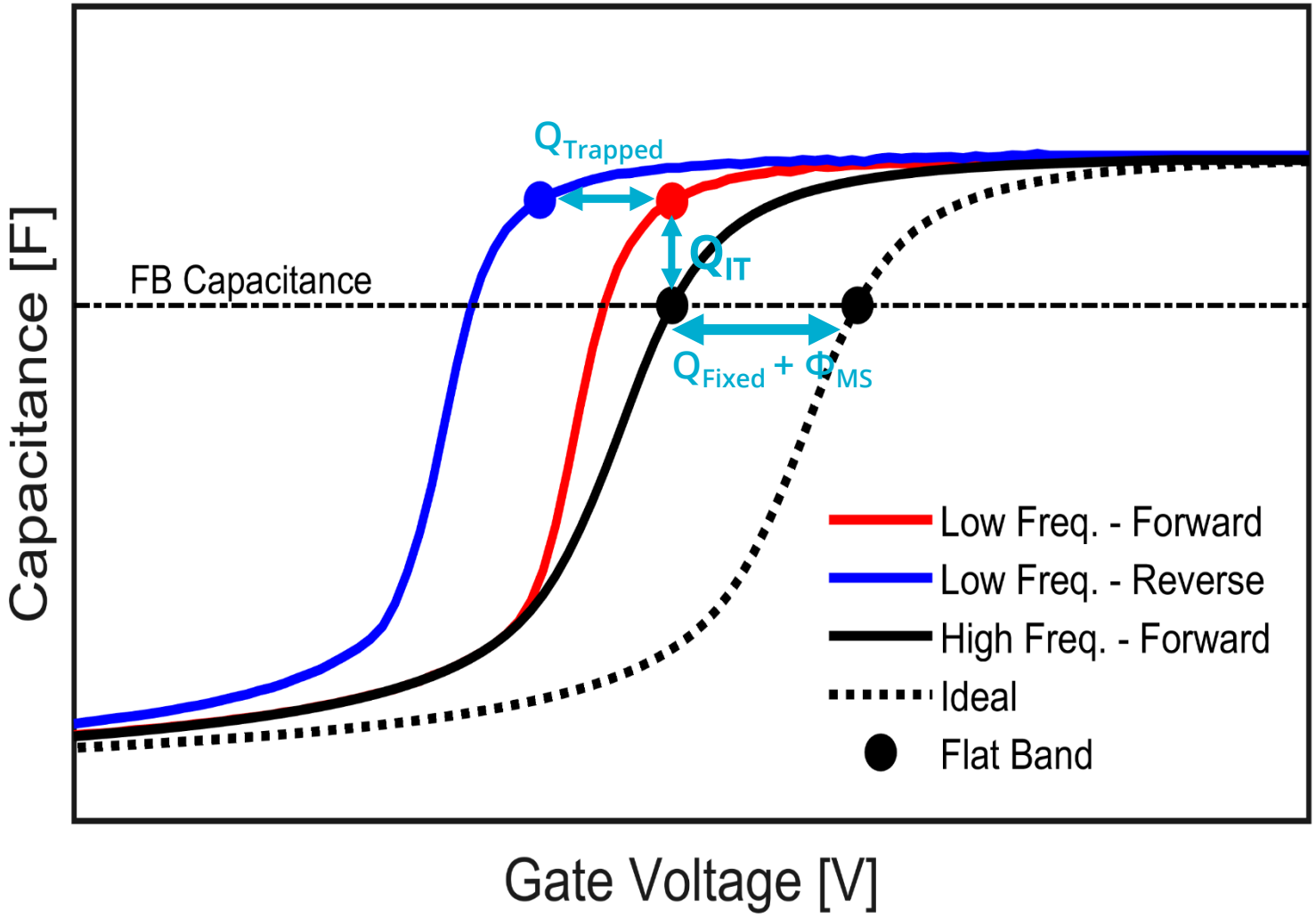
$$\psi_S(V_G) = \int (1 - C_{QS}/C_{OX}) dV_G + A$$

$$\frac{1}{(C_D + C_{IT})^2} \approx \frac{1}{C_{dep}^2} = -\frac{2\psi_S}{S^2 \varepsilon_{SiC} e N_D} \text{(depletion)}$$

$$D_{IT} = \frac{(C_D + C_{IT})_{QS} - C_{D,theory}}{Se^2}$$

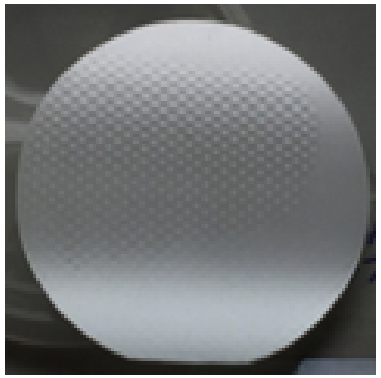
- Expected values for D_{IT}
  - Si – 1e^{10} cm^{-2}
  - SiC – 1e^{11}-1e^{12} cm^{-2}
  - GaN – 1e^{12}-1e^{13} cm^{-2} (not commonly reported)

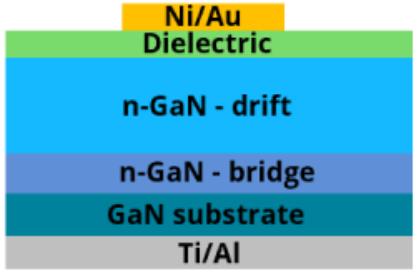
C-V Characteristics used in C-Ψ_s analysis

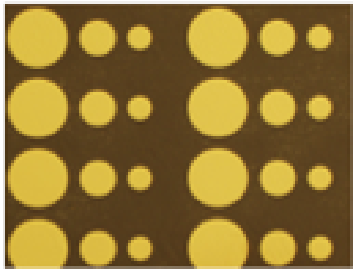


Methods for device fabrication

- Samples prepared on n-type GaN
  - N_d=1.6x10^{16} cm^{-3} drift
- Common surface cleans to substrate
  - 100:1 HF
  - 4:1 Piranha at 80 °C
- ALD deposition
  - 50-nm SiO_2 and Al_2O_3 at 200 °C
- Backside ICP etch using RF bias 125W/10W
  - Gas flow – BCl_3/Cl_2/Ar (15 min)
- Lithography pattern of 500 µm devices
  - Ni/Au top contacts
  - Ti/Al backside contact
- PDAs 700 °C – 850 °C to simulate ohmic contact anneals

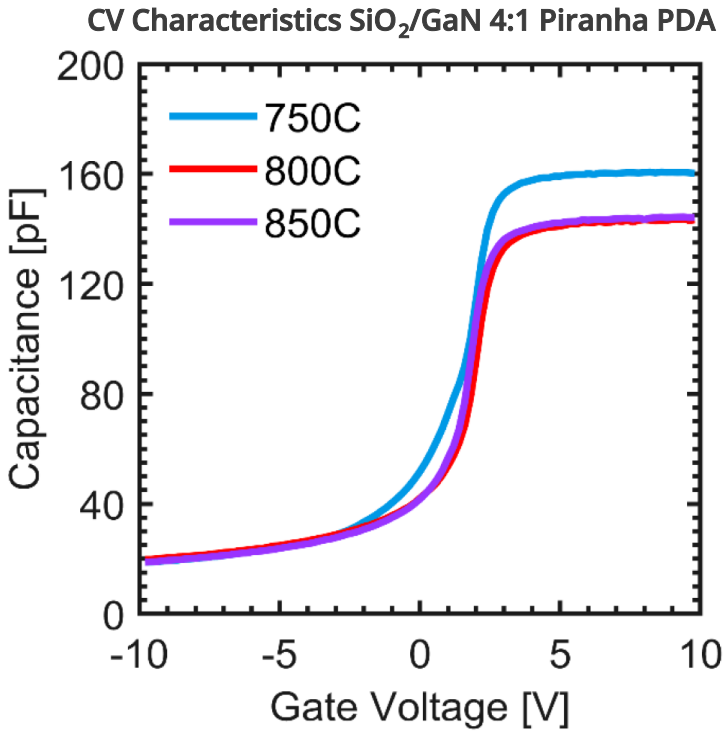


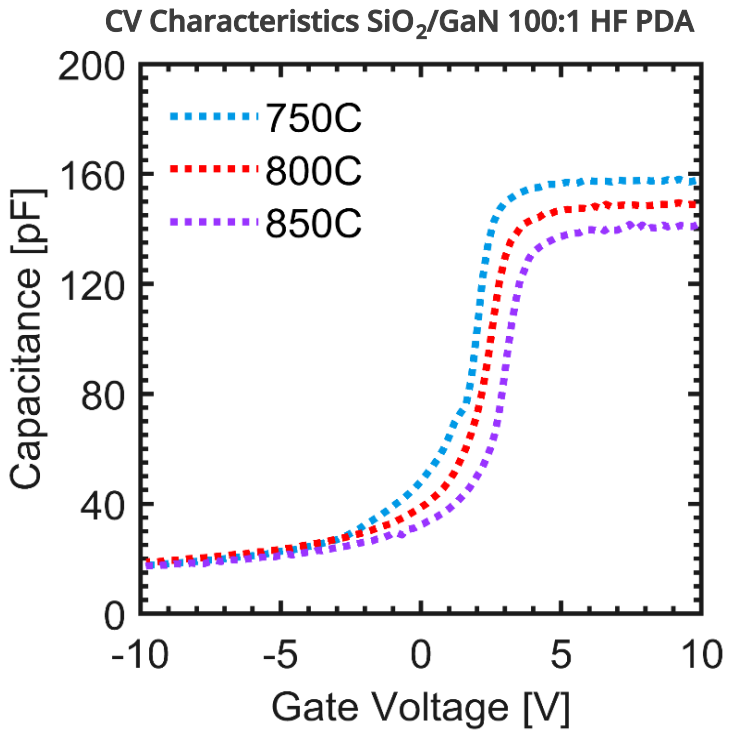




[5] Monsma et al.,"Savannah ALD Systems: Enabling Quick Results," ECS Transactions, 2007.

Reduction in SiO_2 Capacitance related to dielectric constant





- Varying capacitances attributed to dielectric constants changing with PDA temperatures
  - Thickness is not decreasing for SiO_2

$$ = _0 —$$

$$ = 1.96\text{x}10^5\ \text{nm}^2$$

$$ = 50\ \text{nm}$$

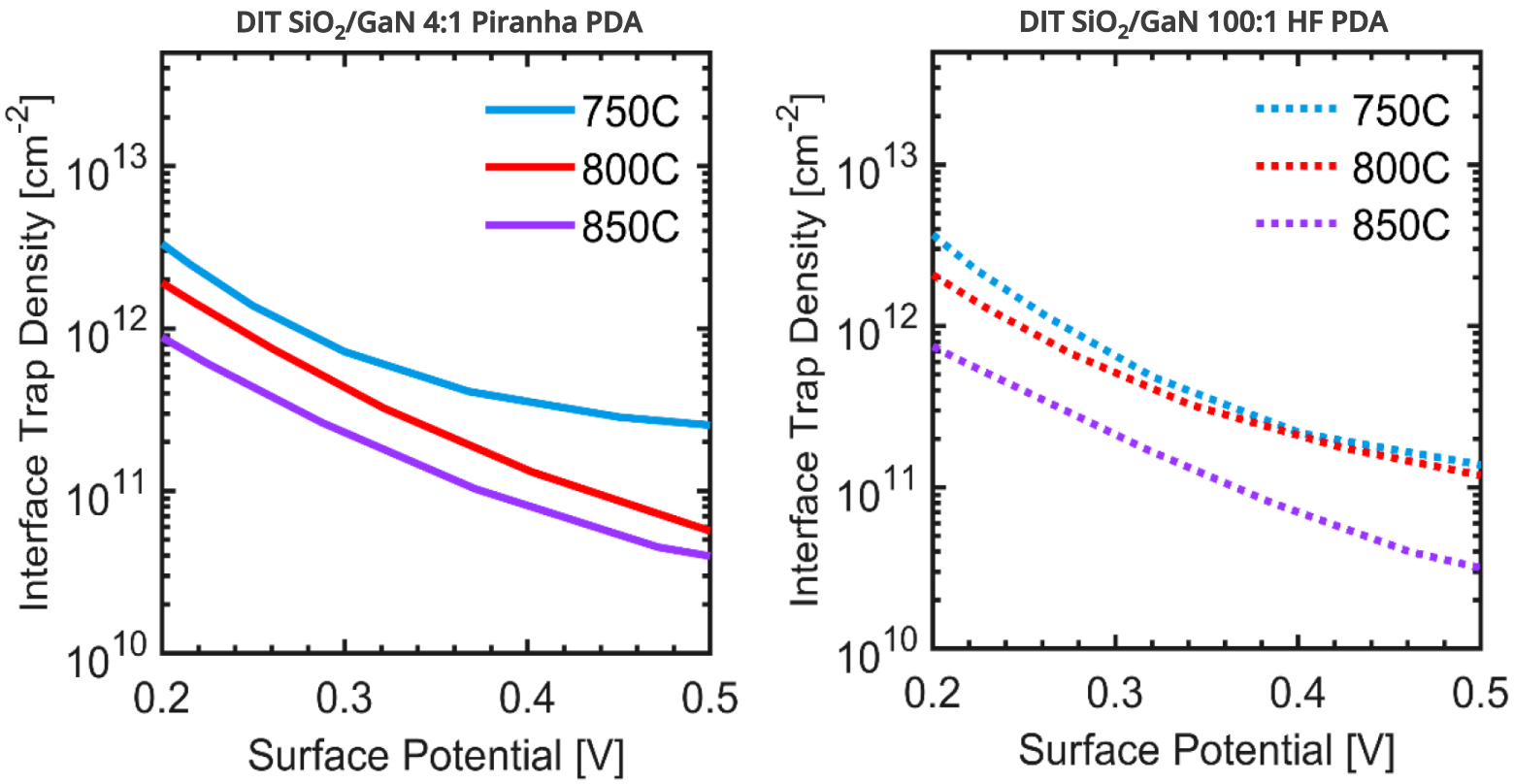
$$\varepsilon_{SiO_2} = 3.9$$

$$_0 = 8.85\text{x}10^{-12}\ \text{F/m}$$

$$C = \varepsilon_{SiO_2}\varepsilon_0\frac{A}{d} \qquad C_{SiO_2} = 136\ \text{pF}$$

Must be changing!

PDAs more significant than surface cleans for reducing D_{IT} for SiO_2

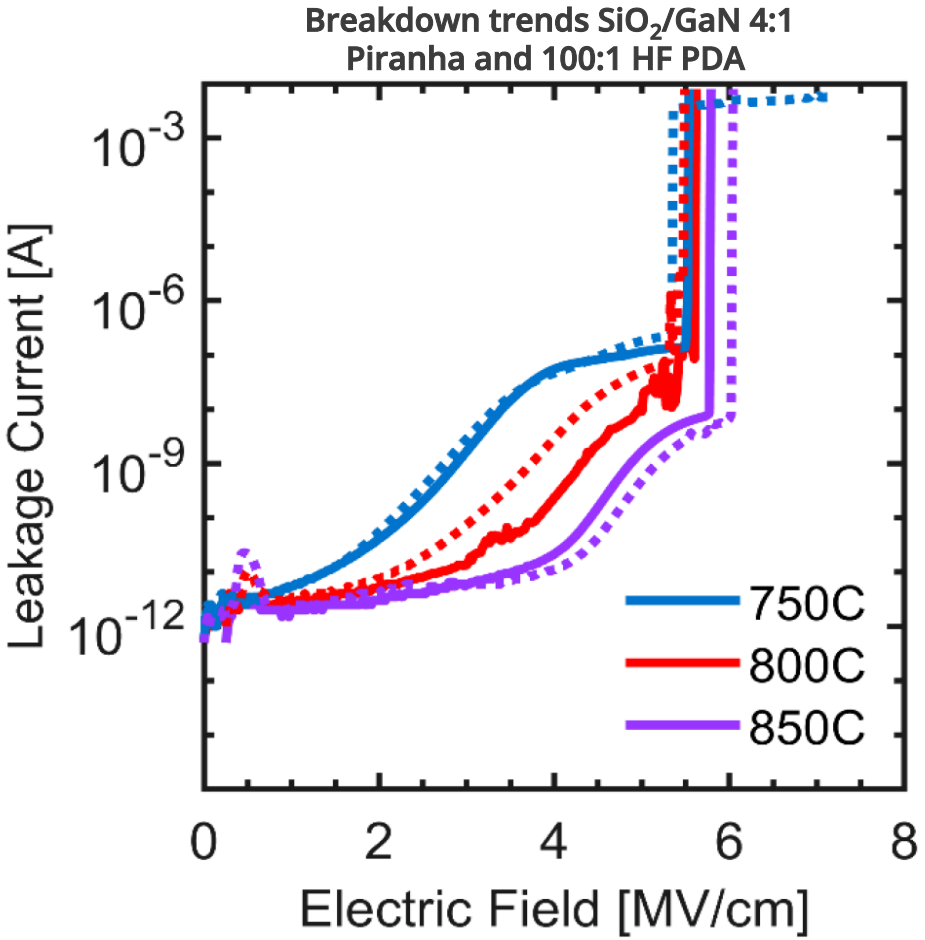


- Post deposition anneals at 850 °C show significant improvement to D_{IT}
- Similar trend shown regardless of surface treatment

High temperature PDA improve SiO_2 breakdown and leakage

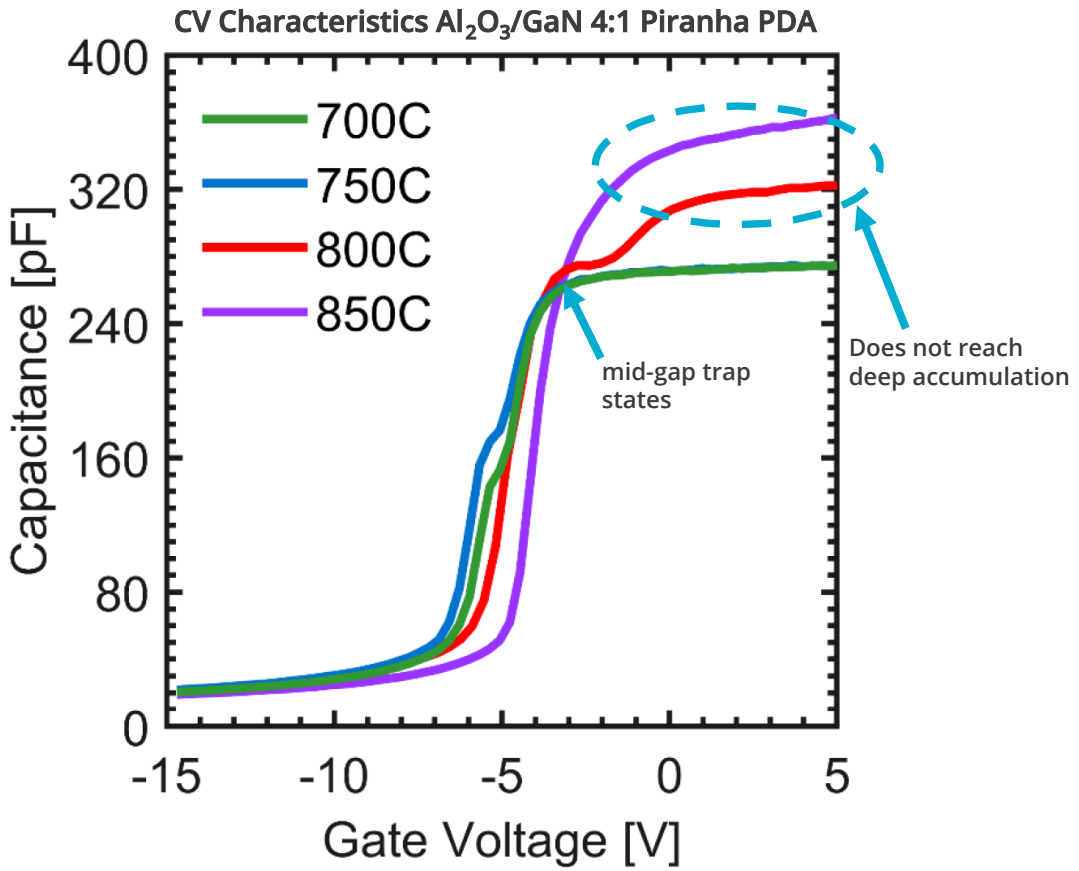
- SiO_2 dielectrics show max breakdown near 6 MV/cm
  - Solid – 4:1 Piranha
  - Dashed – 100:1 HF

- Relative improvements to leakage currents and breakdown strength at 850°C PDA
  - Varying surface treatments show little effect on breakdown or leakage



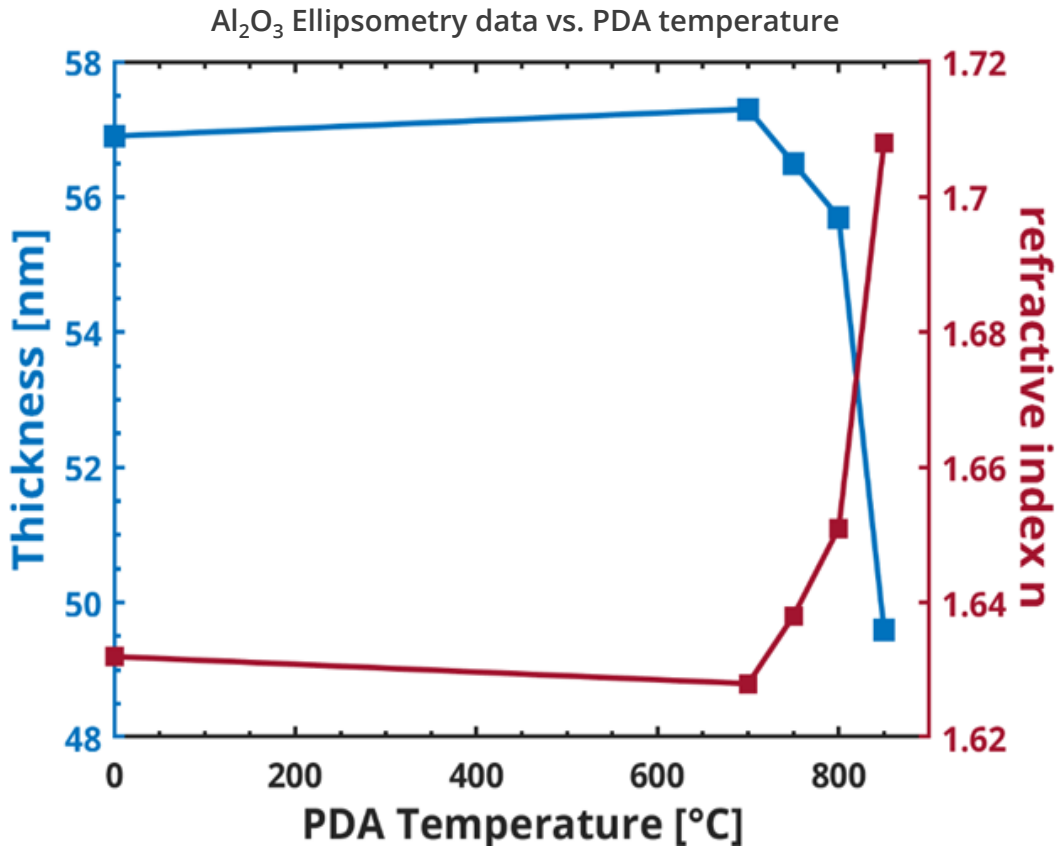
Al_2O_3 dielectrics highly dependent on ALD quality

- Shelf observed for all Al_2O_3 CV curves
  - Associated with mid-gap trap states
  - Reduced with higher temperature PDAs
- 700 and 750°C PDAs exhibit reduced CV characteristics
  - Oxide capacitance at lower PDA temps $\varepsilon_{Al2O3} \approx 7.5$
  - Theoretical $\varepsilon_{Al_2O_3} \approx 9.8$
- 800 and 850°C PDAs improve dielectric constant
  - Data more consistent with theoretical capacitance



$$= {}_0$$

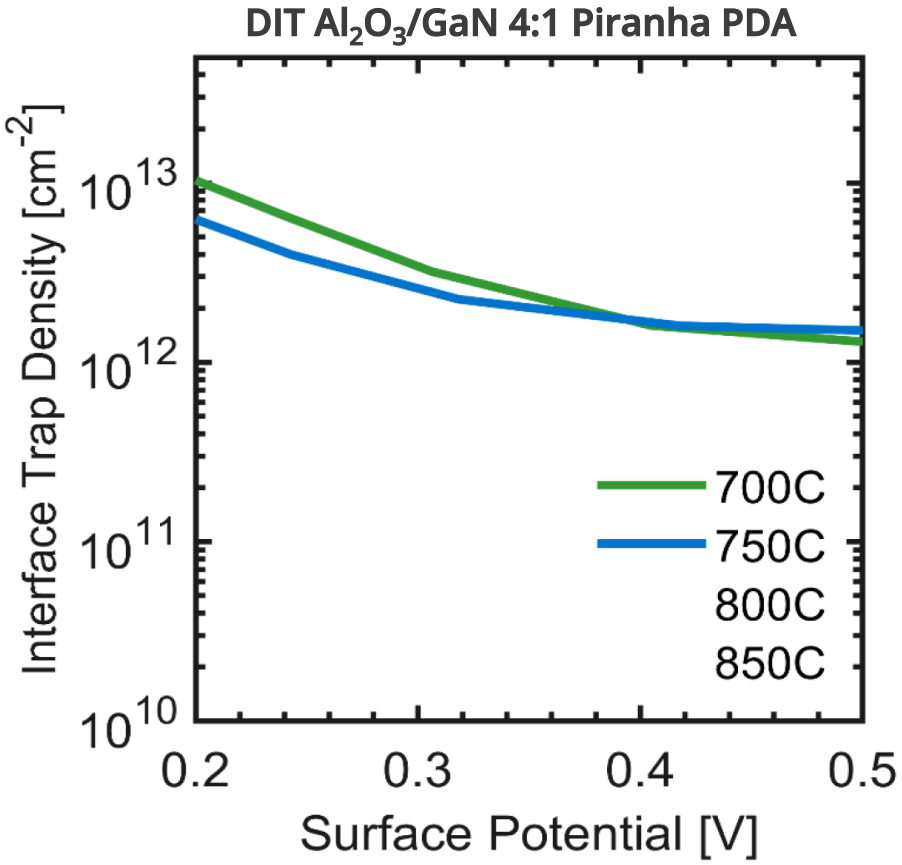
Ellipsometry data shows changes in Al_2O_3 films



- Temperature-induced crystallization/densification
  - Large increase for PDA temperatures above 800 °C
- Data shows change to physical and optical properties
  - Results in non-real results using C-Ψ_s method

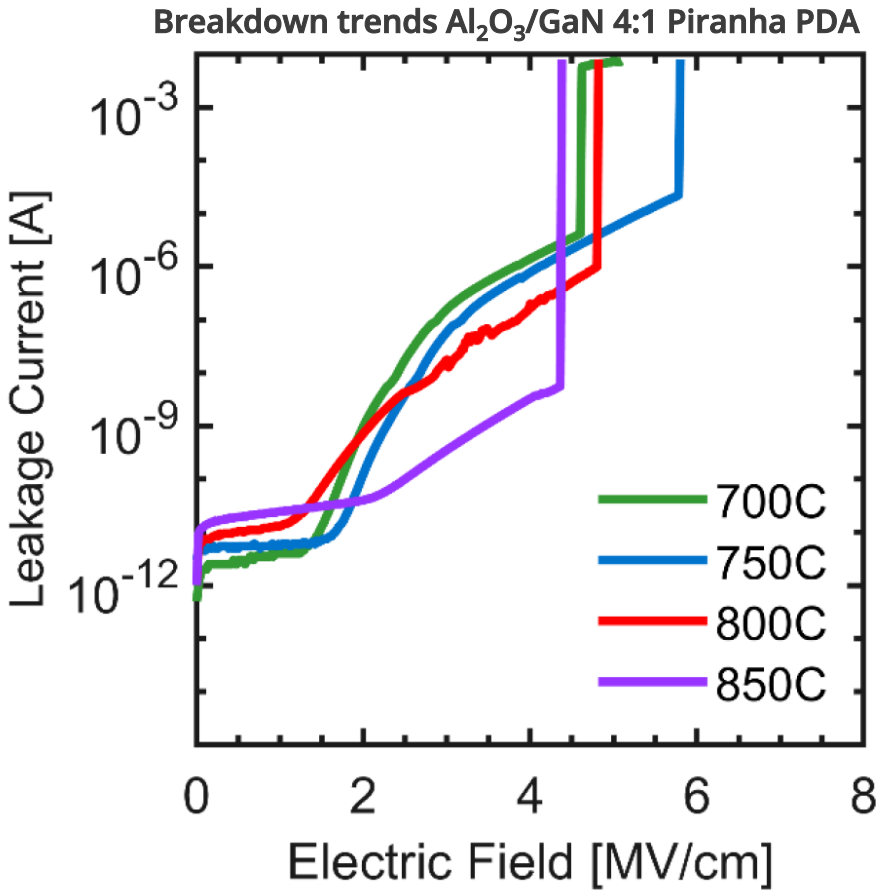
Anomalies in Al_2O_3 CV data make accurate D_{IT} analysis difficult

- Changes to CV characteristics make accurate D_{IT} analysis difficult
- 700 °C and 750 °C results may not be accurate due to the presence of mid-gap states
  - Shelf of high density of monoenergetic trap states reduces accuracy of analysis
- 800 and 850°C device D_{IT} is not possible
  - Devices do not reach stable accumulation capacitance



PDA and surface cleans do not significantly impact Al_2O_3 breakdown

- Breakdown measurements show representative curves for each PDA relative to surface treatment
- Al_2O_3 film breakdown tests
  - Small variation with breakdown trend near 5 MV/cm for 750 °C PDA
  - Higher temperature PDAs reduce leakage current and breakdown voltages, but increase crystallization



Conclusions

- SiO_2/GaN films show D_{IT} within range of current SiC power devices
- Increased integration time during testing may allow for more trap interaction
- D_{IT} did not notable change with varying surface clean
- Largest improvements to D_{IT} and leakage reduction with 850°C PDA
  - Al_2O_3 films at 850°C unable to reach deep accumulation
- Increased Al_2O_3 capacitance at higher PDA not entirely dependent on thickness
  - Varying thickness, dielectric constant, monoenergetic traps
- ALD does not provide accurate dielectric constants for SiO_2 or Al_2O_3
  - Requires high temperature PDAs which reduce CV shelf, but crystallize material
  - CV shelf may be reduced via improved deposition and chamber cleans
  - Improved deposition techniques may allow for lower PDA temperatures

Future work

- Modifications to C-Ψ_s method in order to improve reliability of analysis
  - Refine process for wide bandgap materials
- Additional work towards conductance method
  - More complicated process, but will improve D_{IT} accuracy
  - May allow for more accurate analysis of Al_2O_3 films for MOSFETs
- Investigation into improved ALD deposition techniques
  - Additional research into gate dielectrics with higher breakdown strengths

Questions?

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