SAND2022-6874C

Presentation session: **Monday 3B**

A 0.2-2 GHz Time-Interleaved Multi-Stage Switched-Capacitor Delay Element Achieving 448.6 ns Delay and 330 ns/mm² Area Efficiency

Travis Forbes, Benjamin Magstadt, Jesse Moody, Andrew Suchanek, Spencer Nelson

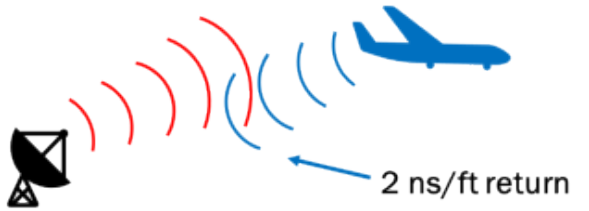
Sandia National Laboratories

Motivation – Limited RF Time Delay

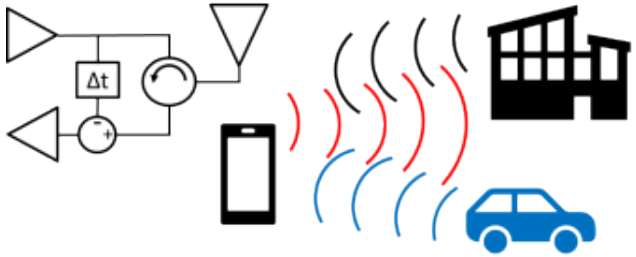
Radar return simulation in radar testers and DRFM devices require > 400 ns broadband programmable delay

- Digital approaches consume watts
- RF delay elements today limited to < 8 ns
- Full duplex will require >> 30 ns for reflections

Radar Scenario

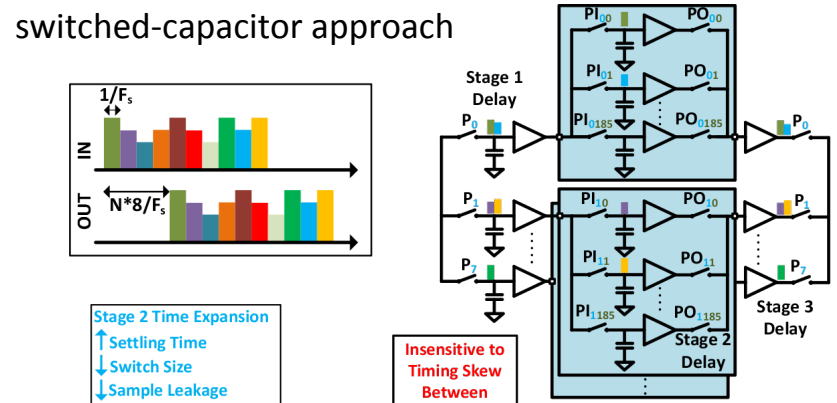


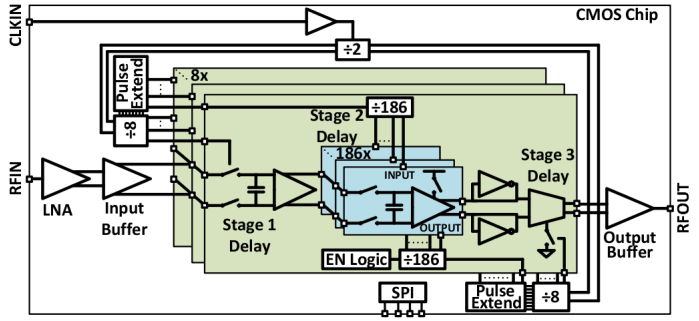
Full-Duplex Scenario



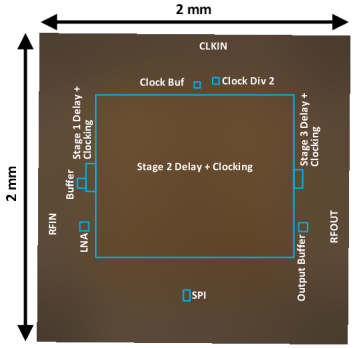
Delay Element Implementation

Proposed time-interleaved multi-stage switched-capacitor approach



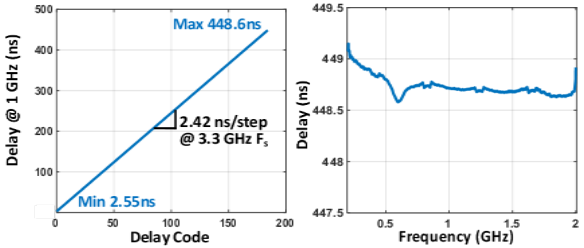


Measurement Results



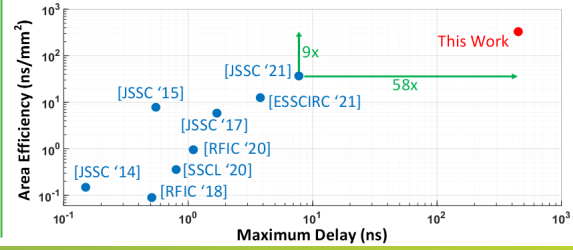
- 45 nm SOI CMOS
- 1.36 mm² active area
- 5x5 mm² QFN package
- 2.55-448.6 ns delay range
- 24 dB gain, 7.1 dB NF
- 80 mW from 1V supply

Delay Performance at 3.3 GHz F_s



- < ±4 ps DNL/INL
- 0.2-2 GHz bandwidth

Performance Comparison



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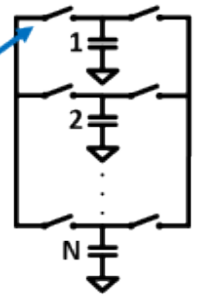
Switched-Capacitor Delay Challenges

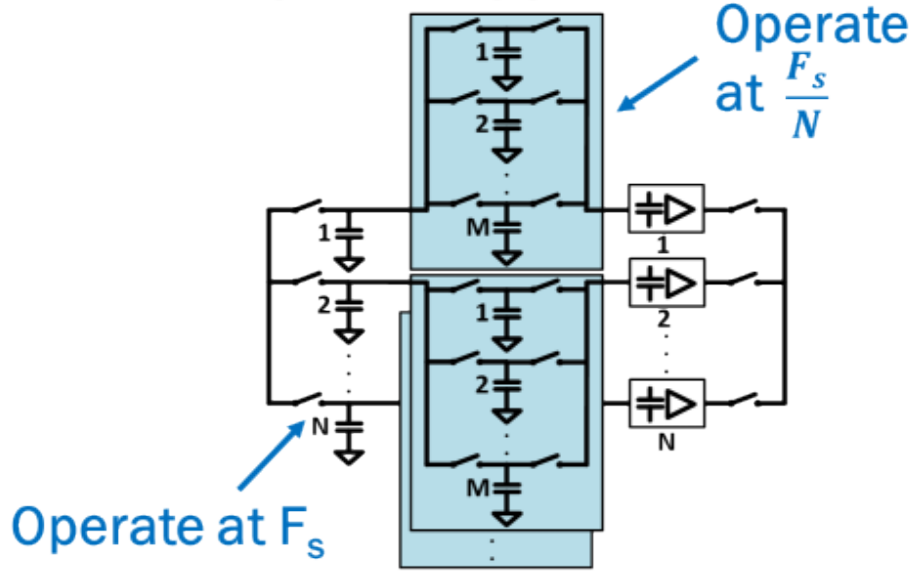
Switched-Capacitor

- ~450 ns Delay @ F_s = 3.3 GHz
  - >1480 sampling capacitors
  - >1480 phase sampling clocks
  - Large RF load capacitance
- Switch leakage challenge
  - Max Delay $\frac{N-1}{F_s}$

Sample in $\frac{1}{F_s}$ time but hold for > $\frac{1480}{F_s}$ time



Proposed Approach



- Max RF Delay $\frac{N(M-1)}{F_s}$
  - Leakage mitigated through time expansion

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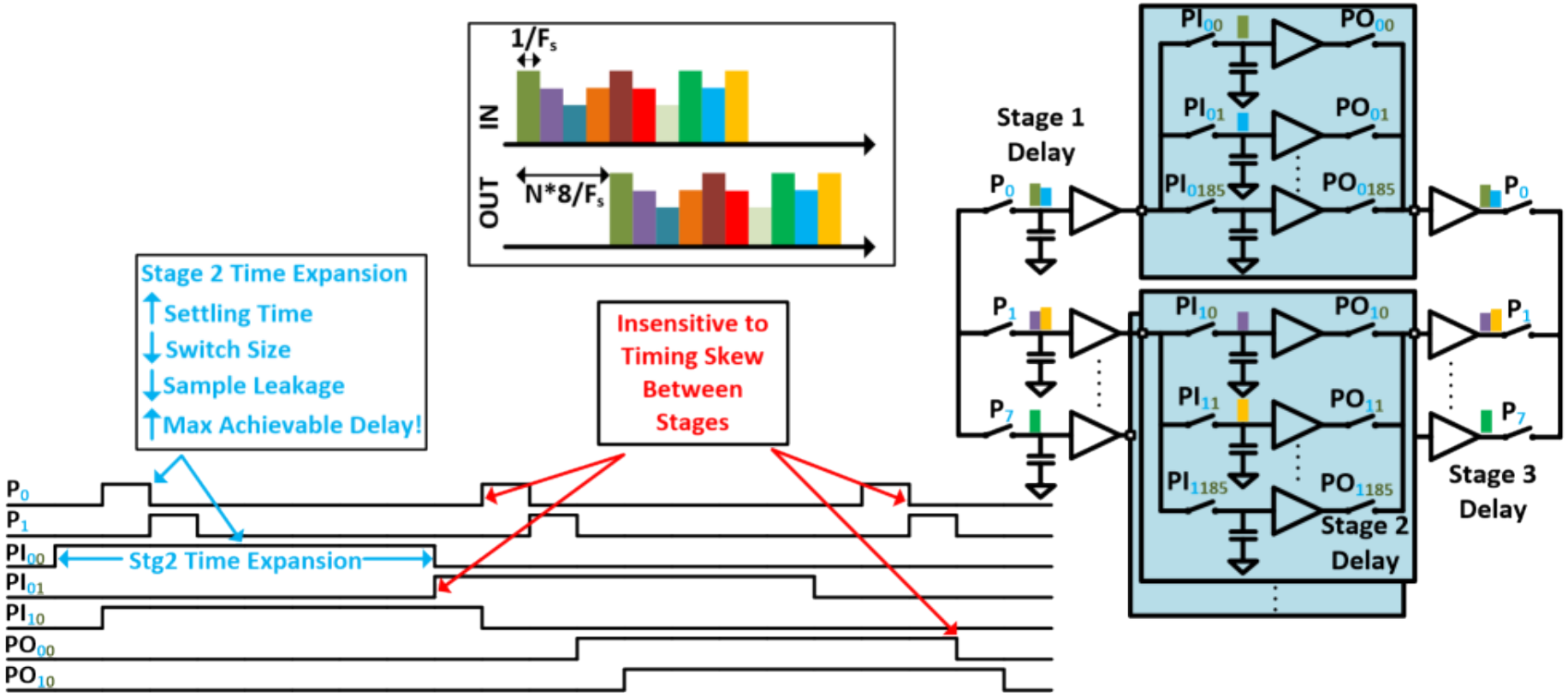
Time-Interleaved Multi-Stage Switched-Capacitor Approach



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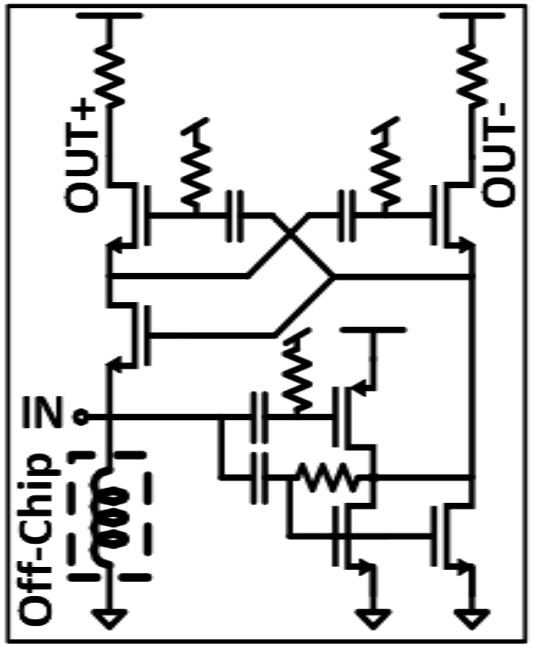
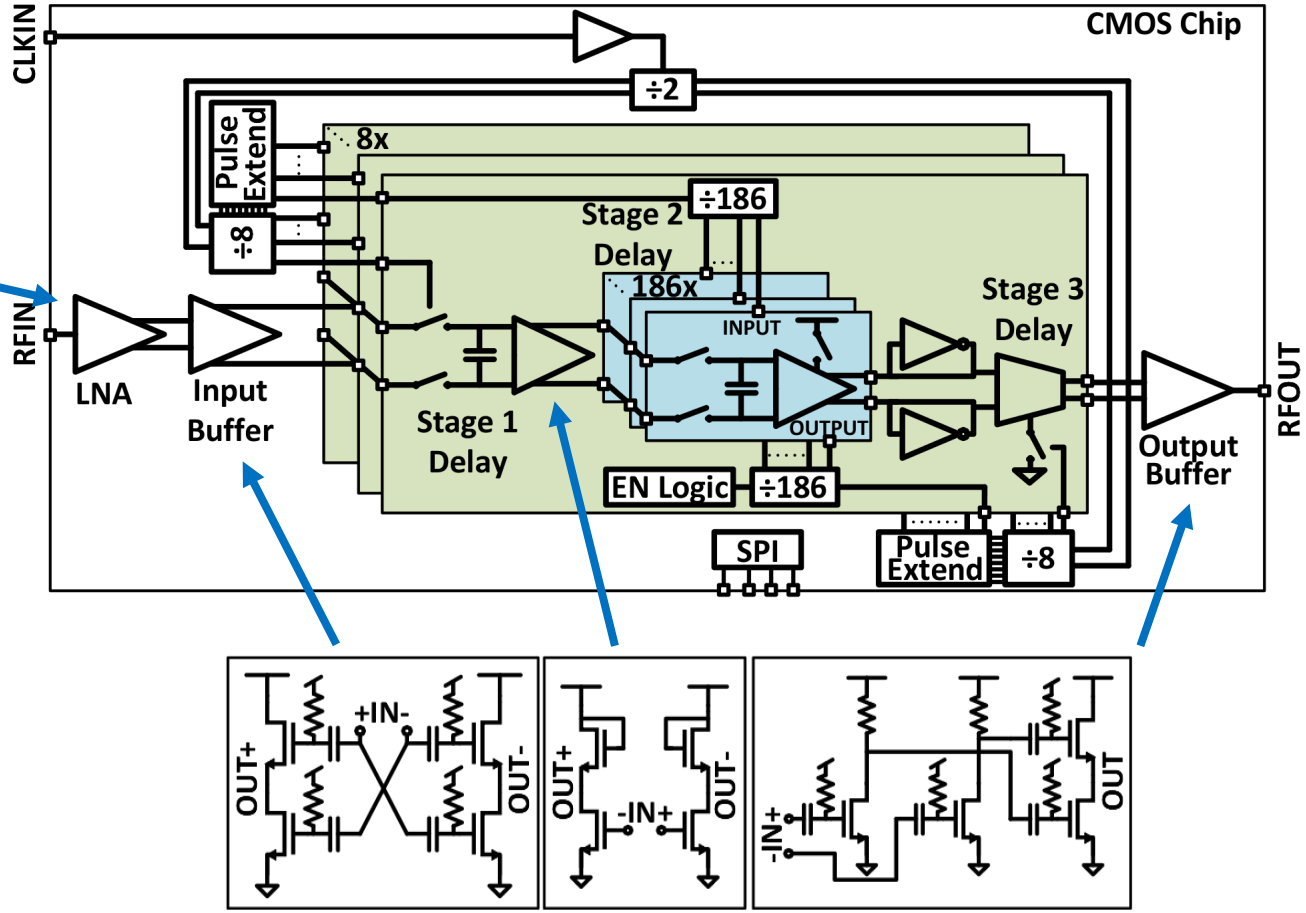
Circuit Implementation



LNA modified from Mak et al., IEEE JSSC 2011



- LNA has 0.0016 mm² area with 3.5 dB NF at 3.5 mW

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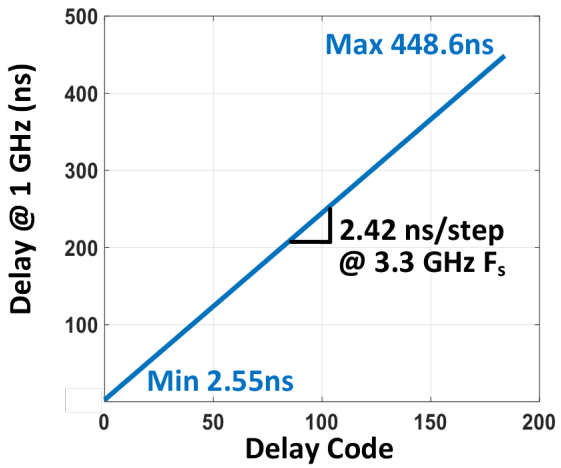
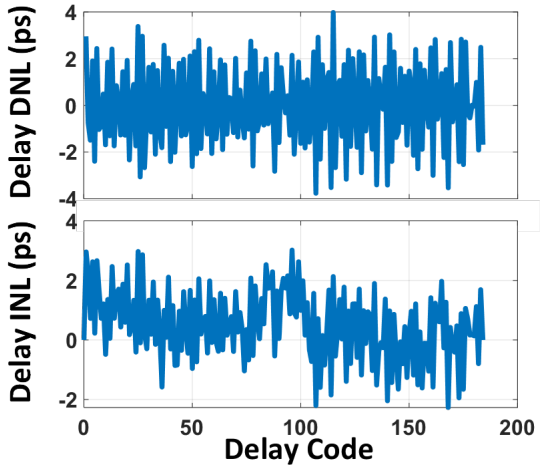
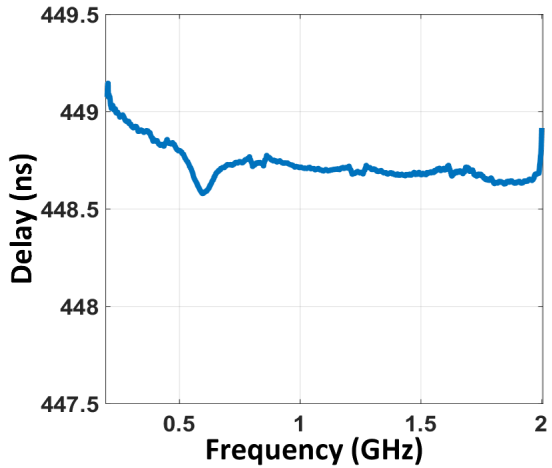
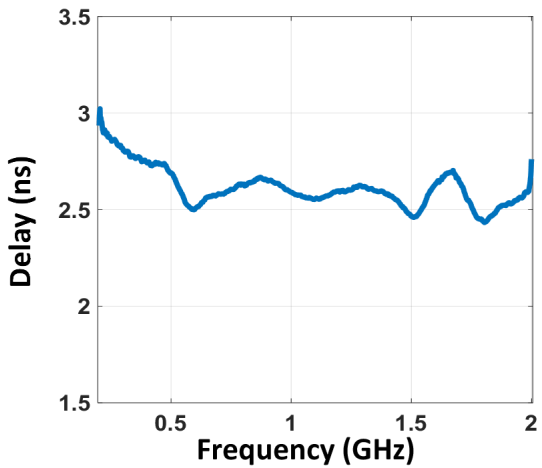
Delay Performance at 3.3 GHz F_s









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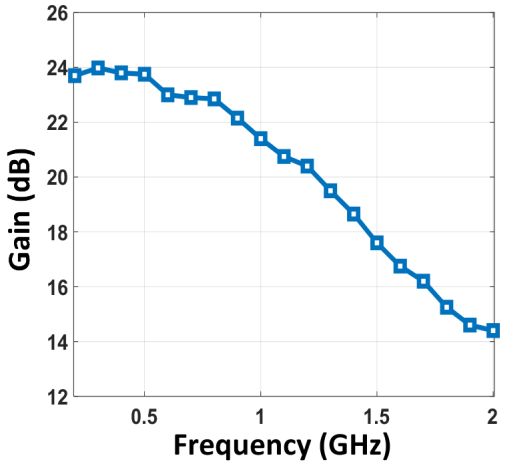
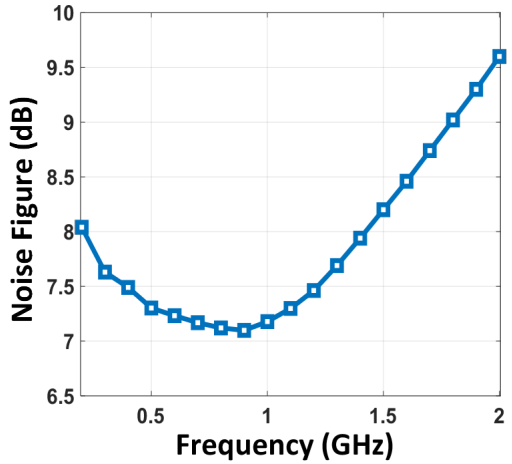
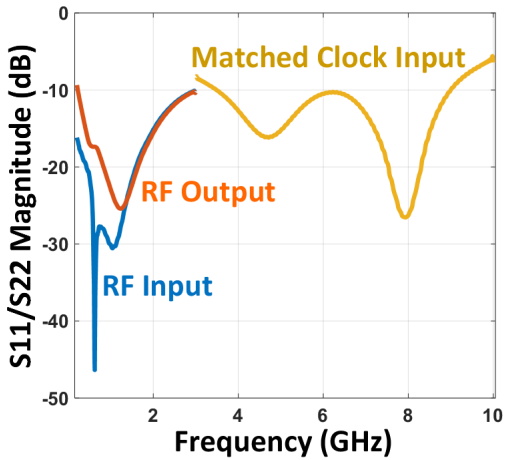
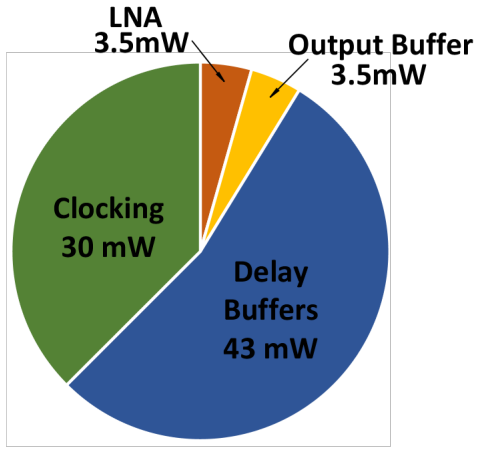
RF Performance









$$\text{ZOH} = \frac{\sin\frac{\pi F_{RF}}{F_S}}{\frac{\pi F_{RF}}{F_S}}$$

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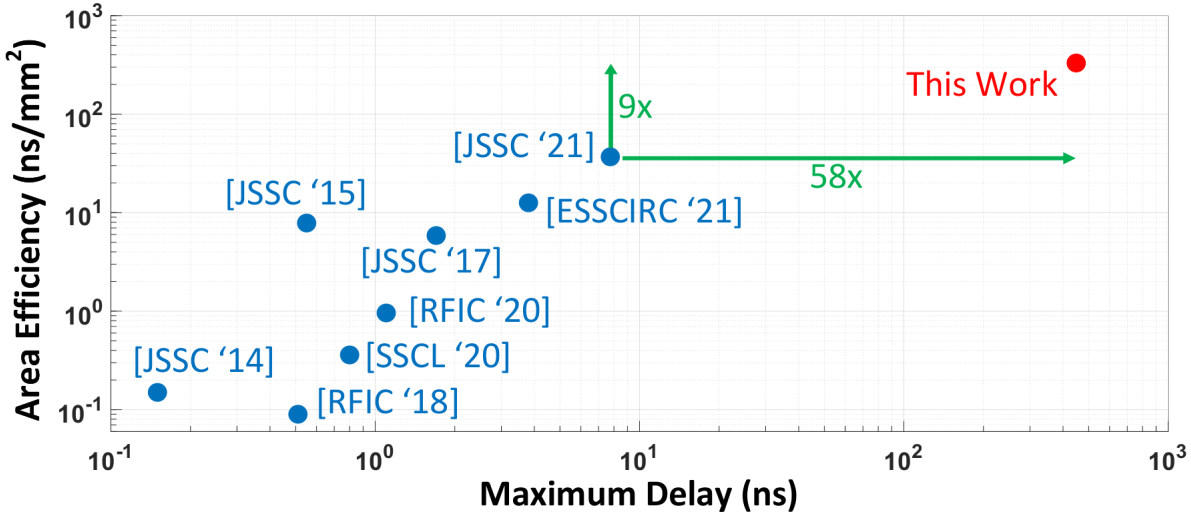
Comparison to Prior Art

	This Work	Nagulu et al., JSSC 2021	Garakoui et al., JSSC 2015	Mondal et al., JSSC 2017
Design	Delay Element	SIC Receiver	4 Channel Beamformer	Delay Element
Architecture	TI-MS Switched-Cap	Switched-Cap	Gm-C	Gm-C
Delay Frequency Range	0.2GHz-2GHz	0.1GHz-1GHz	1GHz-2.5GHz	0.1GHz-2GHz
3-dB Bandwidth	0.2GHz-1.1GHz[a]	0.1GHz-0.5GHz[b]	1GHz-2.5GHz	0.1GHz-2GHz
Max Delay	448.6ns[a]	7.75ns[b]	0.55ns	1.7ns
Delay per Unit Area	330ns/mm^2[2a]	37ns/mm^2[2b]	7.9ns/mm^2	5.9ns/mm^2
Delay Range	175.9x	31x[b]	39.3x[c]	6.8x
Gain	24dB	-19dB[b]	12dB	0.6dB
Noise Figure	7.1dB	-	8dB	23dB
IP1dB	-27dBm	-	-21dBm	-13dBm
Power	80mW[a]	7.4mW[b]	90mW[d]	364mW
Technology	45nm SOI	65nm	140nm	130nm
Delay Active Area	1.36mm^2	0.21mm^2[2b]	0.07mm^2	0.29mm^2

[a]F_s=3.3GHz. [b]Max RF delay element extrapolated from publication. [c]Based on delay step. [d]Single Channel



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Conclusion

- Introduced a time-interleaved multi-stage switched-capacitor delay element technique
- Breaks < 8 ns programmable RF CMOS delay limit with 448.6 ns delay and state-of-the-art area efficiency
- Enables system miniaturization through CMOS delay replacement of non-programmable SAW and coaxial delays

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Backup

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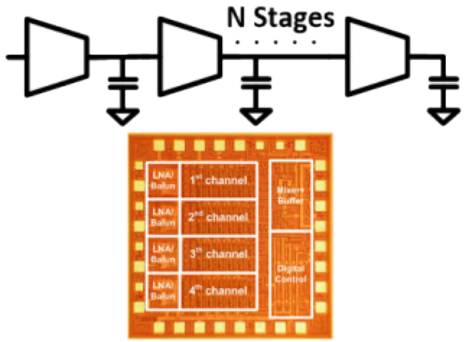
Prior RF Delay Approaches

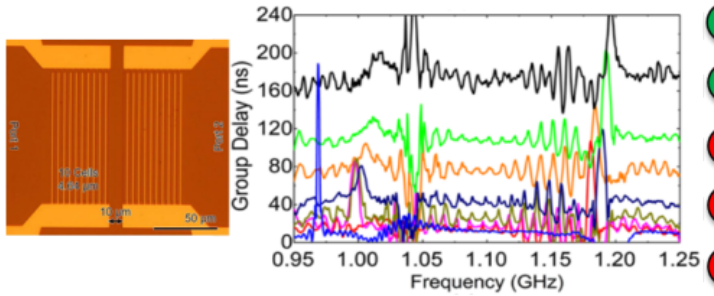
Gm-C All-Pass Filter



Garakoui et al., IEEE JSSC 2015

- < 2 ns delay
- Moderate Area
- Broadband
- Programmable
- Delay Variation

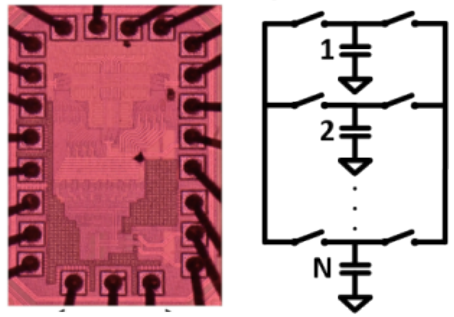
SAW Delay Line



Lu et al., IEEE MTT 2021

- > 400 ns delay
- Small Area
- Narrowband
- Fixed Delay
- Delay Variation

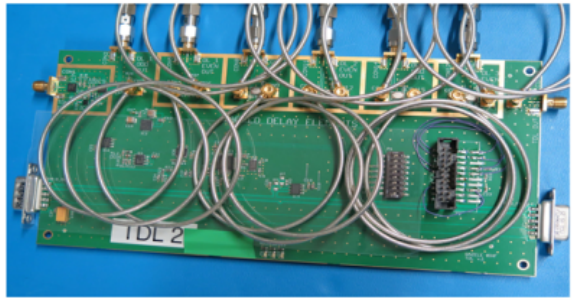
Switched-Capacitor



Nagulu et al., IEEE RFIC 2020, IEEE JSSC 2021

- < 8 ns delay
- Small Area
- Broadband
- Programmable
- Delay Variation

Coaxial Delay



Gadringer et al., IET Radar, Sonar & Navigation 2018

- > 400 ns delay
- Large Area
- Broadband
- Fixed Delay
- Delay Variation