



# QT08.04.01: Atomic Precision Patterning and Alignment for Dopant-based Quantum Devices

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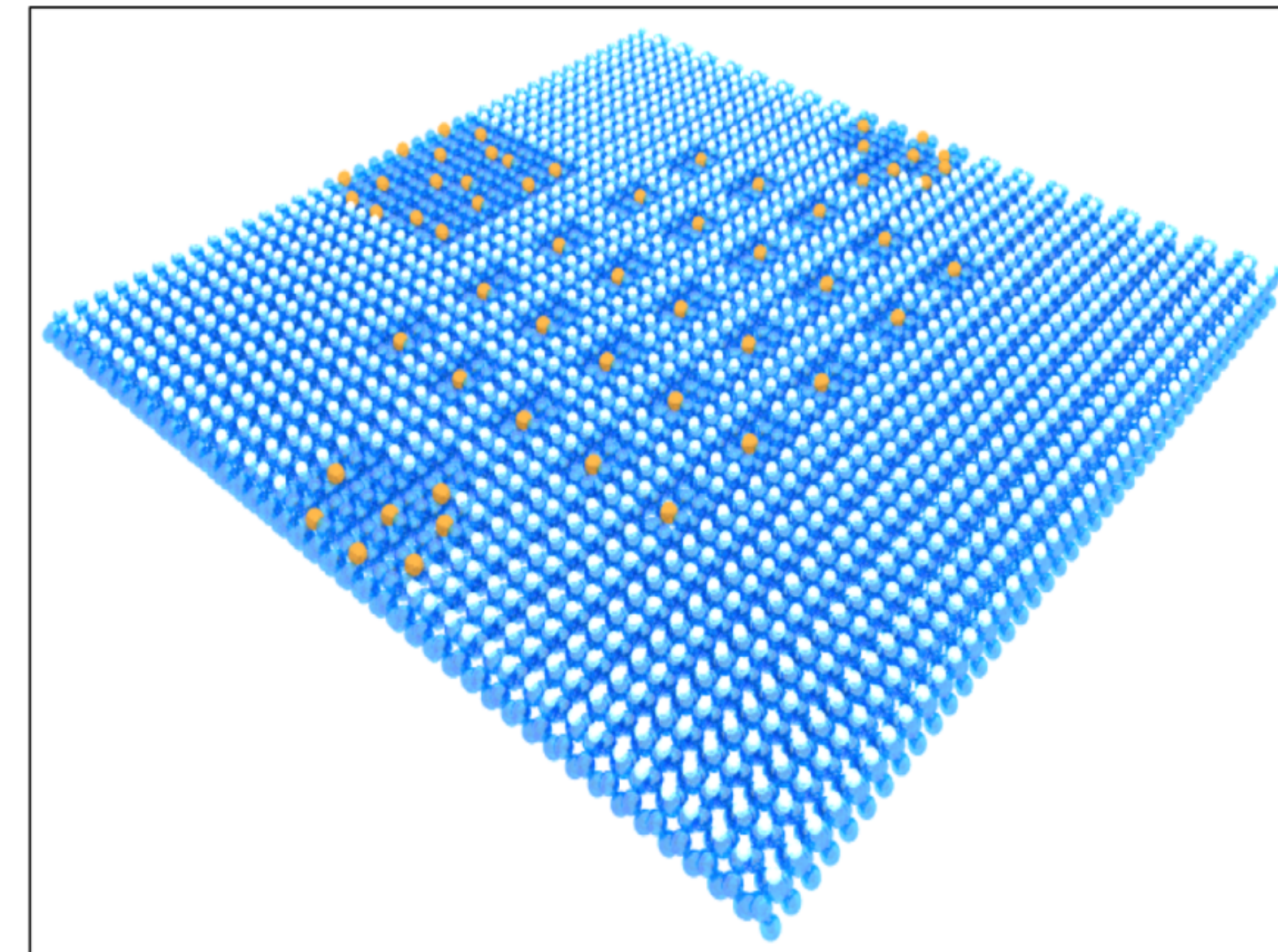
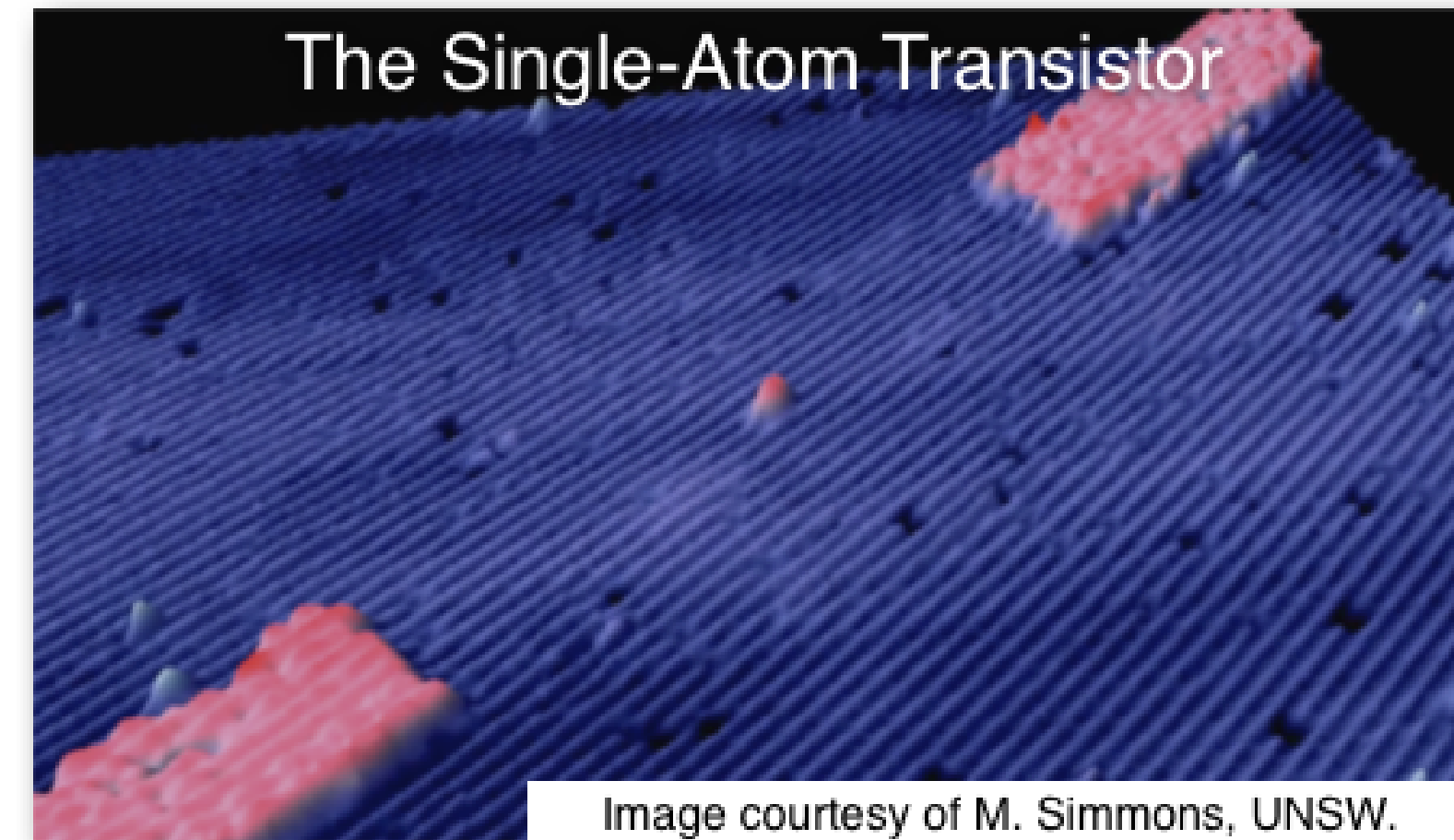
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# Atomically Precise Dopant Placement

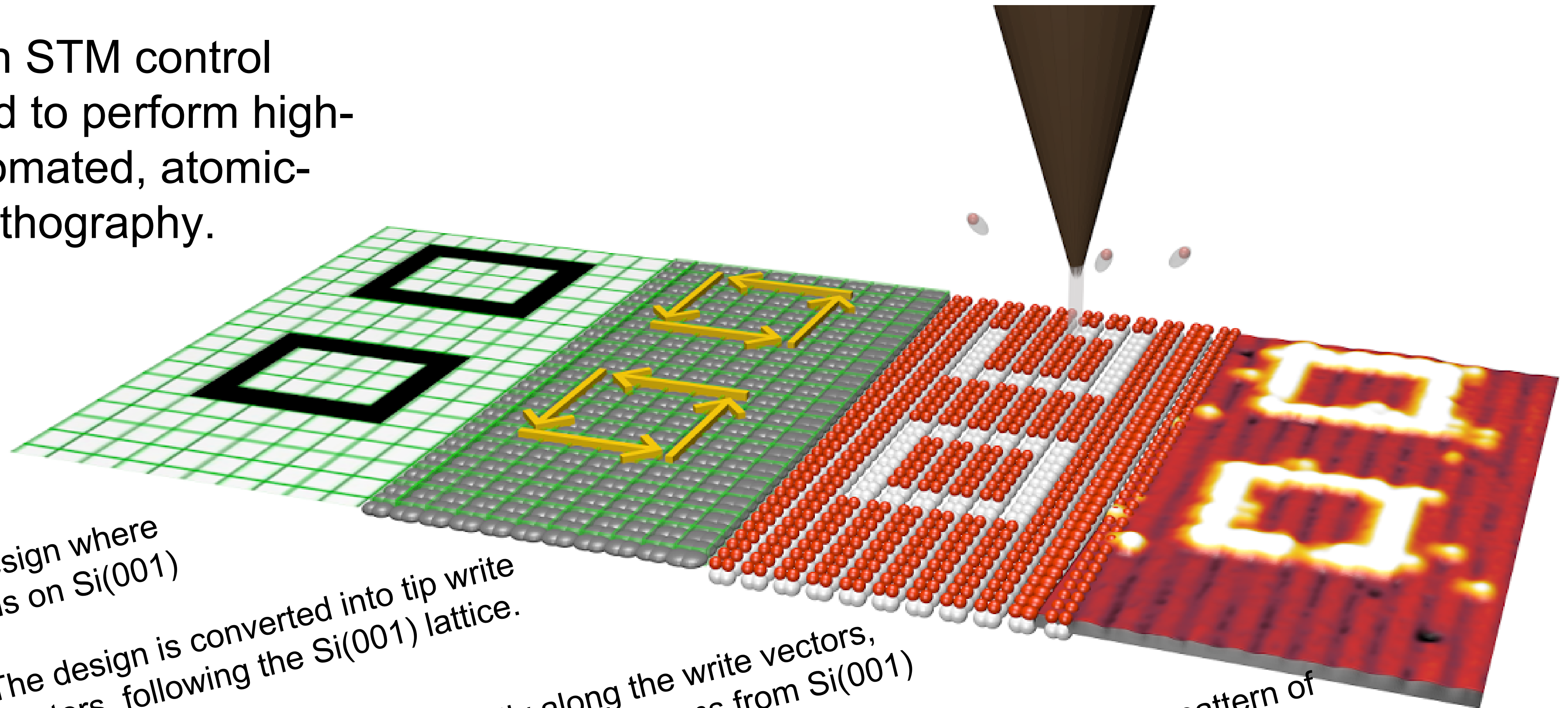
- P-in-Si technology has been demonstrated to make single qubits.
- One design for a useful quantum computer, the surface code computer, requires a 32x32 array of precisely placed P dopant patches.
- An array of single or multiple dopant atoms positioned precisely within Si has also been proposed as an embodiment of an Analog Quantum Simulator.
- 2D Bipolar devices require precise alignment of the patterns of the second dopant to the first.
- Scale up to devices requiring atomically precise positioning of large arrays of dopants with high yield, high reproducibility and high throughput will require new tools
  - Atomically Precise Advanced Manufacturing (APAM)





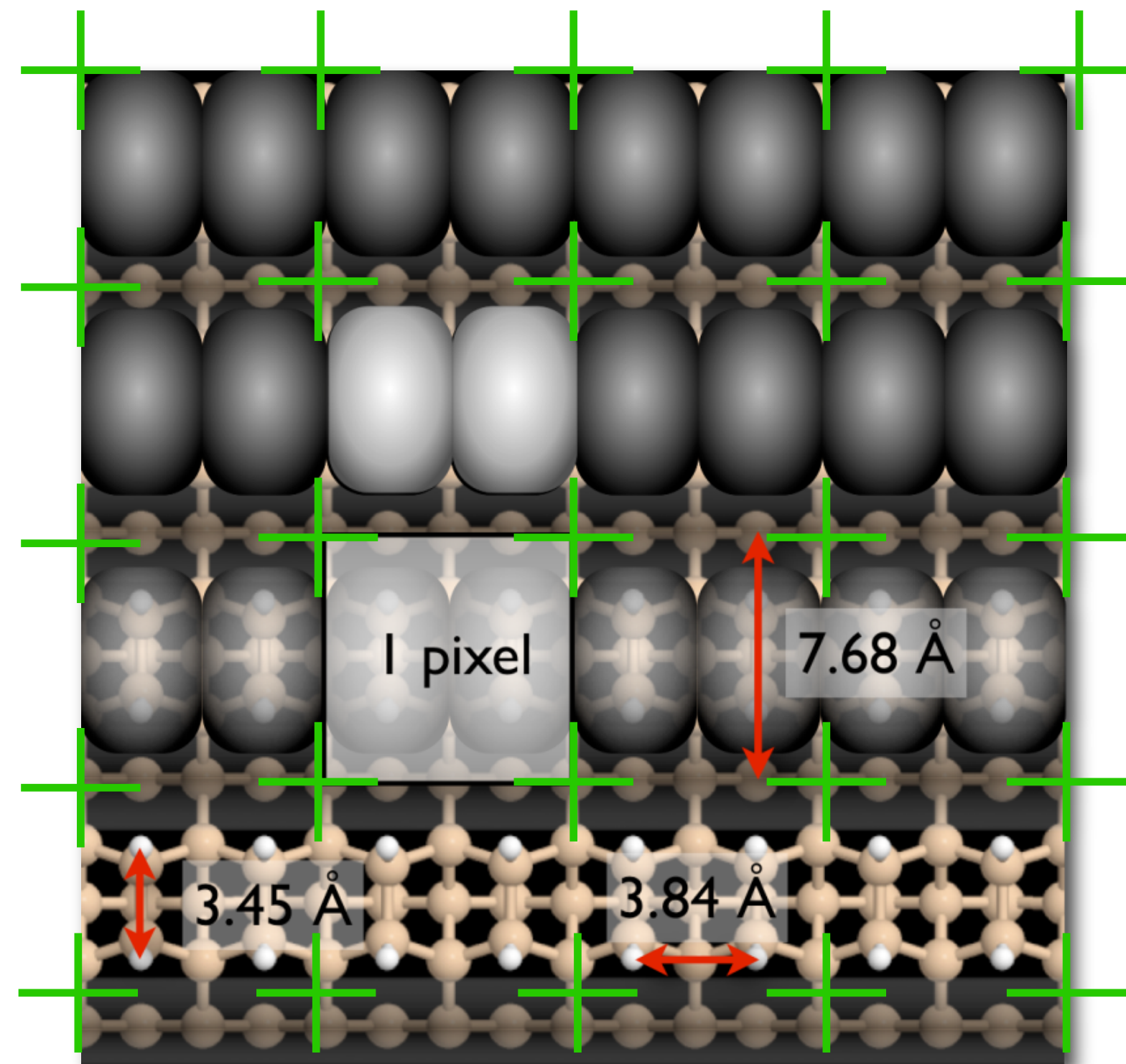
# ZyVector™: the concept

ZyVector™ is an STM control system designed to perform high-throughput, automated, atomic-precision STM lithography.

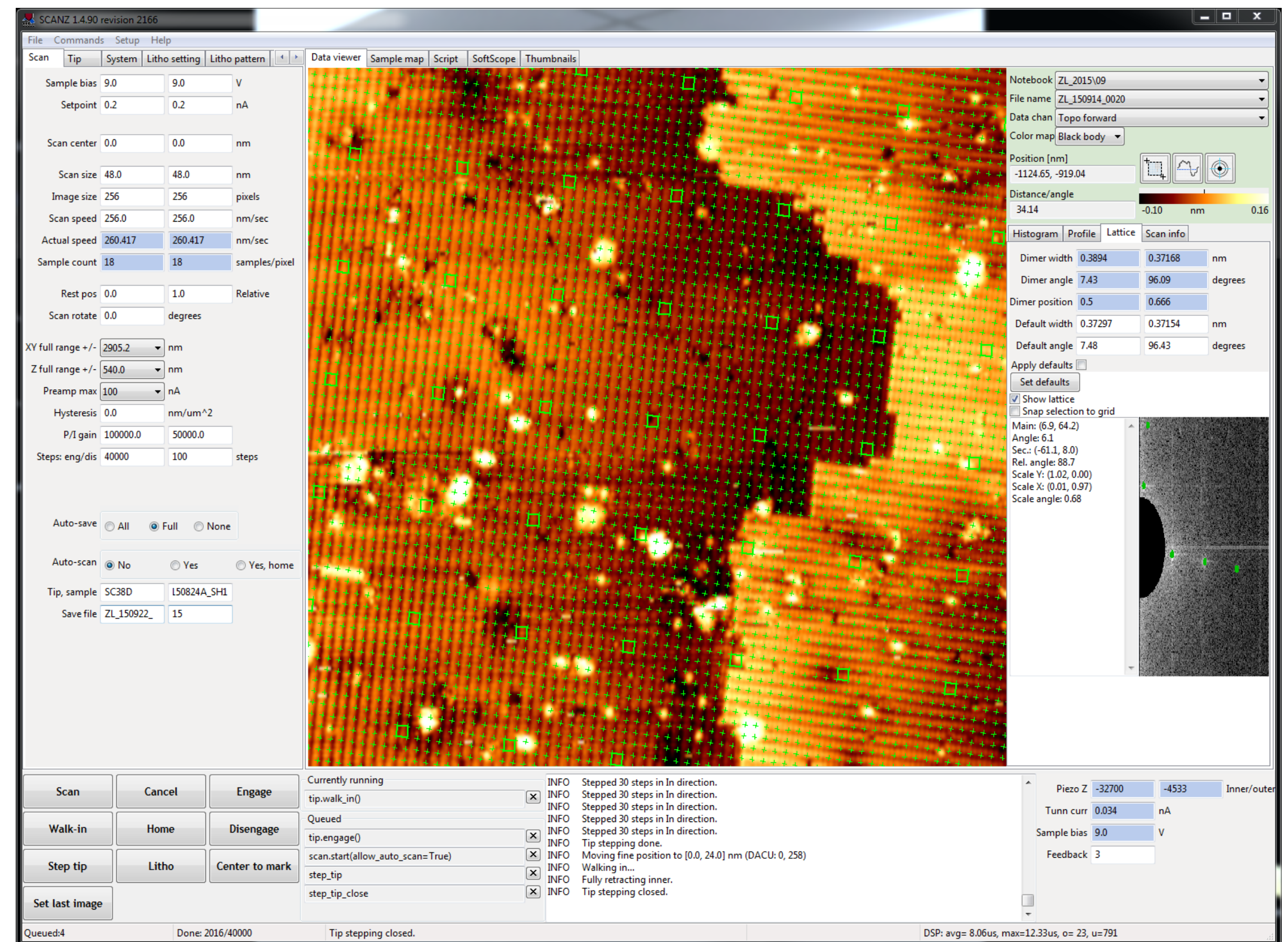




# Atomic lattice as pixel grid



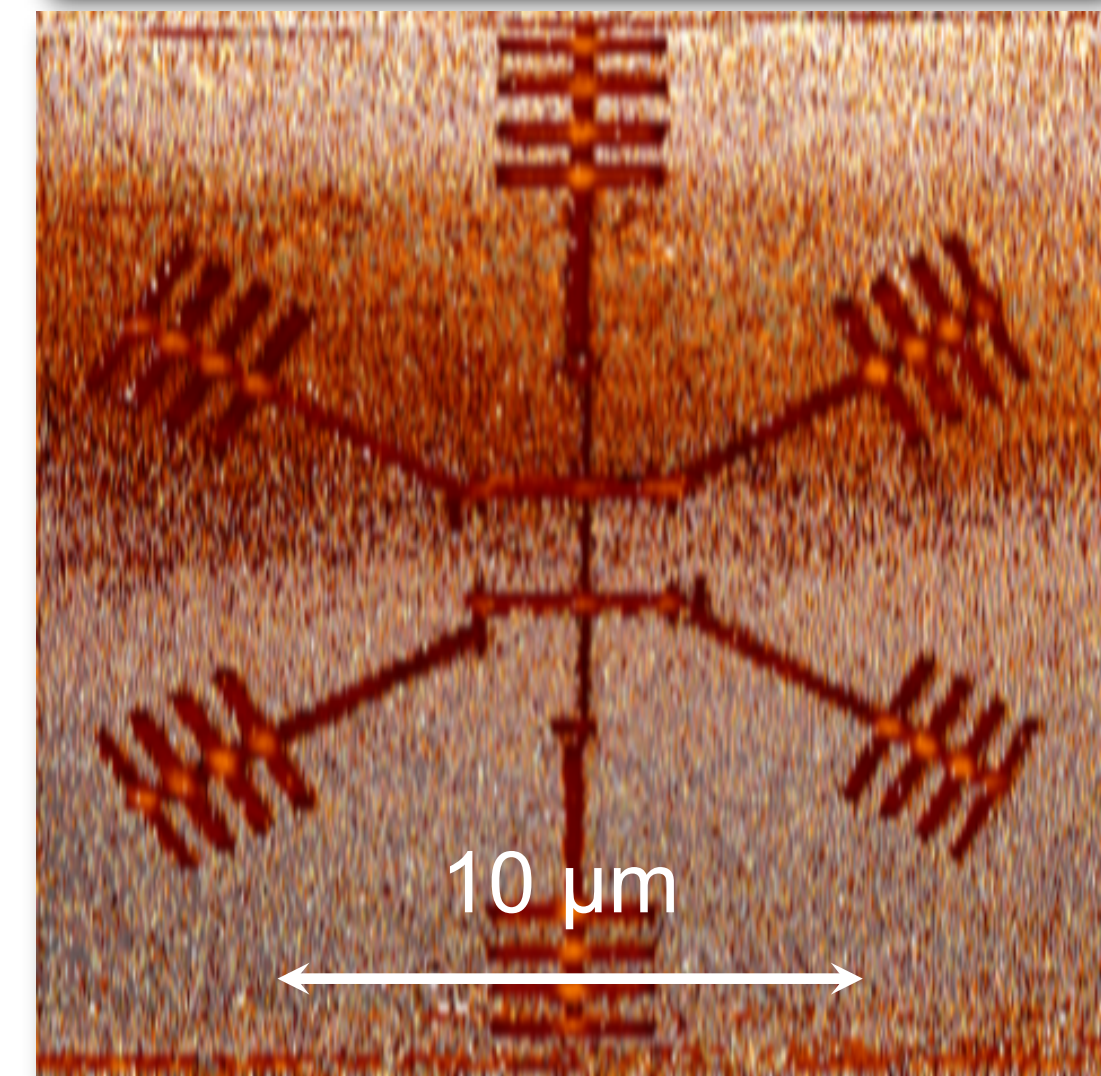
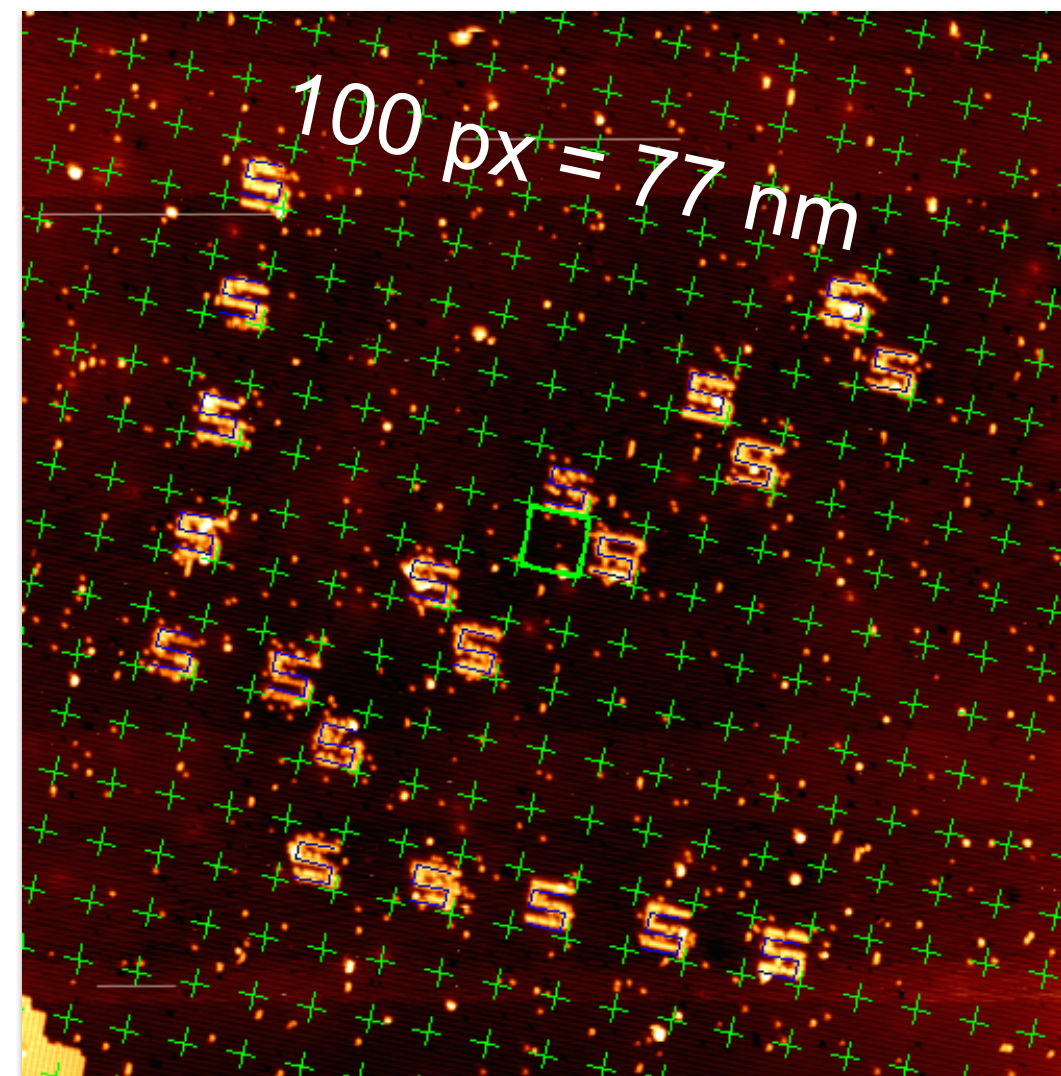
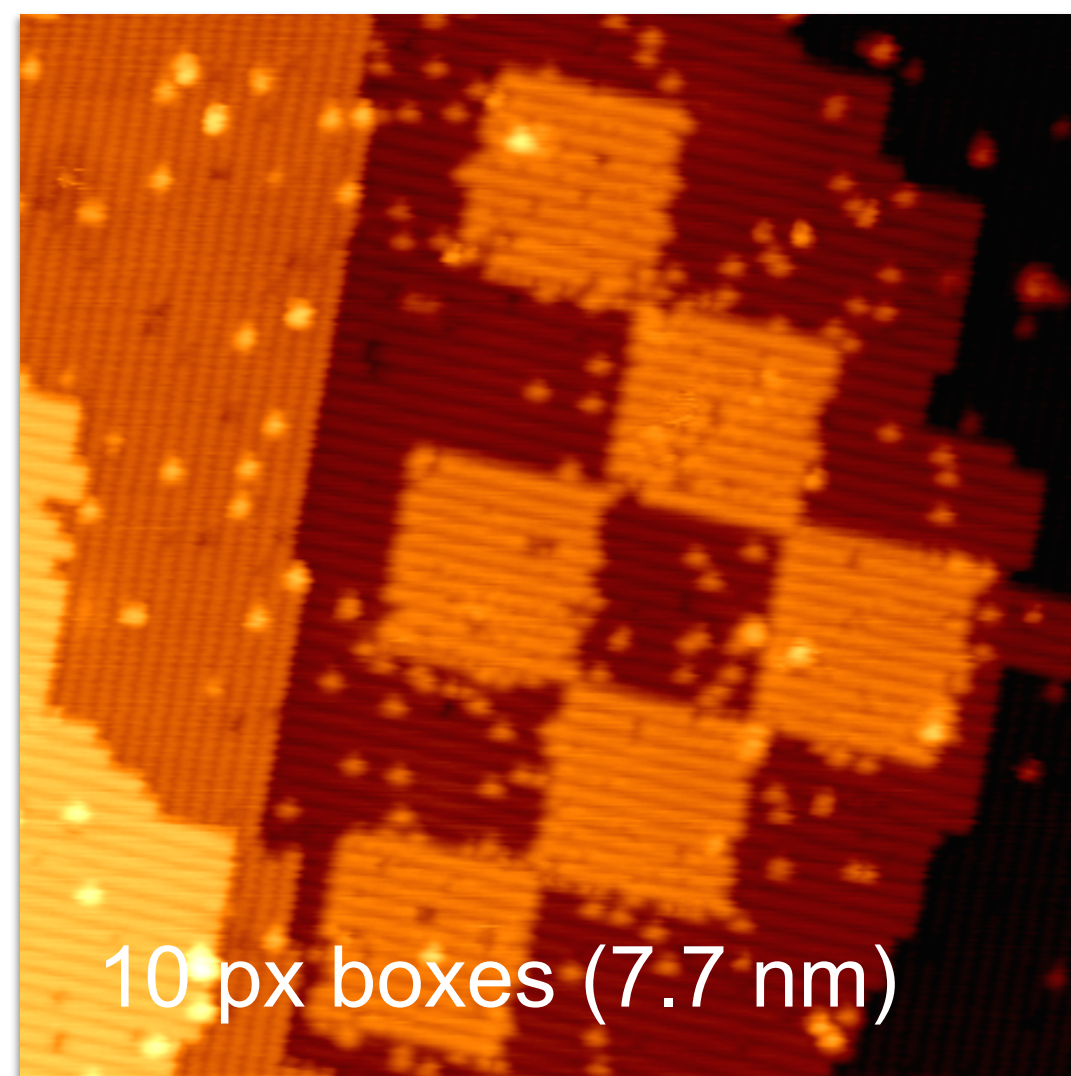
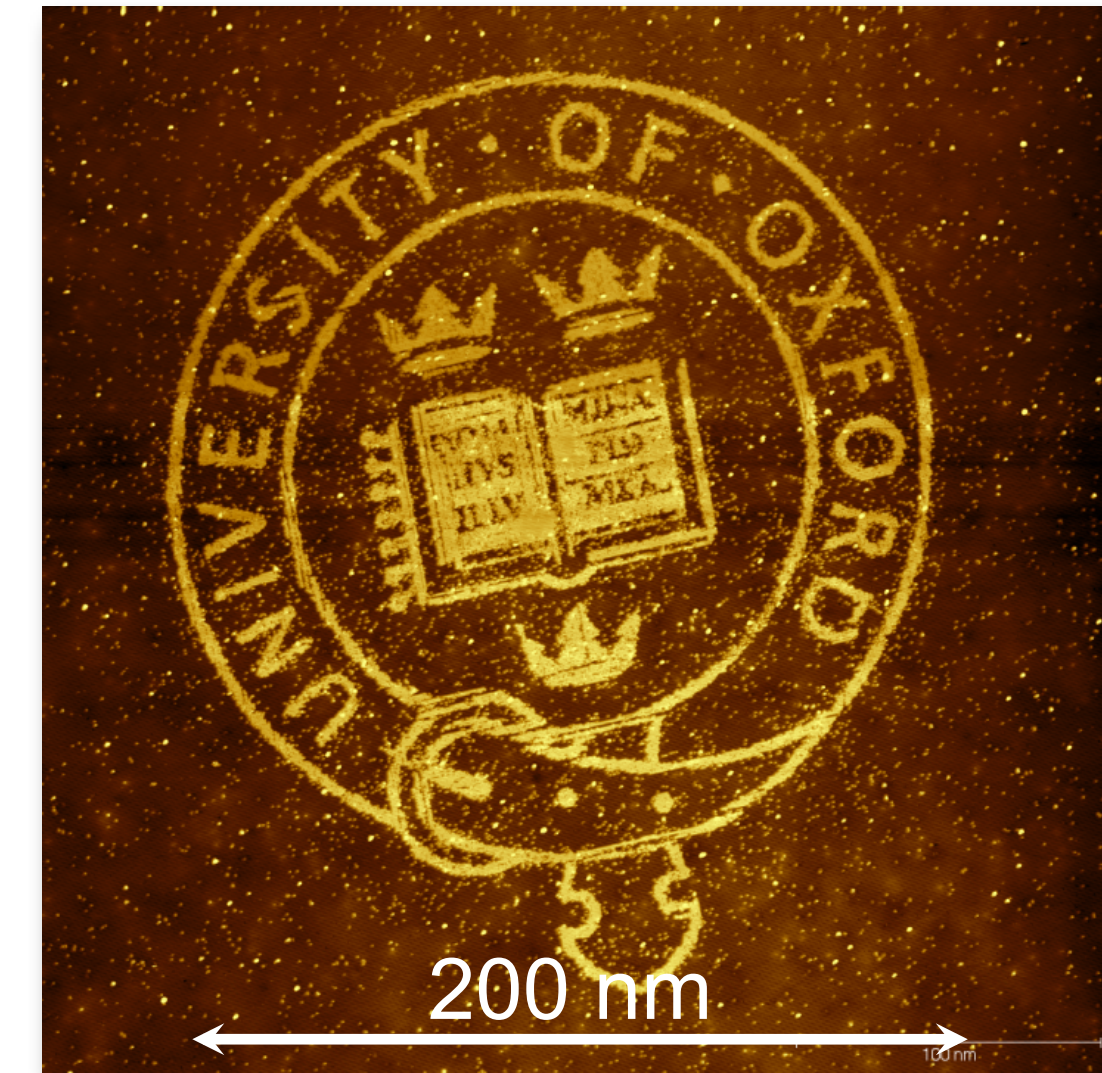
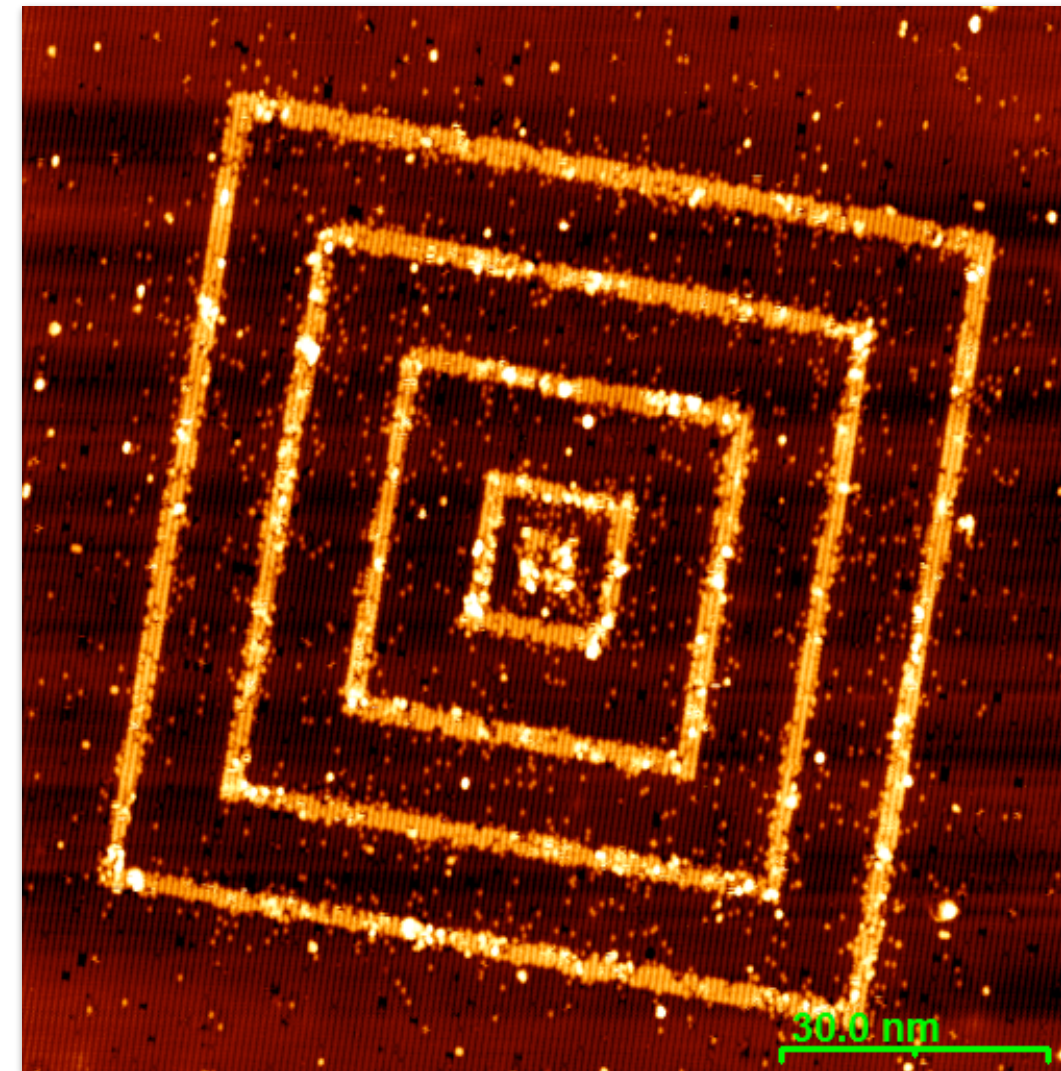
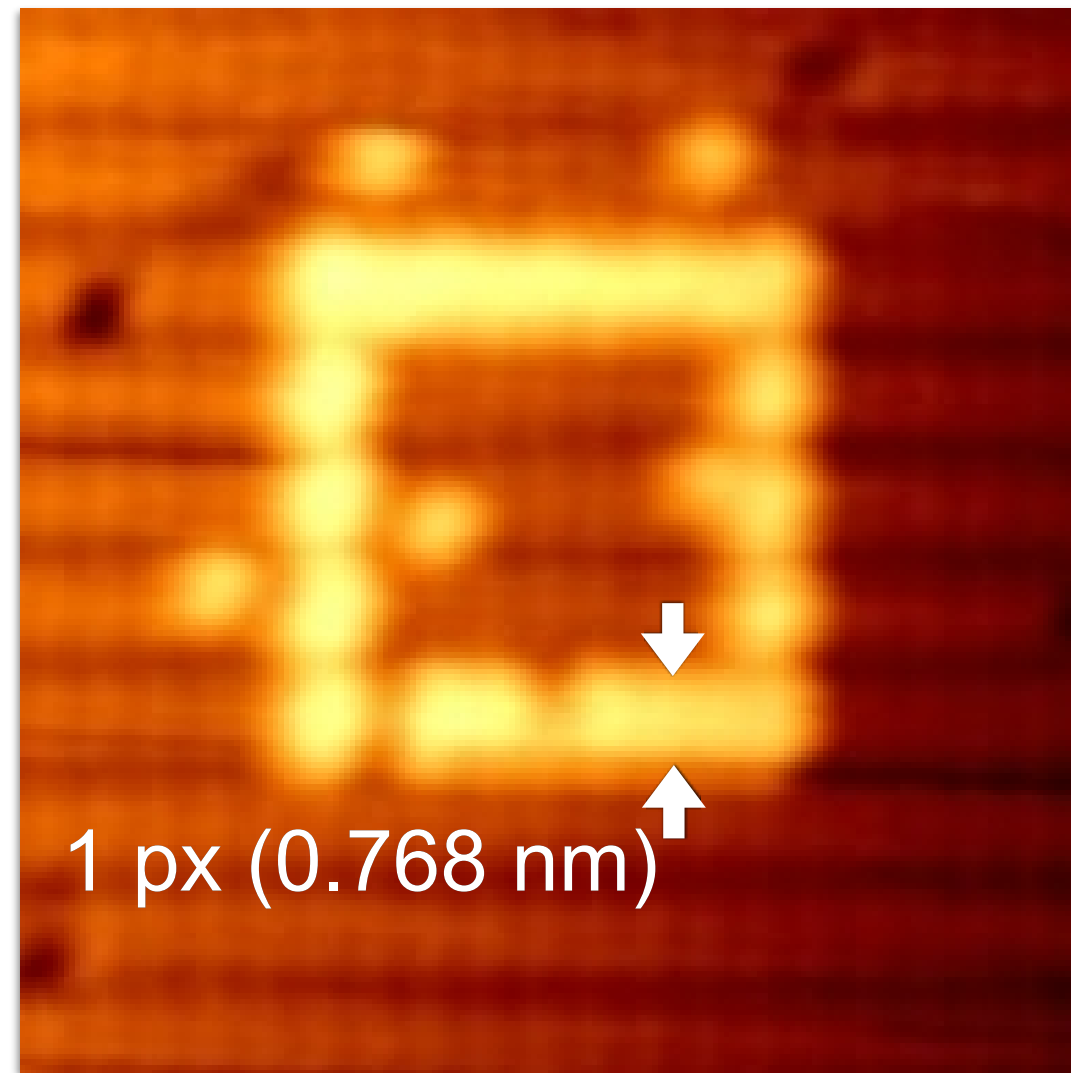
The lithography pixel; 2 dimers on a dimer row, 0.768 nm wide.



To achieve Atomically Precise patterning, we must take account of the discrete atomic lattice. We use Fourier analysis of an STM image to locate the atomic lattice, and lay out the pixel grid. The fundamental litho pixel is defined as 2 dimers, giving a 0.768 nm pixel.



# Automated AP Lattice-Aligned Patterning



Atomically Precise Patterning requires active position correction to fix a variety of inherent piezo positioning error mechanisms.

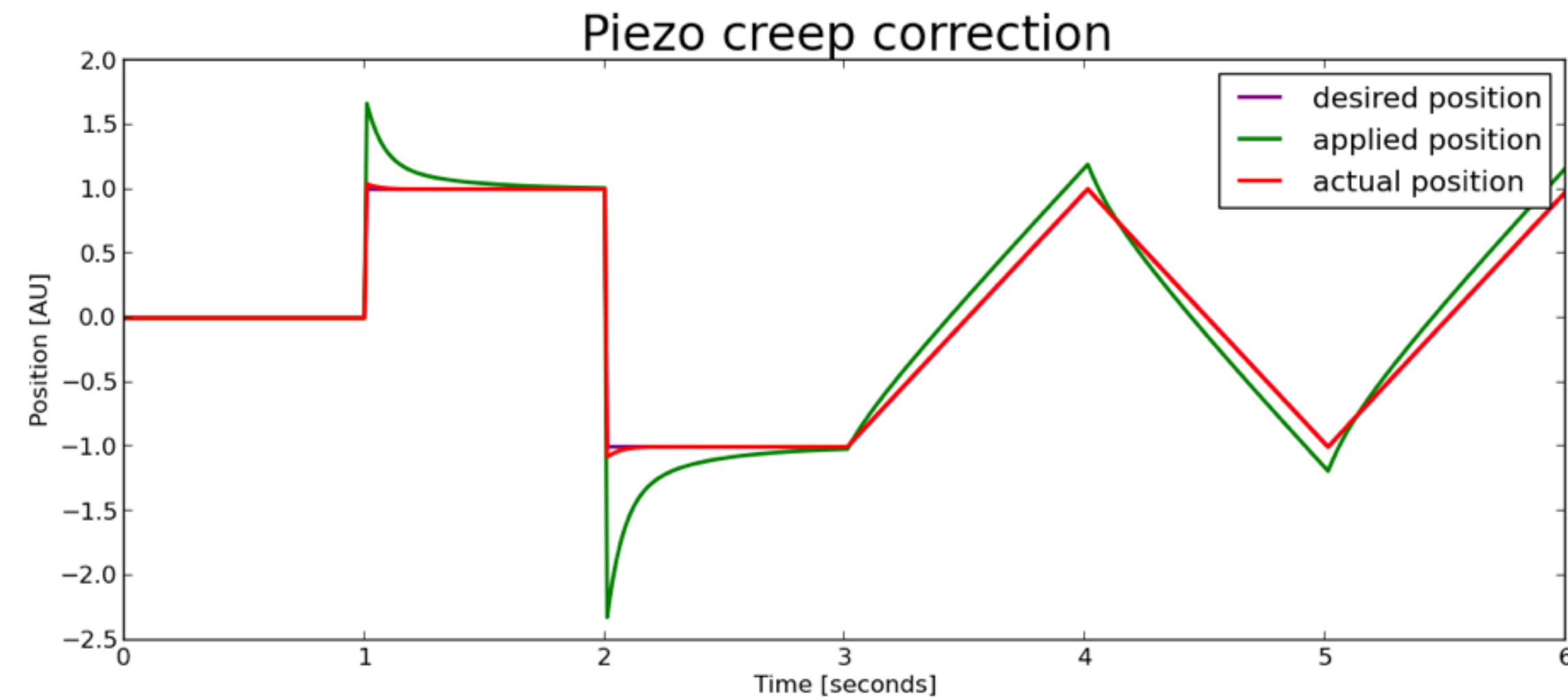
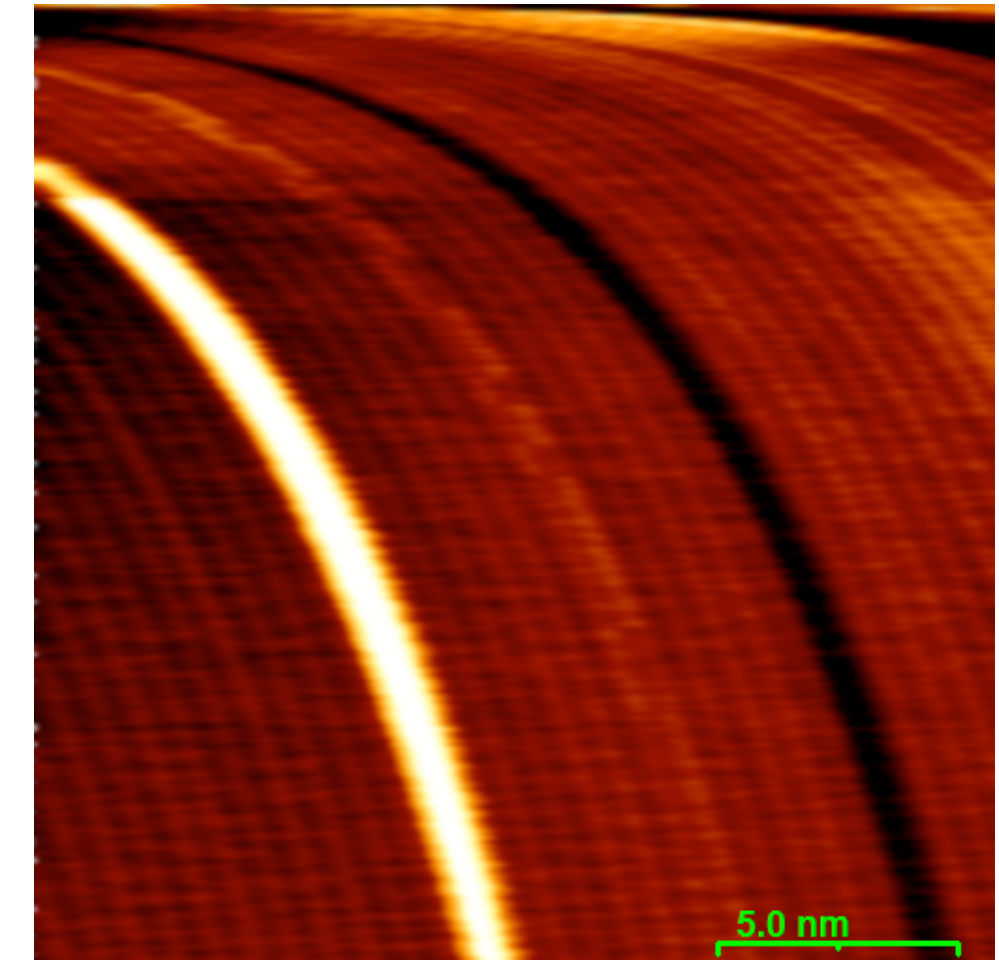


# Real-time Piezo Creep Correction

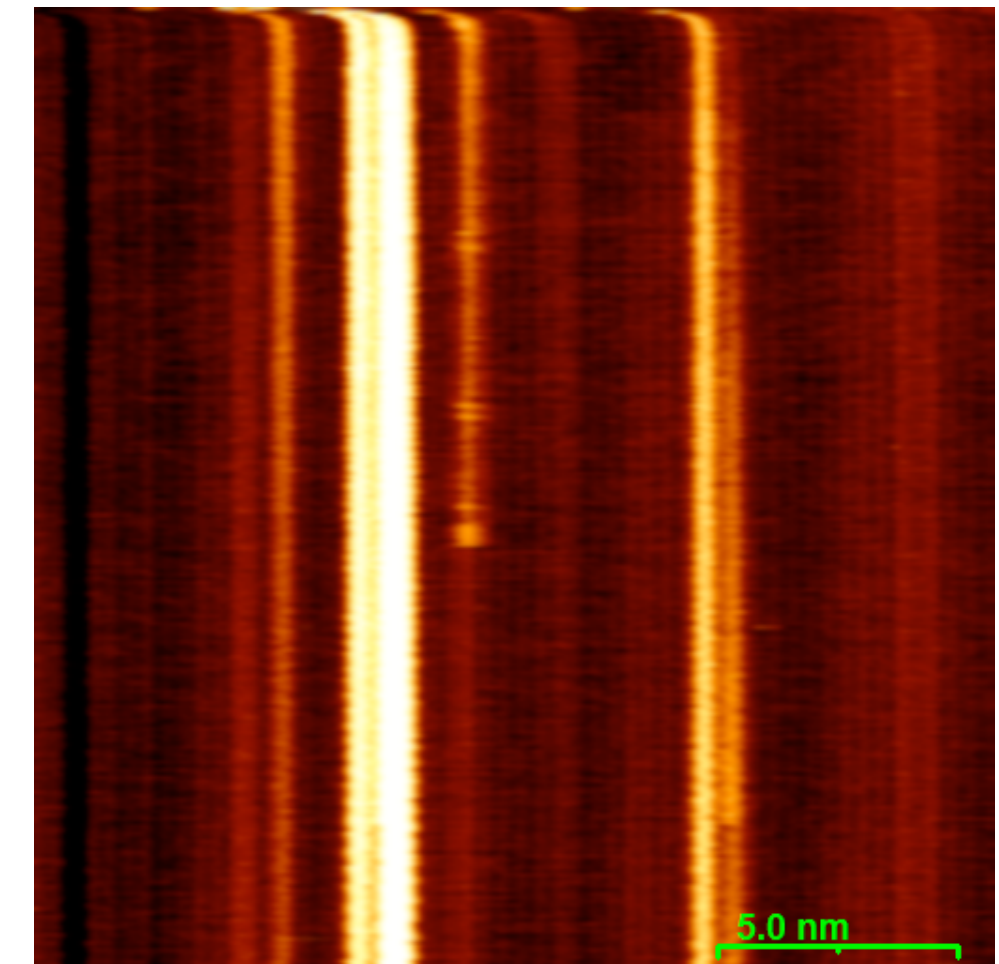


no creep correction

500 nm jump test.



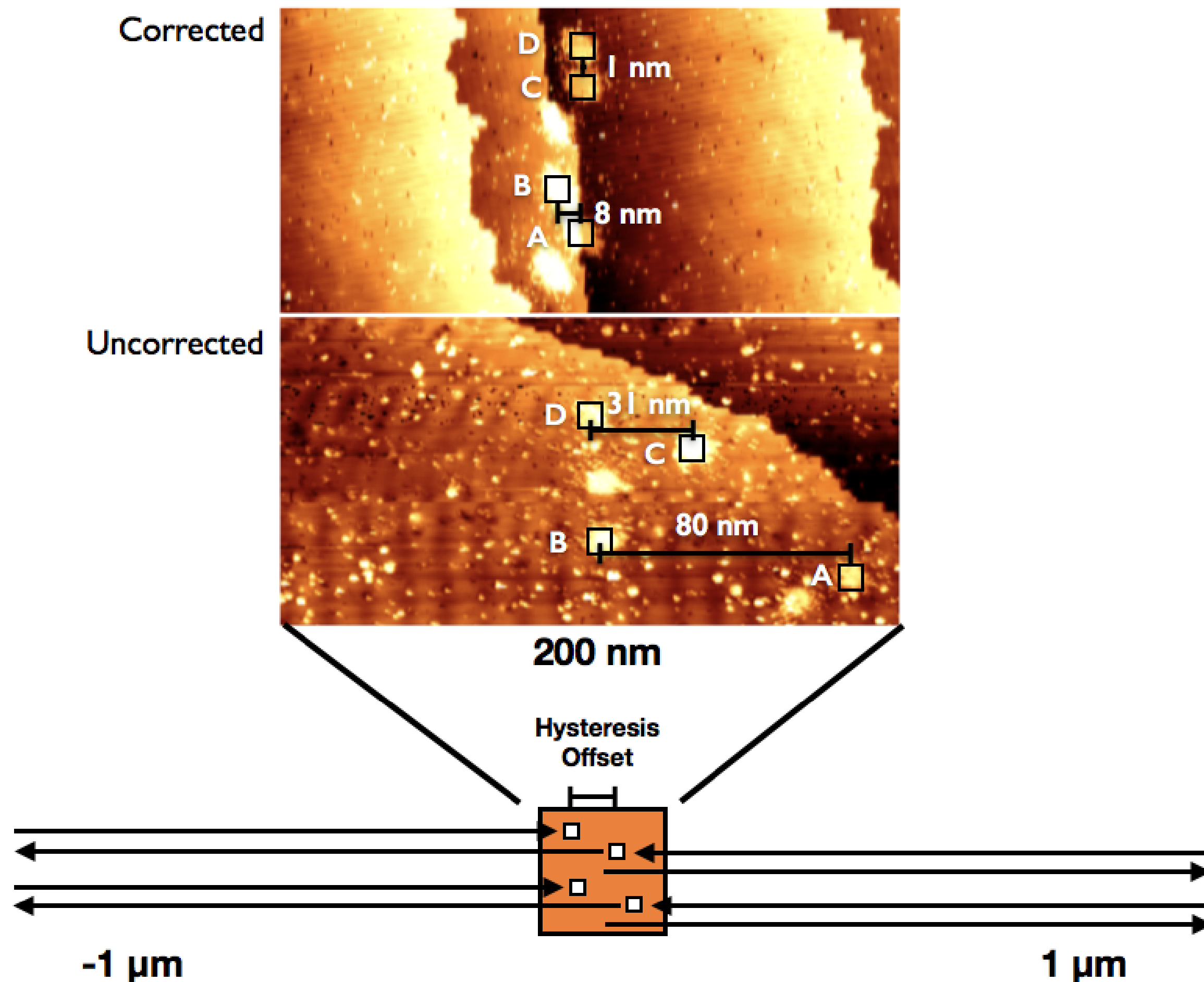
With creep correction



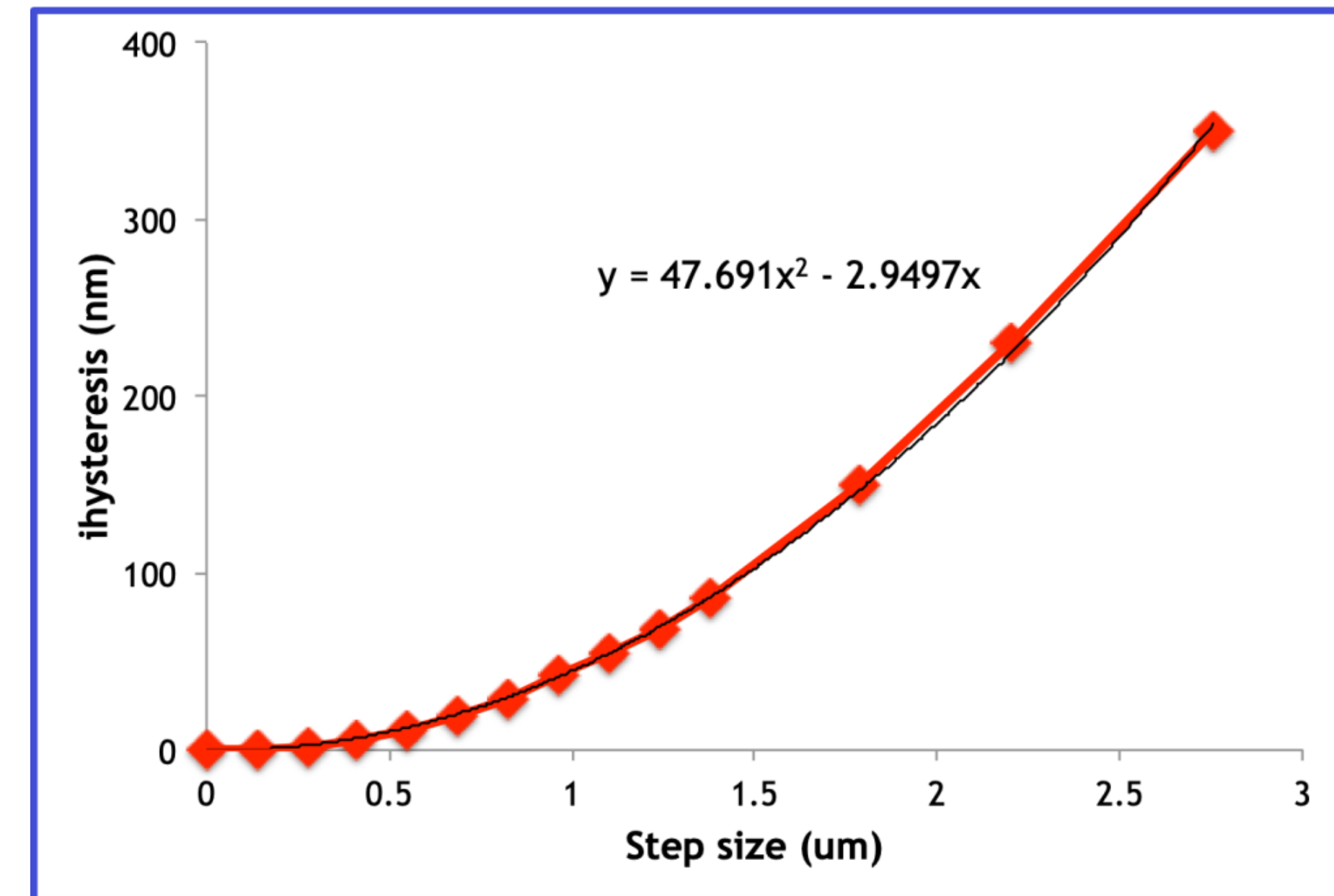
Creep is a linear, timevarying position error. We account for it by applying a voltage overshoot to compensate.



# Hysteresis jump tests



**Jump test to calibrate hysteresis correction.**



Hysteresis is a nontimevarying, quadratic position error.

However, hysteresis induces extra creep which is not completely corrected in our model.

For an uncorrected 1 μm jump, about 50 nm of the apparent error is creep.

Correction reduces the position error by about 90%; remaining error is close to zero after the creep has died away.

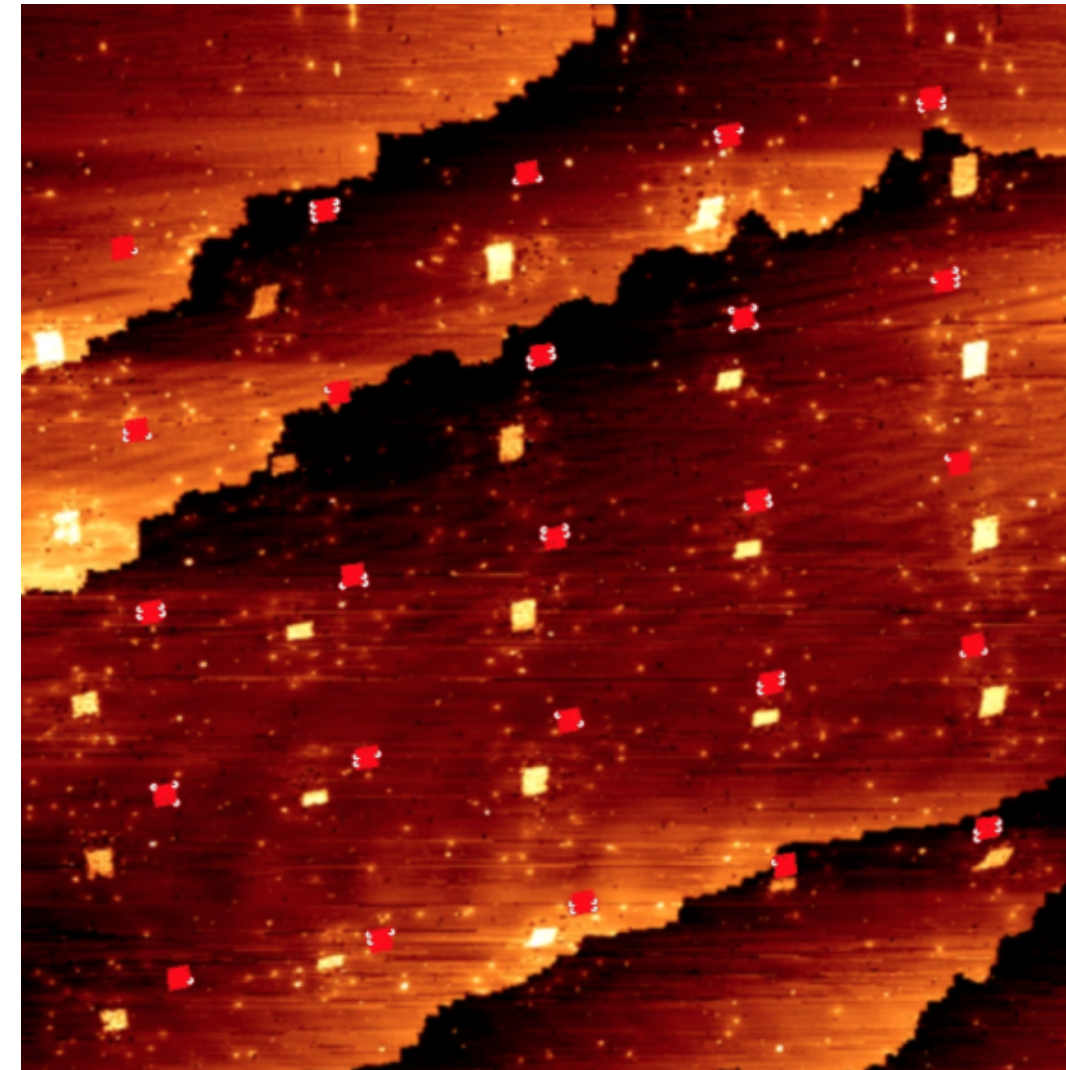


# Effect of Creep and Hysteresis Correction

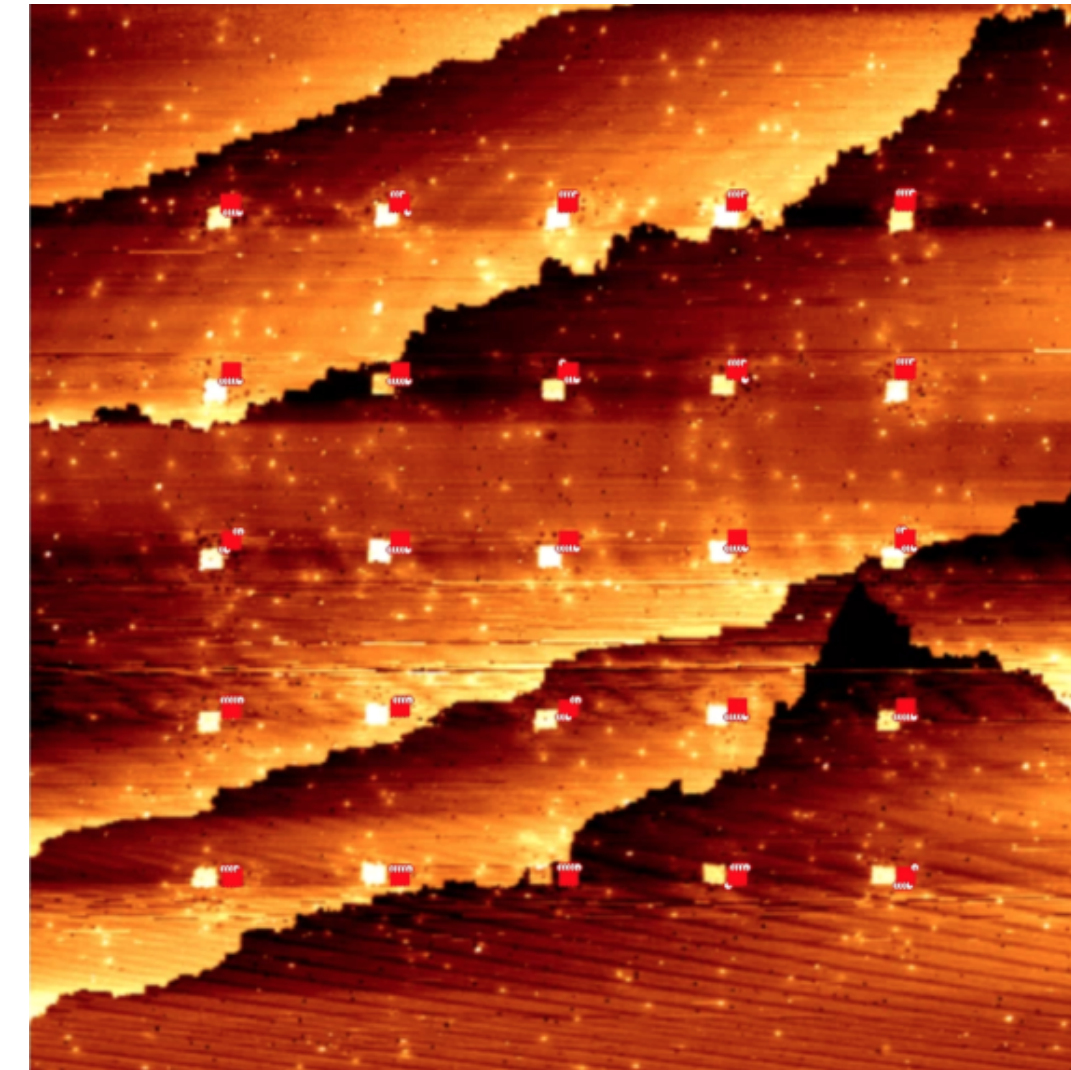
With no correction, the boxes' positions and shapes are both distorted.

**no HC**

**no CC**

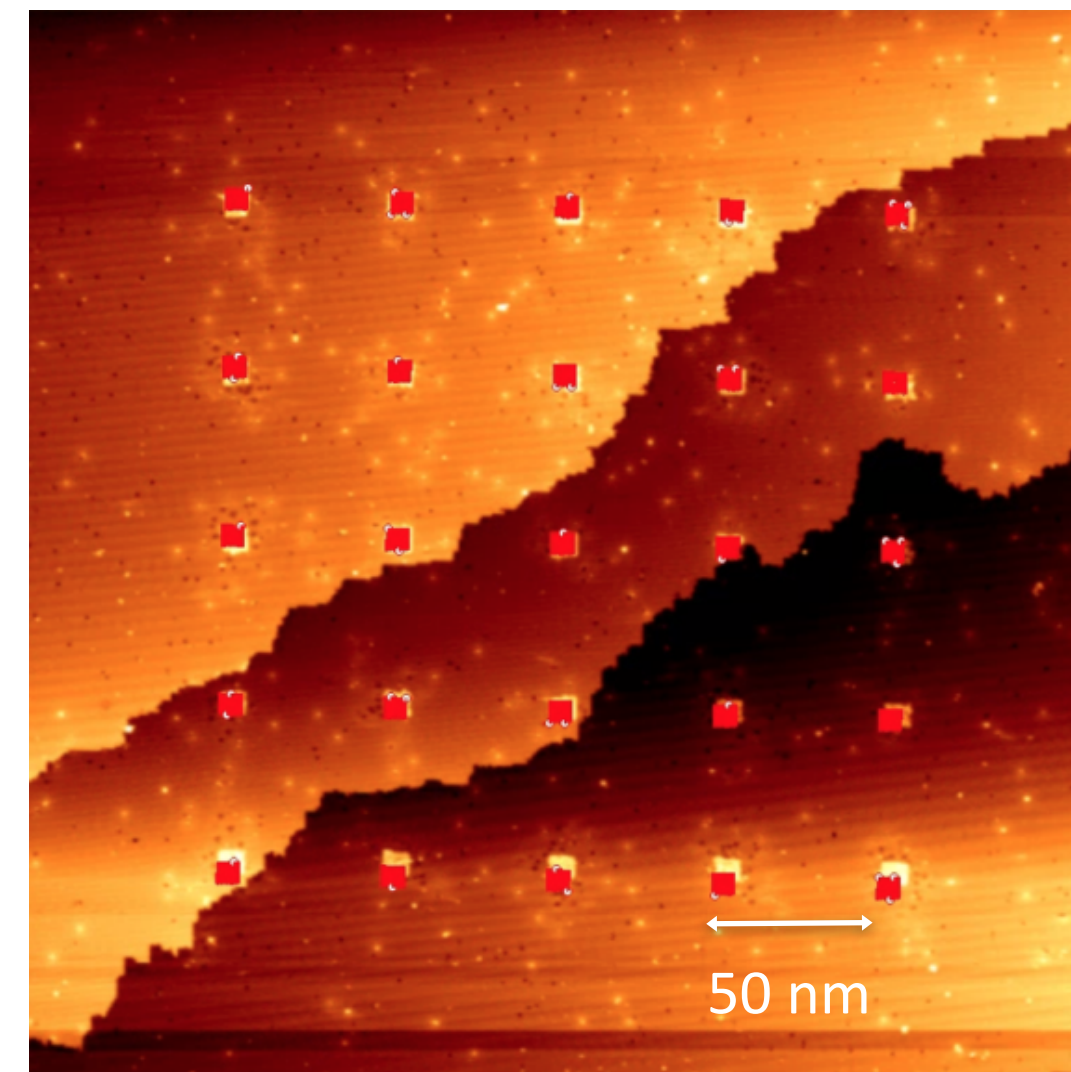
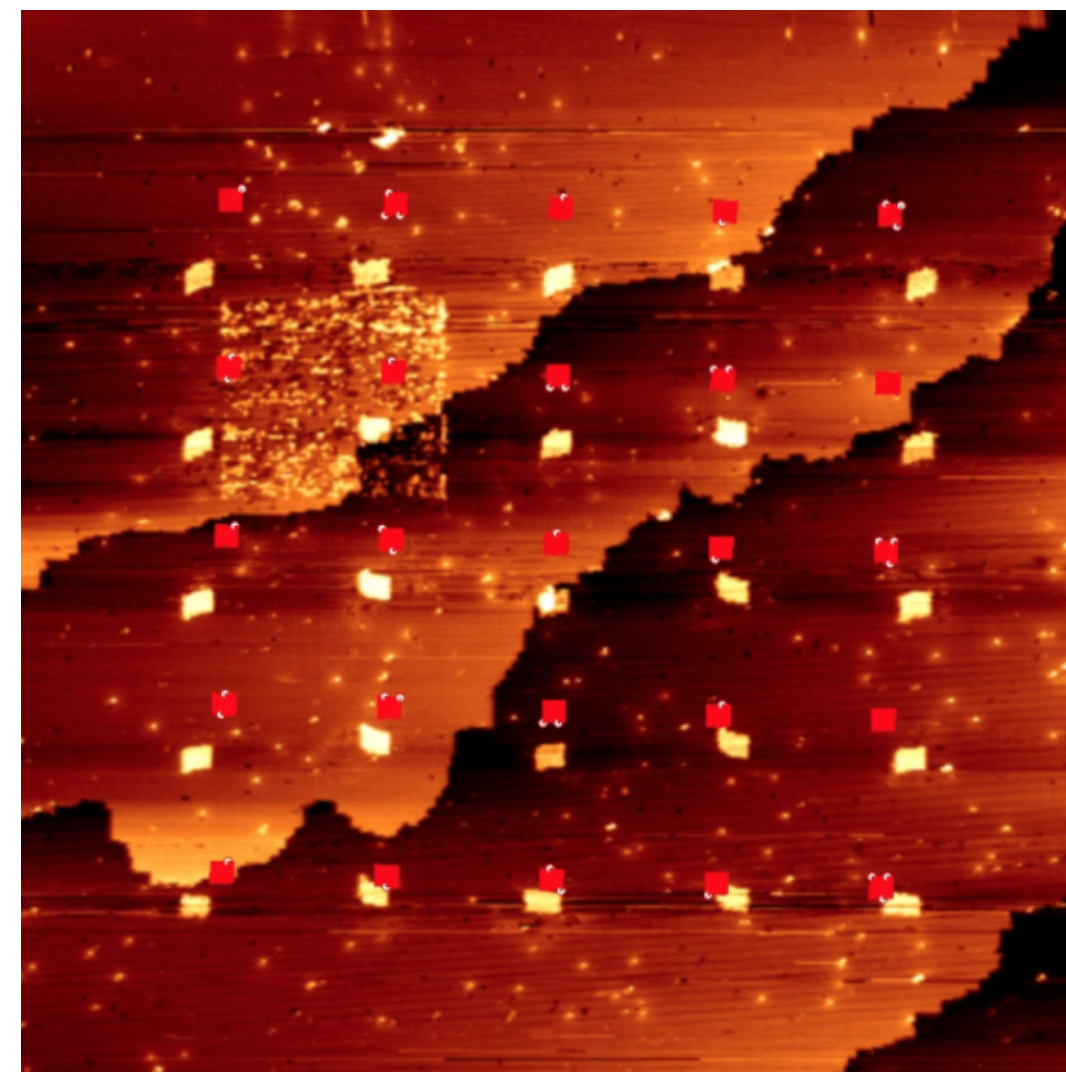


**CC : 10.2 %**



**CC = Creep Correction**  
**HC = Hysteresis Correction**

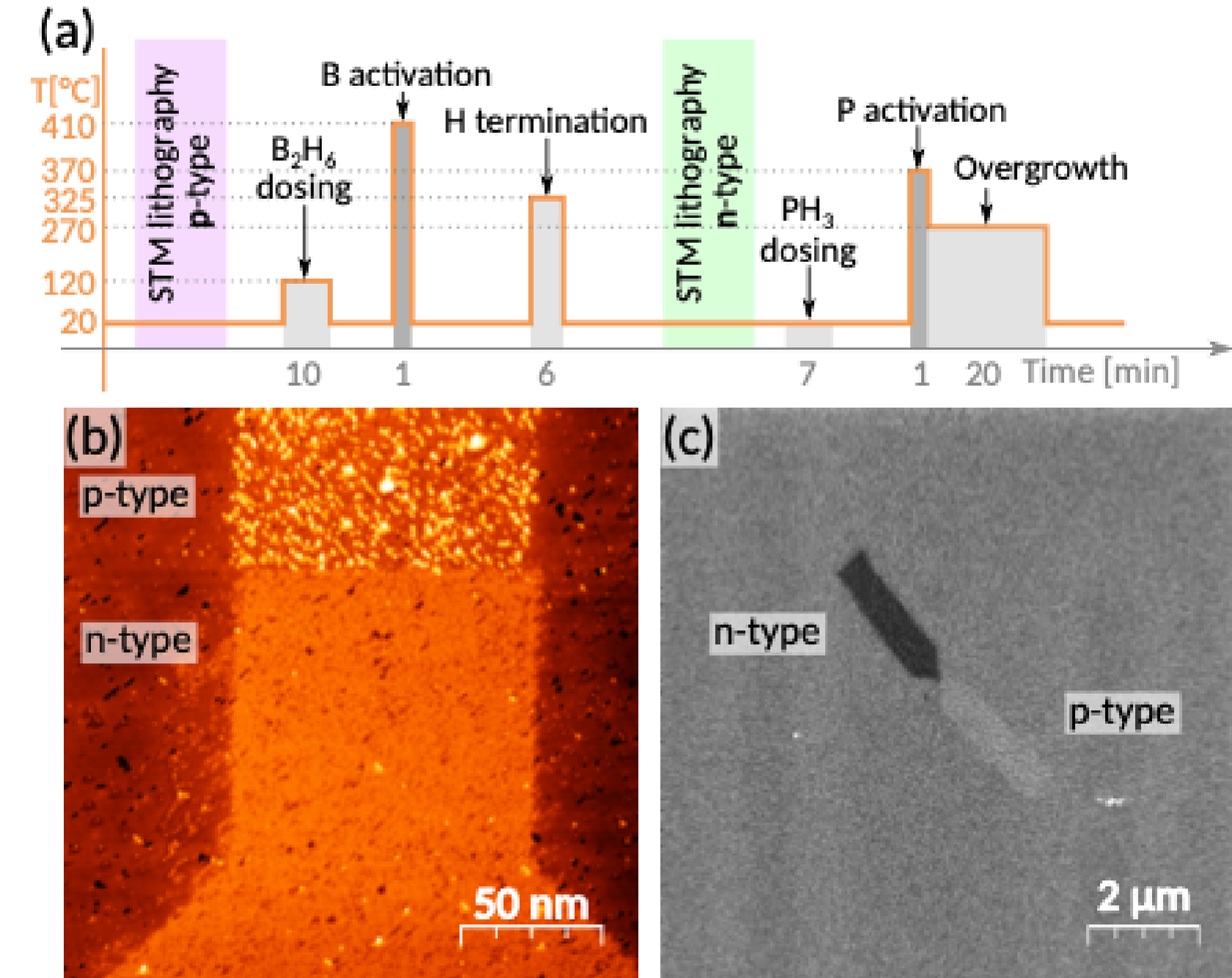
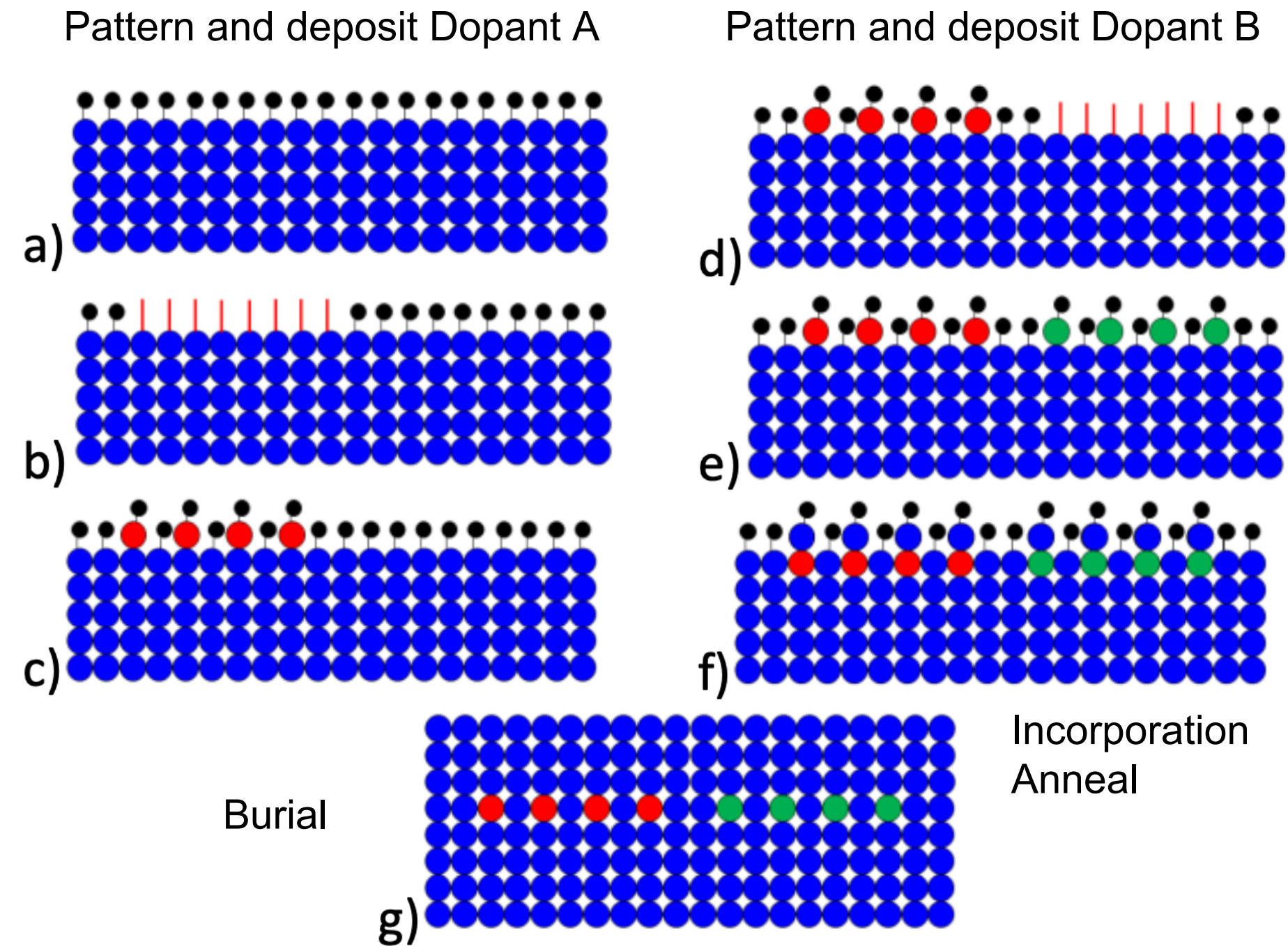
**HC: 12.4%**



With active Creep and Hysteresis correction, the boxes are almost perfectly placed.



# Bipolar devices



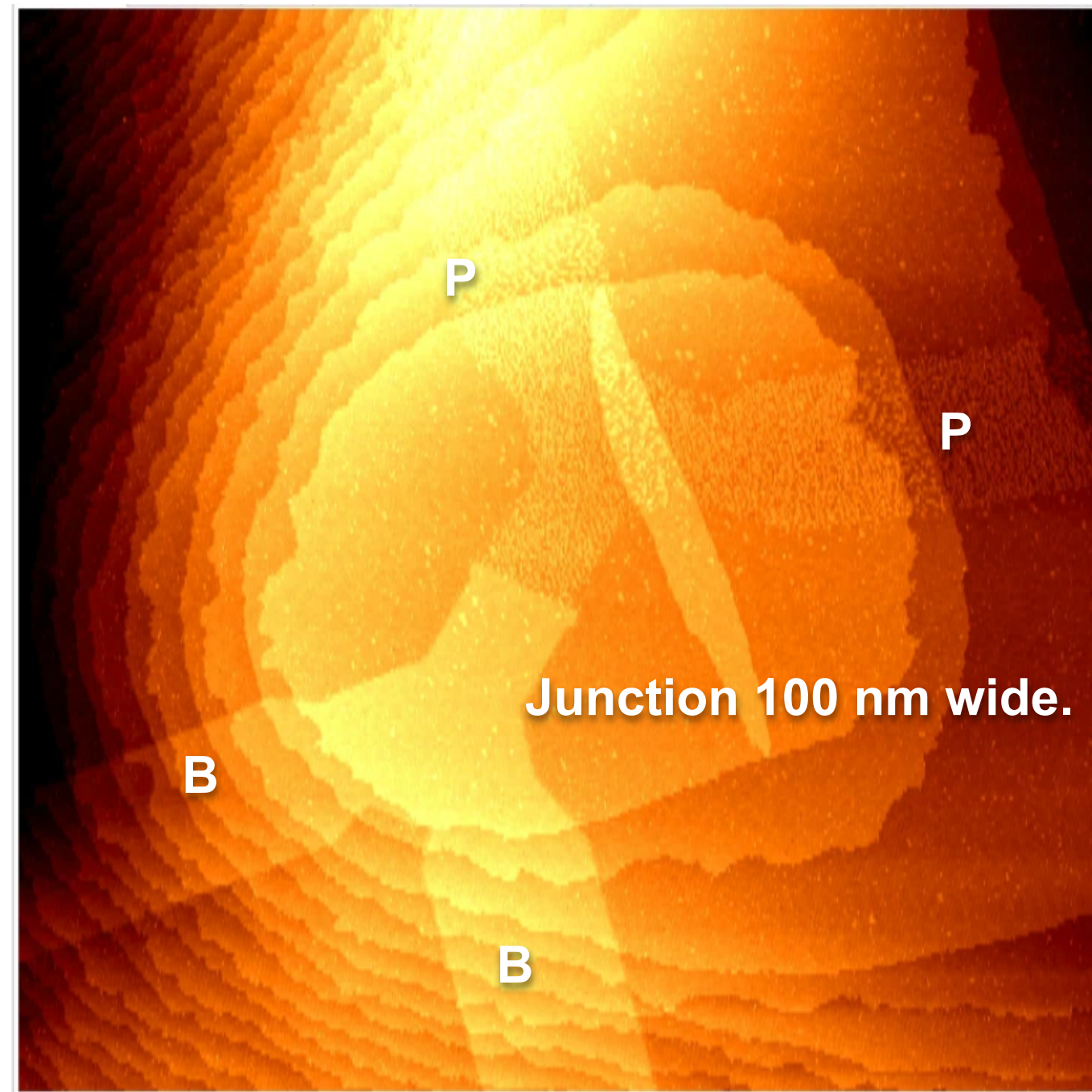
# “Bipolar device fabrication using a scanning tunnelling microscope”

T. Škerek, S.A. Köster, B. Douhard, C. Fleischmann, and A. Fuhrer, Nat. Electron. 1 (2020).

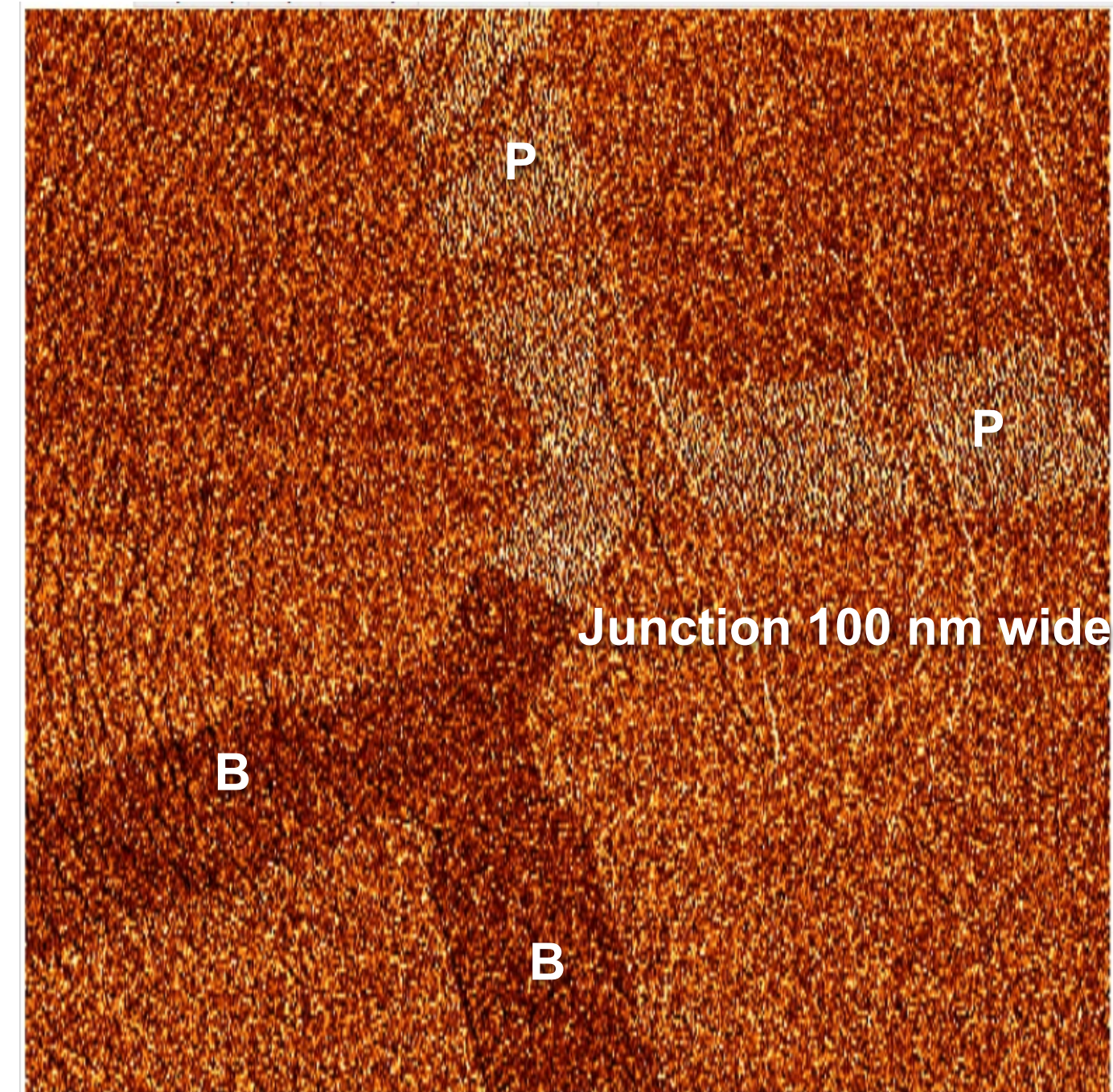
- In order to expand the range of applications of APAM technology, we need precursors for both donor and acceptor dopants.
- Here  $B_2H_6$  and  $PH_3$  were used to make a p-n junction, depositing B first and then P.
- We are using  $BCl_3$  for the p-type dopant precursor.



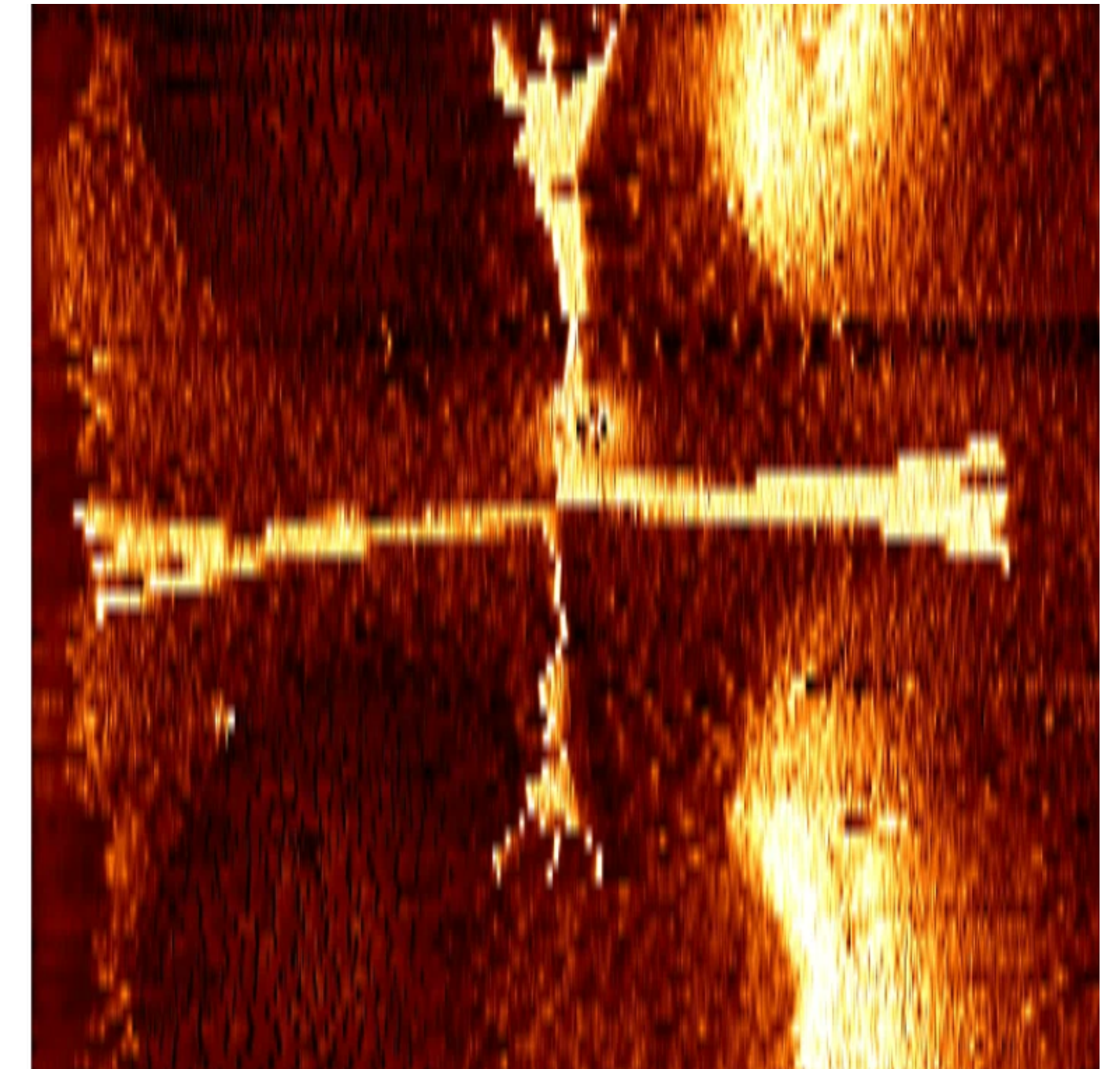
# Device Fabrication using Multipolar Imaging



**Topo**



**dI/dZ**

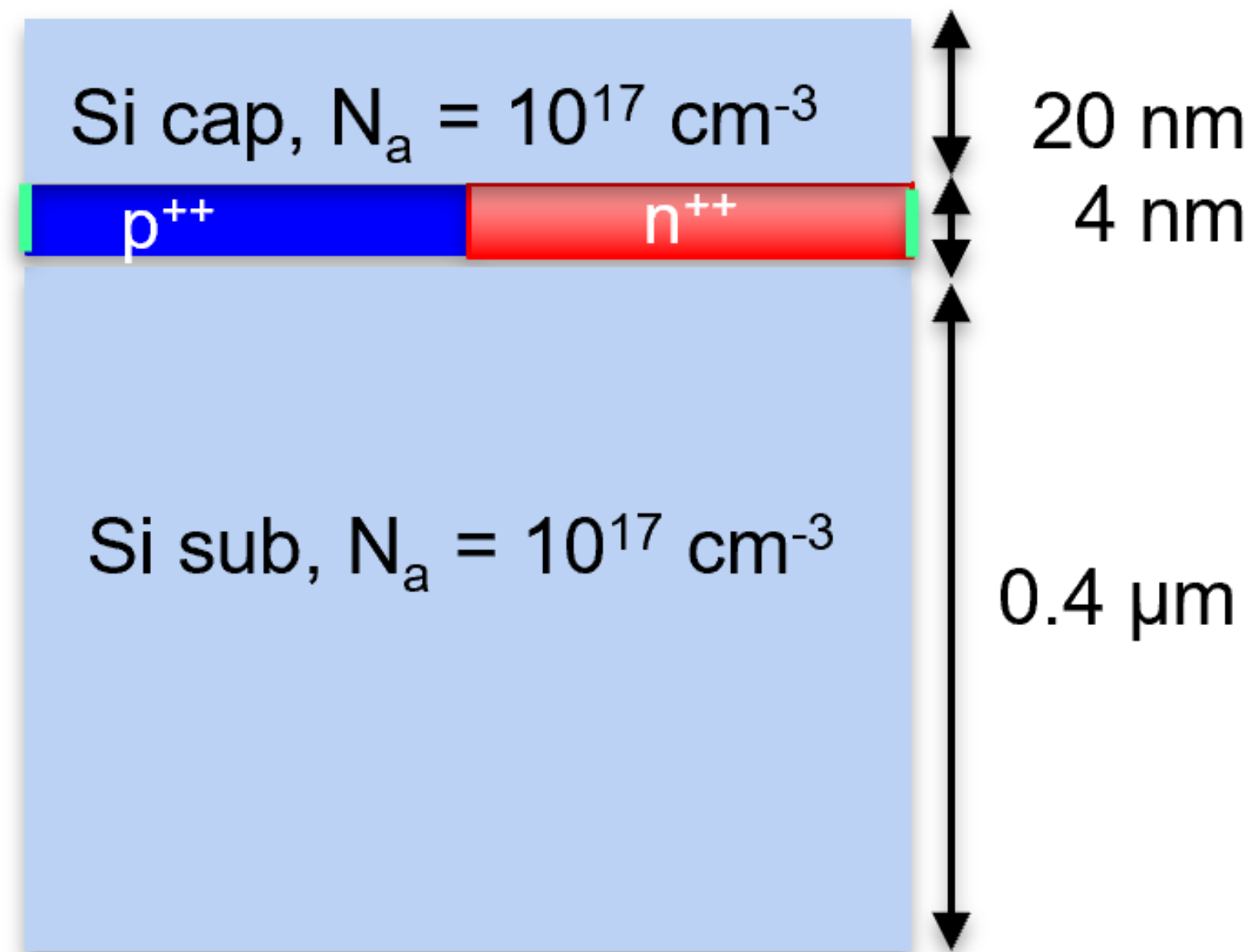


**dI/dV (after 20 nm epitaxy)**

- Trials of bipolar device patterning; alignment of B to P.
- dI/dZ imaging gives good contrast for surface features, such as patterns of bare Si, and surface dopant patches. Here, with dI/dZ imaging, the contrast of the B patch is much clearer, and the pattern for the P electrode can be aligned to the existing B patch with dimer row resolution.
- dI/dV imaging allows buried devices to be imaged, to confirm their presence after the overgrowth process.



# Simulation-Experiment Comparison for p-n delta layers

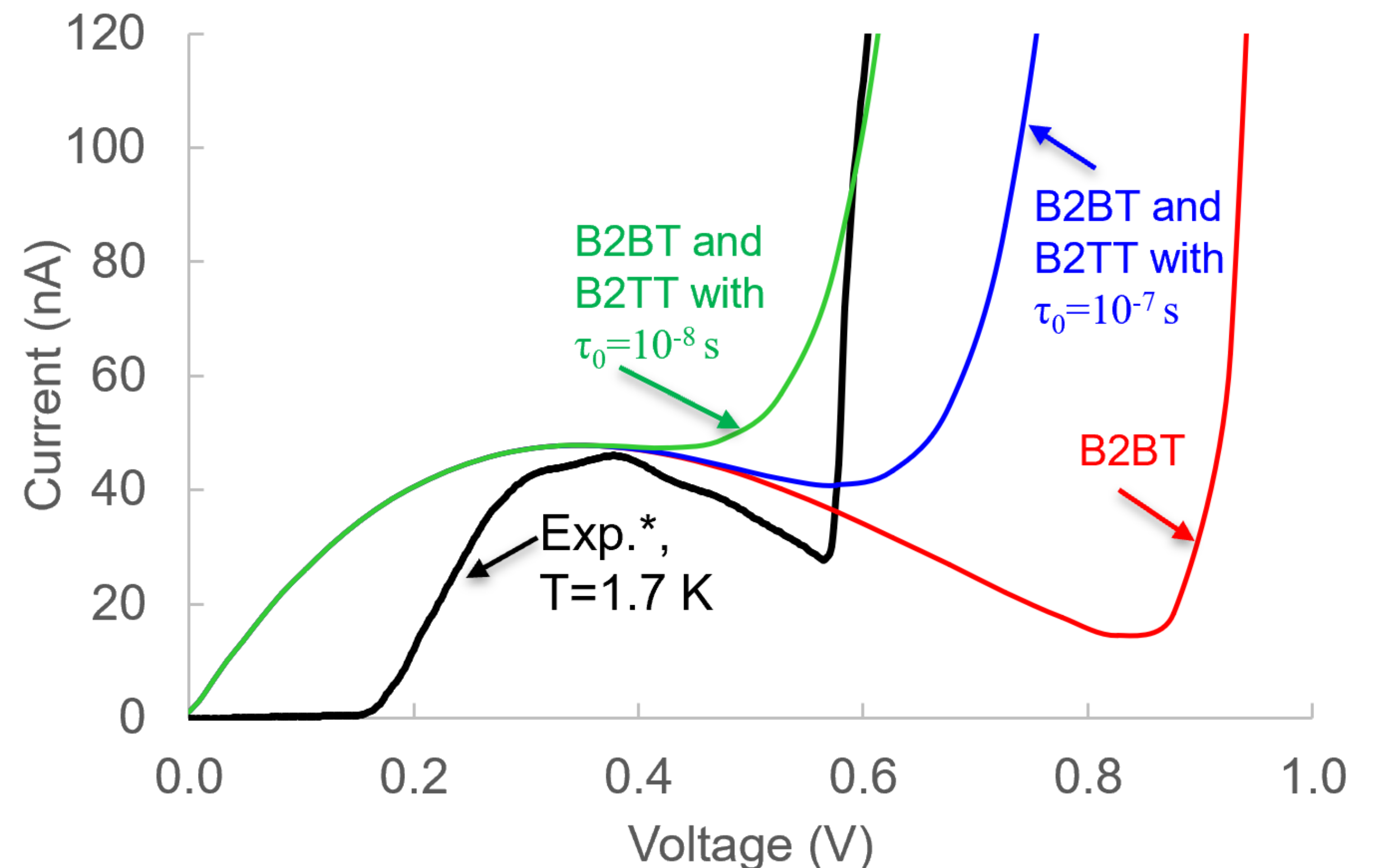


Simulations were done using Charon, an open-source TCAD code developed at Sandia National Labs.



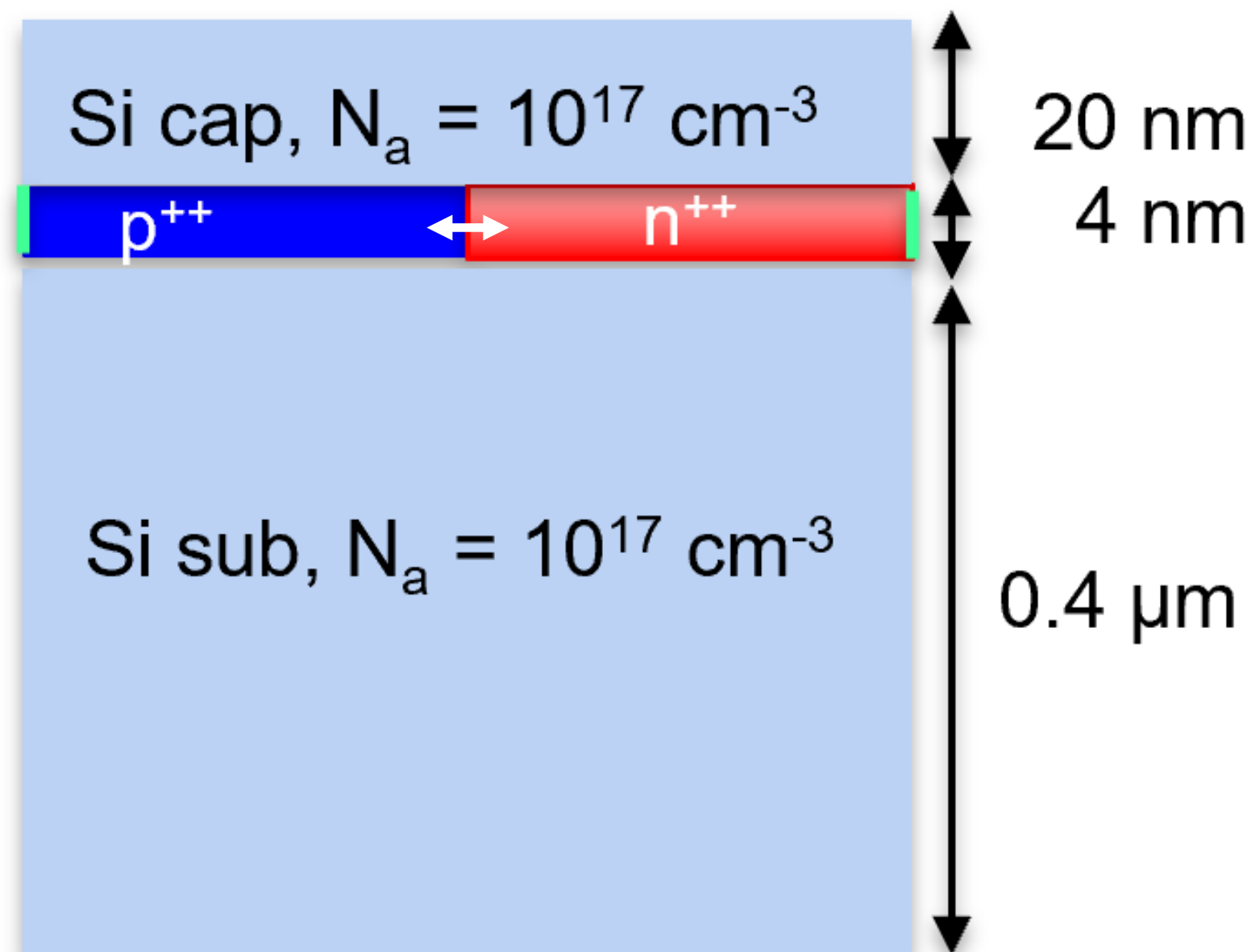
B2BT = Band-to-band tunneling  
B2TT = Band-to-trap tunneling

**With B2BT and B2TT, simulation results are in decent agreement with the experimental data except for voltages less than 0.2 Volts.**



\* T. Škerek et al. Nat. Electron., vol. 3, pp. 524–530, 2020.

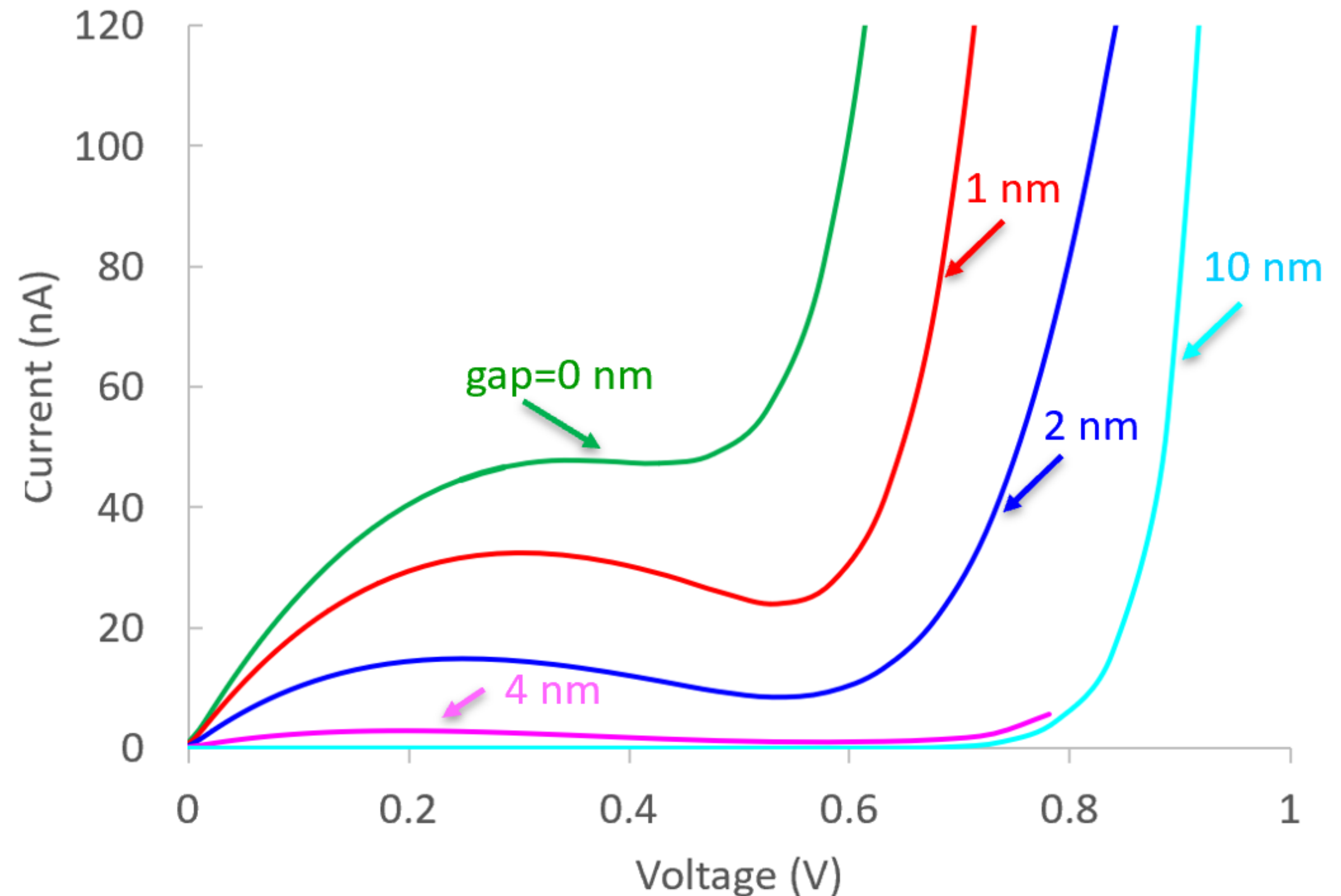
# Simulated I-V dependence on p-i-n gap width



The distance between the two delta layers is varied.

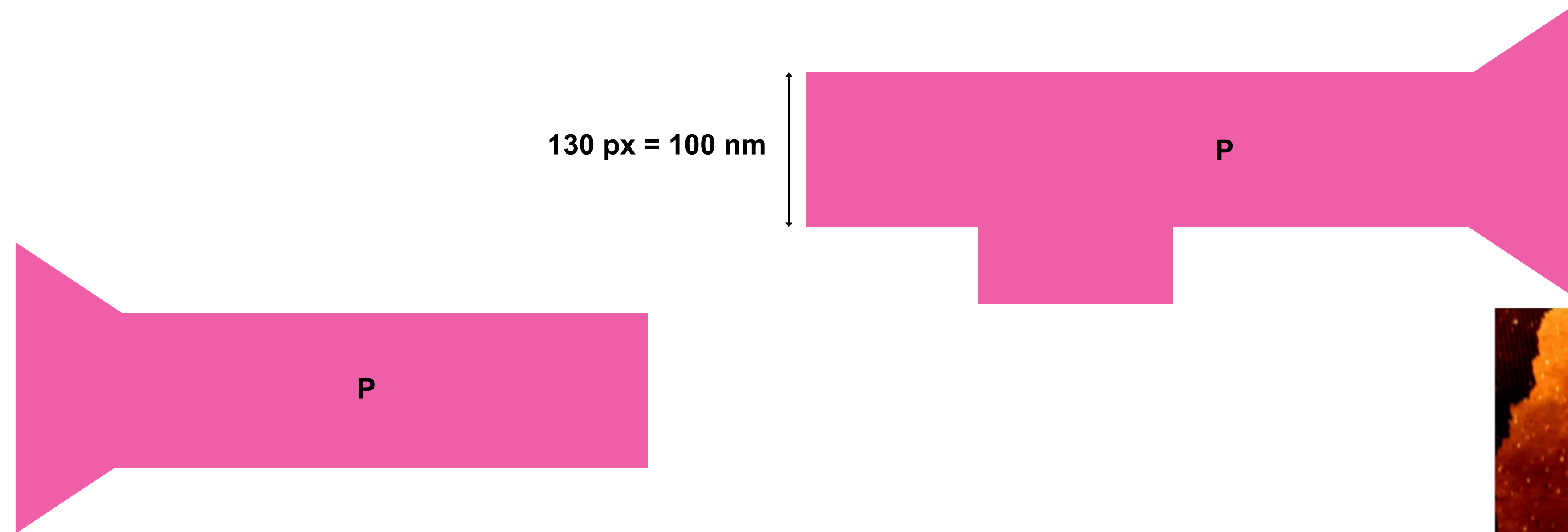
**When the gap is 4 nm or bigger, the negative differential conductance (NDC) behavior is diminished.**

**We are exploring this experimentally.**

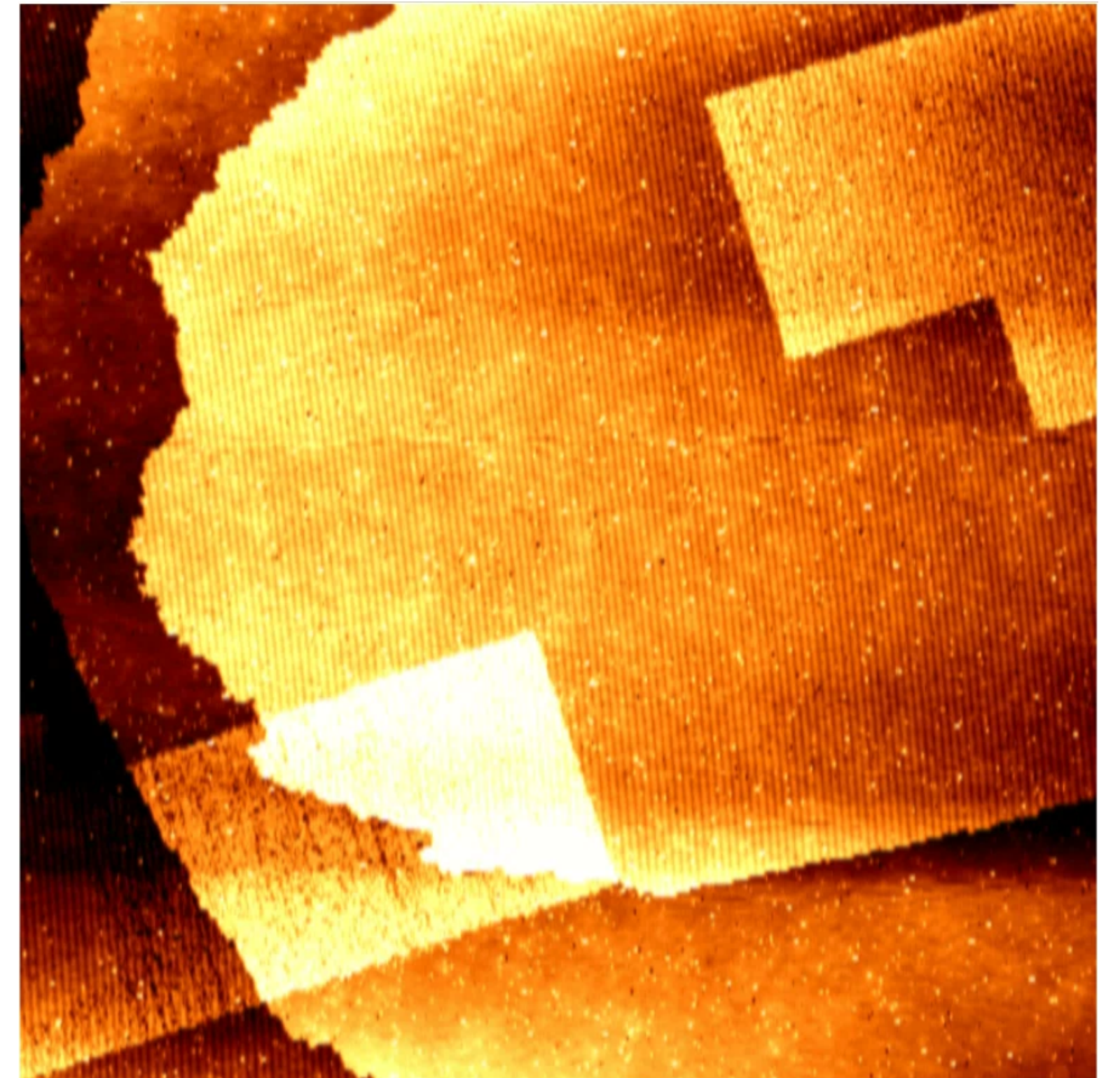




# Fabrication of devices with variable gap widths

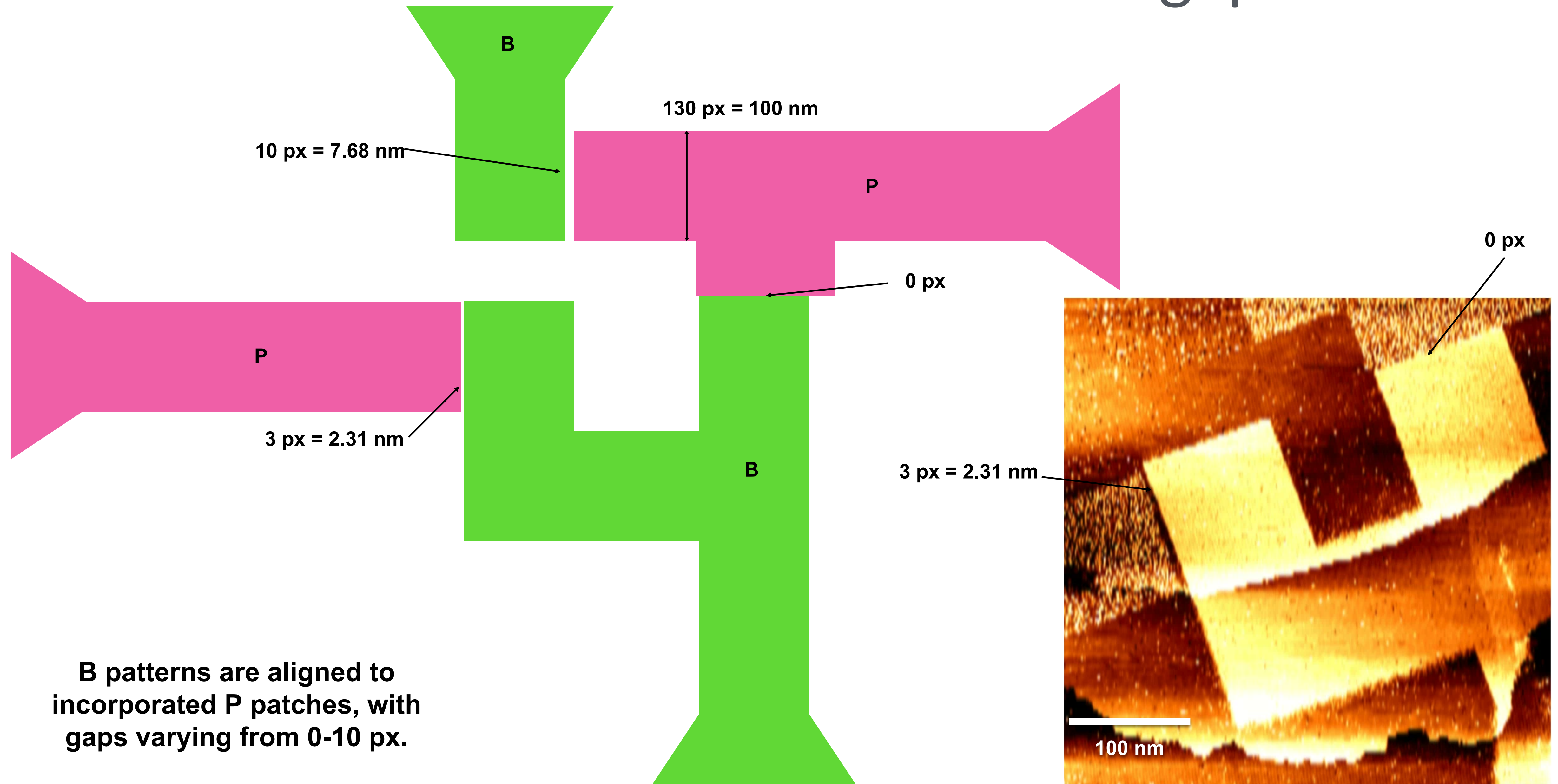


**P patterns are drawn first, and saturated with P using  $\text{PH}_3$ .**





# Fabrication of devices with variable gap widths





# Conclusions

- We are developing automated, atomically precise, STM Lithography.
- Patterns can be drawn from the single-pixel scale, up to the limit of the STM scanner.
- Creep, hysteresis and thermal drift are all causes of STM position errors. These are corrected in real-time in our controller to achieve near-perfect positioning.
- For bipolar devices, the n-type patterns are written first, dosed with  $\text{PH}_3$ , and the P incorporated. The p-type patterns are aligned to the P patches to provide atomic-precision gaps between p and n electrodes.
- $\text{dI/dZ}$  and  $\text{dI/dV}$  imaging simultaneous with topographic imaging provide extra electronic contrast of patterns and incorporated dopants, to make alignment of patterns easier.
- p-i-n junction device simulations indicate that the device behaviour is strongly dependent upon the gap width. A set of junctions of varying width (0,3,10 pixel) have been fabricated to test this prediction.
- The next step will be to measure the electrical properties of these devices, compare to the modelling, and iteratively refine the incorporation and burial processes to improve the properties.