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SAND2022-XXXX C

High-Voltage Polymer Multi-Layer Capacitor Development, Characterization, Environmental Testing



Presented By:

Alex Robinson, Joshua Dye

(505) 844-9520, arobins@sandia.gov

(505) 844-8627, josdye@sandia.gov





Compelling Long-Term Gaps, Needs, and Challenges

Needs:

Higher energy density firing systems for challenging environments

High-energy-density (HED) capacitor robust to wide-ranging environments.

Potential replacement for multi-layer ceramic capacitors (MLCC)

Approach:

Design high-voltage HED polymer multi-layer (PML) capacitors as replacements with potentially smaller footprint

Challenges:

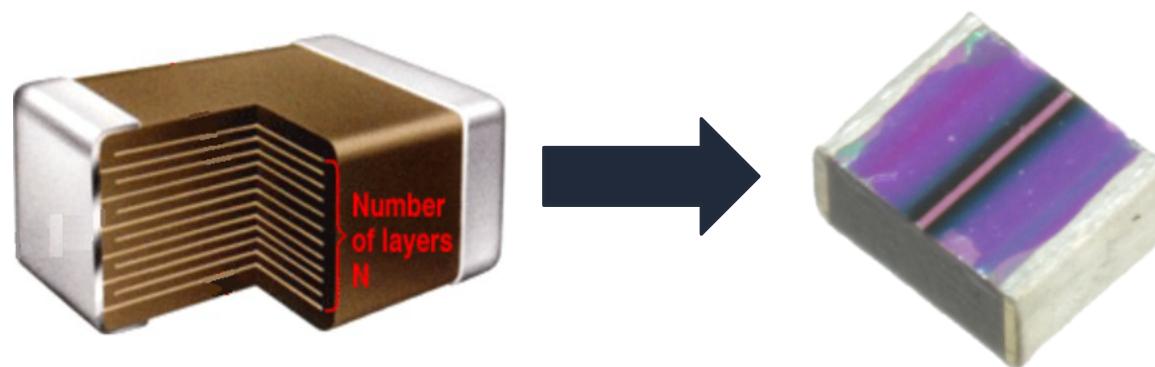
A drop-in PML replacement does not exist

High voltage PML capacitors are new

Next level - higher energy density dielectrics may reduce size with an acceptable trade-off of service lifetime.

Polymer Multi-Layer (PML) capacitors display advantageous characteristics worth pursuing

- High energy density
- Lightweight
- Robust
 - Self-healing
- Stable
 - Temperature
 - Voltage
 - Chemical
 - Humidity



$$C = \epsilon_0 \epsilon_r \frac{A}{d} N$$

C = capacitance

ϵ_0 = permittivity of a vacuum

ϵ_r = relative permittivity of dielectric

A = electrode square area

d = distance between each electrode

N = number of dielectric layers



Capacitor Construction

Internal serialization to achieve desired voltage rating

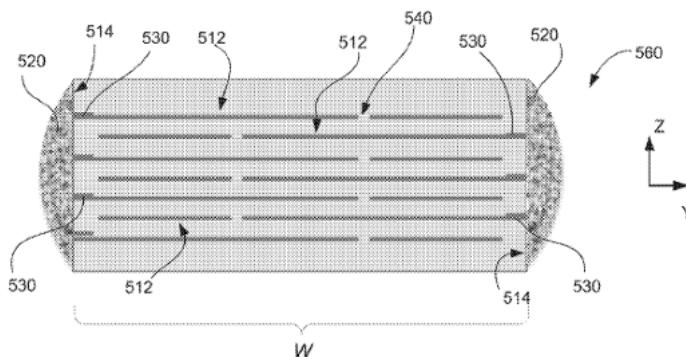


FIG. 5D



- An understanding of the physics guides the design to minimize energy dissipation (i.e. damage) during clearing events (better survivability)

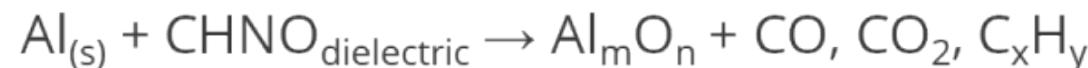
$$E_{\text{clearing}} \propto t^2 V^4 f(p)$$

t = metallization thickness (minimize)

V = voltage across dielectric (minimize)

$f(p)$ = inverse function of interlayer pressure

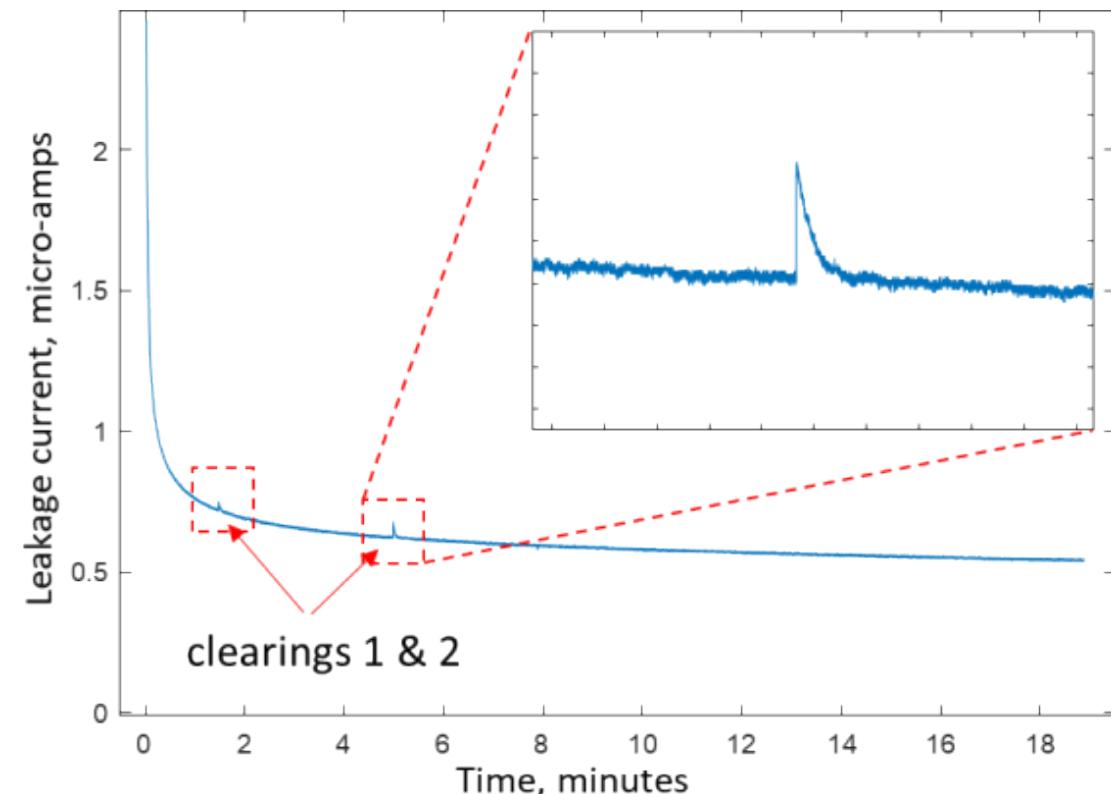
- Balancing the material composition facilitates defect clearing



- A Yializis “Metallized Capacitors” chapter in the *Handbook of Solid state Batteries & Capacitors*, edited by [M. Zafar A. Munshi](#) (1995).
- A Yializis, “Polymeric Monolithic Capacitor,” US Patent 10,102,974, (2018)
- NanoLam® technology



Clearing Capability



- Clearing events are difficult to detect. Voltage does not sag during a clearing.
- ΔC from a clearing is undetectable, but accumulates with progressive clearing events
- Three clearings captured over cumulative 6 hours of charge time on two units up to 130% rated voltage.

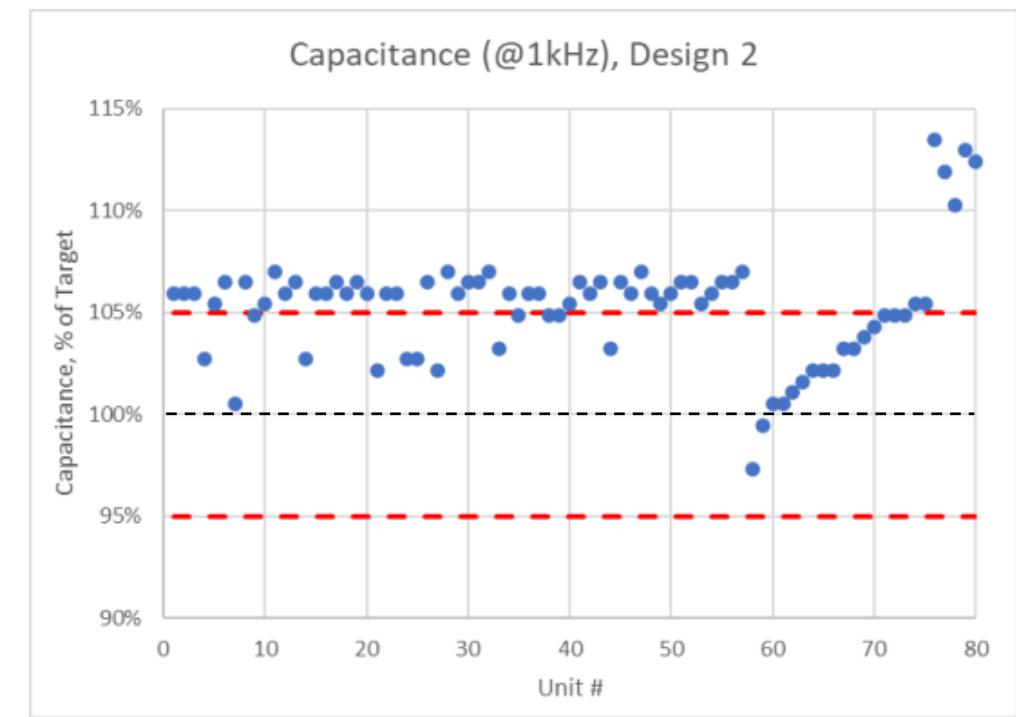
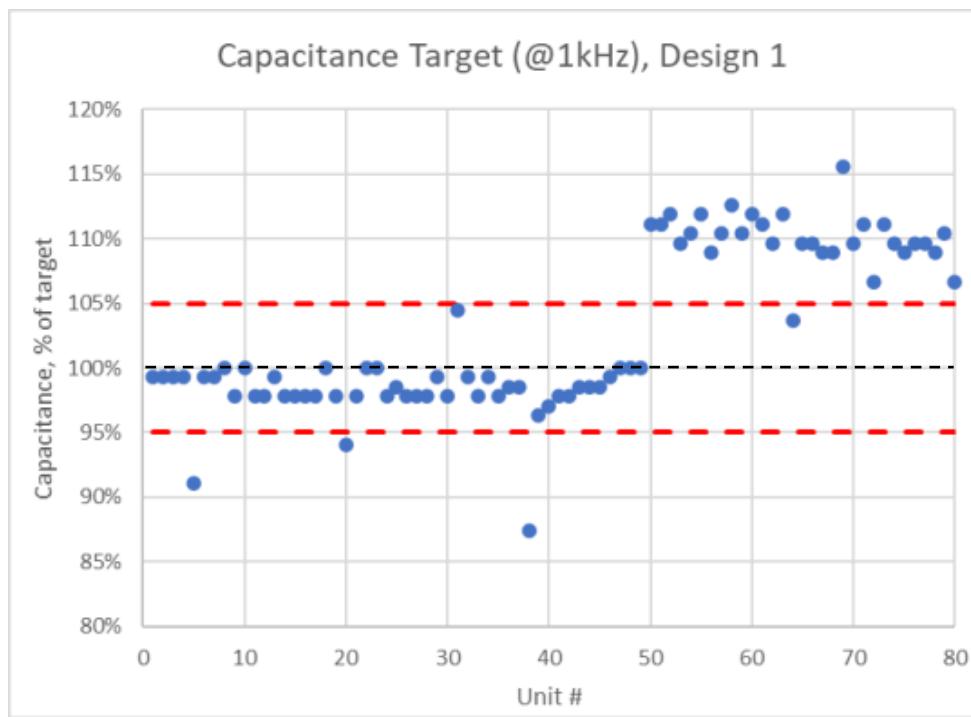
Clearing #1: ~100 mW
Clearing #2: ~290 mW



Baseline Characterization

Baseline characterization

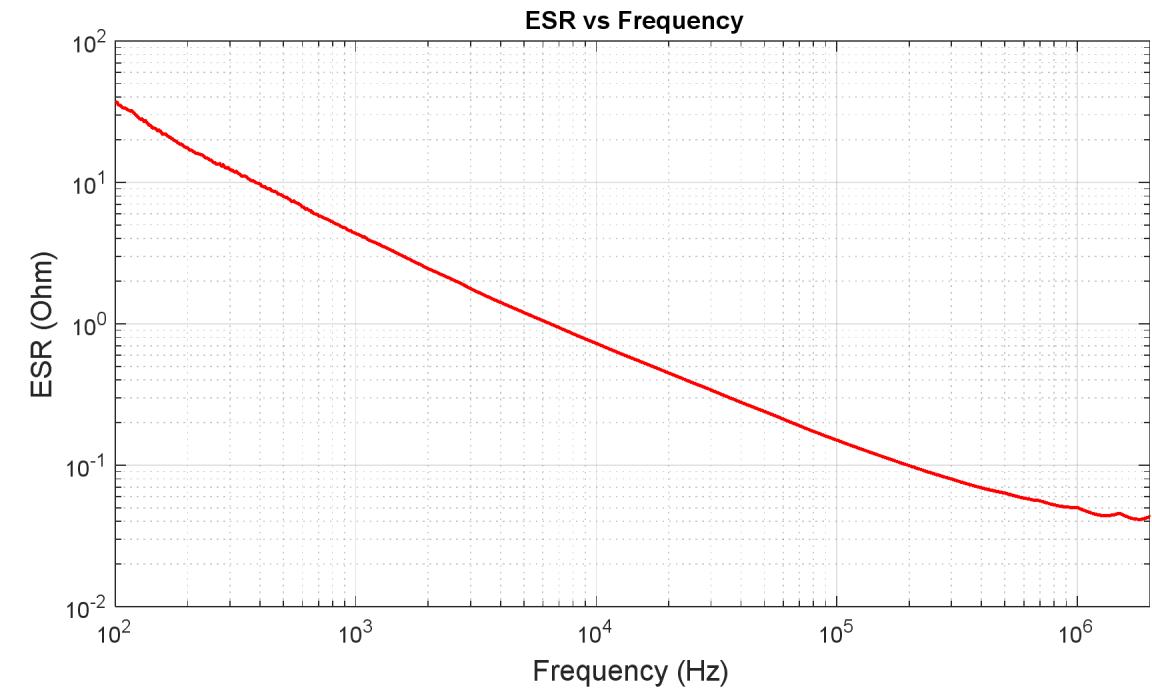
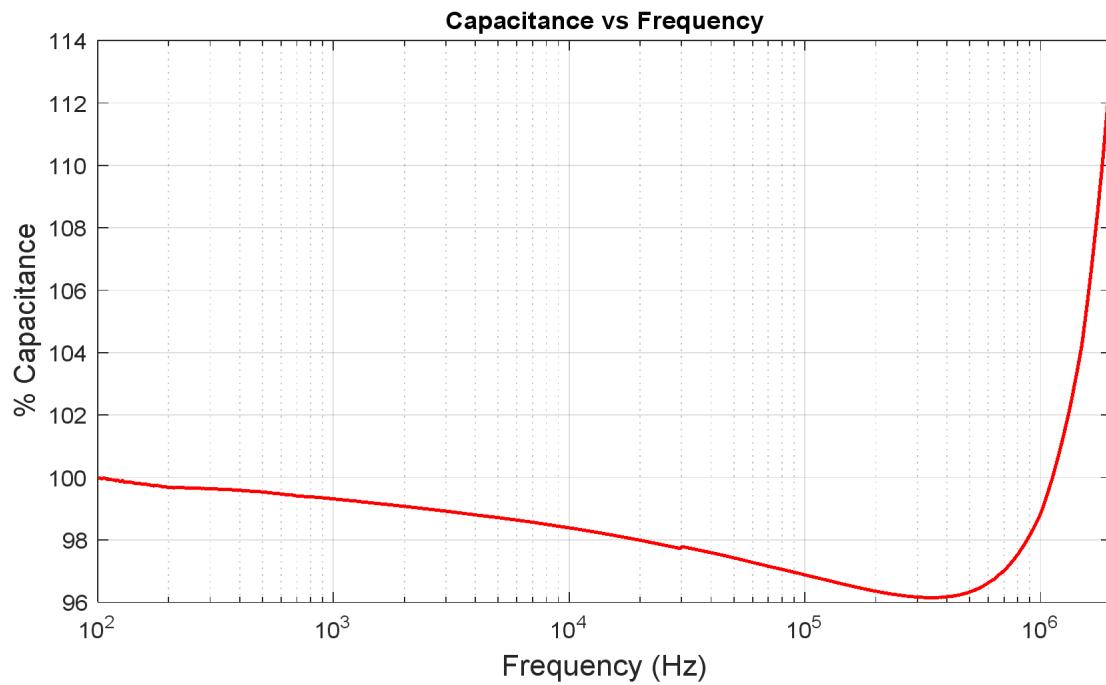
- Capacitance not easy to dial in for small batches, but good consistency within groups
- All but 5 units of Design 11 would be within $\pm 10\%$ of target. Some capacitors spec'd at $\pm 20\%$



Low Voltage Characterization

Low Voltage Characterization

- Capacitance higher than expected
- Dissipation factor: 0.6% (typical)
- Impedance: 25-40 mΩ @ 2.5 MHz (nominal discharge frequency)

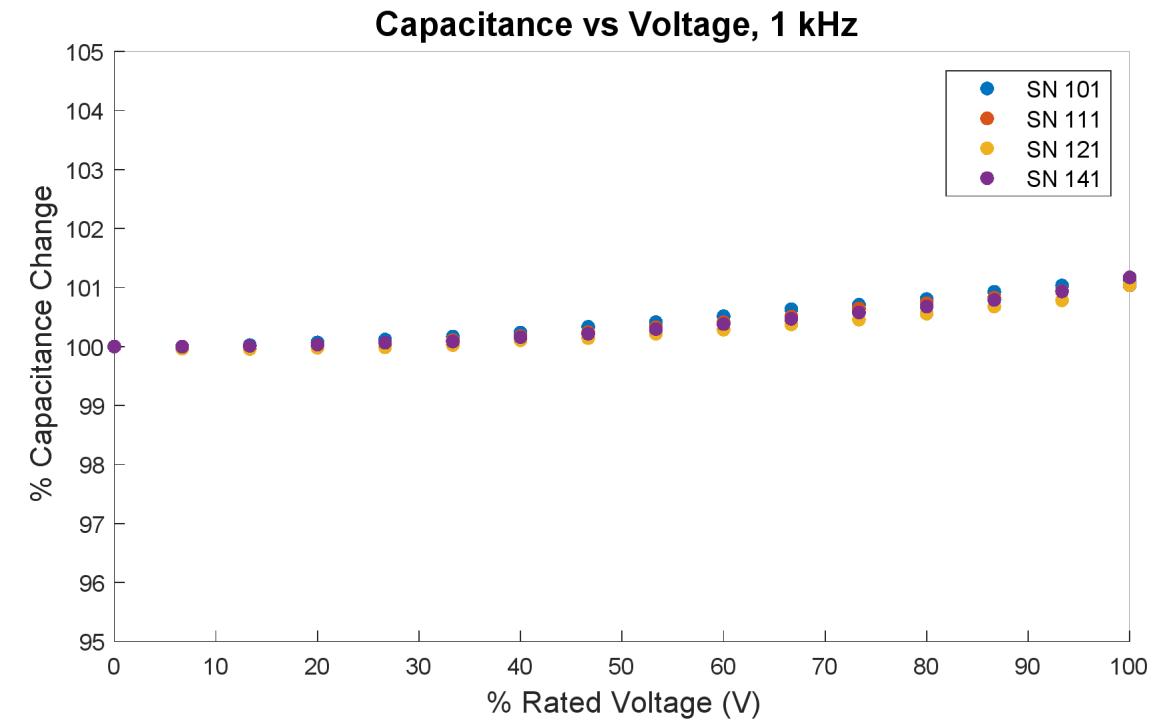
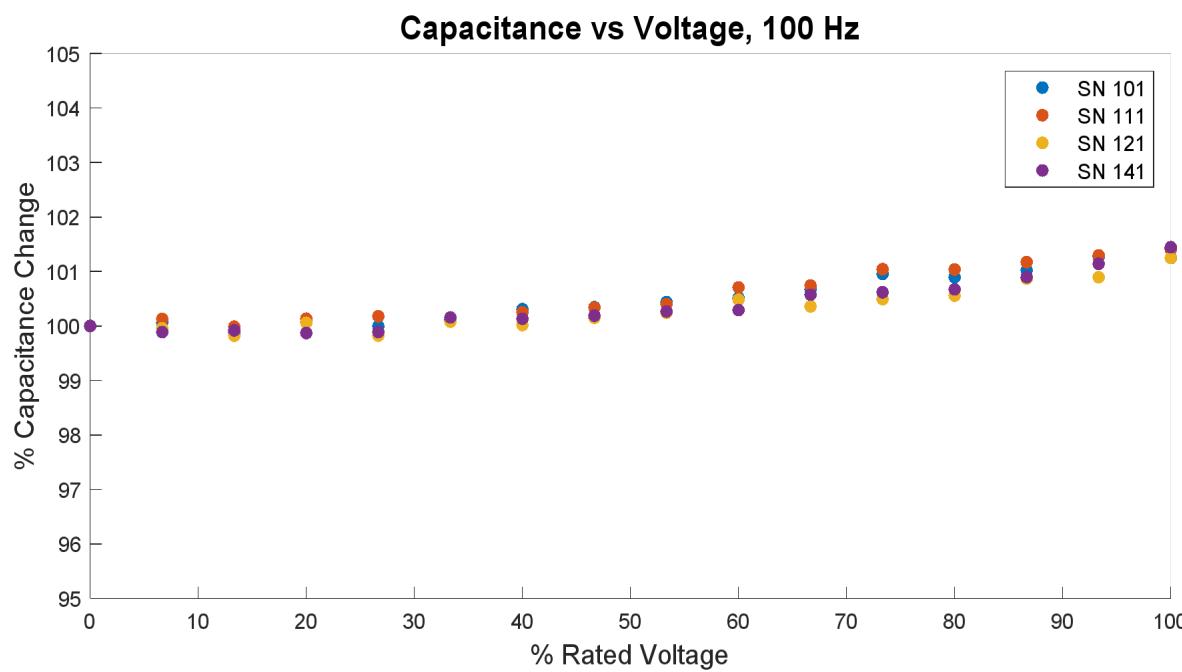




Capacitance vs Voltage

PML capacitors very stable across voltage

- < 2% variation through rated voltage

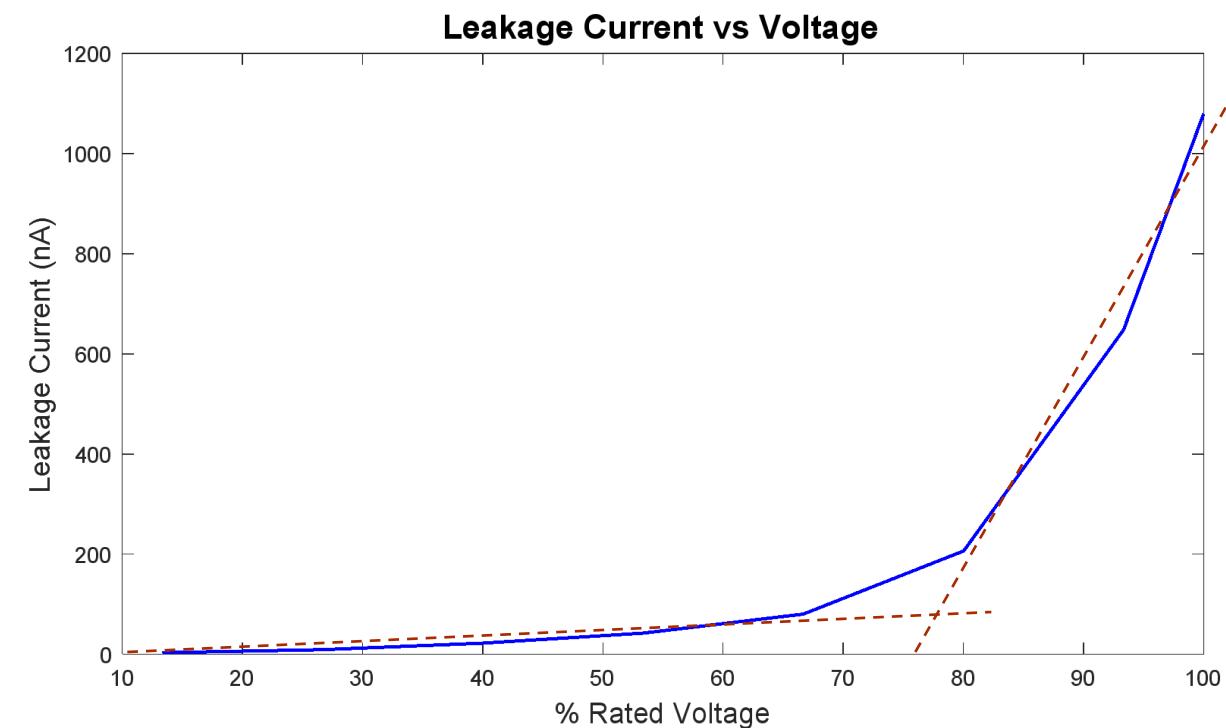
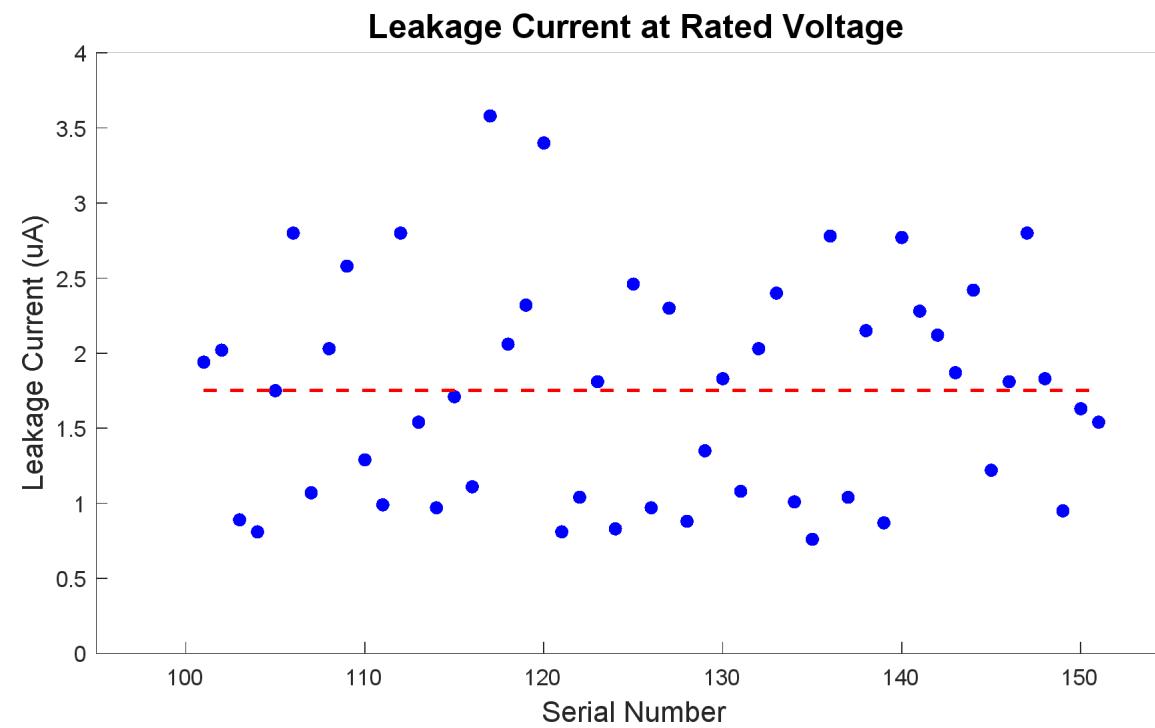




Leakage Current

Leakage current at high voltage

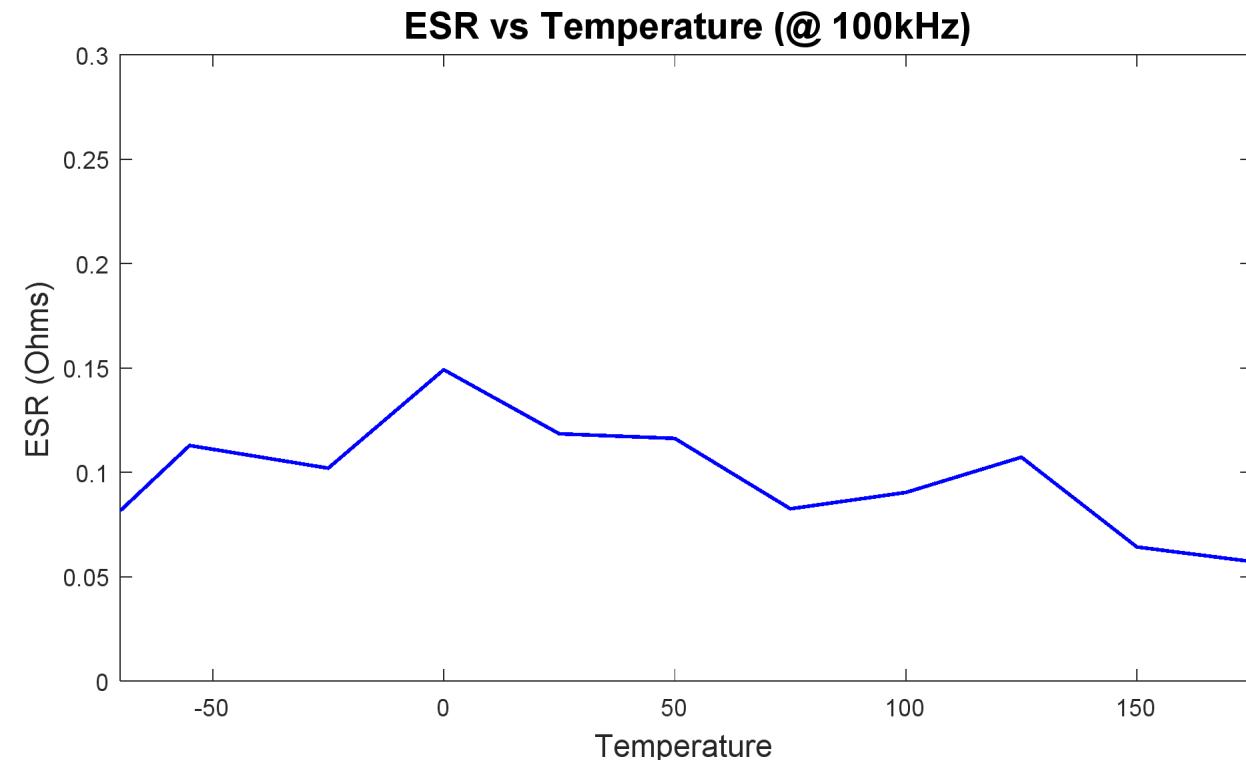
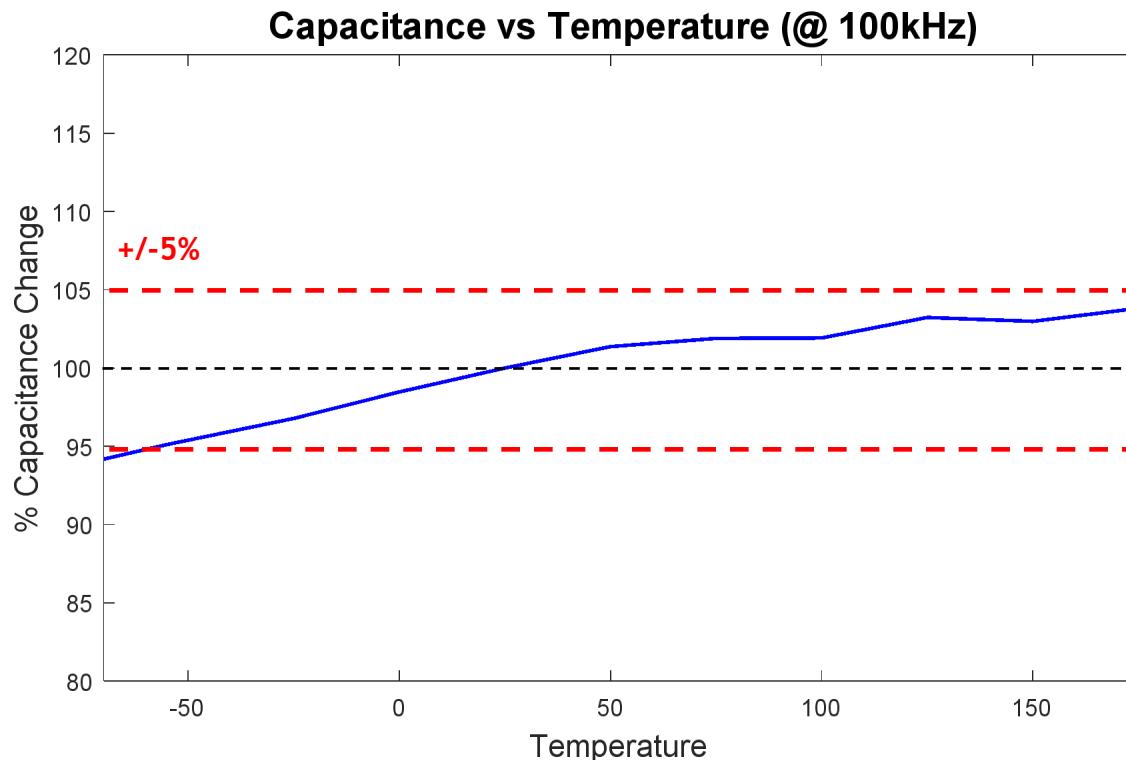
- Leakage current higher than ceramic capacitors, but still low (micro-amps)
- Leakage current versus voltage demonstrates a behavior change $> 80\%$ rated voltage





Low voltage impedance measurement across temperature (-70°C to 175°C)

- Capacitance fairly flat
- ESR fairly flat (< 150 mΩ)

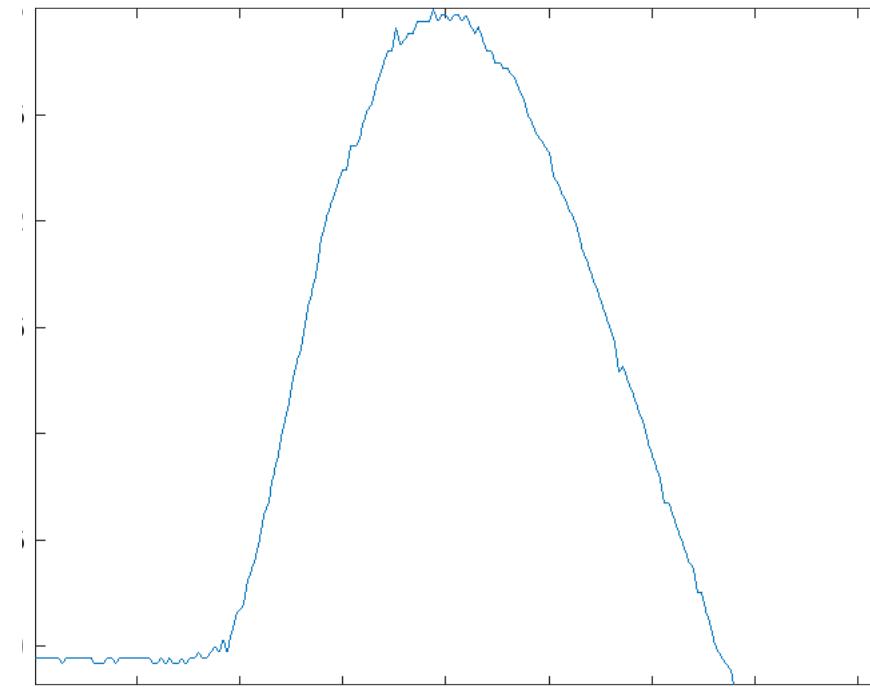
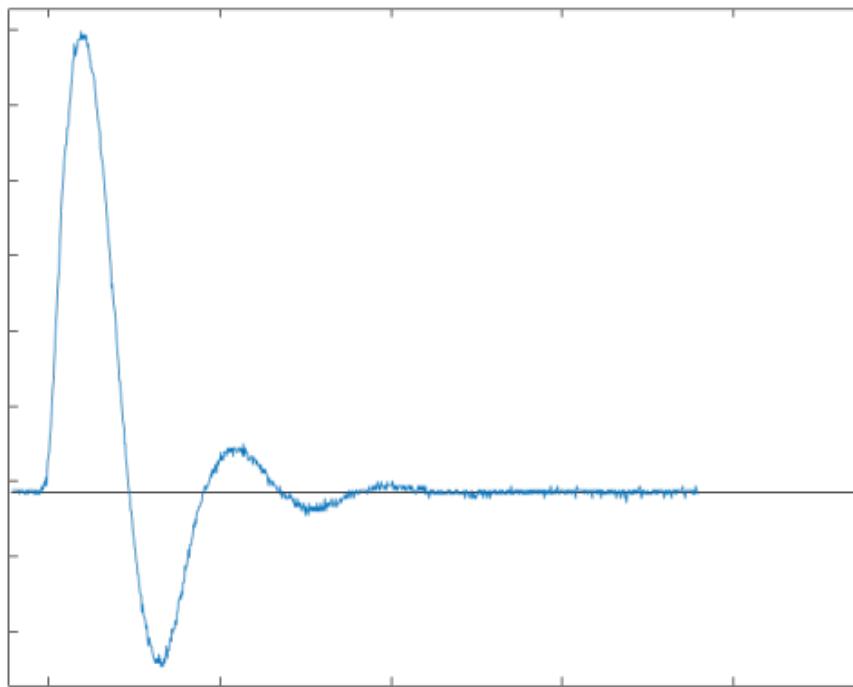




Pulse Discharge

Pulse discharge testing

- Pulse discharges across range of voltages up to 100%
- Characteristics very similar to legacy ceramic capacitor



Repeated Pulse Discharge

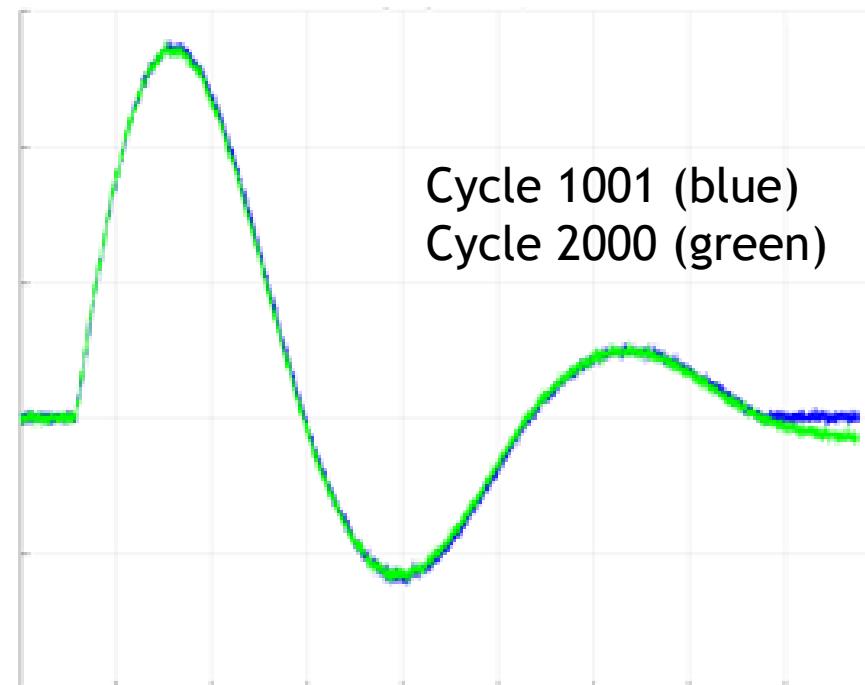
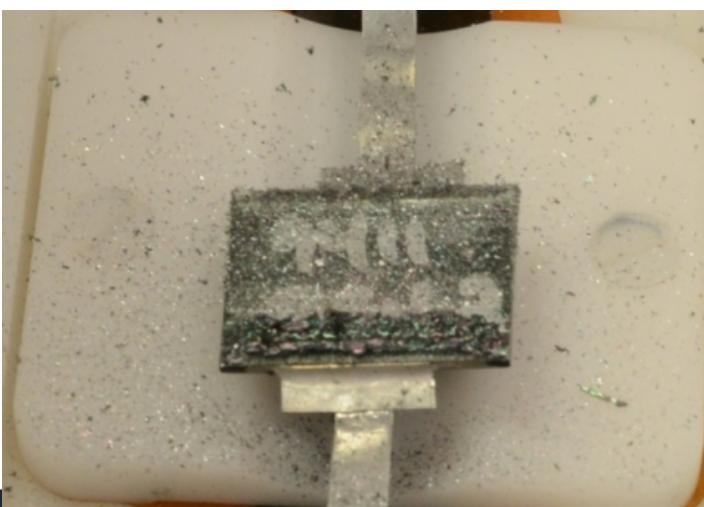
Pulse discharge tester, 5000 discharge cycles

- There was obvious erosion of the metallic end-spray on two units (worst one shown)

One unit after 5000 cycles



Another unit after 5000 cycles



Small losses in capacitance except end-of-life of Unit 1

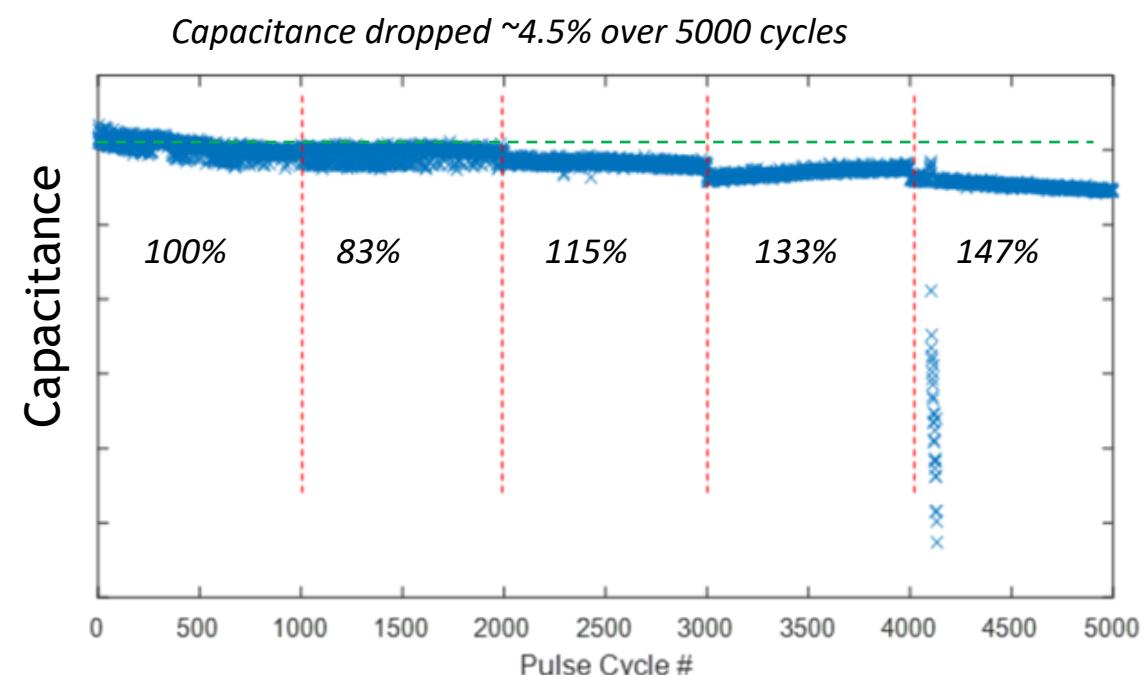
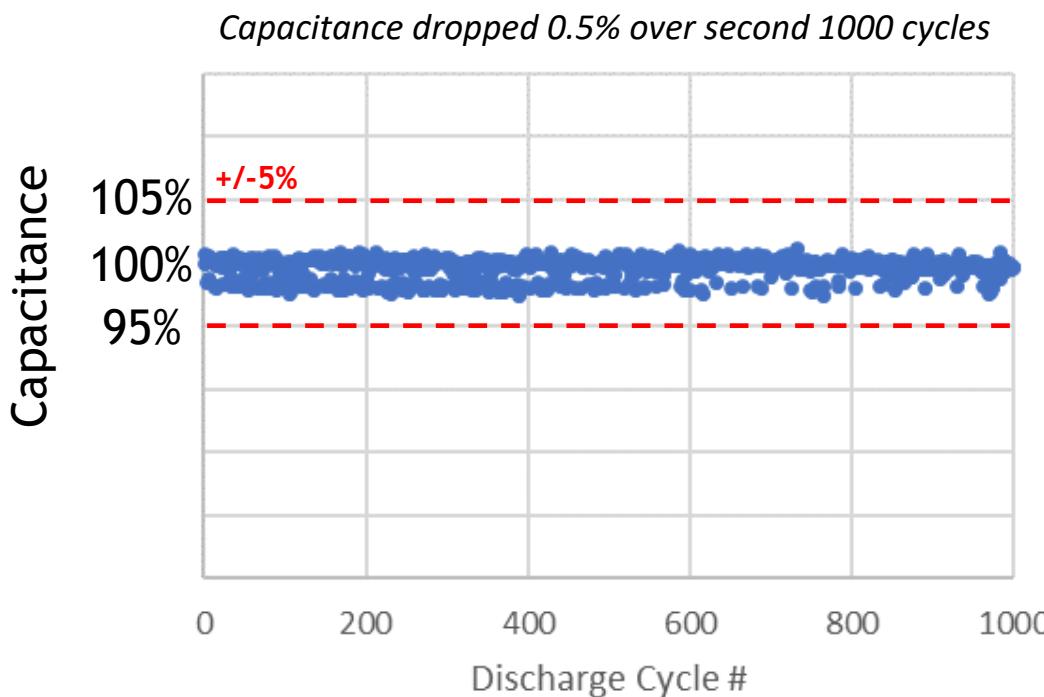
Unit	$\Delta C, \%$
1	-39%
2	-2.5%
3	-3.4%
4	-4.4%
5	-1.2%



Repeated Pulse Discharge

Pulse discharge tester, 5000 discharge cycles

- There was obvious erosion of the metallic end-spray on two units (worst one shown)



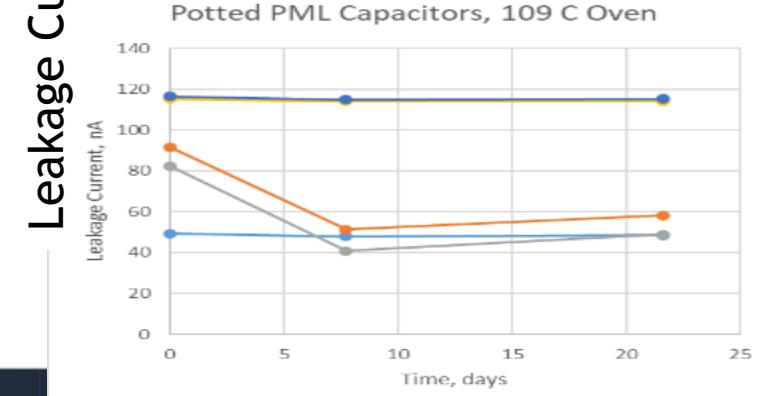
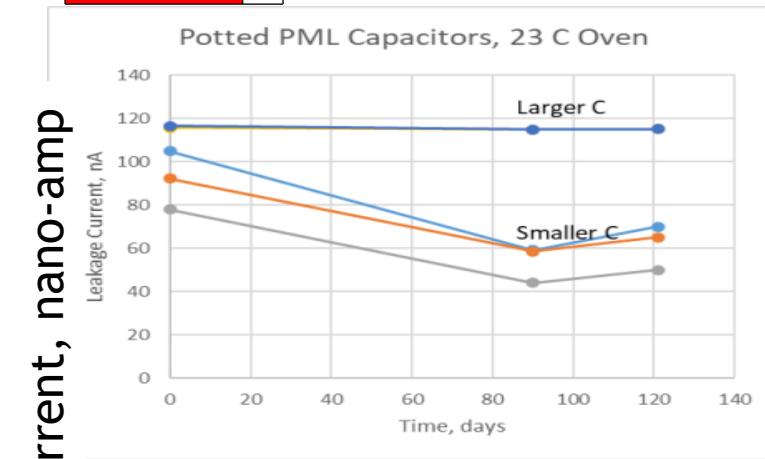
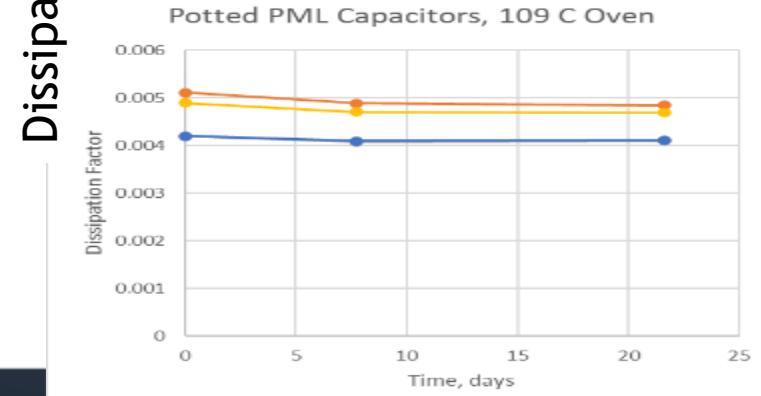
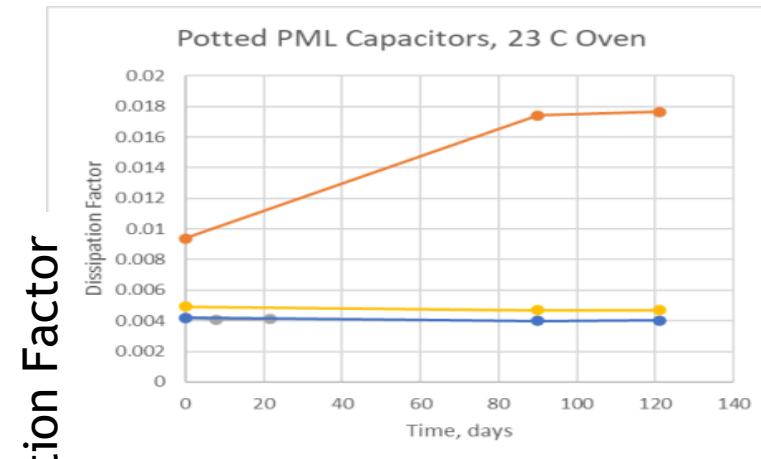
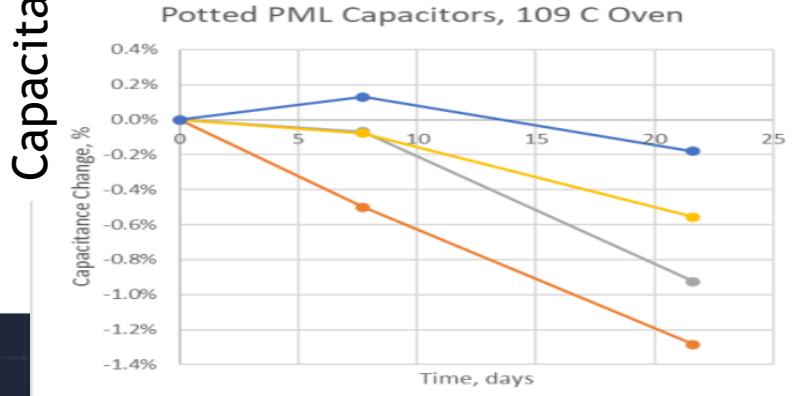
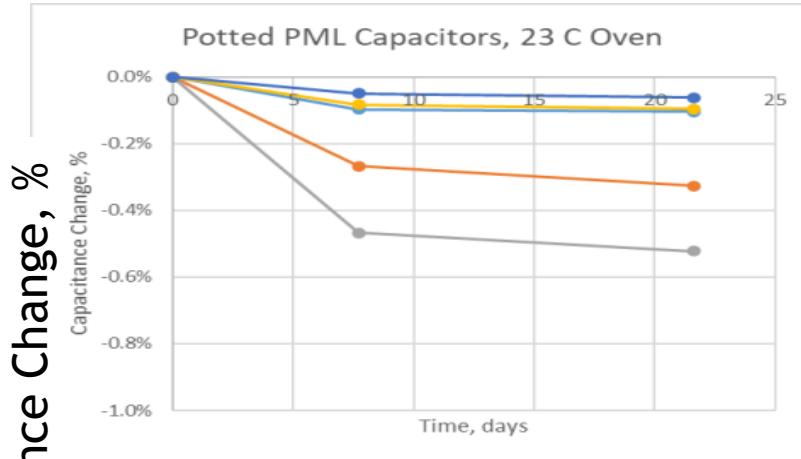
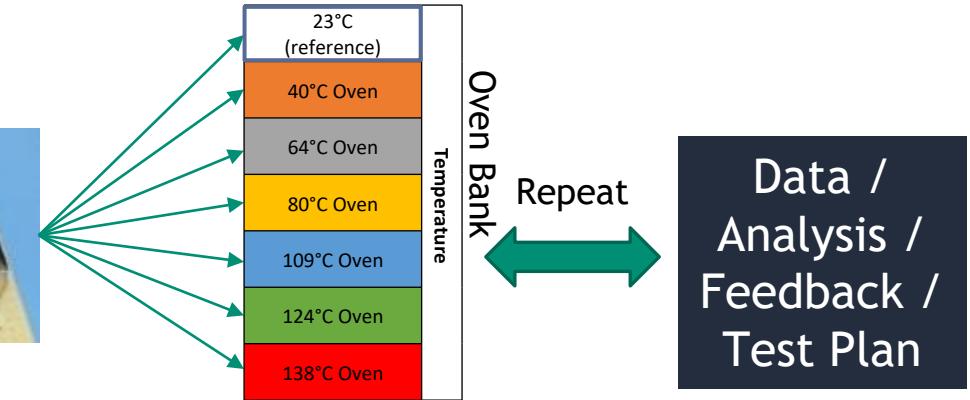
Thermal Accelerated Aging

Bare capacitors up to 138°C

Potted capacitors up to 109°C

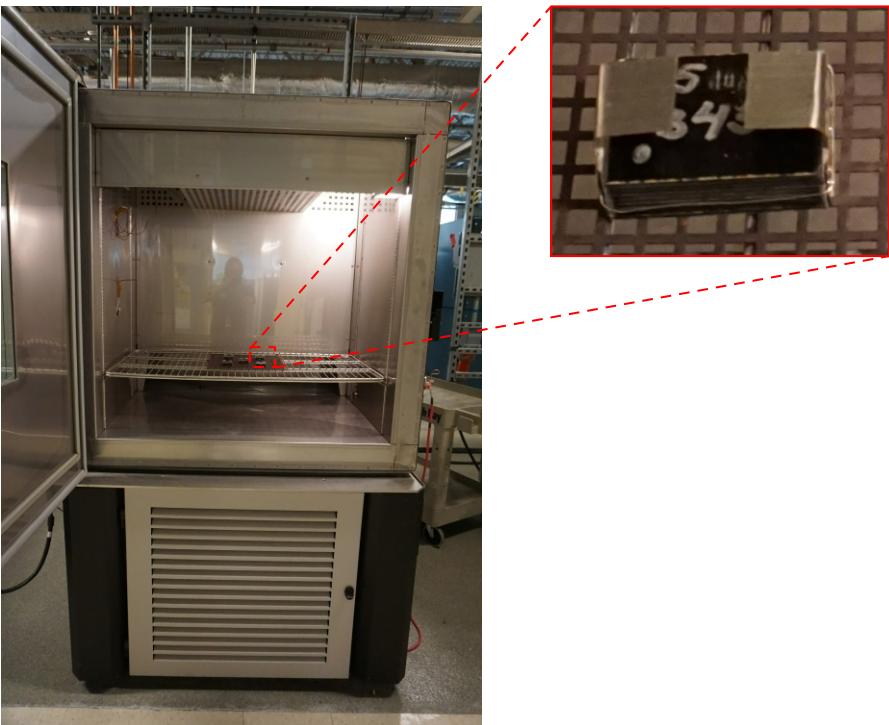
- Reduced leakage current and dissipation factor, likely from moisture removal
- Also 600 hours 95%RH/40°C. Moisture effects were reversed with 40°C drying (24 hrs)

54x Bare PML Capacitors



Humidity Accelerated Aging

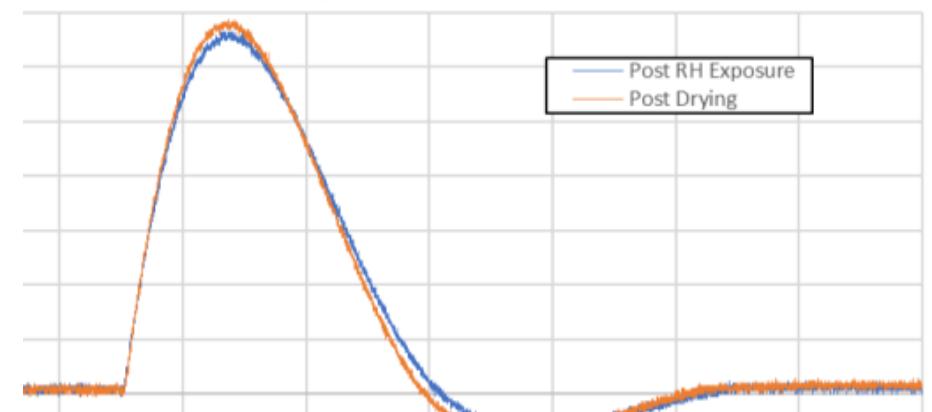
- 5 bare parts exposed to MIL-STD 202 Method 103B, test condition B
 - 95% humidity, 40 °C, 96 hours
 - Capacitance, leakage current, and dissipation factor all increased post-exposure
 - Drying period at 40 °C restored values, except for minor loss of capacitance (one unit lost >10% capacitance)
 - Pulse discharges had more energy when dry (lower dissipation factor)



S/N	Capacitance Change		
	as received	after RH exposure	post-dry
B27	100%	108%	99.4%
B30	100%	108%	99.0%
B43	100%	109%	99.6%
B46	100%	108%	97.1%
B48	100%	107%	89.2%

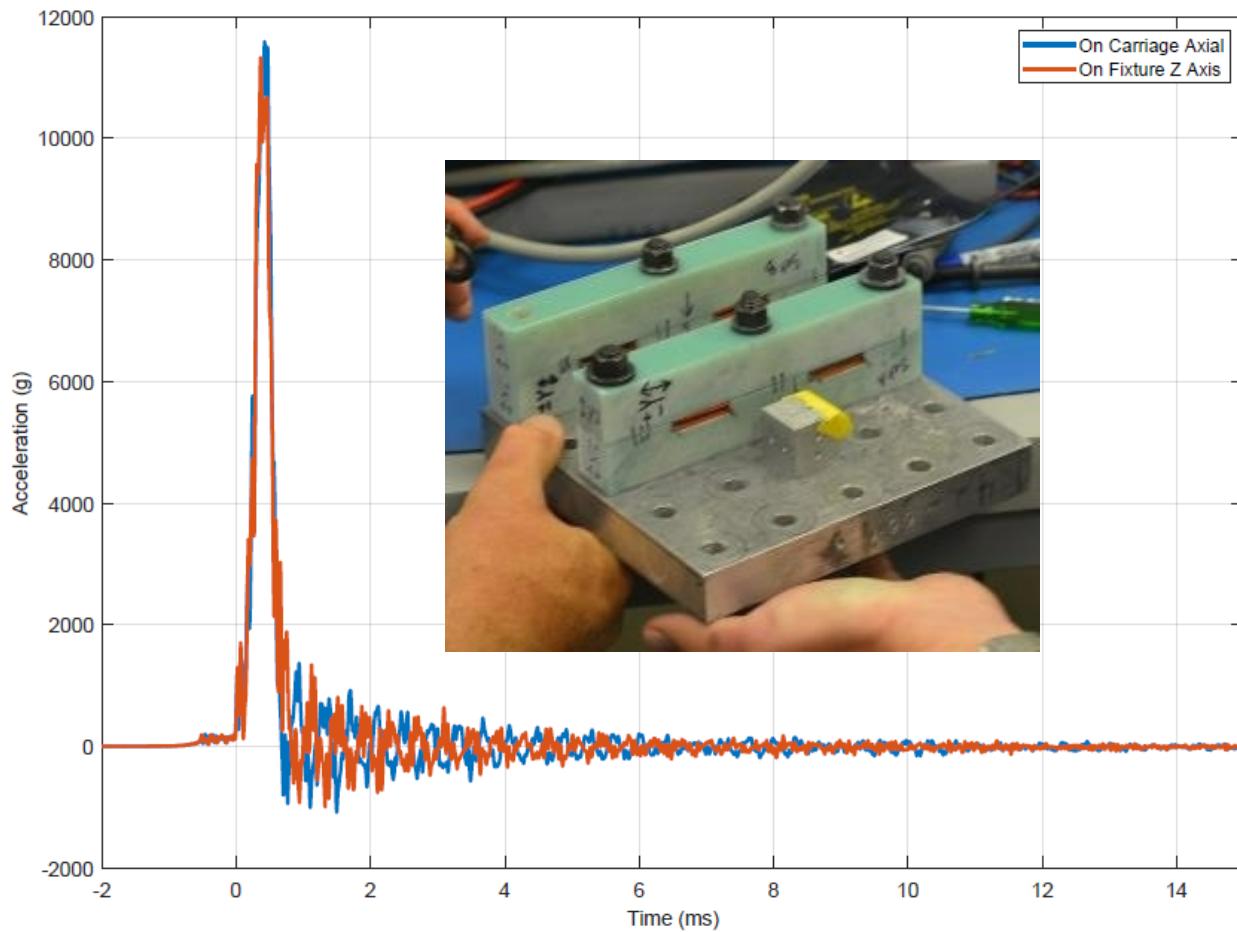
Average DF 0.45% → 0.58% → 0.45%

Pulse Discharge Comparison (unit B46)





Mechanical Shock Testing



Testing:

200G (2 ms)

2000G (0.5 ms)

12,000G (0.5 ms)

5x in each orientation (X,Y,Z) at each level

Individual capacitor chips survived 200 and 2000 G shocks without change.*

*One unit lost ~30% capacitance, but it appeared to be related to the electrical connection. (Verification coming.)

Post-test data not been taken yet for 12,000G shocks.



Conclusions and Future Work

- Two prototype polymer-based multilayer capacitors have been developed
- The technology demonstrates good design versatility for capacitance and voltage
- Chemical, physical, and mechanical testing shows stable properties and broad use environments
- Mechanical impact shock testing and Sandia (12,000 G)
- Upcoming
 - Mechanical shock testing with AFRL coming (60,000 G expected)
 - High-voltage testing at temperature extremes
 - Modeling of impact dynamics, leading to...
 - Next generation design for improved survivability

This work was funded jointly funded by the National Nuclear Security Administration and the Office of the Undersecretary of Defense for Research and Engineering through the Joint DoD/DOE Munitions Program.



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