SAND2022-5999C

arpa·e CHANGING WHAT'S POSSIBLE

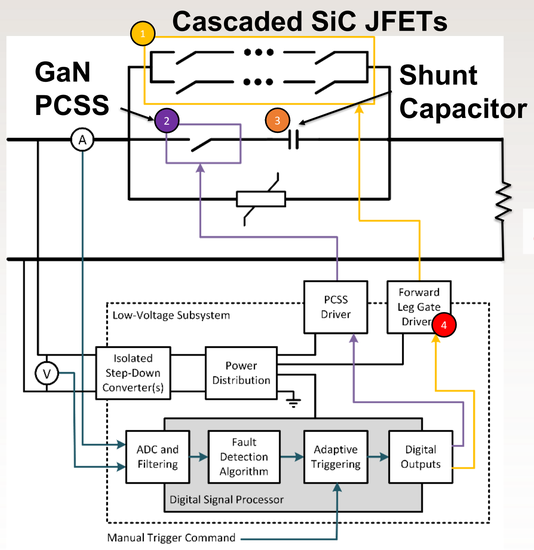
Exceptional service in the national interest

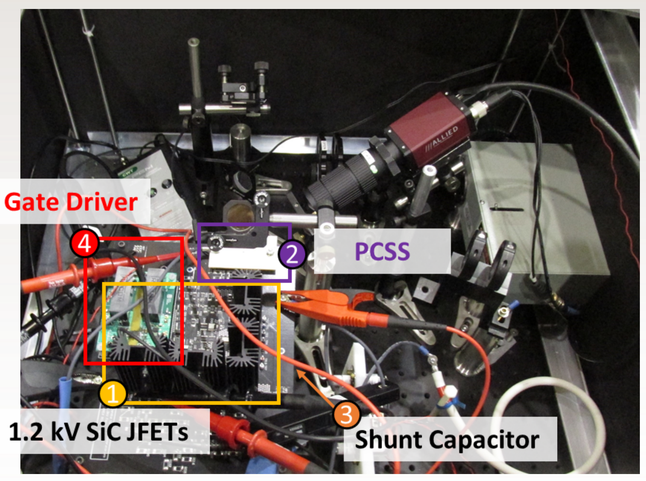
Sandia National Laboratories

ARC-SAFE: Accelerated Response Semiconducting Contactors and Surge Attenuation for DC Electrical Systems

1.5-2 kV/3-10 A Circuit Breaker Demonstration

Approach



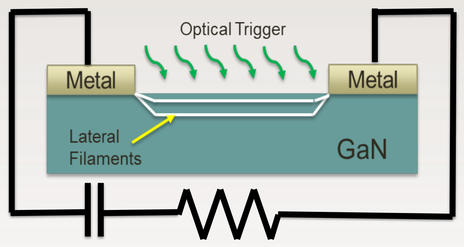


1. Normally-on Leg consists of cascaded SiC JFETs with passive balancing approach
2. Normally-off Leg uses GaN Photoconductive Semiconductor Switch (PCSS)
3. Energy dissipating leg uses shunt capacitor to manage flyback current.
4. System control (sense and trigger) included in low-voltage subsystem
   - Instrumented to allow characterization of circuit breaker components
   - Shrinking design for 10 kV/100 A target

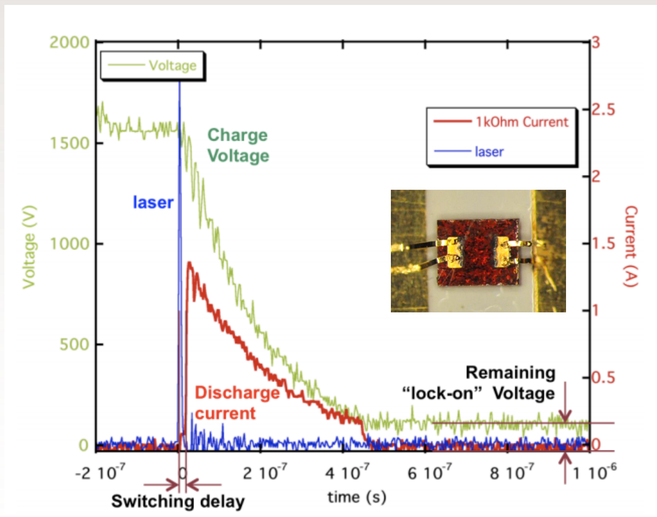
Benefits

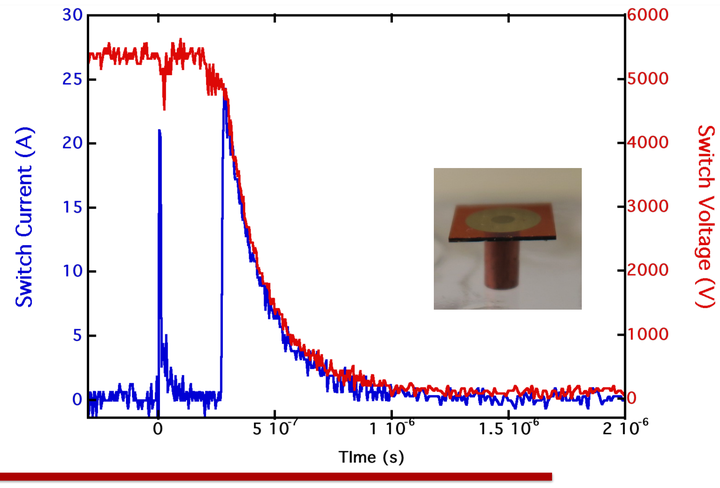
- *Normally on, low loss JFETs improve CB efficiency*
- *Galvanic isolation from optically triggered GaN PCSS (fast acting)*
- *System control powered from HV side voltage tap*

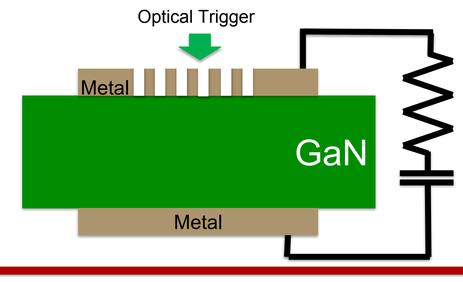
GaN PCSS (Lateral and Vertical Designs)



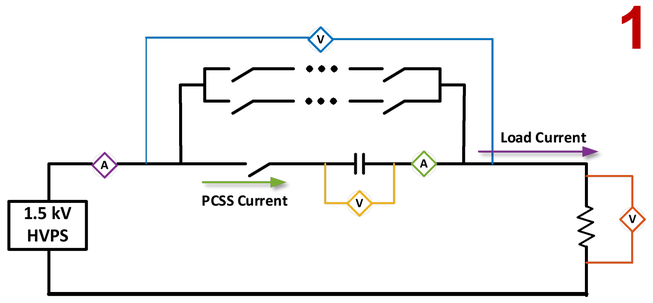
- Lateral GaN PCSS scales voltage by pad spacing.
- < 2 kV switches using 0.6 mm gap
- Optically triggered using 532 nm (Nd:YAG laser)
- Vertical GaN PCSS uses bulk semi-insulating GaN for voltage holdoff (>>5 kV)
- 2D array scaling using current filaments

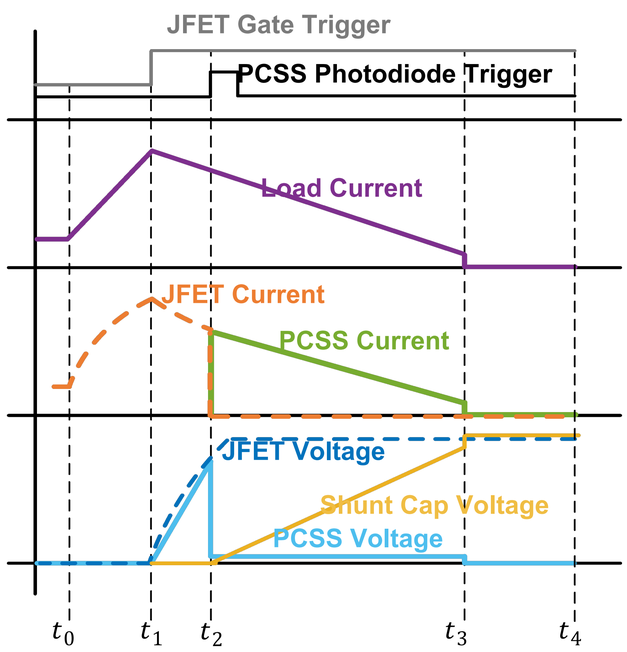






1.8 kV/10 A, DC Circuit Breaker Demonstration





Interval I $[t_0 \rightarrow t_1]$

• Fault current rises at t_0 until t_1 when the fault current is detected, turning JFETs OFF

Interval II $[t_1 \rightarrow t_2]$

• JFET voltage starts to rise at t_1 and JFET/load current starts to decrease.

Interval III $[t_2 \rightarrow t_3]$

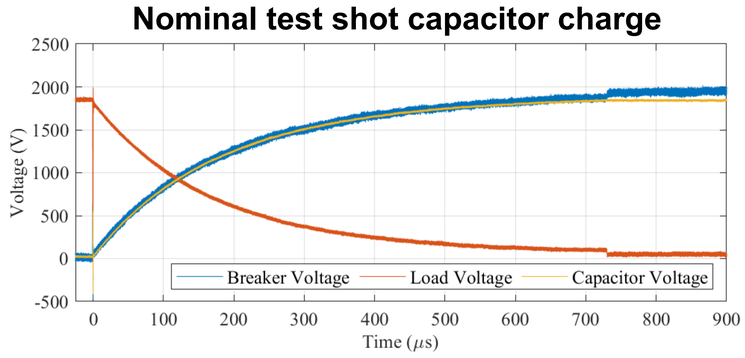
• PCSS is triggered at high-gain mode at t_2, diverting fault current from JFET leg to shunt cap.

• Shunt capacitor voltage rises based on RC value.

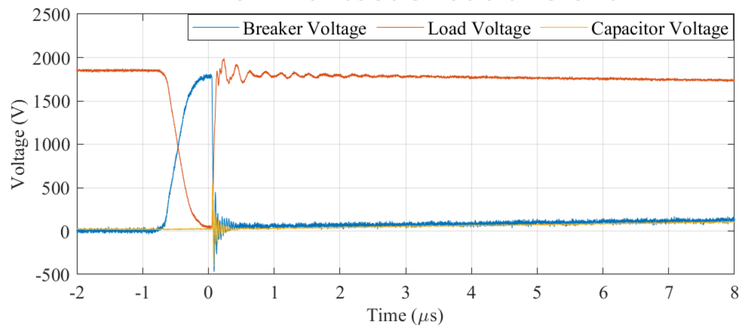
Interval IIV $[t_3 \rightarrow t_4]$

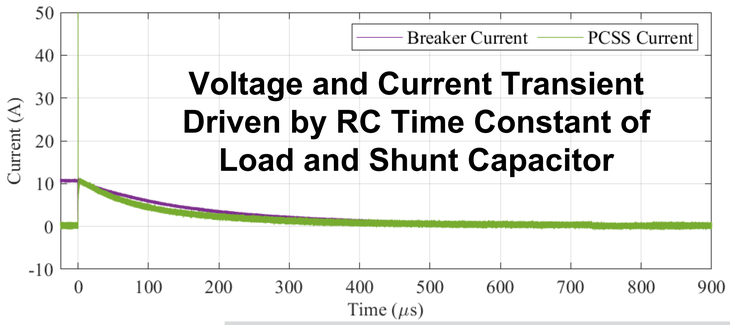
• PCSS voltage reaches OFF state and breaks remaining current.

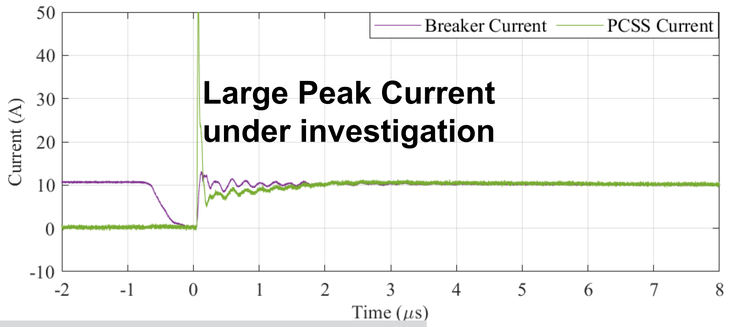
Nominal test shot capacitor charge



Nominal test shot transient







Path Forward to 10 kV/100 A

- ***Scaling Normally-On JFET design to 10 kV, 100 A capacity***
- ***Moving to vertical GaN PCSS to scale current performance***
- ***Compact packaging design to meet power density targets***

U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

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