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Veeco D-125 MOCVD system

Selective Area Regrowth of p-type GaN and AlGaN for Power Diodes

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U.S. DEPARTMENT OF ENERGY

Outline

- Selective area p-type doping for diodes and transistors
- PN junction formation by P-GaN regrowth on etched n-GaN
  - Ex-situ processing to remove residual etch damage
  - In-situ XeF2 to remove residual etch damage
- PN junction formation by regrowth in $Al_{0.3}Ga_{0.7}N$ diodes
  - Planar, non-selective area PN junctions
  - PN junctions with selective area p-type $Al_{0.3}Ga_{0.7}N$ doping
- Summary

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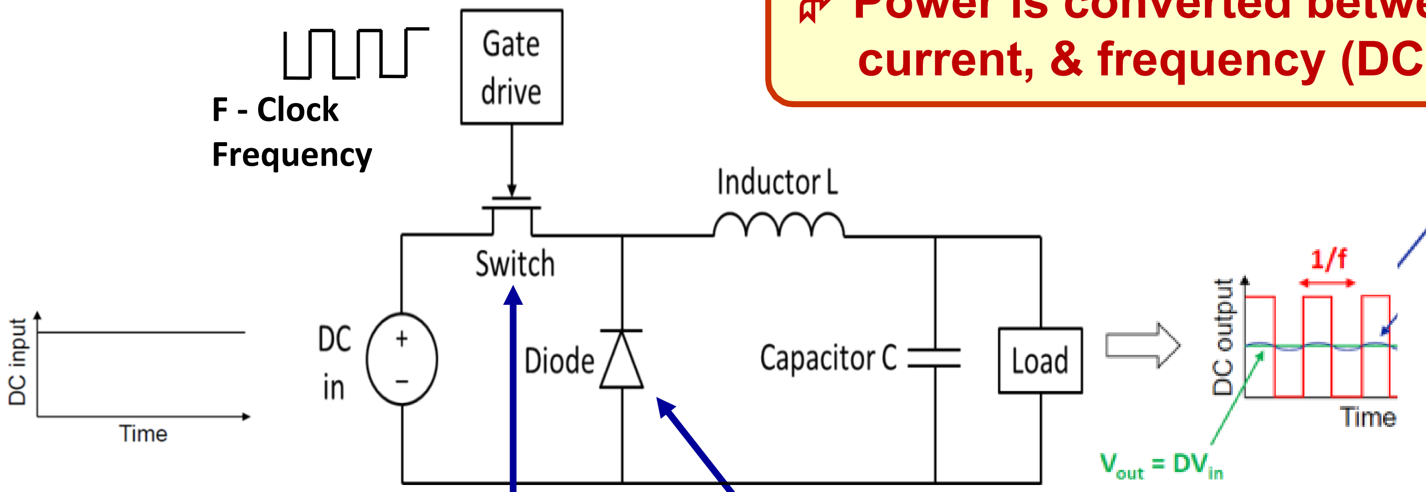
Example: (Step down)DC to DC Buck converter

> Power is converted between voltage, current, & frequency (DC & AC)



$$\frac{V_{ripple}}{V_{out}} = \frac{1-D}{8LCf^2}$$

Increasing f allows one to reduce L and C while keeping the ripple constant

Switching transistor

- Vertical current flow for high-current & voltage
- Voltage dropped across thick drift layer
- D-MISFET, JFET, MOSFET ..etc..

Diode

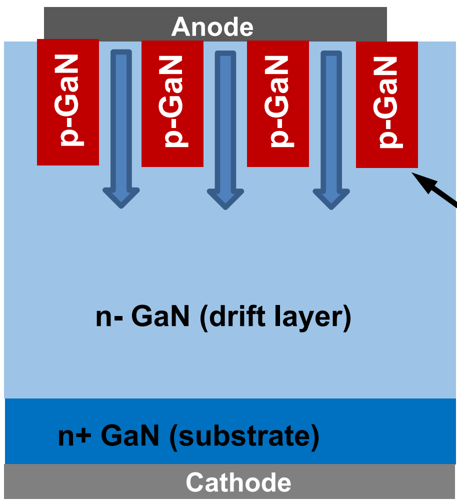
- Vertical current flow
- SBD, PIN, and MPS diodes

> *Power management is based on diodes and transistors*

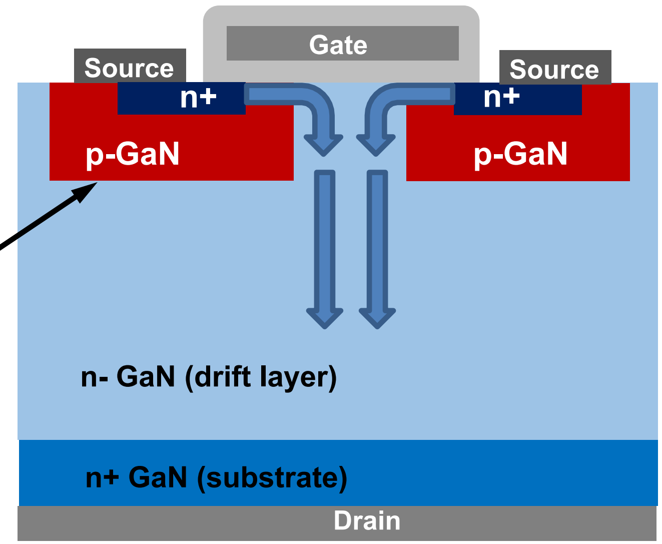
Practical high-voltage diodes and transistor require selective area p-type doping

Merged PIN Schottky (MPS) diode

Double-well Metal-Insulator-Semiconductor Field-Effect-Transistor (D-MISFET)



p-well formed by selective area doping



- **Reverse-bias PN junction key to multi-kilovolt blocking voltage (V_{br})**
  - **Must have low reverse leakage current**
- **P-layers formed by ion implantation and annealing for Si and SiC device**
  - **p-implant into GaN is challenging but advancing**

Form the p-well by ICP etch epitaxial regrowth of p-GaN

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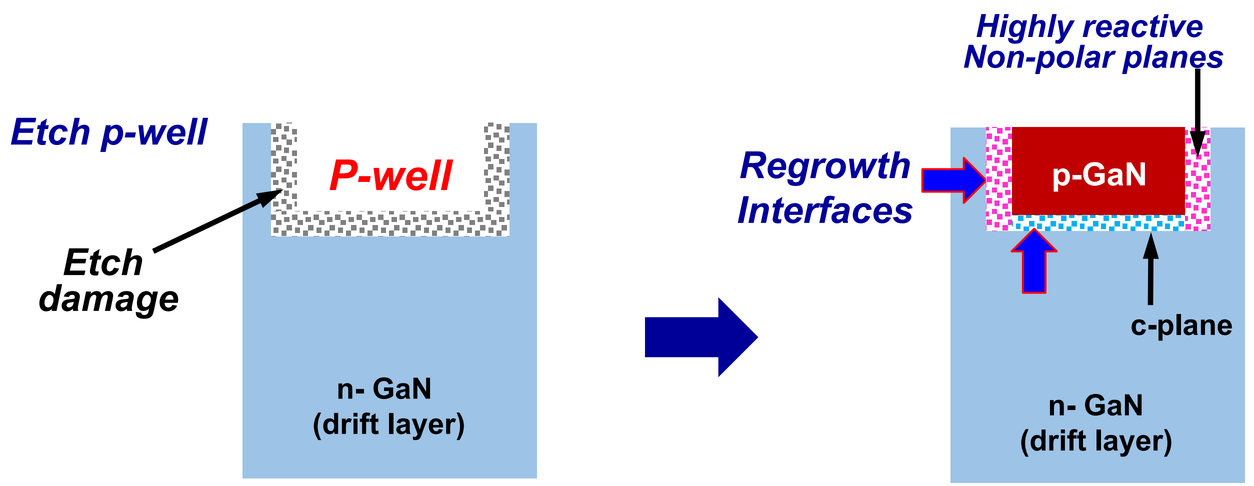
Sources of current leakage at regrown PN interface



- Electrically active impurities (Si, O, etc.)
- Damage to crystal structure from ICP etch resulting in extended (?) and point defects (e.g. vacancies).
- Incorporation rates of impurities and growth rates depend on crystal plane
- Use maskless approach to regrowth — avoid growth and mask removal problems

Start simple, p-GaN regrowth on c-plane drift layers

Current-voltage characteristics of continuously grown and etched/regrown diode

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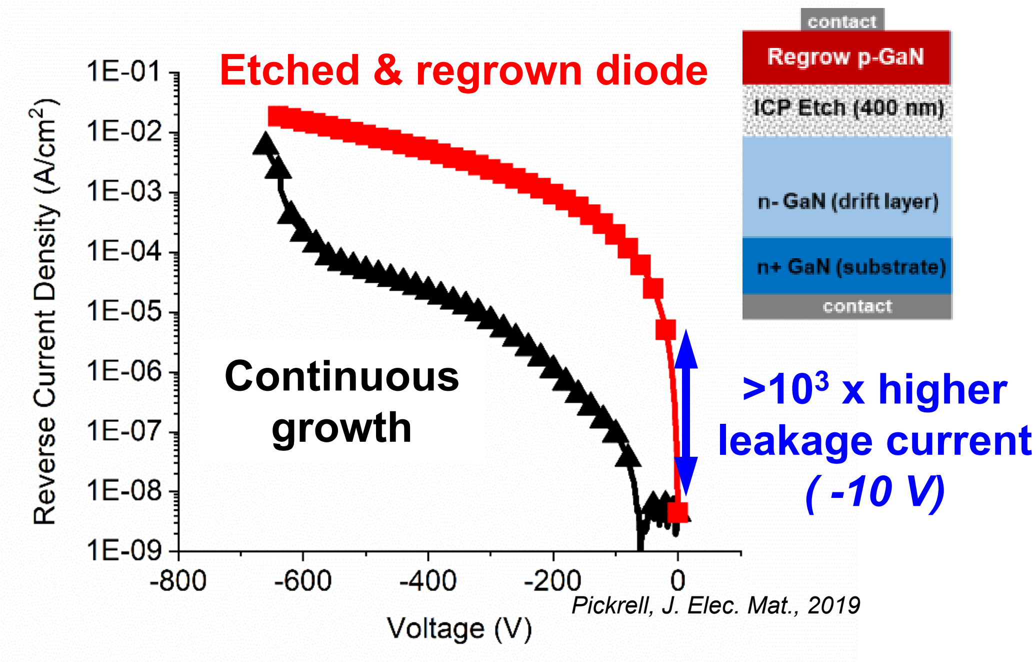
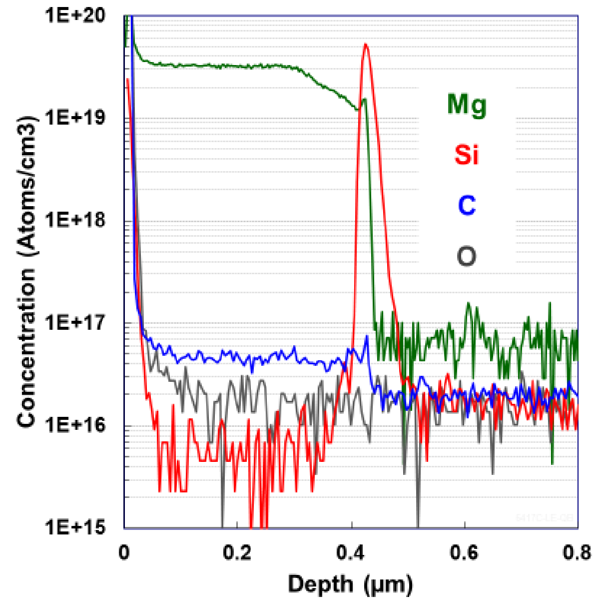
Reverse IV Characteristics of GaN PN diodes



Pickrell, J. Elec. Mat., 2019

- **Quality of PN junction revealed within first 10-20V in reverse bias**

SIMS: Regrowth of p-GaN on ICP etched n-drift layer



- **Si spike found on surfaces exposed to air**

Differences between continuous diodes and etch and regrown diodes

- ***High reverse leakage near 0 V***
- ***High Si concentration at regrowth interface***

Sub-surface etch damage from ICP etching

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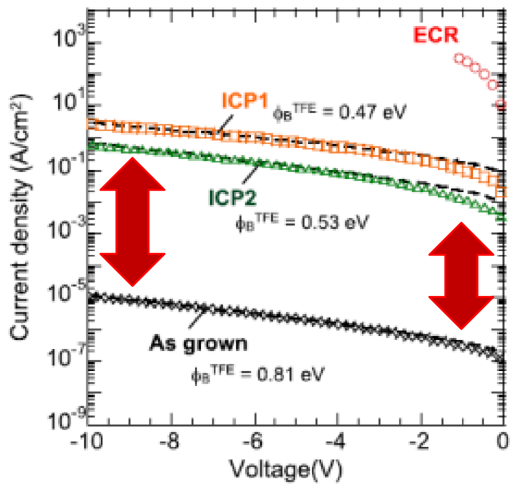
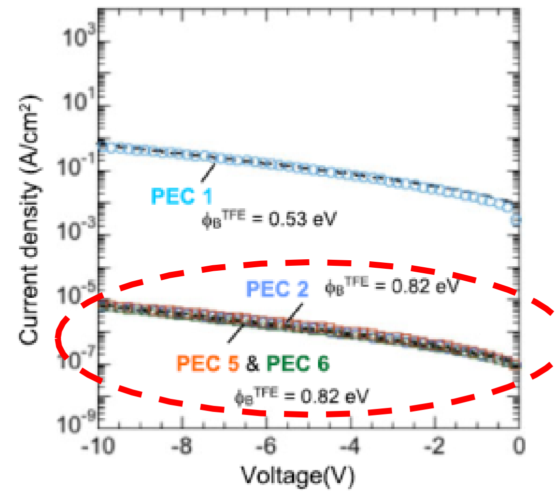
- ***Photo-assisted electrochemical (PEC) etching (Matsumoto, Jpn. J. Appl. Phys. 2018)***

Reverse IV Characteristics of GaN SBDs (-10V)

- **ICP, ECR etched GaN drift layers**
- **PEC oxidation + TMAH oxide etch to remove sub-surface etch damage**
- **Fabricate SBDs**
- **Sub-surface etch damage:**
  - **ECR etching ~ 230 nm**
  - **ICP etching ~ 70nm**



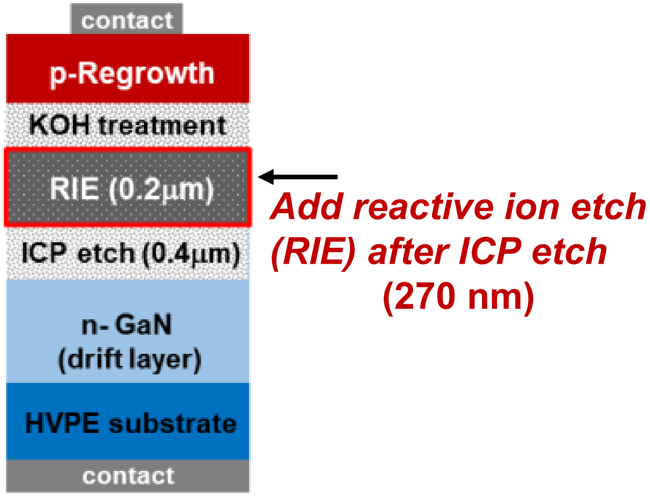
- **SBDs on ICP etched GaN have 10^4 x higher leakage**



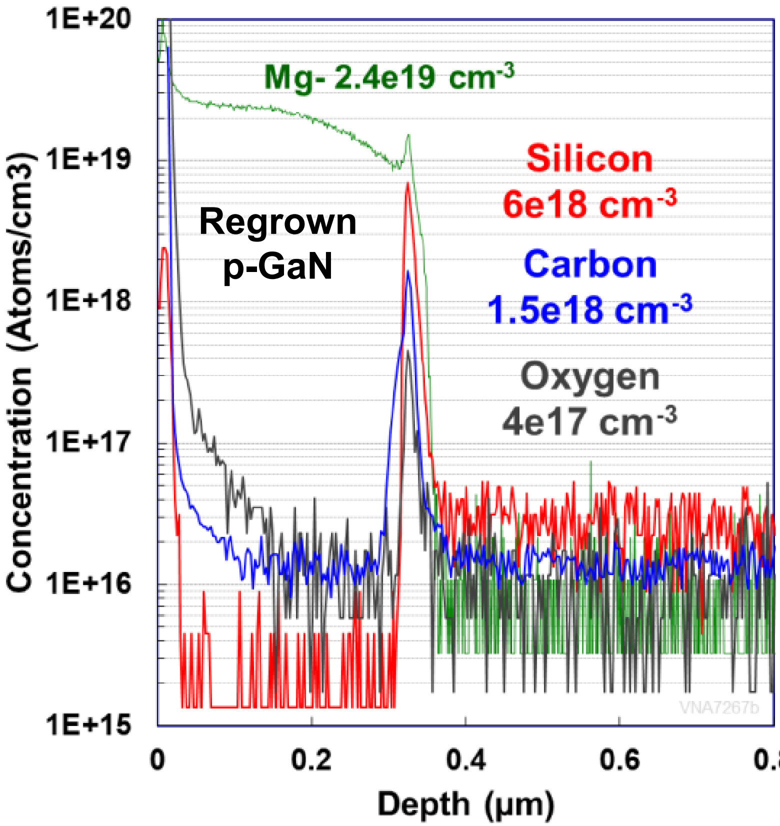
- **Following PEC, IVs matched SBDs on as-grown GaN**

> **Sub-surface ICP etch damage ~ 50-300 nm**
>
> **Either prevent sub-surface etch damage or remove it**

Reactive ion etch (REI) to "clean up" damage from ICP etch



SIMS of Regrown PN Diode



Blanket etching of n-drift layer

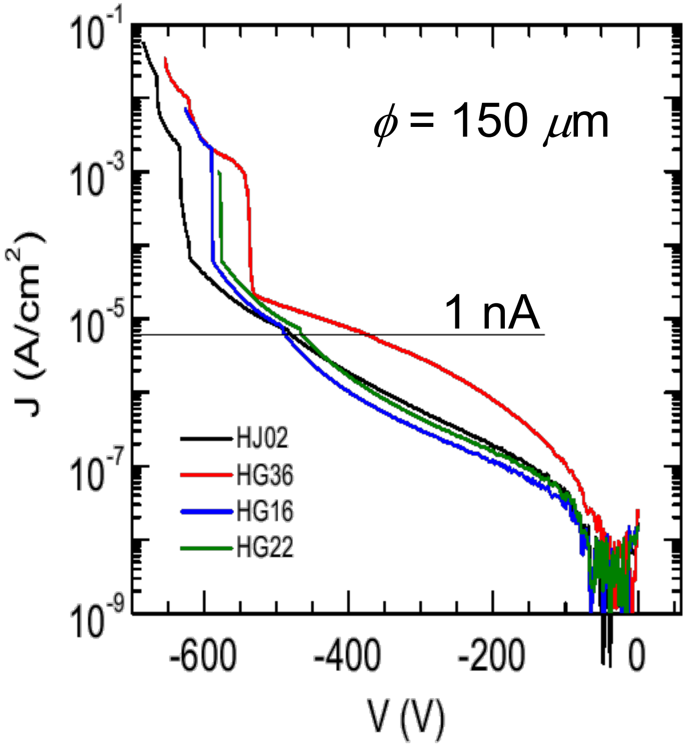
- **RIE etch - low damage etch used for gate recess for HEMTs**
- **RIE 270 nm — remove sub-surface ICP etch damage**
- **Finish with KOH, 10 min., 80 °C, DI rinse, N2 dry**

- **Very high levels of Si, C & O at regrowth interface**

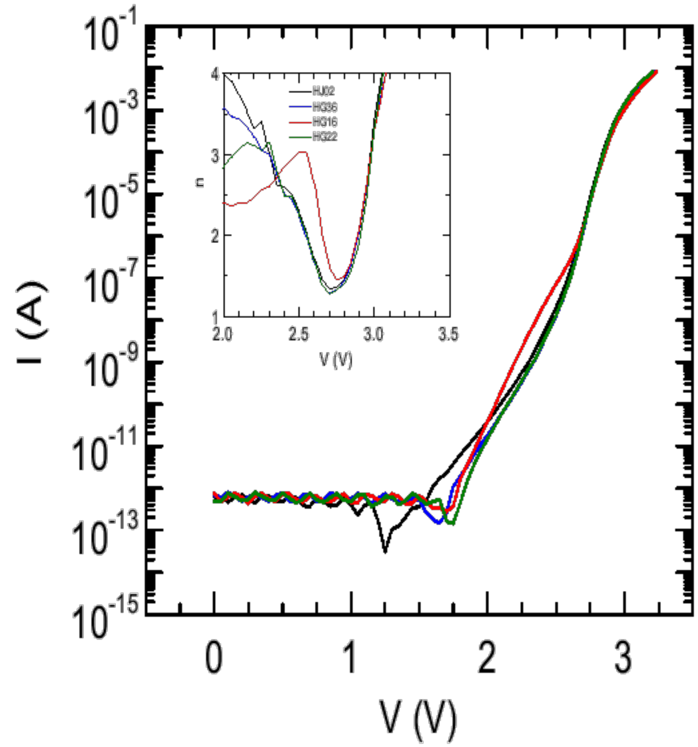
Test low-damage RIE "clean-up" etch to remove sub-surface ICP etch damage

IV characteristics of ICP+RIE etched / regrown diodes

Reverse IV Characteristics



Forward IV Characteristics



- **1 nA (6 mA/cm²) @ 500 V**
- **ASU: 20 mA/cm² @ 500 V (etched regrowth)**
- **Cornell: 2 mA/cm² @ 500 V (w/o etch regrowth)**

- **Low leakage < 2 V**
- **Ideality factor ~ 1.3**

Low leakage etched and regrown diodes demonstrated with RIE removal of sub-surface ICP etch damage

Use in-situ etching to remove sub-surface ICP etch damage to GaN

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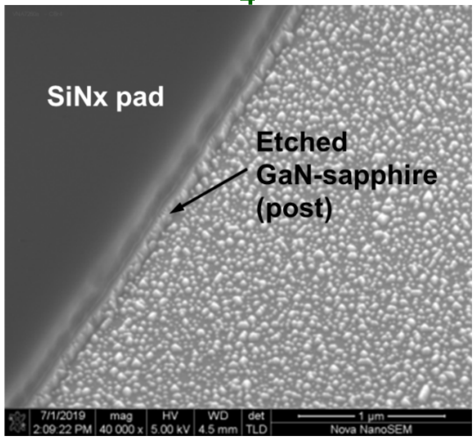
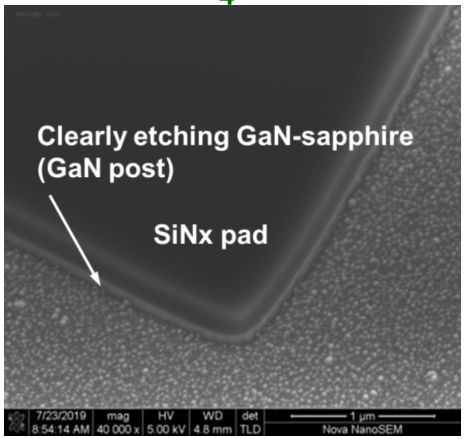
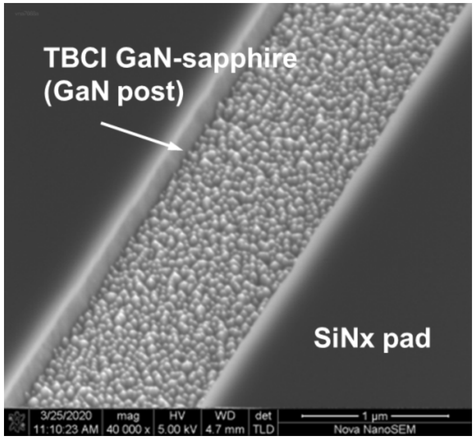
CBr_4



CCl_4

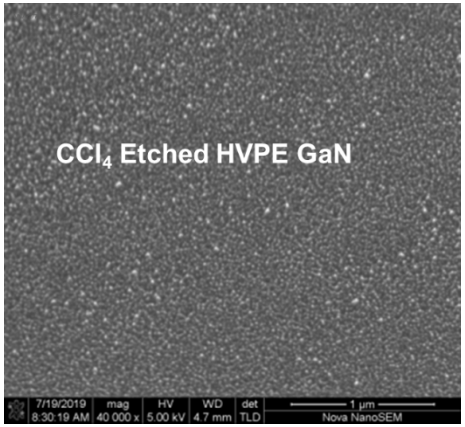


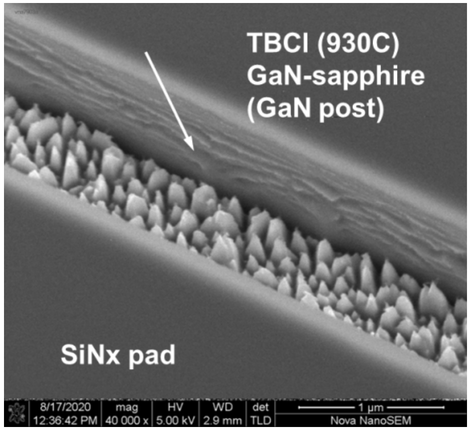
TBCl



- *Surfaces exposed to air (months)*
- *Si always present by SIMS, > 1e19 cm-3)*

- **Better surfaces follow J. Han's (APL 2019) conditions:**
  - **pressure**
  - **temperature**
  - **low NH3**
- **No reduction of Si spike with listed halide sources**



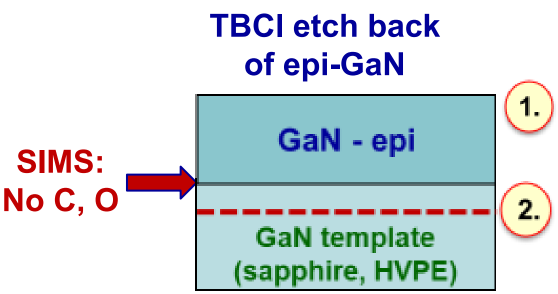


- *Typical poor surface observed for many etch conditions*
- *Rough surface if etching HVPE GaN, ICP etched GaN…*

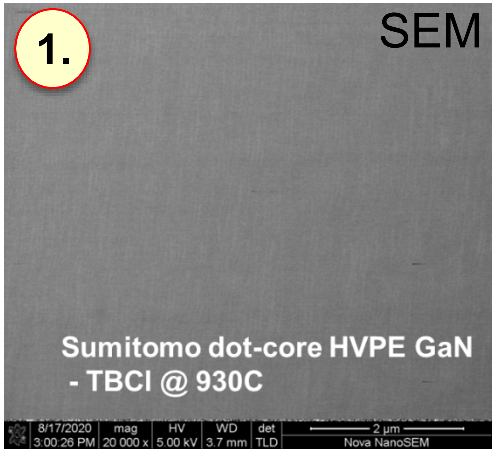
Æ Rough etched surfaces regardless of reactor conditions, chemistry or GaN crystal (HVPE, on sapphire) when surface is exposed to air.

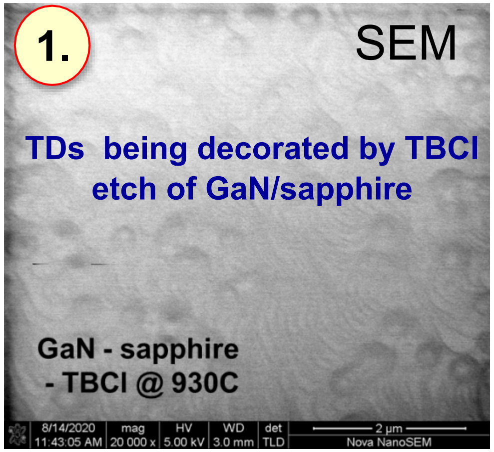
In-situ TBCl etching of GaN grown ***without exposure to air***

TBCl etching of GaN epi surface following growth (No exposure to air)



- **Smooth etch for epi on HVPE GaN not exposed to air**



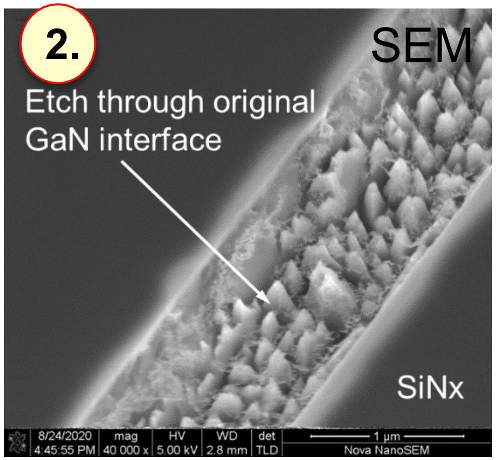


- **Smooth etch for epi on HVPE GaN and GaN on sapphire**

Æ Very different morphology for TBCl @ 930C depending on exposure to air

Æ Starting GaN surface (air exposure ⇒Si) is more important than etch conditions?

Æ Focus on Si removal as "surface prep"



- **Rough etch once through re-growth interface for epi on HVPE GaN**

Removal of Si at regrowth interface using XeF_2

Andrew Koehler (NRL)

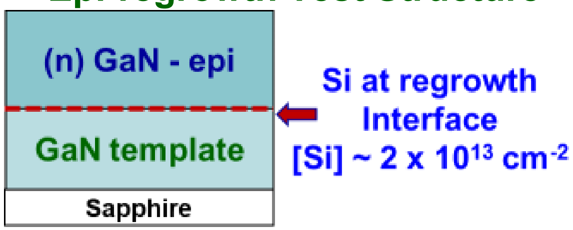
Use Si etch tool (XeF2) to remove interfacial Si prior to regrowth

- **Utilize commercial GaN/sapphire templates with consistently high surface Si concentration**
- **Expose GaN to different Si etch recipes (Si etch tool with pulsed XeF2, RT process)**

  $2XeF_2 + Si \rightarrow 2Xe + SiF_4$

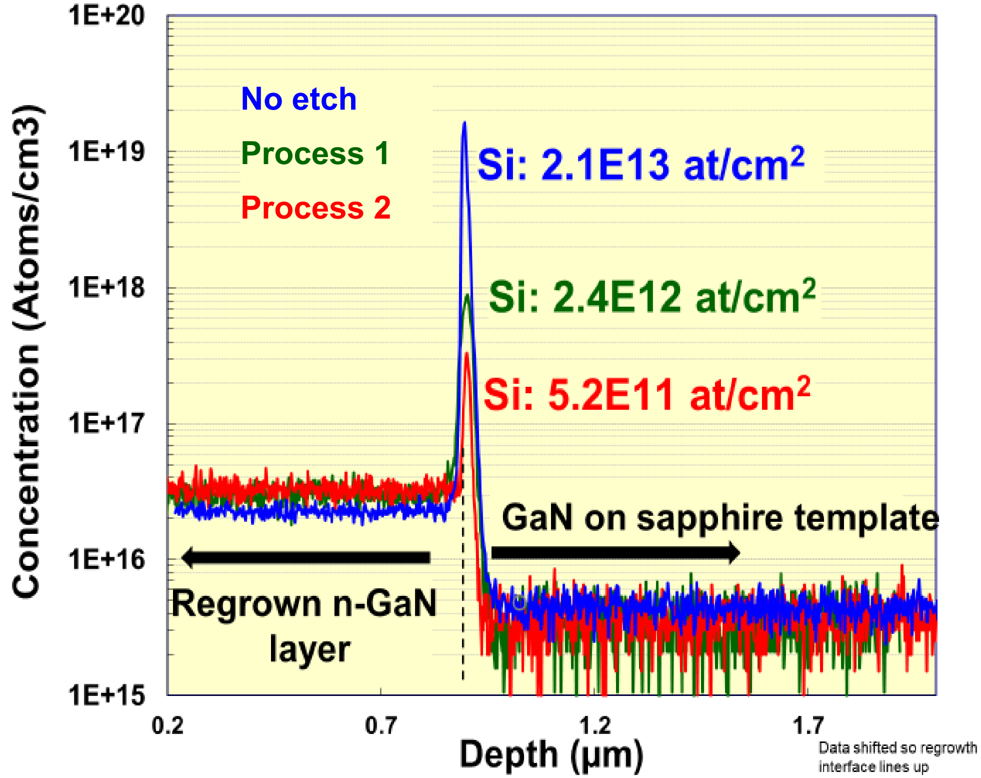
- **Regrow GaN drift layer – (CV, SIMS)**

Epi-regrowth Test Structure



Æ **Good diodes made with intentional Si ~ 5e11 cm^{-2}**

Si at regrowth interface (SIMS)



➪ **> 10x reduction in interfacial Si with XeF_2 process in Si etch tool**

➪ ***Try XeF_2 on MOCVD system***

In-situ removal of Si at regrowth interface and etching using XeF$_2$

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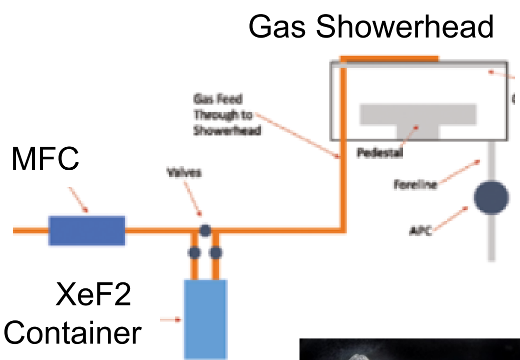
Replicate Si etch tool (XeF2) process in MOCVD chamber

Drysdale (2015) – XeF2 etching of Si

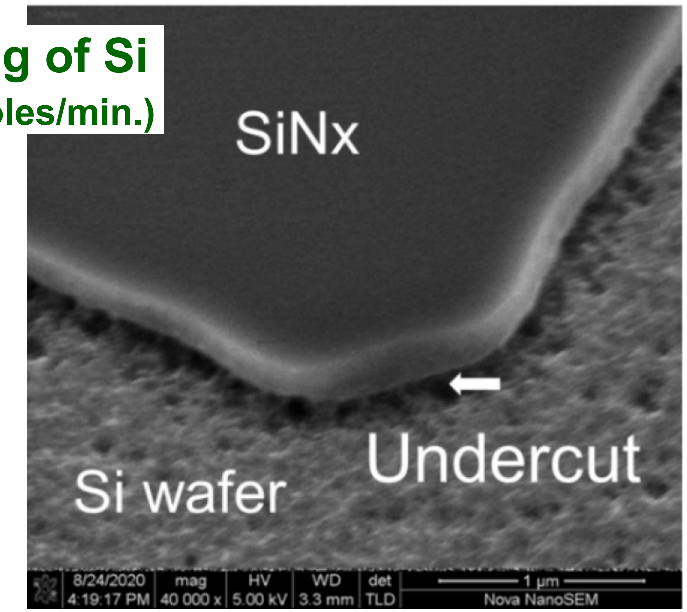
- **Continuous XeF2 flow (1-9 torr)**



White Crystals, 3.8 torr @ 25C (Dock Chemical)

Æ Essentially a MOCVD setup operating at ~10 torr

XeF_2 etching of Si
(25C, 10 μmoles/min.)



- **Si etch: ~ 1500 Å/hr @ RT**
  - ➯ *XeF_2 is reaching surface*
- **Johnson (APL 2019) - XeF_2/BCl_3 etching of GaN**
  - ➯ *Try etching GaN with XeF2*

In-situ XeF_2 etching of GaN (Air Exposed surface)

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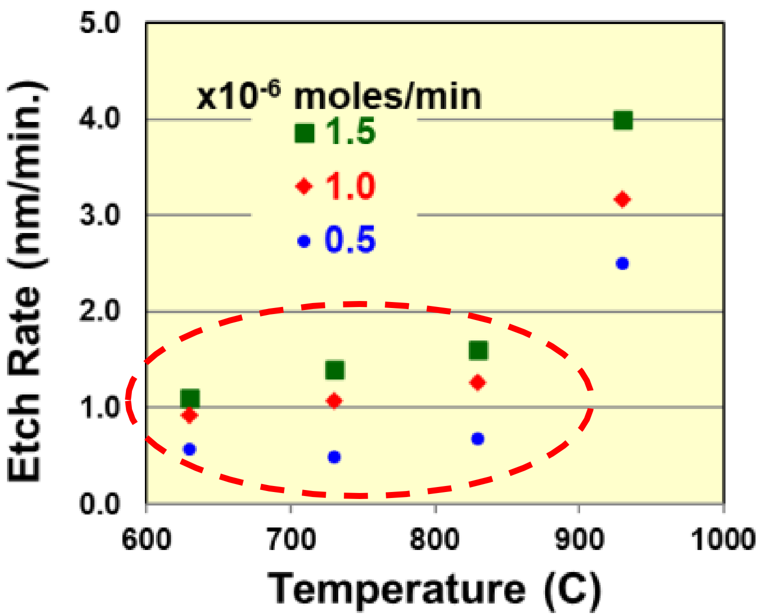
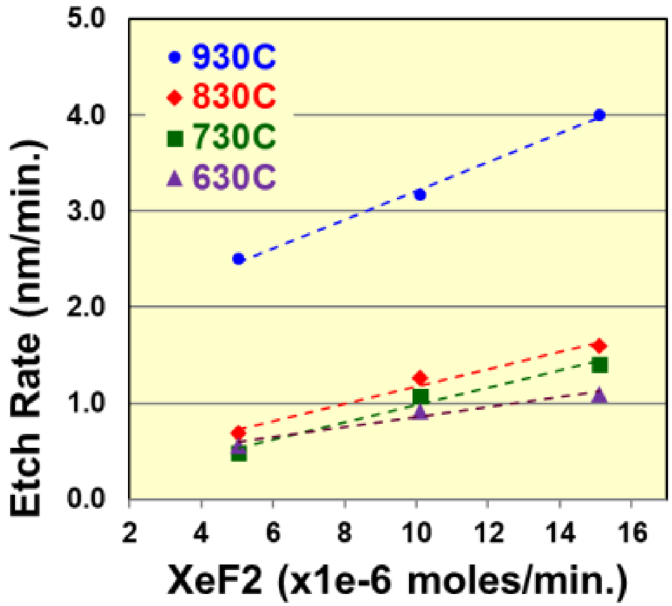
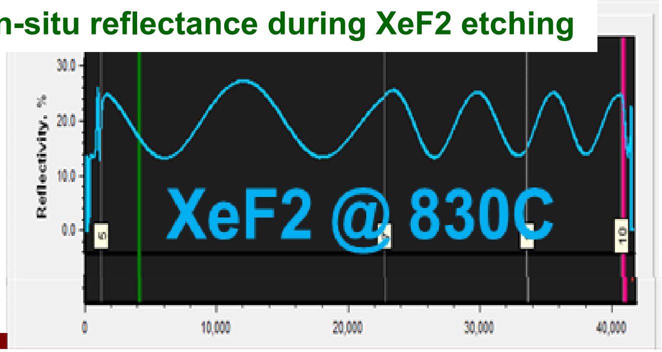
Etch Rate vs. Temperature



Etch Rate of GaN vs. XeF2 Flux



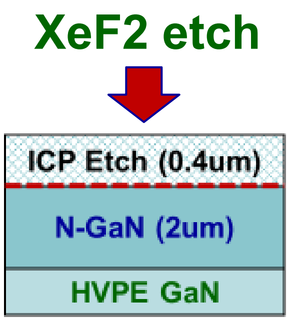
In-situ reflectance during XeF2 etching

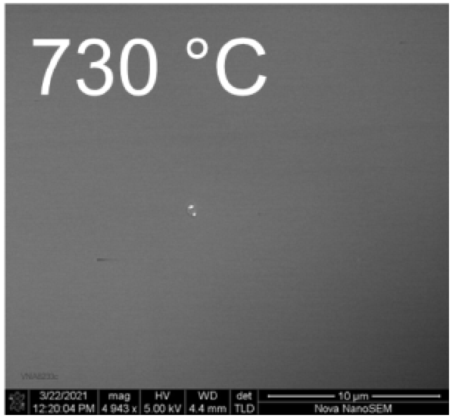


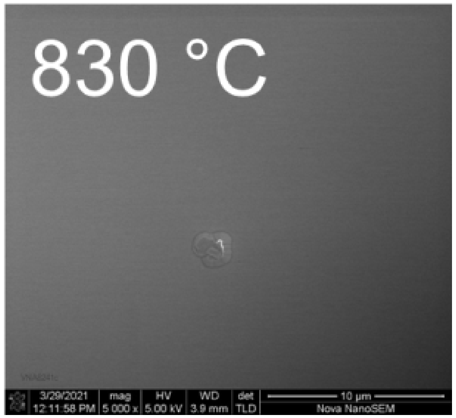
- *Etch rate is linear with XeF2 flow*
- *Stable reflectance @ 730C, 830C*

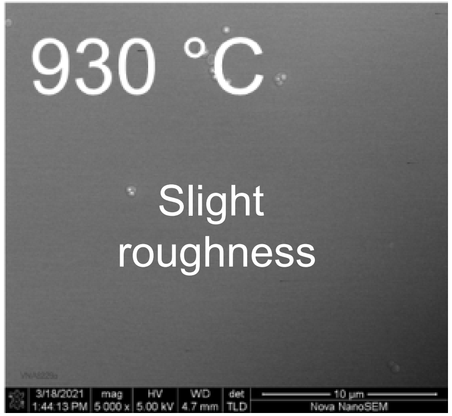
In-situ XeF_2 etching of GaN (air exposed surface)

SEM of XeF2 etched - ICP etched GaN (air exposed)

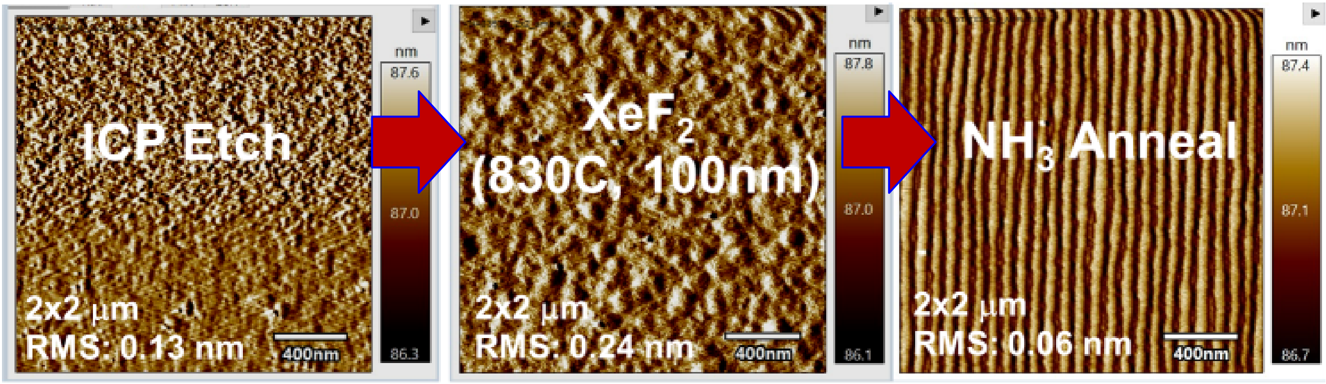


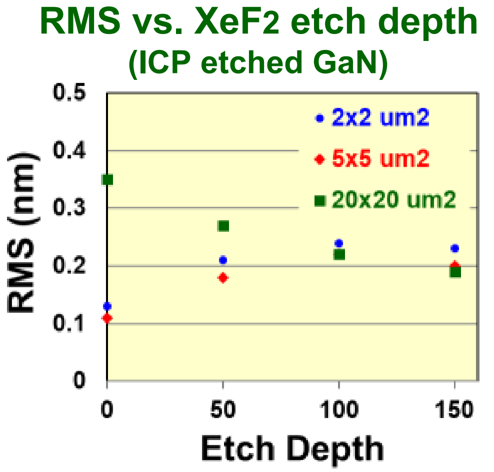




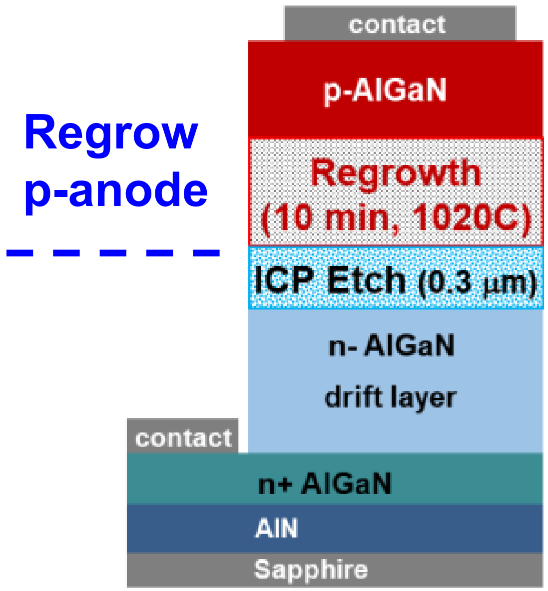


AFM of XeF2 etched - ICP etched GaN (air exposed)

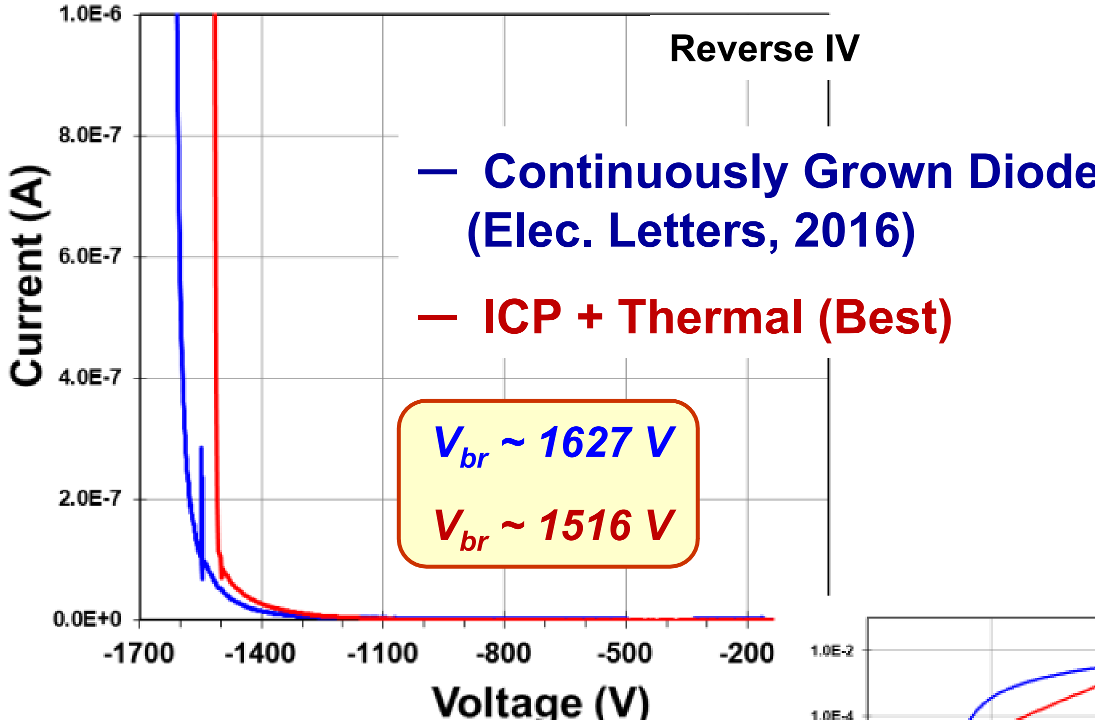


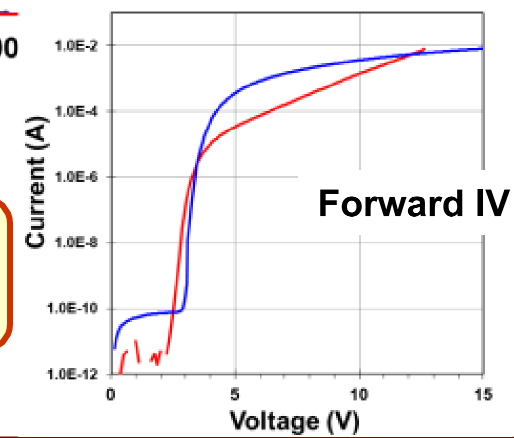


$Al_{0.3}Ga_{0.7}N$ "Quasi-Vertical" ***REGROWN*** PN diode on sapphire



- ***PN Diode IV Characteristics***





Regrown anode on ICP-etched drift region can produce AlGaN PN diodes equal to continuously grown diodes (c-plane)

$Al_{0.3}Ga_{0.7}N$ PN Diode: Regrowth on ICP etched drift layer

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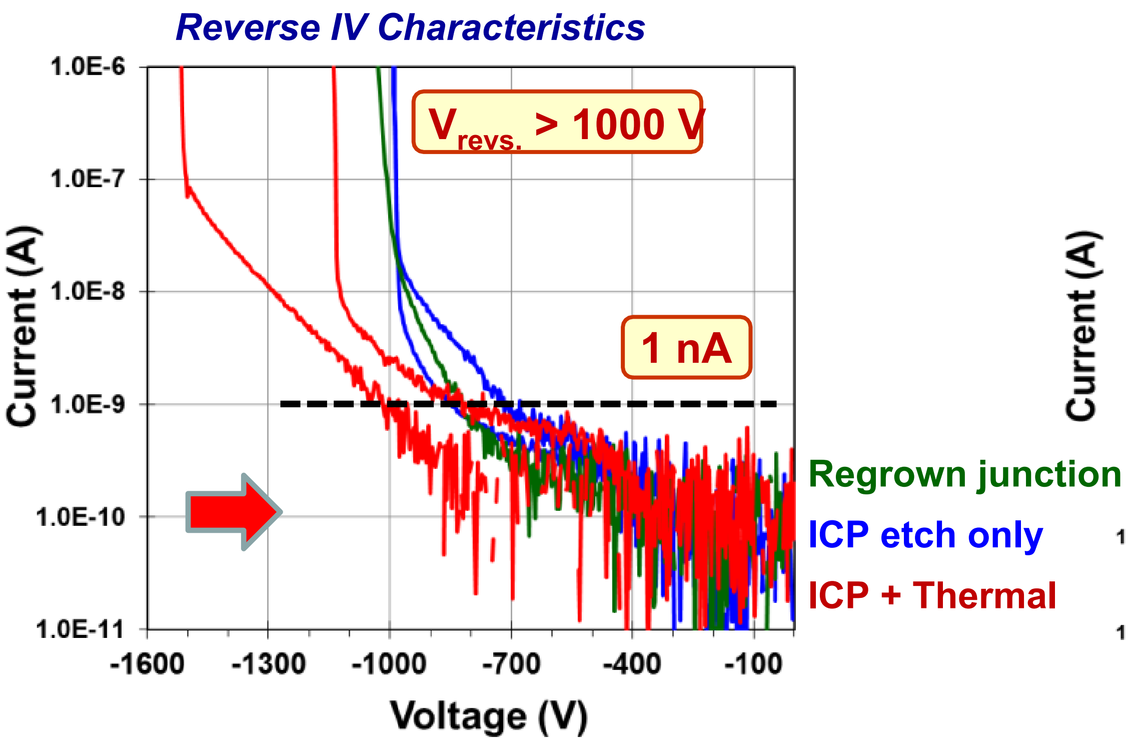
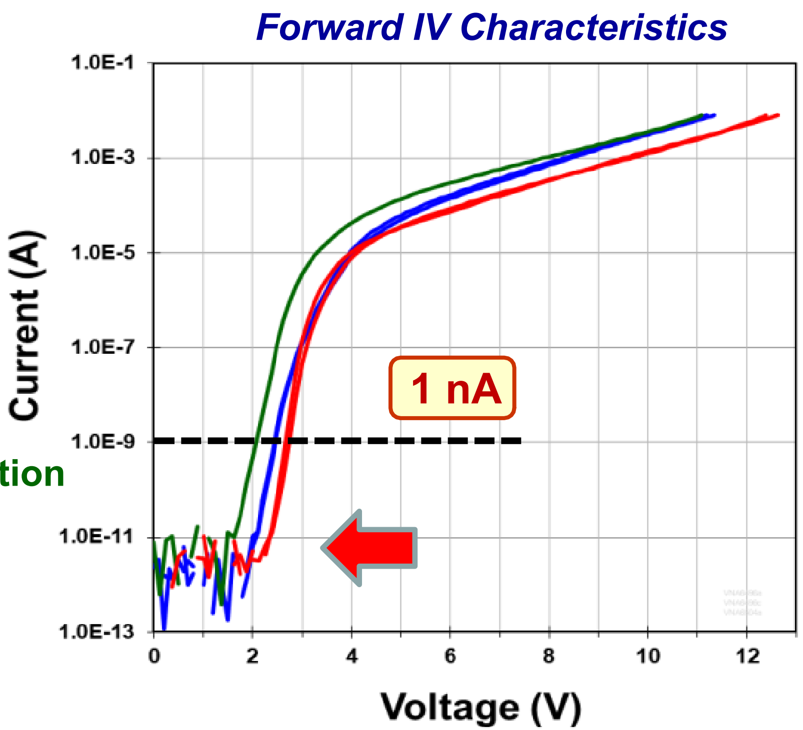
PN Diode IV Characteristics on an ICP-etched drift layer





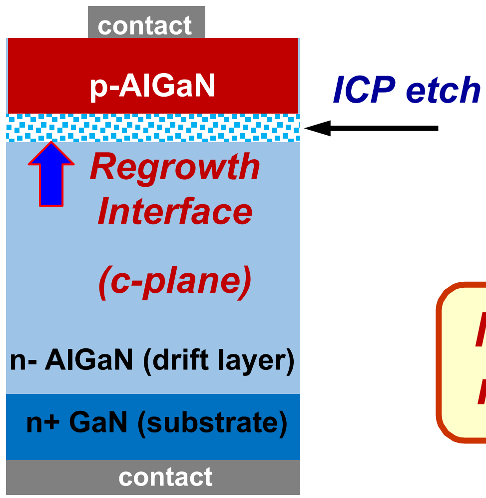
- **Regrowth with thermal treatment reached $V_{revs.}$ > 1500V (@ 1μA)**
- **Regrowth on "as-grown" diode repeated**
- **ICP-etched reached $V_{revs.}$ ~1000V (@ 1μA)**

- **Very low forward current leakage indicates a good PN junction (*TDD = low 10^9 cm^{-2}*)**

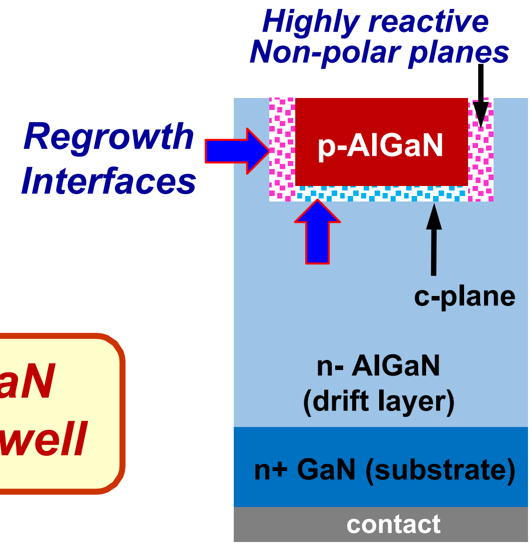
Regrowth of p-AlGaN on *ICP-etched* AlGaN yields kilo-volt class PN diodes with low leakage!

Next develop p-AlGaN regrowth in etched well

Regrowth on etched c-plane



Regrowth in etched p-well



Next develop p-AlGaN regrowth in etched well

NOT significant:

- **Electrically active impurities at regrowth interface**
- **Damage to crystal structure and point defects from ICP etch**

Still in question:

- **Incorporation rates of impurities and growth rates depend on crystal plane**
- **Non-selective mask or etch-back**

PN diode by regrowth of p-30%AlGaN

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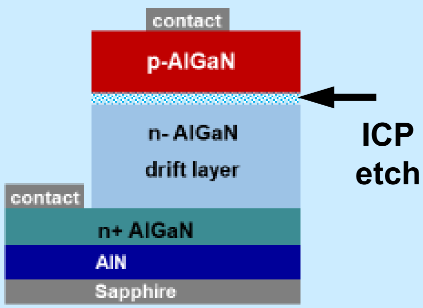
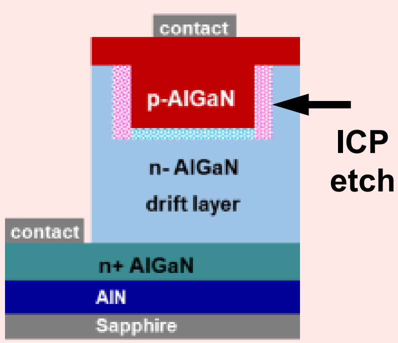
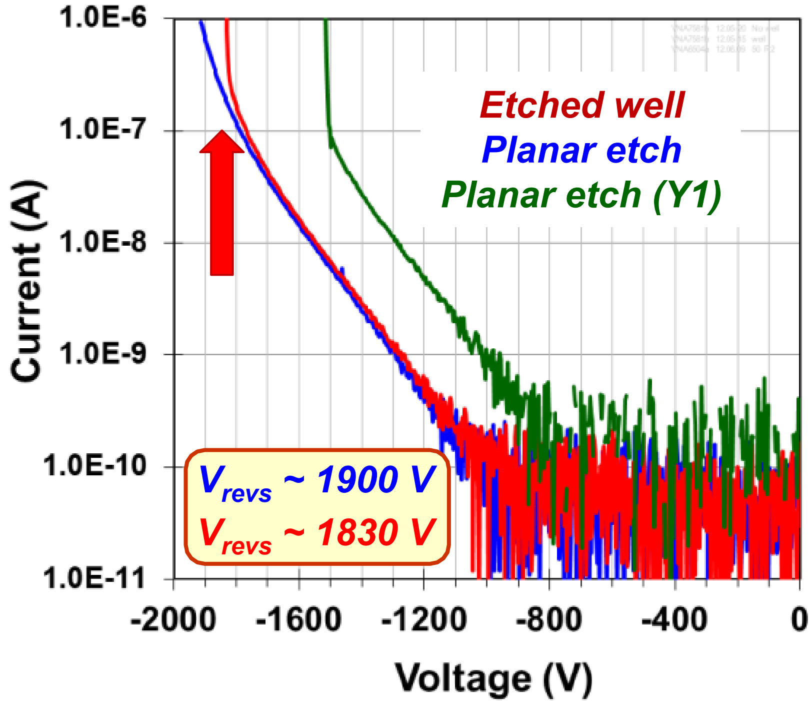
P- anode regrowth on planar etch drift layer



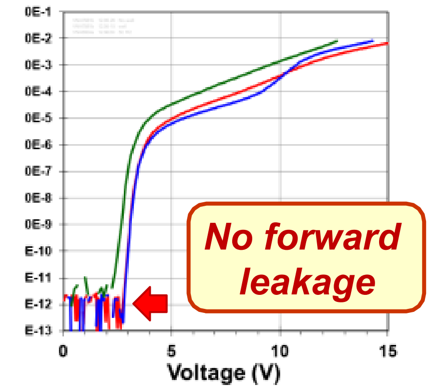
P- anode regrowth in *etched well* in drift layer



Reverse IV



Forward IV



Reverse leakage < 10^{-10} A out to 1kV (noise floor)

I_{revs} ~ 2e-6 A/cm^{-2}

- *NO difference between regrowth in etched well, planar etch and continuous growth! ($Al_{0.3}Ga_{0.7}N$)*
- *First SArG PN junction equal to continuously grown PN junction*
- *Foundational element for practical power devices: MPS diode and J-FET, D-MISFET transistors*

Summary

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- **Plasma etched and regrown PN diodes in GaN face two problems**
  - **Due to crystalline defects induced by dry-etch process result in high revers leakage currents**
  - **High levels of Si contamination are present at the regrowth surface**
- **Use of novel XeF2 source in MOCVD is effective at in-situ etching of GaN to remove residual ICP etch damage**
- **XeF2 is effective at removing Si contamination on the surface of GaN epilayers**
- **High performance regrown AlGaN PN diodes are tolerant to residual etch damage and surface Si contamination, unlike regrown GaN diodes**

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