

Maintaining Low Voiding Solder Die Attach for Power Die While Minimizing Die Tilt

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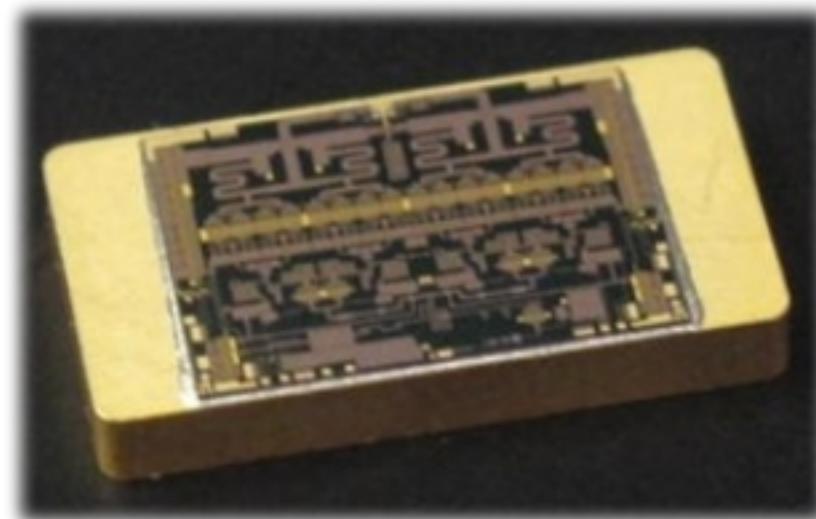
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Background

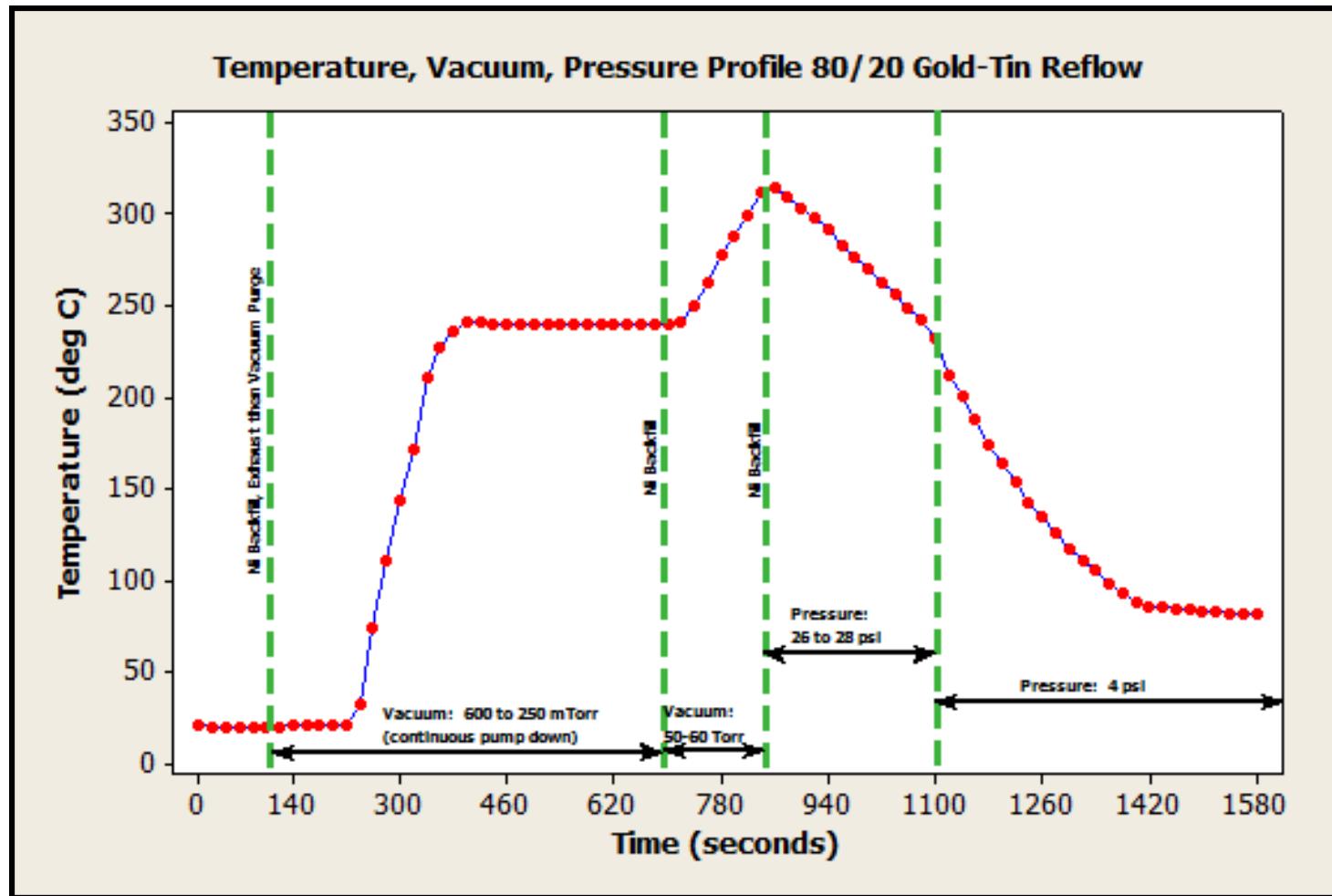
- **Multichip module critically dependent on a large gallium-arsenide (GaAs) power amplifier die**
 - Die size: 9.0 X 6.5 mm
 - Dissipates 75 Watts of energy
- **Assembly Process**
 - Die soldered to thermally conductive heat spreader using 80Au-20Sn
 - Die-on-spreader assembly then incorporated into MCM
- **Customer Requirements**
 - Low voiding percentages in critical locations
 - Consistent bondline
 - Minimizing die tilt
- **Measurement**
 - Acoustic Image
 - Voiding locations
 - Voiding percentages
 - Bondline and die tilt
- **Improved**
 - Die functionality
 - Reliability
 - Manufacturability



Assembly Process

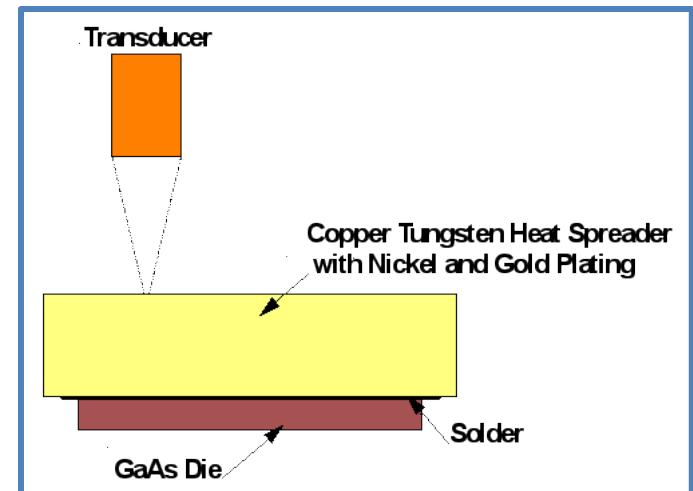
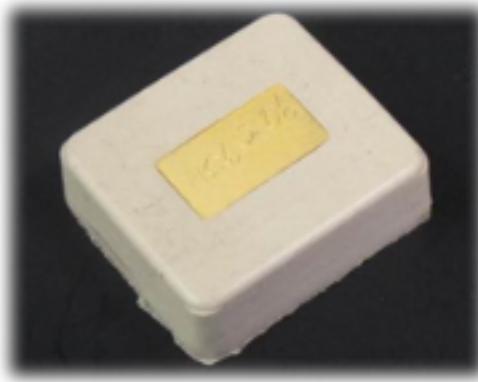
- **Process developed for soldering large GaAs die to nickel-gold plated copper-tungsten heat-spreader**
 - Gold (4 μm) on die backside
 - Nickel (4 μm)/gold (1 μm) plated spreader
- **Pick-and-place with pulsed heat and scrub was attempted**
 - Successfully used on smaller die (1.25 mm x 1.25 mm)
 - Did not work for this larger die, significant voiding
- **Batch process vacuum solder reflow station (SST International Model 1200)**
- **80Au-20Sn solder preform**
 - 50 μm thick
 - 50 μm smaller than die in both X & Y
- **Temperature profile with vacuum/pressure transitions at critical times**
 - Solder melted under vacuum so if voids exist, they are vacuum-filled
 - Pressure then imposed to help collapse the voids

Temperature Profile with Vacuum/Pressure Transitions



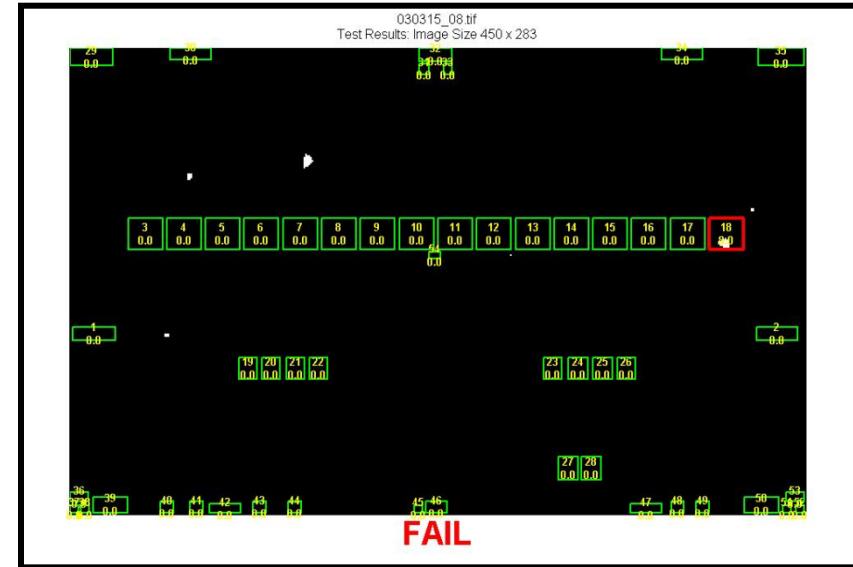
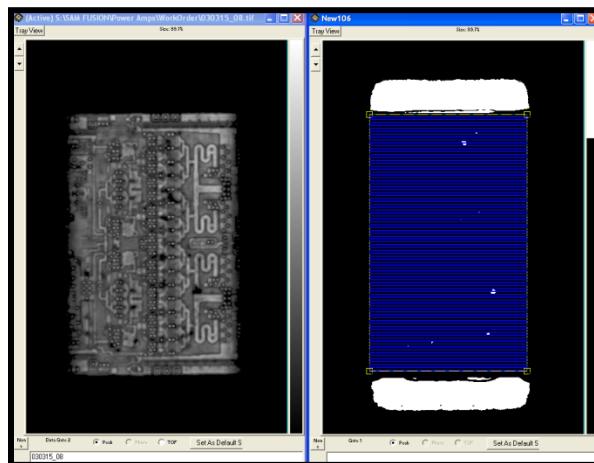
Acoustic Imaging

- **Acoustic imaging used for evaluation of the solder die attach**
 - X-ray not a viable option because of density of copper-tungsten spreader
 - Acoustic imaging preformed using 100 Mhz, 6.4 mm diameter, 12.7 mm focal length transducer
 - Images taken of solder joint from the spreader side
- **Assembly mounted in rubber boot**
 - Immersion in water
 - Seals around edge of the spreader
 - Keeps die dry and free from contamination

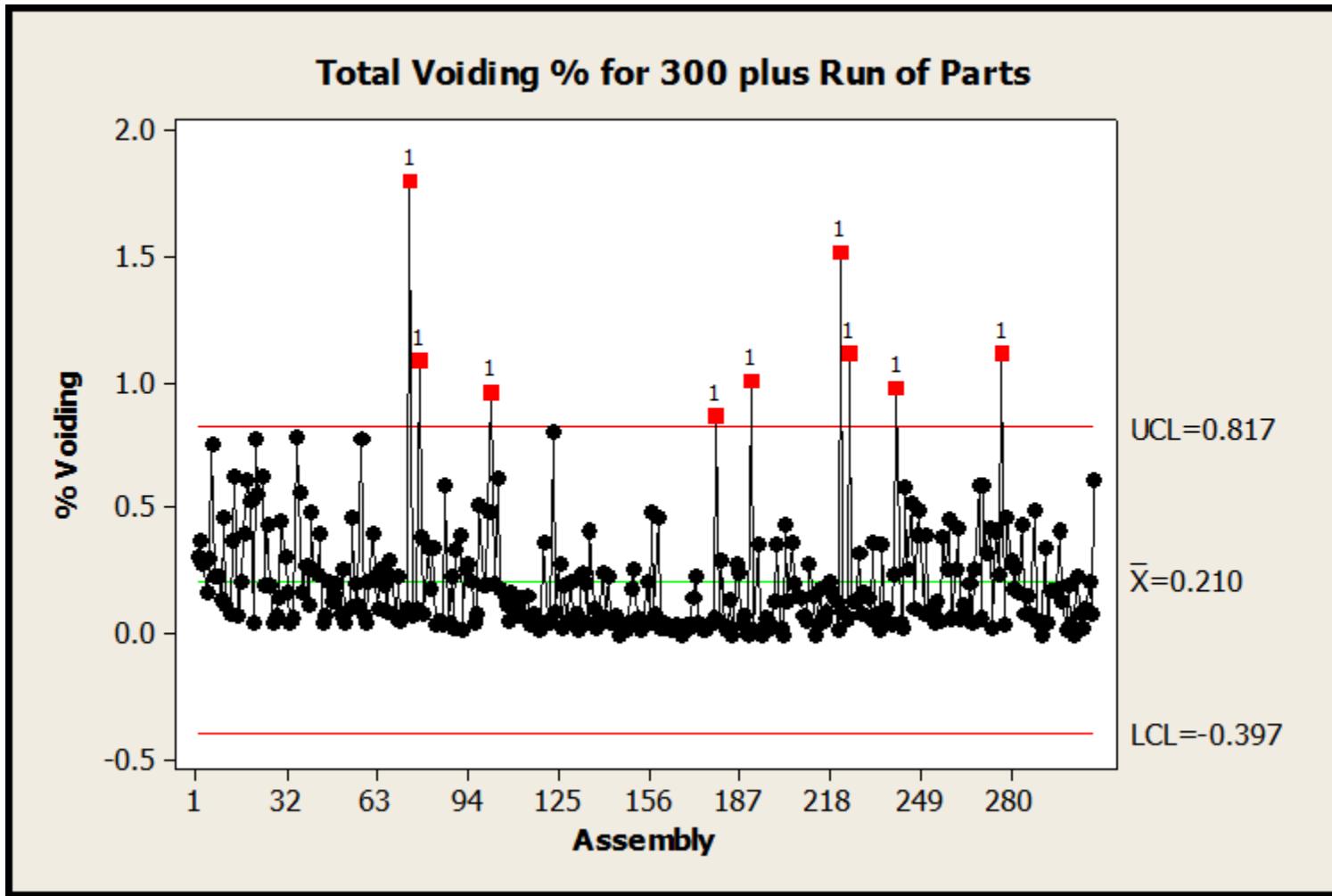


Acoustic Imaging

- **Units imaged, resulting in gray scale picture**
 - Grey scale converted to black and white, using appropriate sensitivity level
 - Calculation is made of total voiding, which is tracked and used for process control
- **For pass/fail used Matlab with overlay of critical die zones**
 - Determine location and size of voids under thermally or mechanically critical zones
 - Maximum voiding allowed in thermally critical zones is 5% (FETs and diodes)
 - Maximum voiding allowed in mechanically critical zones is 20% (wirebond pads)
 - Rejects a void with a lateral size of 15 μm under a FET in a 50 μm bondline
 - Pass/fail rate of approximately 75%



Total Voiding Tracked for Process Control

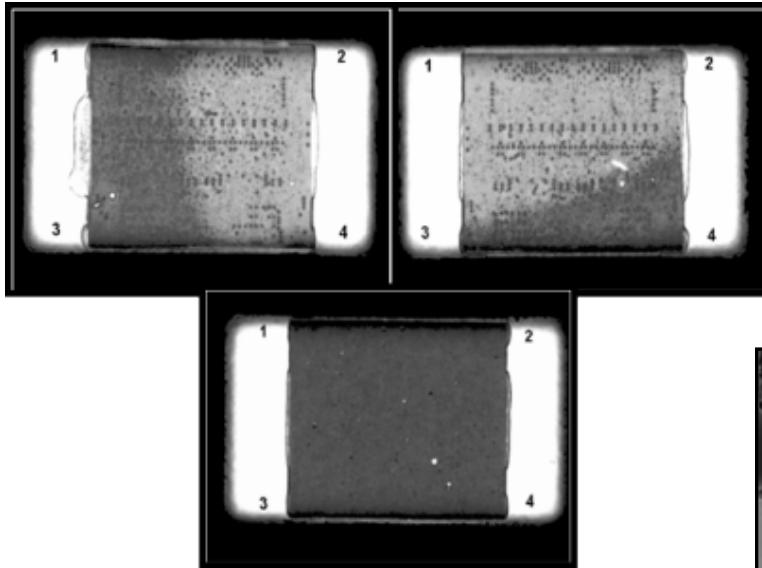


Bondline and Die Tilt Measurement

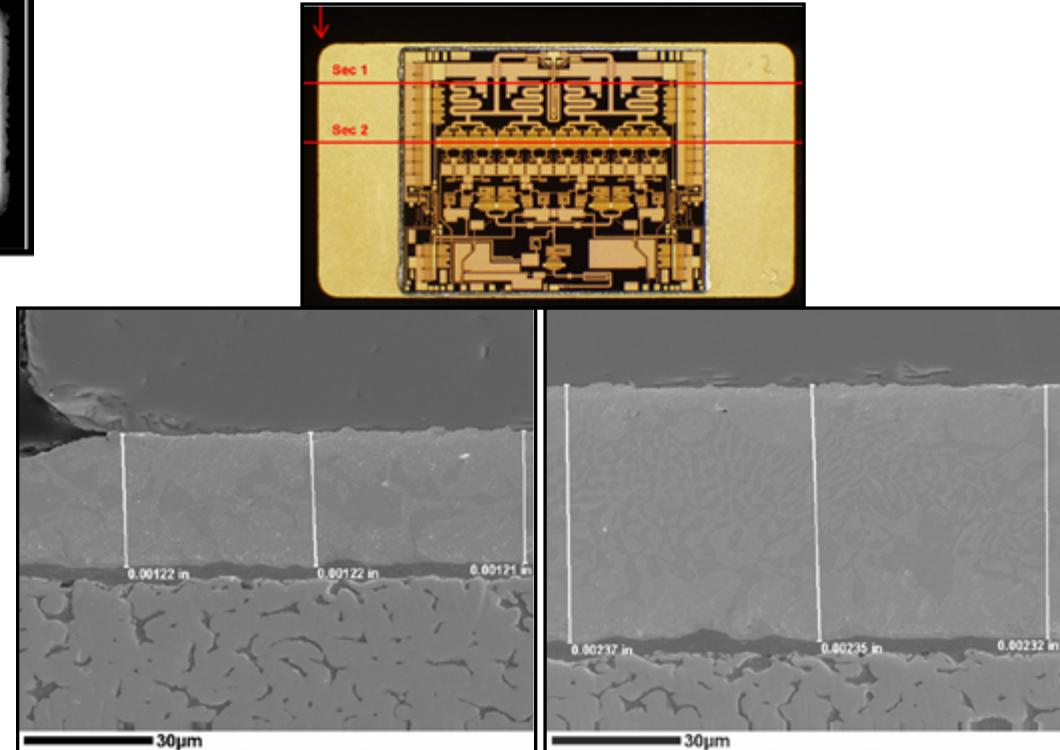
- **Bondline and die tilt measured for all parts**
 - An optical method and non-contact laser profilometer method evaluated
 - Chose the non-contact laser profilometer
 - Reliable data
 - Easier to use
 - Height measurements taken at four corners, from heat spreader top surface to active surface of the die
 - Subtract die thickness (100 μm)
 - Four corner measurements averaged to get estimate of bondline thickness
 - Minimum measurement subtracted from maximum measurement to get estimate of die tilt
- **Initial review of acoustic images**
 - Difference in gray scale intensity across part
 - To confirm grey scale image to die tilt correlation, parts cross sectioned

Bondline and Die Tilt Measurement

Grey Scale Images Showing Potential Die Tilt



Cross Sections to Verify and Measure Die Tilt



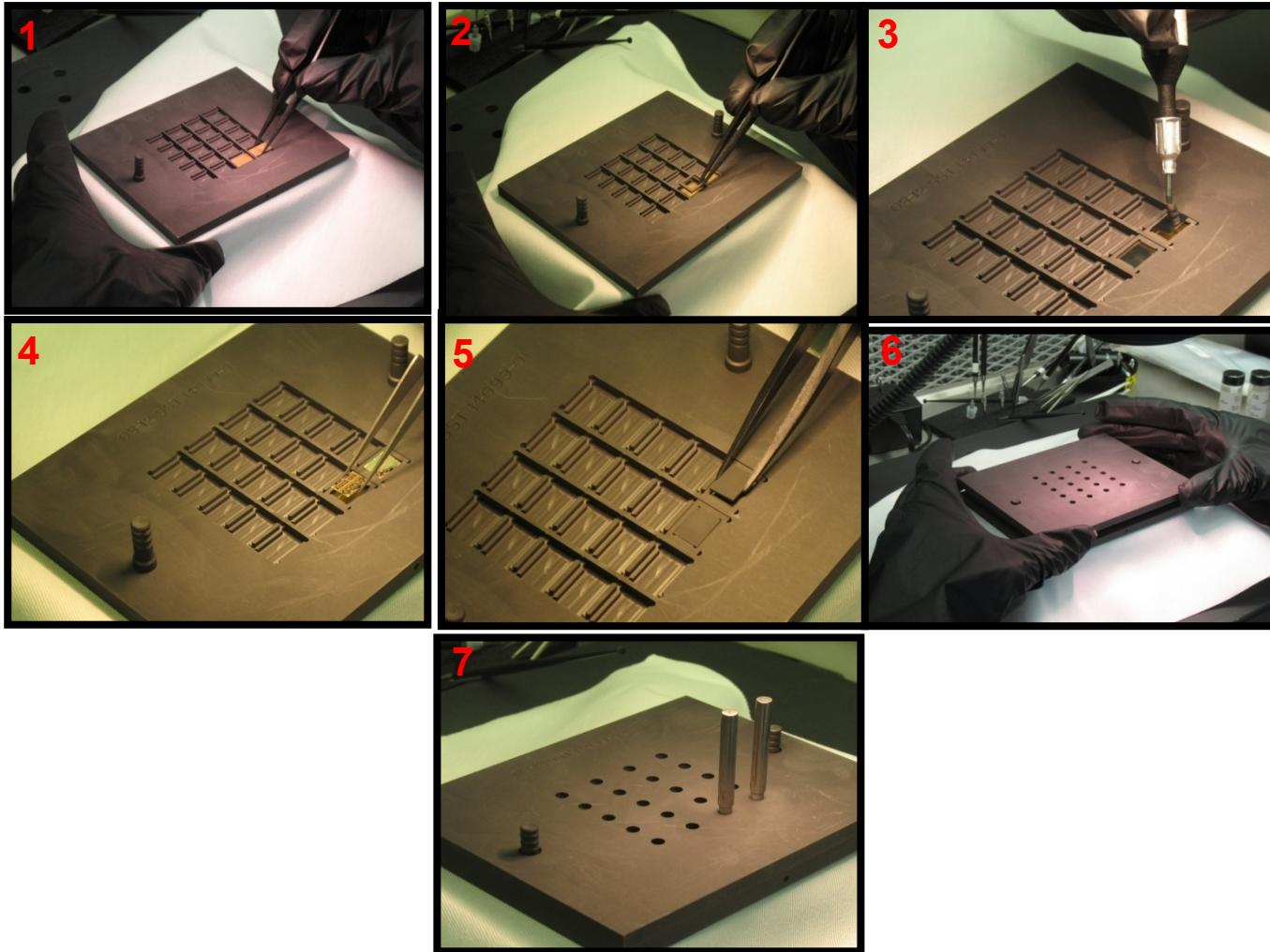
- Die tilt ranged from 30-50 µm across die (0.2 degree tilt)
- Darker gray scale is thicker bondline
- Lighter gray scale is thinner bondline

Minimizing Die Tilt Experiment

- In batch process vacuum solder reflow station (SST International Model 1200) graphite tooling is used
 - Easy to machine and good thermal conductor
 - Graphite machined to create tooling to hold the spreader, solder preform and die in place
 - Weight is applied with rods via a bezel placed on top of the die
- Tooling variables were the bezels and the weight rods
 - Three different bezels
 - Three feet: touch the die on top (designed to evenly apply weight but avoid air bridges and other critical circuitry)
 - Four feet: touch the die on top (designed to evenly apply weight but avoid air bridges and other critical circuitry)
 - Edge: touch top surface edge (angled walls, similar to inverted pyramid scrub collet)
 - Two weight rod combinations
 - One weight: rod at center of bezel
 - Two weights: rods at both ends of bezel
 - 4 grams of total weight to minimize voiding
 - > 4 grams weight caused solder to wet and flow onto prohibited areas of the spreader
- A group of parts soldered and measured for each combination of bezel and weight
- Best tooling combination for minimizing die tilt
 - 3 footed bezel with 1 weight rod
 - All combinations using a single weight rod had lower average die tilt than combinations with 2 weight rods
- Original goal was to achieve die tilt of 12 μm or less
 - Present process can attain 24-40 μm tilt across a 9.0 X 6.5 mm die
 - This amount of tilt was acceptable based on computer simulation and direct temperature measurements during operation

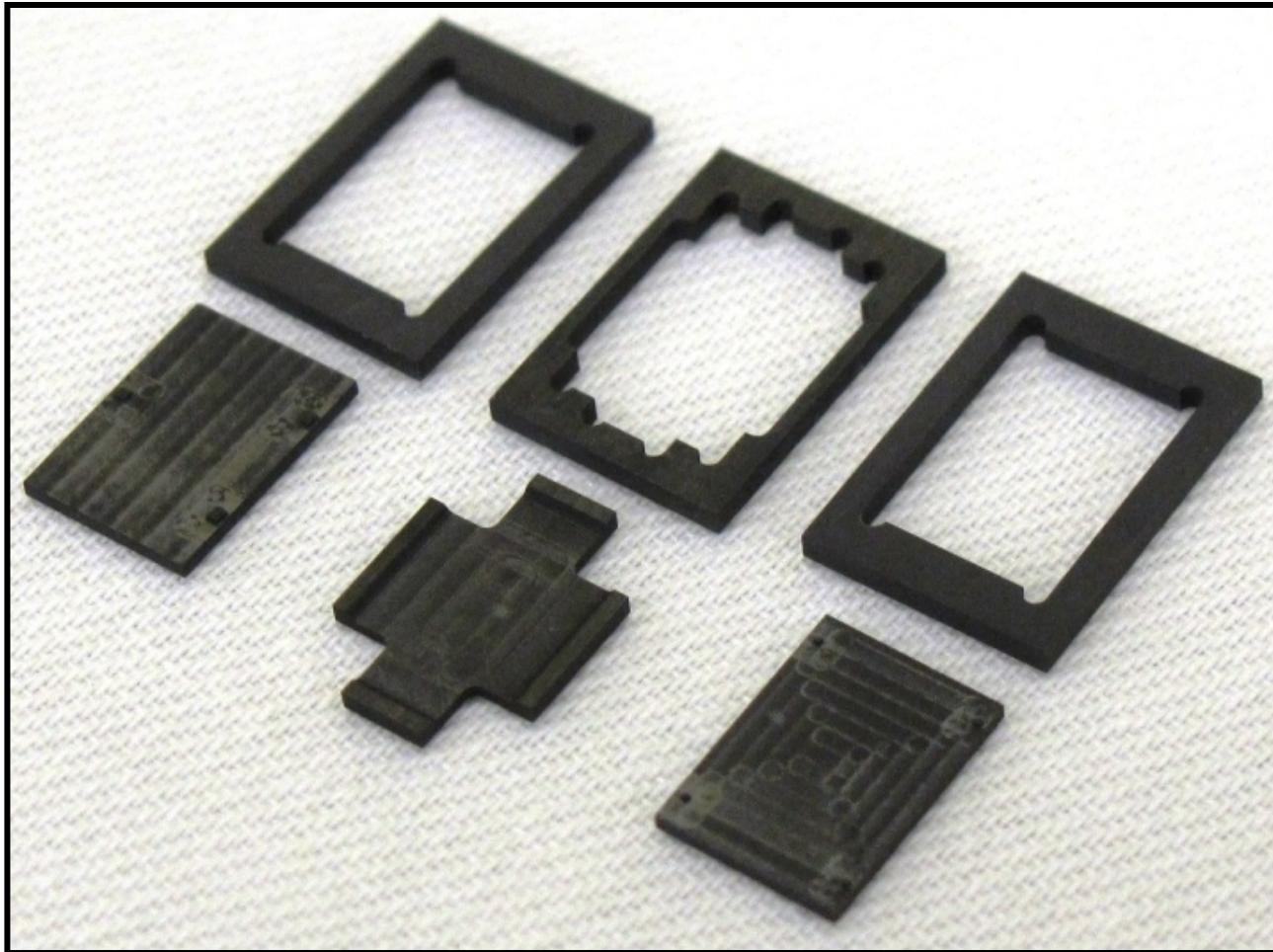
Minimizing Die Tilt Experiment

Tooling with Bezels and Weight Rods

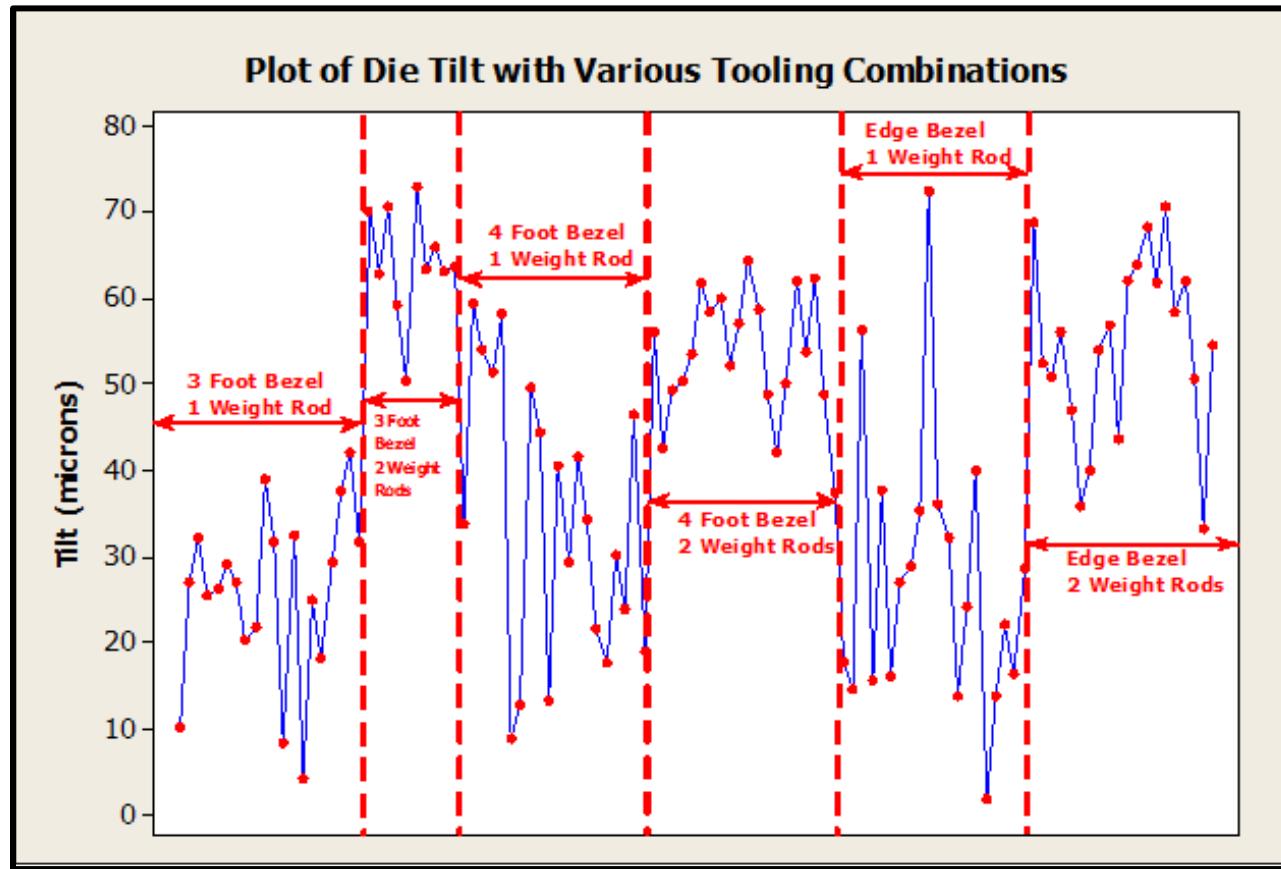


Minimizing Die Tilt Experiment

Graphite Bezels: 3 feet, Edge and 4 feet



Minimizing Die Tilt Experiment



Bondline and Tilt Measurements (μm)						
Tooling Combo	3 ft/1 Weight	3 ft/2 Weight	4 ft/1 Weight	4 ft/2 Weight	Edge/1 Weight	Edge/2 Weight
Bondline Avg	47.2	49.7	41.4	40.4	43.6	41.9
Bondline Std Dev	2.82	2.59	2.03	3.07	4.67	4.50
Tilt Avg	26.0	64.1	34.5	53.5	27.6	54.6
Tilt Std Dev	9.68	6.10	15.49	7.19	15.77	10.31

Conclusions

- **Assembly process**
 - Die soldered to thermally conductive heat spreader using 80Au-20Sn
 - Temperature profile with vacuum and pressure transitions at critical times
- **Customer requirements**
 - Low voiding
 - Minimizing die tilt
- **Acoustic image with Matlab and image overlay**
 - Maximum voiding percentages (5% and 20%) allowed under critical zones
 - Pass/fail yield rate of 75% was achieved
- **Die tilt measured non-destructively and verified using cross section**
- **Evaluation of tooling combinations to minimize die tilt**
 - 3 footed bezel with 1 weight rod best for minimizing die tilt
 - All combinations using a single weight rod had lower average die tilt than combinations with 2 weight rods
- **Present process can attain 24-40 μm die tilt across a 9.0 X 6.5 mm die**
 - Original goal was to achieve die tilt of 12 μm or less
 - This amount of tilt was acceptable based on computer simulation and direct temperature measurement of die during operation

Acknowledgments

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References

- [1] L. Yin, L. Yang, G. Zu, H. Yan, Y. Chen, W. Yang, S. Li, J. Zhang, "Effects of die-attach materials on the optical durability and thermal performances of HP-LED, Proceedings, 2011 Int. Conf. on Electronic Packaging Technology & High Density Packaging, pp.1116-1119.
- [2] G. Q. Lu, J. N. Catala, Z. Zhang, J. G. Bai, "A lead-free low temperature sintering die attach technique for high performance and high temperature packaging," IEEE CPMT Cong. On High Density Microsystem Design and Packaging and Component Failure Analysis, June-July 2004, pp. 42-46.
- [3] P .J. Wang, J. S. Kim, C. C. Lee, "Fluxless bonding of large silicon chips to ceramic packages using electroplated eutectic Au\Sn\Au Structures," Journal of Electronic Materials, Vol. 38, No. 10, 2009, pp. 2106-2111.
- [4] T. A. Tollefson, A. Larsson, O. M. Lovvik, K. E. Aasmundtveit, "High temperature interconnect and die attach technology: Au-Sn SLID bonding," IEEE Trans. CPMT, Vol. 3, No. 6, June 2013, pp. 904-914.
- [5] T. Tak-Seng, D. Sun, H. K. Koay, M. F. Sabudin, J. Thompson, P. Martin, P. Rajkomar, S. Haque, "Characterization of Au-Sn eutectic die attach process for optoelectronics device," Proceedings, 2005 Int. Symp. on Elect. Mat. And Packaging, (EMAP 2005), December 11-14, 2005, pp. 118-124.
- [6] J. C. McNulty, "Processing and reliability issues for eutectic AuSn solder joints," Proceedings IMAPS 2008, pp. 909-916).
- [7] G. Matijasevic, C. Lee, "Void-free Au-Sn eutectic bonding of GaAs dice and its characterization using scanning acoustic microscopy," Journal of Electronic Materials, Vol.18, No. 2, 1989, 327-337.
- [8] V. R. Manikam, S. Paing, A. Ang, "Effects of soft solder materials and die attach process parameters on large power semiconductor dies joint reliability," 2013, IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), pp. 152-155.
- [9] H. Zheng, Y. Wang, X. Luo, L. Xu, S. Liu, "Effect of die shape on die tilt in die attach process," Proceedings, 14th Int. Conf. on Elect. Pack. Tech., 2013, pp. 651-655.
- [10] G.S. Matijasevic and C.C. Lee, "A reliability study of Au-Sn eutectic bonding with GaAs dice," Proc.: 27th Annual Reliability Physics Symposium (1989) pp. 137-140.
- [11] C. Yue, M. Lu, Z. Niu, "The influence of die tilting on the thermal response and die attach stress of a bottom exposed package," Proc: Int. Conf. on Elect. Packaging Tech. & High Density Packaging, 2012, 685-690.
- [12] H. Zheng, Y. Wang, L.Li, and X.Luo, "Mechanism investigation on die tilt in die attach process based on minimal free energy theory," 2014 IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm) (2014) pp. 1251-1255.
- [13] J. F. DalPorto, D. H. Loescher, H. C. Olson, and P. V. Plunkett, "LSI packaging that passes PIND test", IEEE Trans CHMT, Vol. CHMT-4, No. 4, December, 1981, pp. 471-475.
- [14] S. S. Kim, J. H. Kim, S. W. Booh, T. G. Kim, and H. M. Lee, "Microstructural evolution of joint interface between eutectic 80Au-20Sn solder and UBM," Materials Transactions, Vol. 46, No. 11 (2005) pp. 2400-2405.
- [15] K. Mizuishi, M. Tokuda, Y. Fujita, "Fluxless and virtually voidless soldering for semiconductor chips," IEEE Trans. CHNT, Vol.11, No. 4, December (1988), pp. 447-451.
- [16] SST International, "Void-Free/Flu-Free Die Attachment for Multichip Modules