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Superconductor Electronics and the International Roadmap for Devices and Systems

D. Scott Holmes
Booz Allen Hamilton
College Park, Maryland, USA
scott.holmes@alum.mit.edu

Erik P. DeBenedictis
Center for Computing Research
Sandia National Laboratories
Albuquerque, New Mexico, USA

***Abstract*—The international technology roadmap for ~~devices and systems~~semiconductors (~~IRDS~~ITRS) ~~has replaced~~ changed its name to the ~~international~~ International technology ~~r~~Roadmap for ~~semiconductors~~ Devices and Systems (I~~T~~RDS)~~. The~~ to reflect a change in scaling driver from physical dimensions to applications requirements and ~~updated roadmapping process is driven by application requirements rather than by scaling of physical dimensions and is more open to~~ inclusion of a broader range of non-semiconductor technologies, such as superconductor electronics (SCE). We review ~~C~~current applications for SCE ~~are reviewed~~, ~~including~~ ranging from development~~al~~ activities to small-scale commercial products. ~~Larger scale applications such as~~Computational accelerators within data centers and other large applications will require significant improvements in circuit density, complexity, functional capability, memory capacity, and data rates in and out of the cryogenic environment. ~~A~~ We propose a process for developing an application-driven roadmap for superconducting digital computing ~~is proposed~~ that will include key decisions to be made by the superconductor electronics community.**

Keywords—superconductor electronics; SCE; SFQ; roadmap; ITRS; IRDS

I. Introduction

The International Technology Roadmap for Semiconductors (ITRS) [1] projected technology requirements and potential solutions for ~~the~~ semiconductor ~~industrys~~ ~~for about two decades~~from 2001-2014. The ITRS used ~~metrics such as~~ transistor feature sizes, density, ~~and~~ clock rate, and other metrics to roadmap ~~technology evolutio~~the future of~~n of~~ integrated circuits ~~(ICs)~~. In ~~2014~~2015, the ITRS committee presented a new roadmap, called ITRS 2.0, for key systems that contain integrated circuits and drive process, design, and integration technologies [2]. Subsequent partnering of ITRS 2.0 with the IEEE Rebooting Computing (IEEE RC) Initiative resulted in the International Roadmap for Devices and Systems (IRDS) [3].

The IRDS mission is to "Identify the roadmap of electronic industry from devices to systems and from systems to devices", which represents a broadening of the scope. "Beyond CMOS" is one of the focus topics and includes technologies other than Complementary Metal-Oxide Semiconductor (CMOS) electronics such as memristors, spintronics, straintronics, and superconductor electronics.

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Superconductor electronic circuits can be analog, digital, quantum, or hybrid [4]. Superconducting digital logic is based on the single flux quantum (SFQ) and includes logic families such as RSFQ [5], RQL [6], EFSFQ [7], eSFQ [8], AQFP [9], and phase mode logic [10]. Past SCE roadmapping efforts [11]–[20] ~~were not sustained, but~~ provide a base for future efforts. As participants in the Beyond CMOS committee, the authors ~~have~~ introduced superconductor electronics to the IRDS and ~~have initiated~~lead the first IRDS roadmap section for the area ~~the roadmapping process~~.

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II. Applications and Drivers for Superconductor Electronics

Among application areas relevant to superconductor electronics in Table I, research and development (R&D) is expected to be significant to dominant for the near term by measures such as chip area or money spent. This is different from semiconductor electronics, which is dominated by commercial applications. Current R&D drivers include quantum information processing, sensor and detector arrays, and superconducting computing.

TABLE I. SCE Applications and Drivers

Application	Drivers	Metrics
Research & development	Quantum information processing, advanced sensors, computing, government funding	Foundries, process design kits, process capability, layer count, feature sizes, yield
Metrology	Voltage standard	Accuracy, precision, voltage range, frequency range (for ac)
RF signal processing & control	RF processor	Clock rate, signal-to-noise ratio, bandwidth
Data pre-processing	DSP: digital signal processor	Clock rate, throughput, bits, circuit density
Network routing	SOC-NW: system-on-chip, networking	throughput
High performance computing	MPU-HP: microprocessor unit, high performance	Floating point computation, memory performance, data rate, chip area, physical volume, energy efficiency
Data center	Microserver	Integer computation, memory performance, data rate, chip area, physical volume, energy efficiency

Commercial applications currently include Josephson voltage standards [19], digital-RF receivers, and quantum annealing coprocessors for computing [4]. Cryogenic sensor arrays for astronomy and other applications are growing to the point that multiplexing and signal processing is needed close to the sensors. Quantum computing approaches that require cryogenic temperatures are likely to need RF signal processing and control as well as digital computation within the cryogenic space. Microprocessor units and memories are currently under development, but not yet available as commercial products. Further in the future are large-scale computing applications that require many parallel processors for high performance computing or data centers [21].

The application and driver examples included here are preliminary and require further development.

III. Benchmarking and Metrics

Beyond-CMOS electronics must consider new devices, circuits, and architectures. Determining which emerging or novel technologies are most promising and thus most deserving of development effort can be difficult, especially for significantly non-conventional technologies. Needed are fair metrics and figures of merit for comparison.

A. Devices and Circuits

Recent efforts to benchmark a variety of beyond CMOS technologies include [22]–[24]. Nikonov and Young [22] included in traditional energy-delay comparisons some state variables other than voltage (e.g., magnetization, polarization, spin current, orbital state) and extended comparisons from switching devices alone to logic circuits as large as an arithmetic logic unit (ALU). Still, the existing benchmarks and metrics are limited as computing also requires interconnects and memories, not just logic circuits, and did not consider superconducting electronics. One reason for the omission is that superconductive technologies have very different characteristics that make meaningful comparisons difficult at the level of devices or subcircuits.

As an example for how to add superconductor electronics to existing comparisons, consider switching energy versus delay for a 32-bit ALU. Nikonov and Young's projected data for ALUs using beyond-CMOS devices fabricated at the 10 nm scale is in Table 7 of their supplemental material [22]. ~~Energy and delay parameters are measured at the component level, a 32-bit adder in this example.~~

Dorojevets, et al. [25] give in their Table I ~~similar~~ data for ~~an~~ a simulated ALU using reciprocal quantum logic (RQL), a type of superconductor logic. The equivalent performance figures are 205 aJ/op (32 bit) and 402 ps delay for operation at 4.2 K with critical current density J_c = 100 μA/μm², device current I_c = 38 μA, and 16.3 GHz clock rate. ~~The equivalent performance figures are 205 aJ/op (32 bit) and 402 ps delay for operation at~~ ~~Characteristics at 4.2 K include:~~ ~~For reference, the Josephson Junction technology is characterized by a peak current of~~ ~~J_c = 100 μA/μm², a device current of I_c = 38 μA, and a clock rate of 16.3 GHz.~~ For direct comparison at 300 K, the energy dissipated at 4.2 K must be multiplied by a factor to account for refrigeration. Refrigeration efficiencies of commercially available refrigeration systems vary depending on capacity and type, so a range was used from 10,000 to 400 (W @ 300 K)/(W @ 4.2 K) [21]. The result is shown in Fig. 1. ~~205 aJ/op (32 bit), 402 ps.~~

~~For direct~~Meaningful comparison ~~must account for the difference in operating temperature, room temperature (300K) vs. the energy dissipated at 4.2 K, and differences in interconnect wire behavior must be multiplied by a factor to account for refrigeration. The result is shown in Fig. 1., with the differences explained in detail below.~~

Some applications require the electronics to run a~~There are energy overheads for both conventional and superconducting electronics. Given perfectly Carnot efficient refrigeration and accounting for both the computer's power supply and refrigerator energy, the energy of a computer operating at 4.2 K should be multiplied by the factor 300K / 4.2K to compute equivalent wall-plug energy. There is an additional overhead of about 2× for power management and air conditioning in conventional machine rooms. The equivalent overhead for cryogenic computers is the inverse of the Carnot efficiency, which would tend to be in the range of 4-5 for a large installation. To compare ALUs that must operate a~~ at 4.2 K, such as digital-RF receivers, focal plane arrays for astronomy, quantum computing, and magnetic resonance imaging (MRI). ~~t~~The RQL point in Fig. 1 would drop by a factor of 1,000 for these applications while the ~~and the~~ other points would stay about the same. In this case RQL has a clear advantage over the other technologies considered. ~~Examples of applications with a cryogenic environment that could benefit from cold data processing include digital-RF receivers, focal plane arrays for astronomy, quantum computing, and magnetic resonance imaging (MRI).~~

A generalized methodology for comparing superconductor electronics with other technologies will require several developments. To avoid the effort of full-circuit simulations performed in [25], models must be developed for circuit area, delay, and energy for a variety of superconductor technologies. Interconnect delay and energy models are needed for both Josephson transmission lines (JTL) and passive transmission lines (PTL). Clocking delay must be included for logic families such as RSFQ that require clocking of each gate. Standard refrigeration multipliers and ranges are required as a function of operating temperature. Also ~~needed, but yet to be resolved, is a fair accounting of~~ are benchmarks and metrics specifically for wire delay in cryogenic computing technologies. ~~The energy versus delay plots of [9] are a start, but need to add considerations such as the number of gate operations per clock cycle~~correct at the gate level, but computers must wire gates together to be meaningful. In CMOS systems, the energy and delay attributable to wires dominates system performance. Superconducting wires, in contrast, propagate signals at a consistent velocity of about 1/3 the speed of light across an entire chip without repeaters. ~~Some logic families such as RSFQ require clocking of each gate, and thus can perform only 1 operation per clock cycle, whereas other logic families such as RQL and phase-mode logic have combinational gates that allow multiple gate operations per clock cycle.~~

Commented [HD[2]: Notes:
1. Accounting for delay in gates that must be clocked (set gate delay = clock cycle time?)
2. Wire delay and energy. Note that a JTL has delay of tau ~ 2 ps and energy ~ Phi_0 * Ic for each stage and the length of a stage is proportional to 1/Ic. A PTL has overhead of about 2x a single JTL stage, plus the transmission time (small for all but long lines).

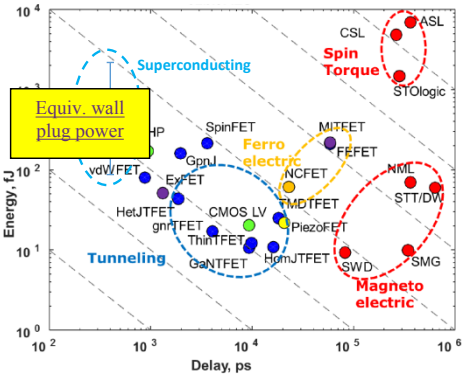

Fig. 1. Switching energy at 300 K versus delay for a 32 bit ALU. Superconducting ALUs show a range ~~of~~ for commercially available refrigeration efficiencies from 10,000 to 400 W/W (300 K/4 K) with the dot at 1,000 W/W.

B. *Systems and Applications*

Pan and Naeemi [24] make the case that some beyond-CMOS devices offer fundamentally different or unique characteristics best suited to novel circuit implementations not well evaluated by traditional metrics and benchmarks. ~~Needed are m~~IRDS will need methods for including energies and delays of key system components to more accurately predict the performance of complete digital computing systems based on emerging technologies. ~~A first step for evaluating s~~We expect superconducting digital computing ~~will be to create~~ to address this need through a figure of merit including both computation and communication (data movement).

IV. Technology Roadmaps

A technology roadmap is worthwhile when the benefits from coordination and collaboration exceed the effort required. Superconducting digital computing is one application area that could benefit from a technology roadmap as multiple organizations will be required to make useful products ~~and~~. For example, foundries capable of producing complex circuits are too expensive for most organizations to support.

Each IRDS team will assess present status and future evolution of the ecosystem in their specific field of expertise and produce a 15 year roadmap. Initial roadmaps are being developed for presentation in late 2017. Given the current state of the technology, the initial roadmaps for SCE are expected to be far less detailed than those for CMOS.

A. *SCE Technology Roadmap*

IRDS roadmaps will include current, near-term (next 7 years), and long-term (following 8 years) coverage with projections for odd years. Technology areas in the SCE roadmap might include: foundry and fabrication processes, packaging and integration, and design tools.

Foundry and fabrication is a key technology area for SCE and faces some challenging decisions. Foremost is identification of suitable foundries. Of the two foundries currently capable of producing complex superconductor circuits (>100,000 Josephson junctions), MIT Lincoln Laboratory ~~cannot~~ is not allowed to produce commercial products and the D-Wave Systems foundry has limited access. Needed is at least one foundry that can handle the materials specific to SCE and produce commercial products with sufficient yield. Multi-project wafer (MPW) service seems desirable, but will require well-characterized processes and more complete process design kits (PDKs) than currently available. New materials, processes, and devices will need to be added. How these will be developed and incorporated into the foundries is an open question. The achievable rate of progress must be considered.

The packaging and integration area might include parameters such as chip sizes, contact count and layout, and memory interface specification.

B. *Scaling Models*

Models are needed to predict achievable metrics such as circuit density, complexity, or efficiency from parameters in the technology roadmap. The effort can start from previous work such as [9], [26]–[27], but will need to be extended considerably.

V. Conclusions

Participation in the IRDS process gives the SCE community a seat at the table and a framework for creating and maintaining technology roadmaps for our benefit. Anyone interested in participating should contact the authors or the IRDS.

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