SAND2022-4429C

RFIC

Mo3B-1

# A 0.2-2 GHz Time-Interleaved Multi-Stage Switched-Capacitor Delay Element Achieving 448.6 ns Delay and 330 ns/mm² Area Efficiency

T. Forbes, B. Magstadt, J. Moody, A. Suchanek, S. Nelson



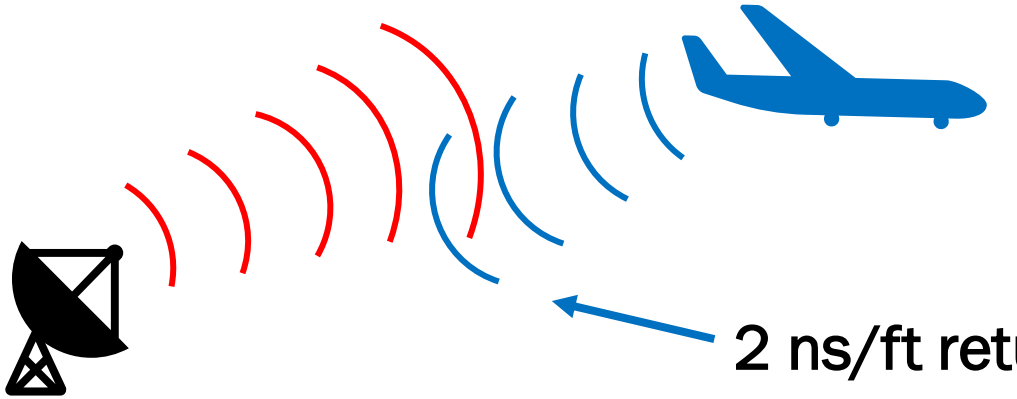

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

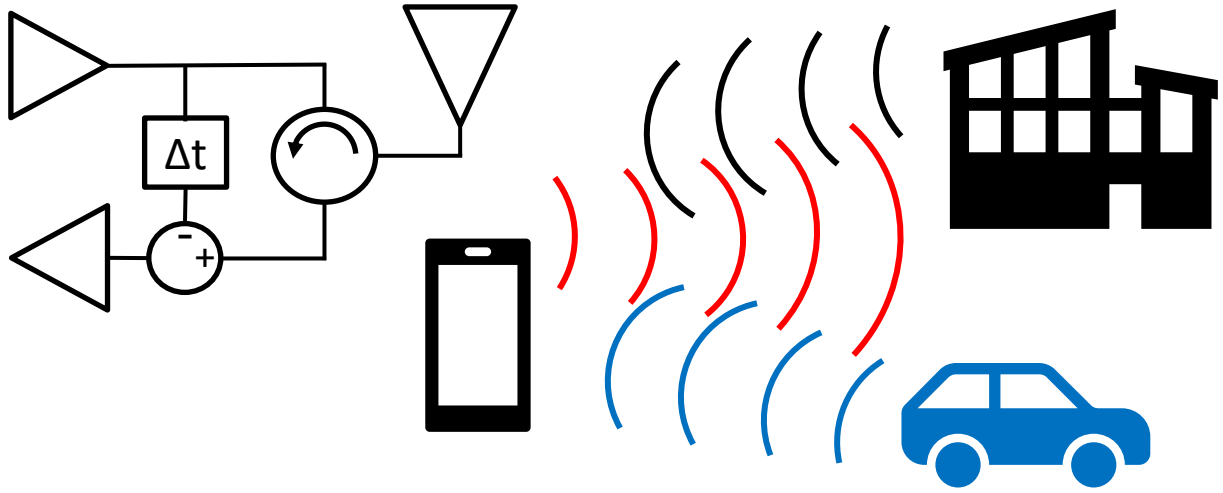
# Outline

- Motivation and Prior Art
- Delay Element Operation
- Circuit Implementation
- Measurement Results
- Conclusion

# Motivation – Limited RF Time Delay

- Radar return simulation
  - Radar testers and DRFM
- Require > 400 ns broadband programmable delay at RF
  - RF delay elements today < 8 ns
  - Digital delay consumes watts

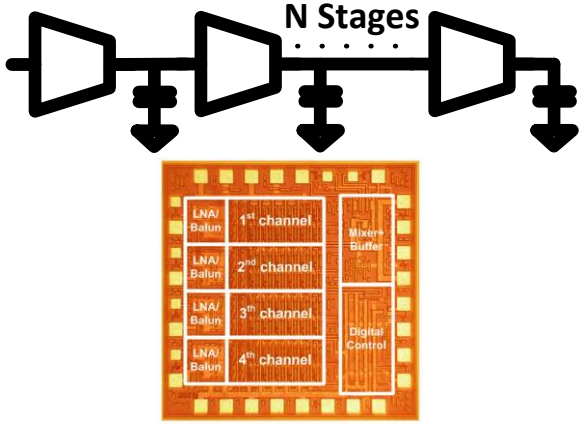



- Full-duplex communication looks just like a radar
  - Objects such as cars and metal buildings have large reflections
  - Will require >> 30 ns delays in canceller at RF to deploy

# Prior RF Delay Approaches

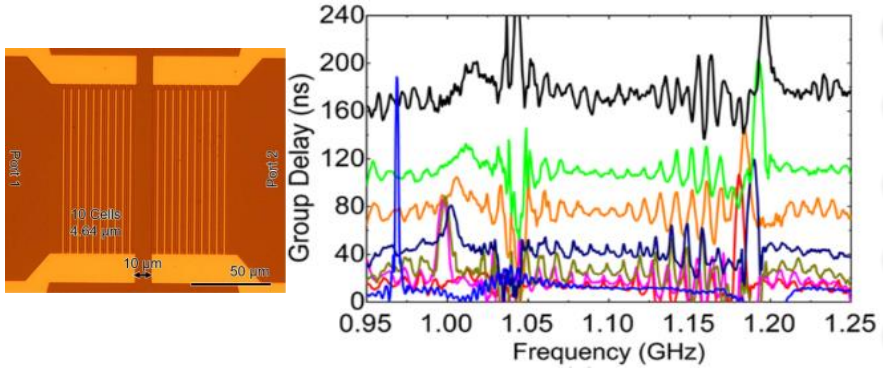
## Gm-C All-Pass Filter




Garakoui et al., IEEE JSSC 2015

- < 2 ns delay
- Moderate Area
- Broadband
- Programmable
- Delay Variation

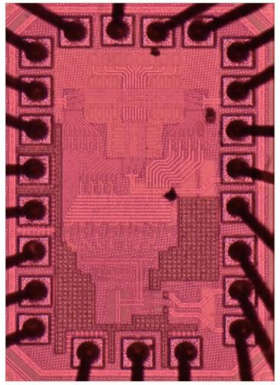
## SAW Delay Line

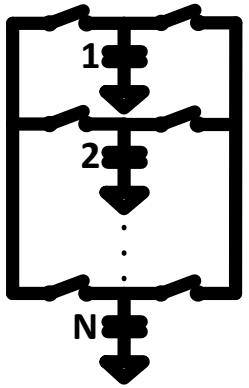



Lu et al., IEEE MTT 2021

- > 400 ns delay
- Small Area
- Narrowband
- Fixed Delay
- Delay Variation

## Switched-Capacitor

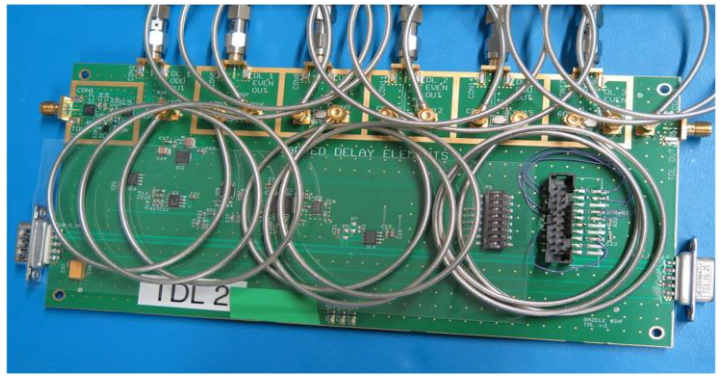





Nagulu et al., IEEE RFIC 2020,
IEEE JSSC 2021

- < 8 ns delay
- Small Area
- Broadband
- Programmable
- Delay Variation

## Coaxial Delay




Gadringer et al., IET Radar, Sonar & Navigation 2018

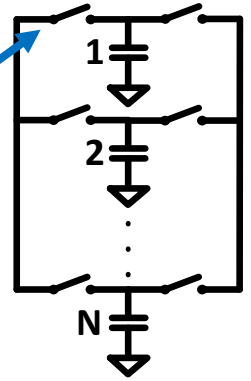
- > 400 ns delay
- Large Area
- Broadband
- Fixed Delay
- Delay Variation

# Switched-Capacitor Delay Challenges

## Switched-Capacitor

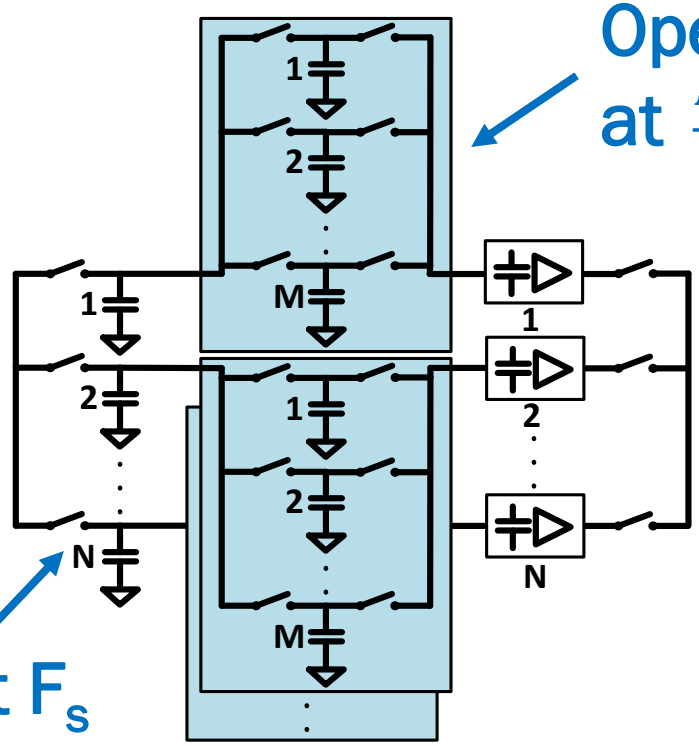
- ~450 ns Delay @ $F_s$ = 3.3 GHz
  - >1480 sampling capacitors
  - >1480 phase sampling clocks
  - Large RF load capacitance
- Switch leakage challenge
  - Max Delay $\frac{N-1}{F_s}$

Sample in $\frac{1}{F_s}$ time but hold for > $\frac{1480}{F_s}$ time




## Proposed Approach

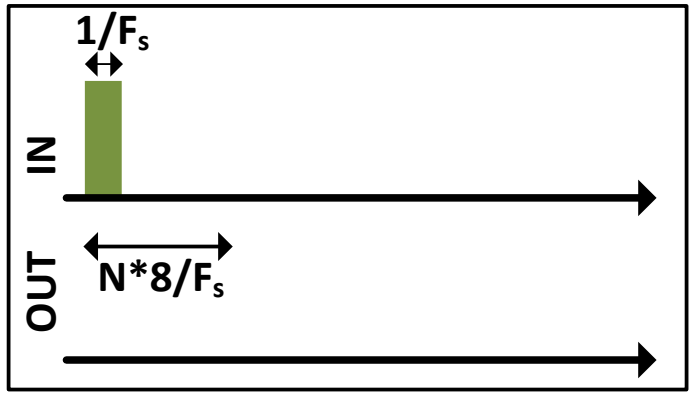
Operate at $\frac{F_s}{N}$

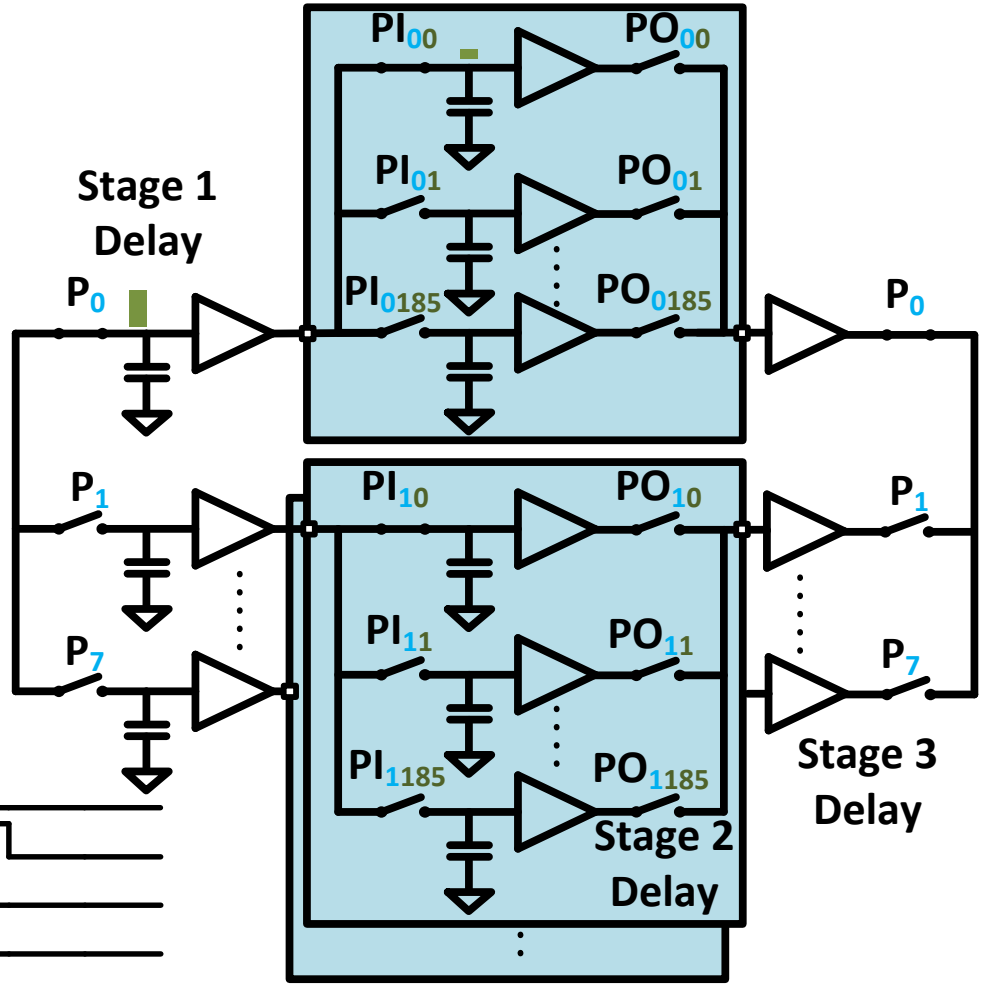


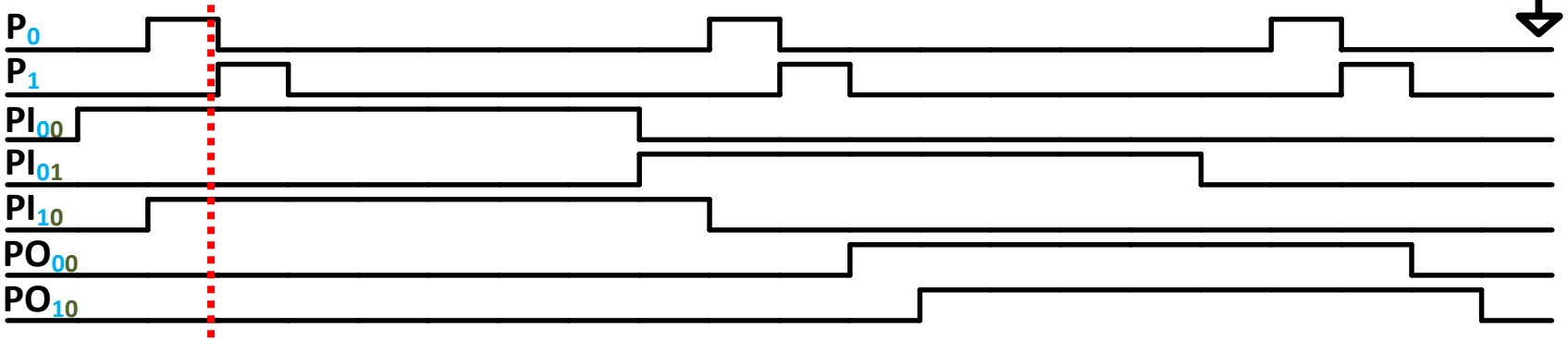

Operate at $F_s$

- Max RF Delay $\frac{N(M-1)}{F_s}$
  - Leakage mitigated through time expansion

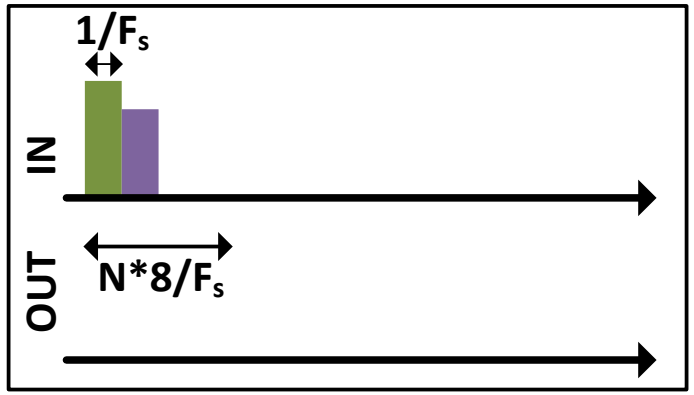
# Time-Interleaved Multi-Stage Approach

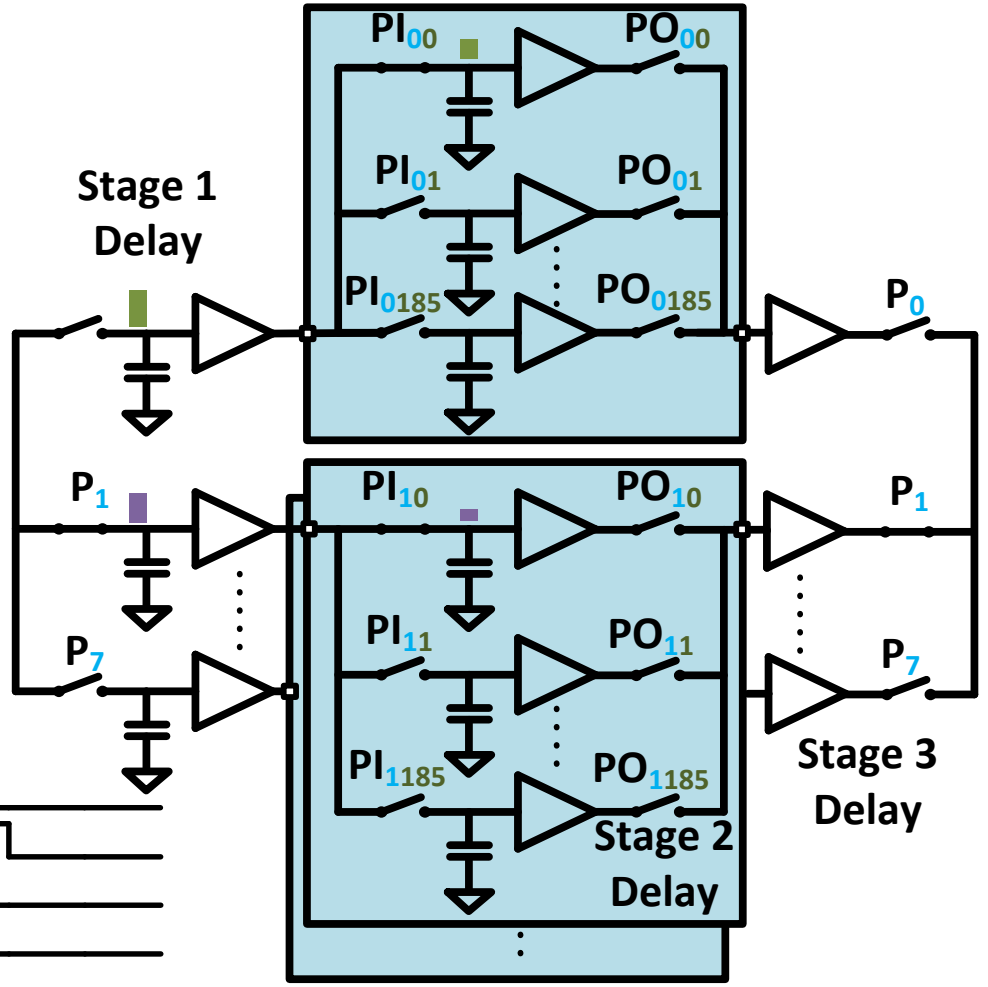


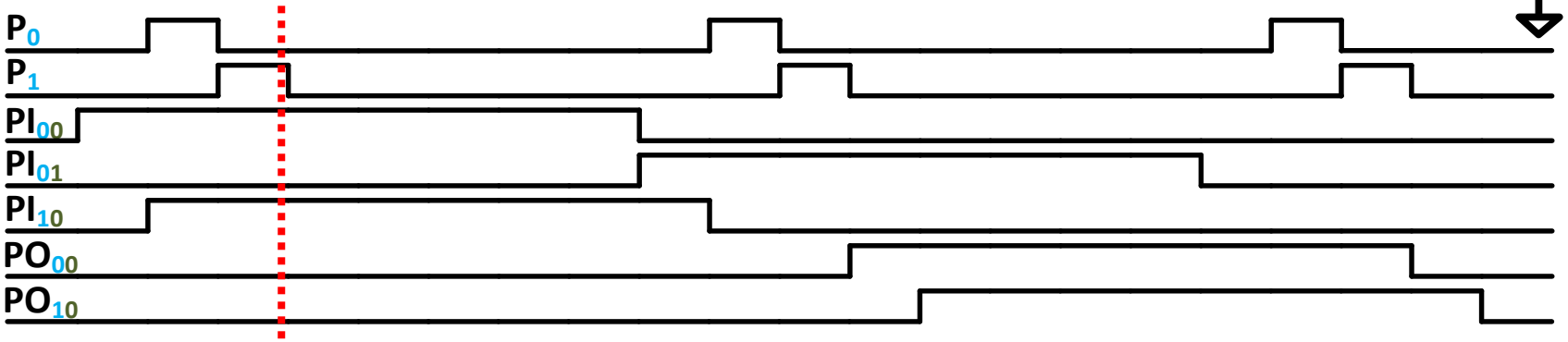



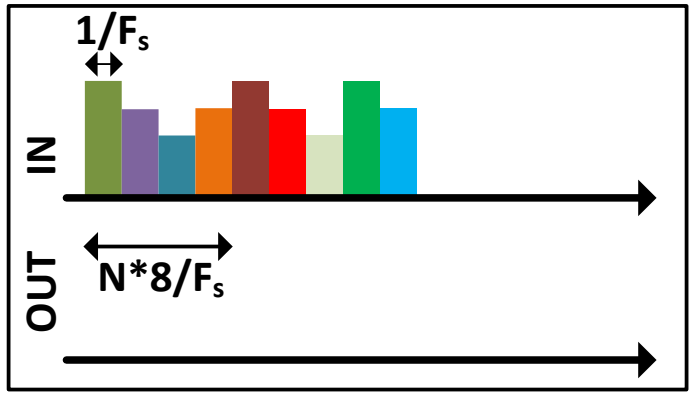
# Time-Interleaved Multi-Stage Approach

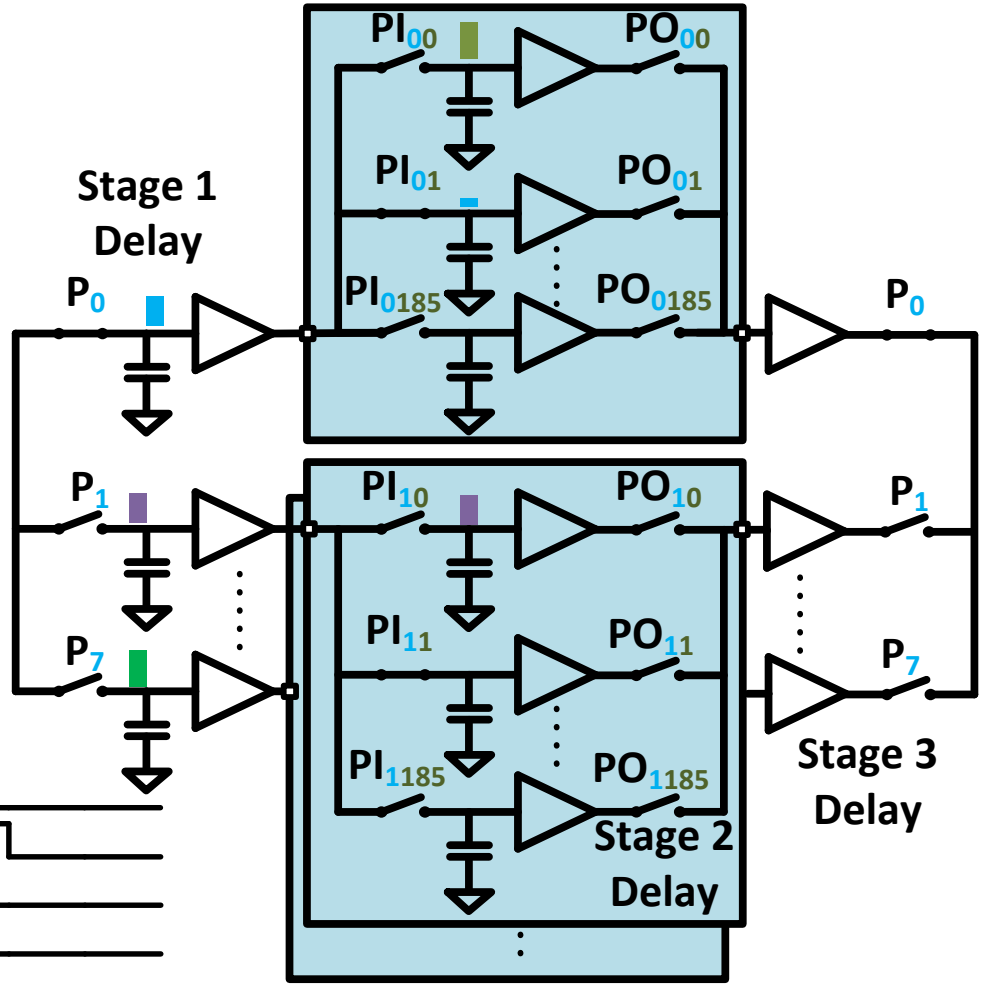


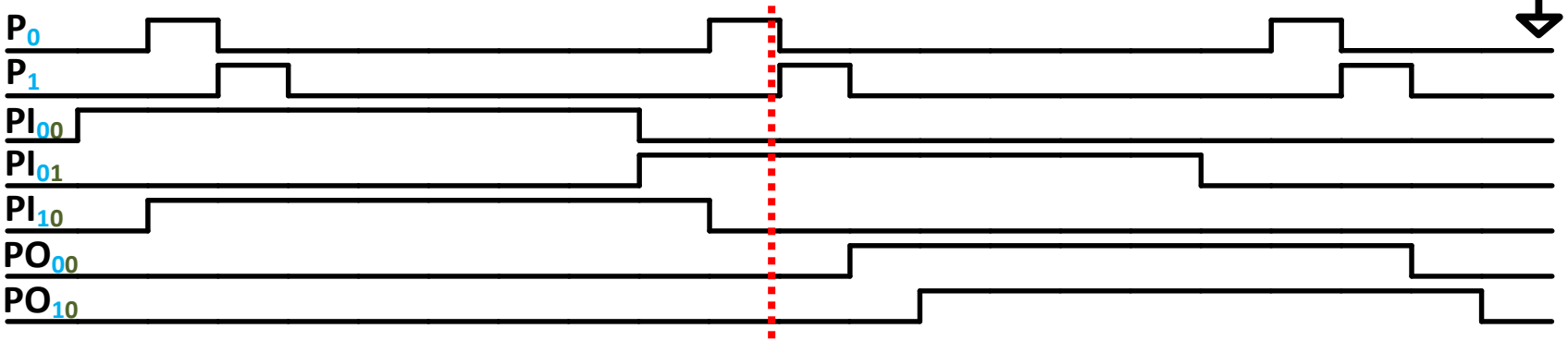



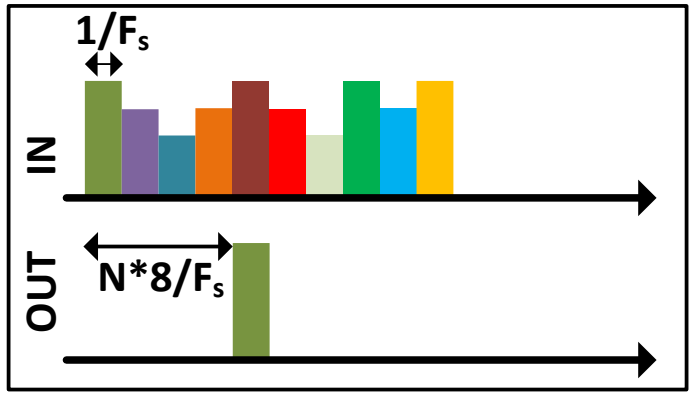
# Time-Interleaved Multi-Stage Approach

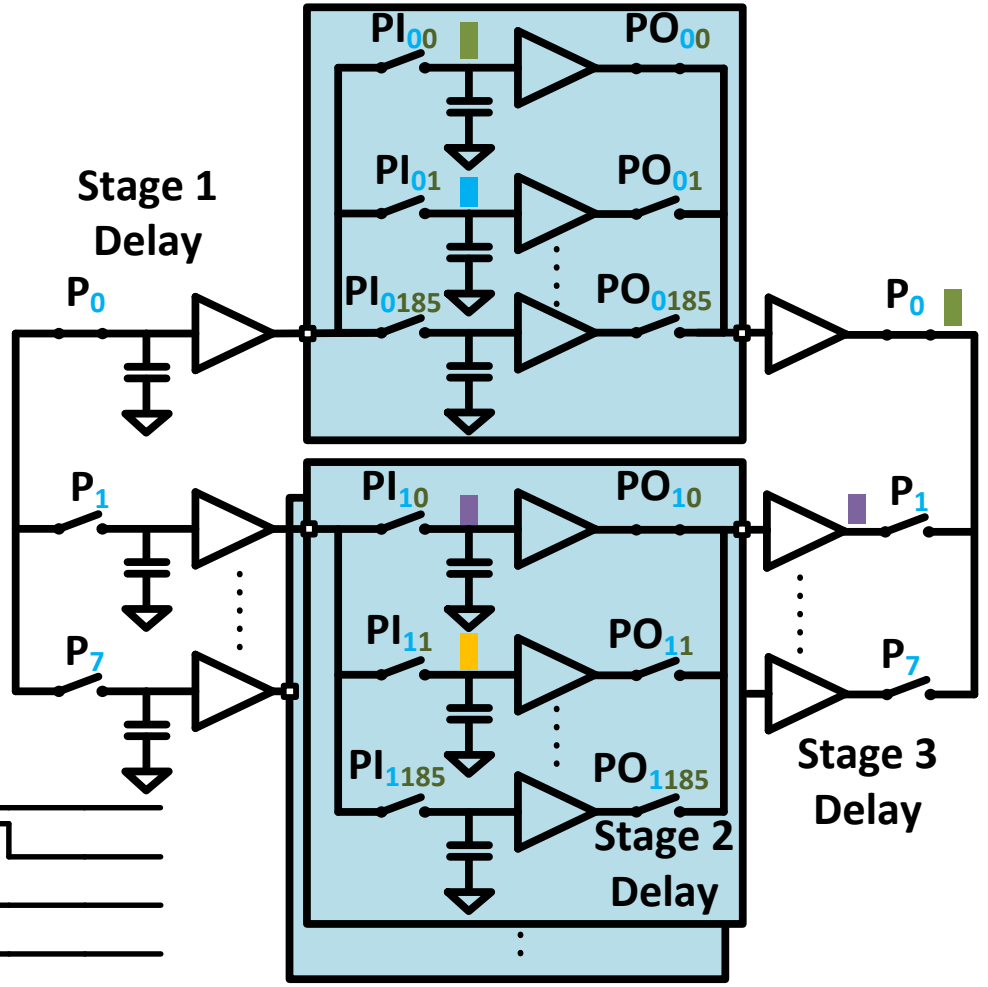


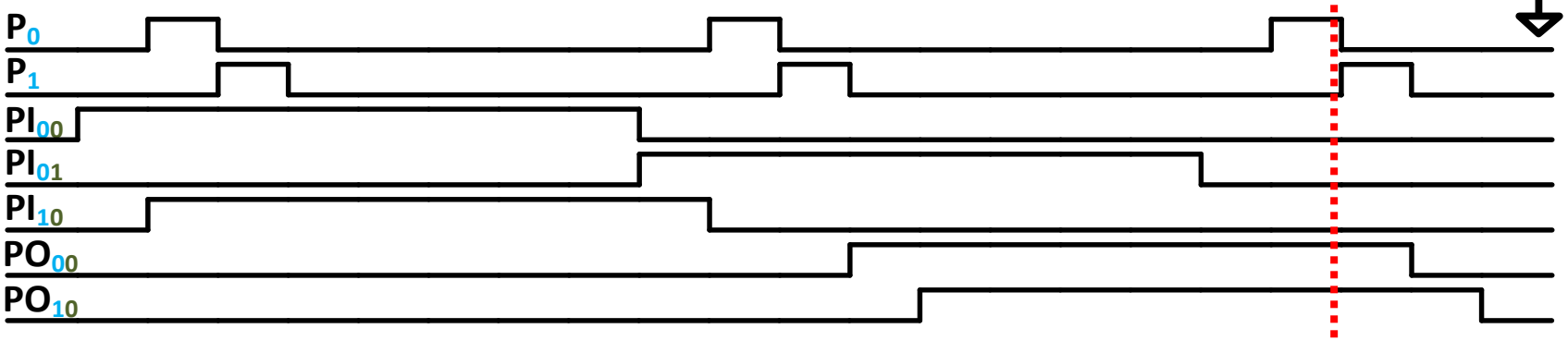



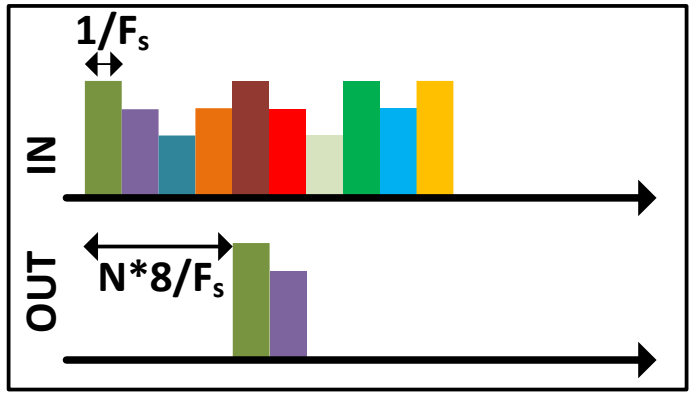
# Time-Interleaved Multi-Stage Approach

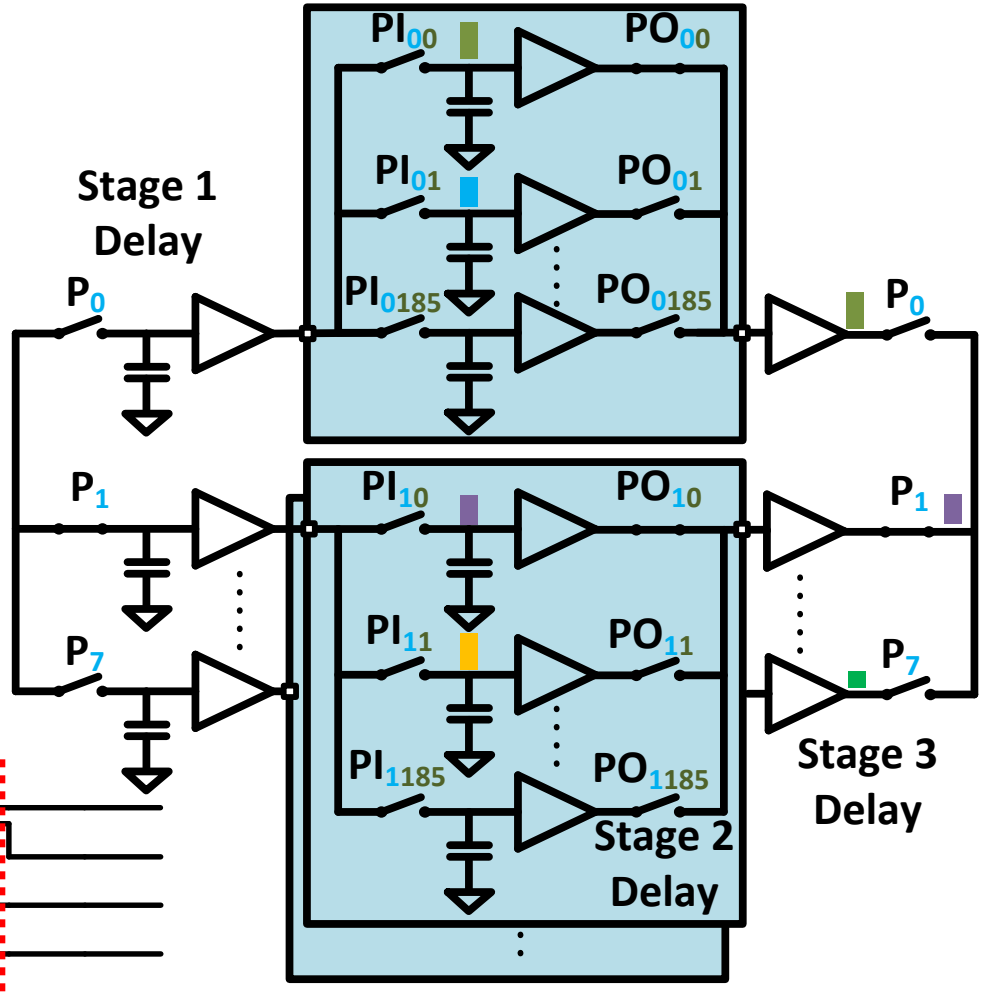


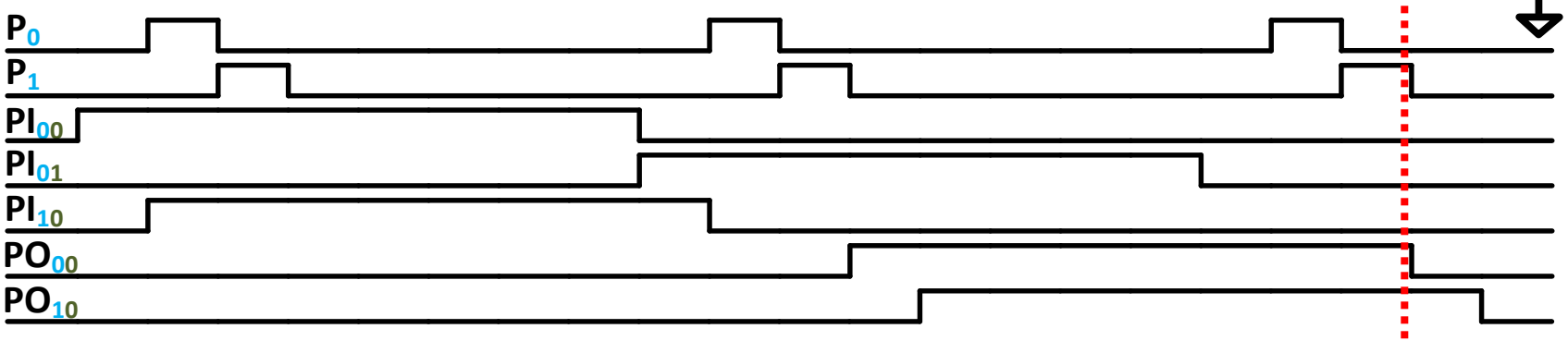



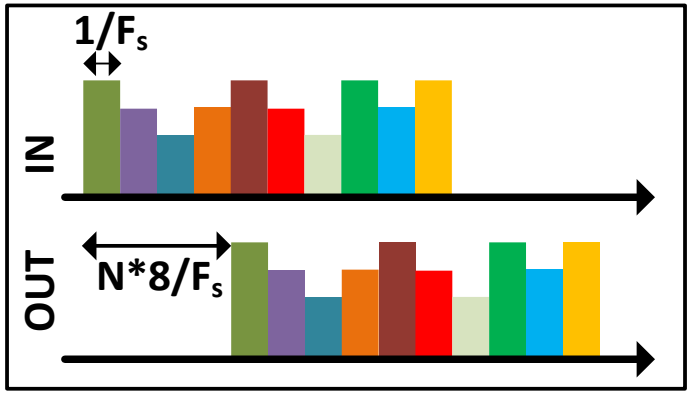
# Time-Interleaved Multi-Stage Approach

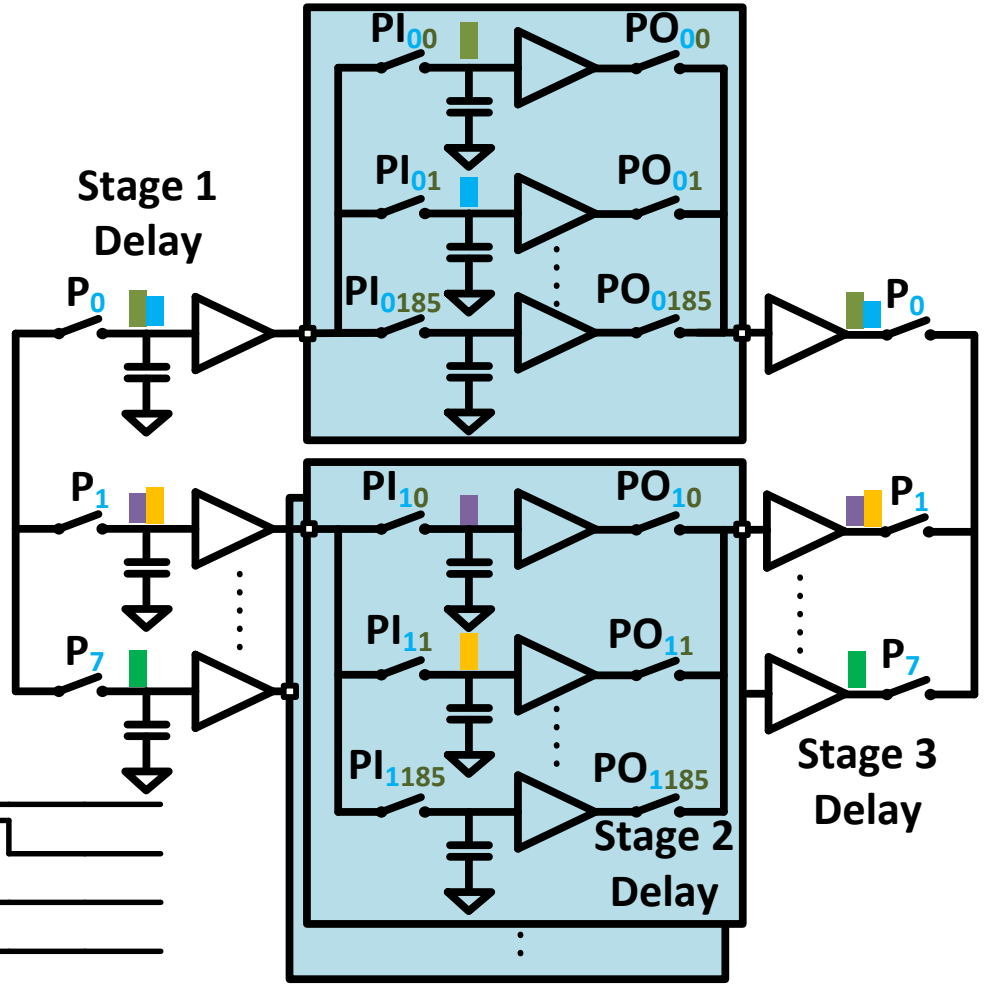


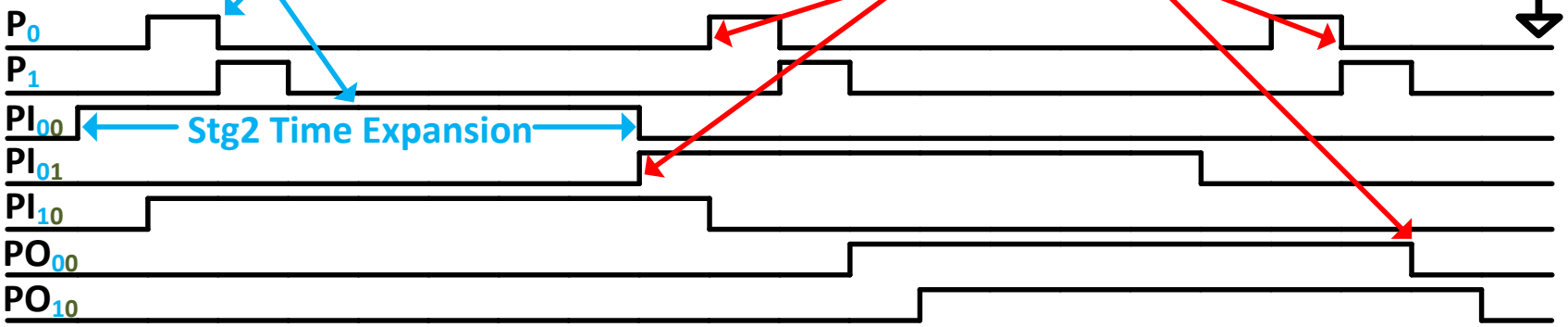
# Time-Interleaved Multi-Stage Approach



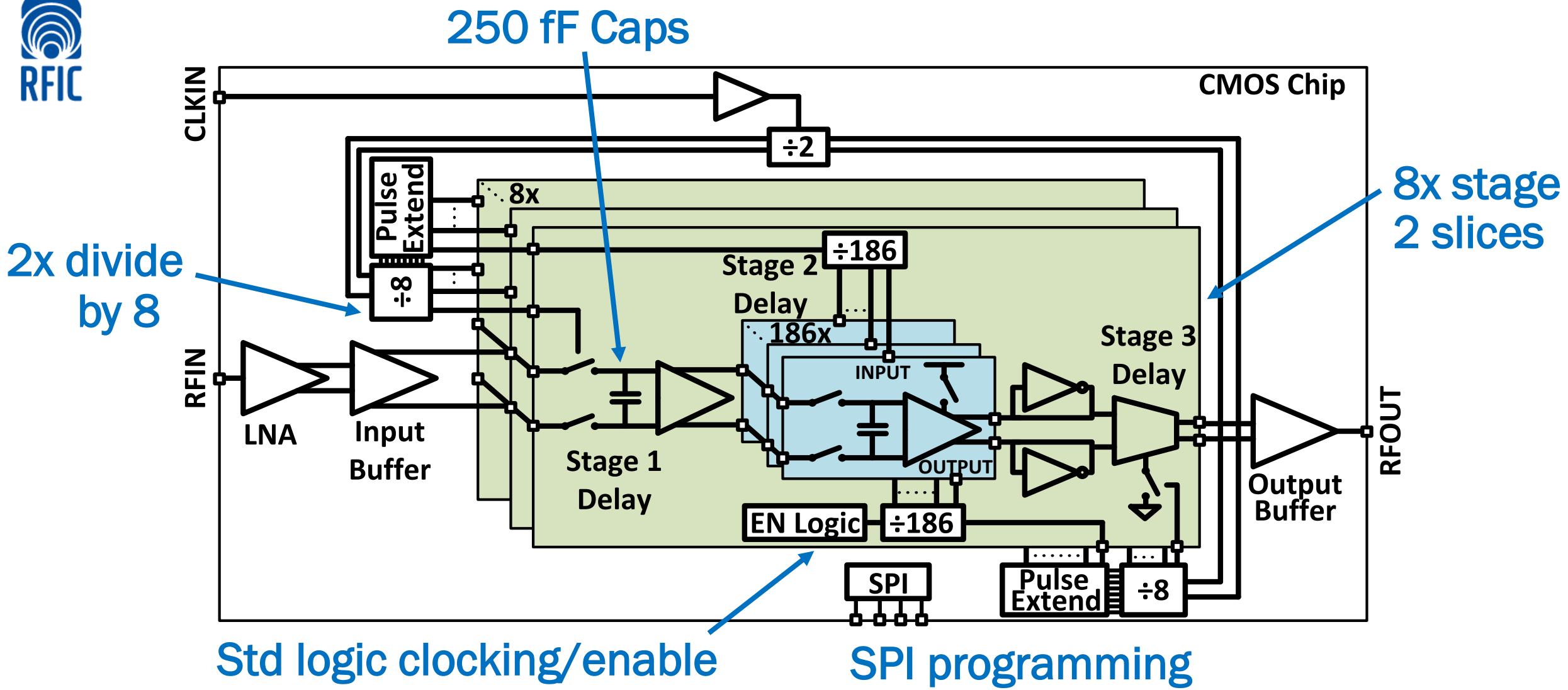




Stage 2 Time Expansion
- ↑ Settling Time
- ↓ Switch Size
- ↓ Sample Leakage
- ↑ Max Achievable Delay!

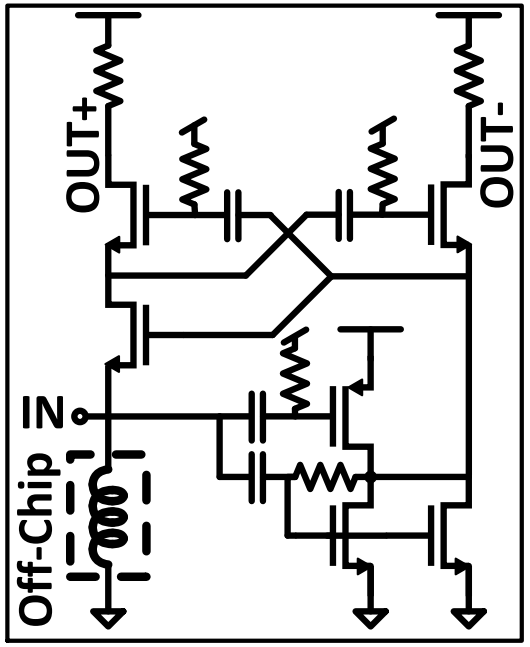
Insensitive to Timing Skew Between Stages



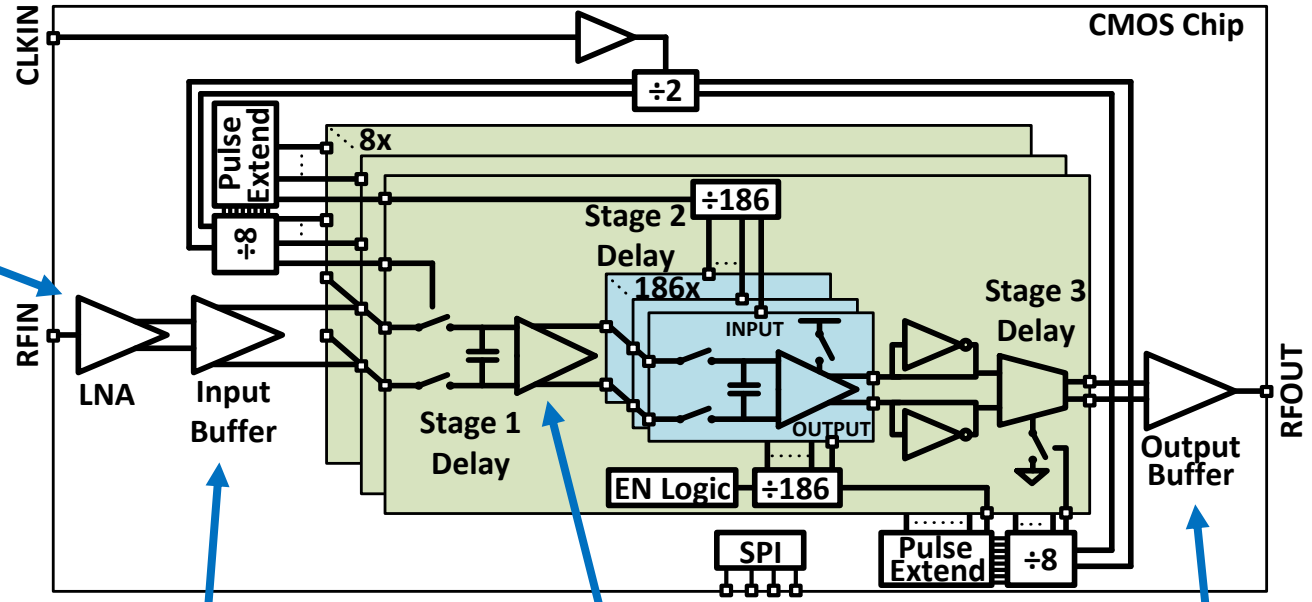
# Circuit Implementation

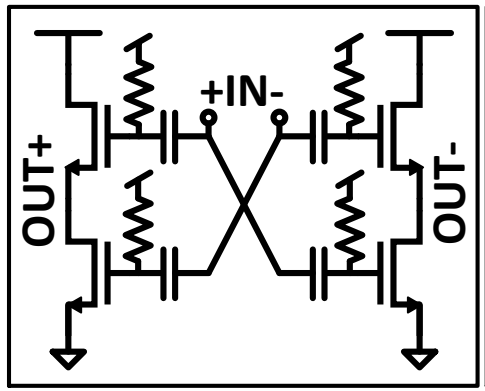


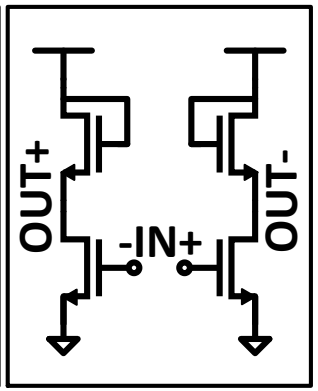
# Circuit Implementation

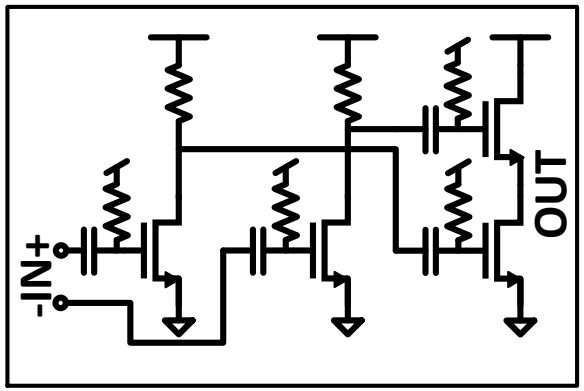



LNA modified from Mak et al., IEEE JSSC 2011



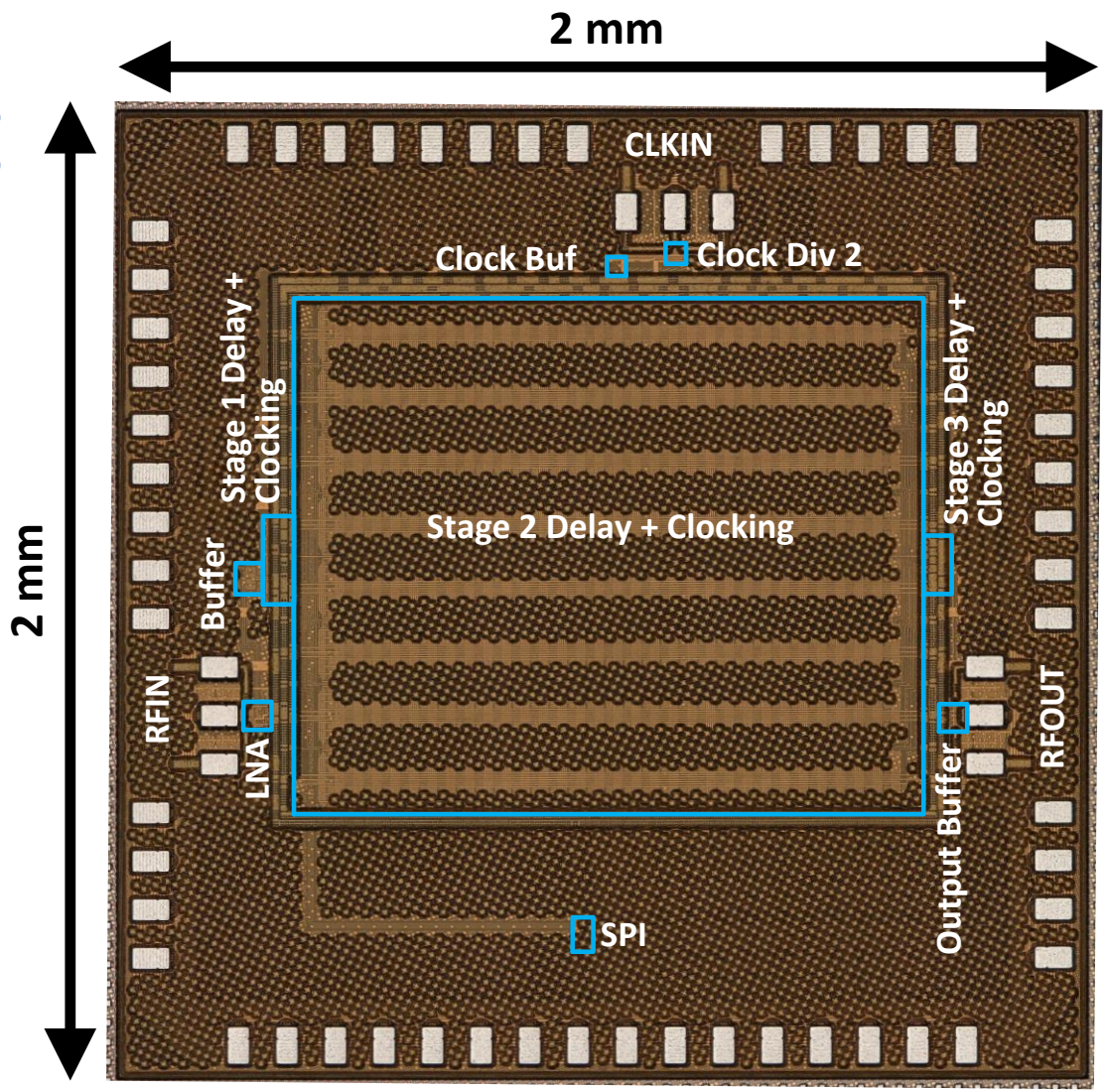



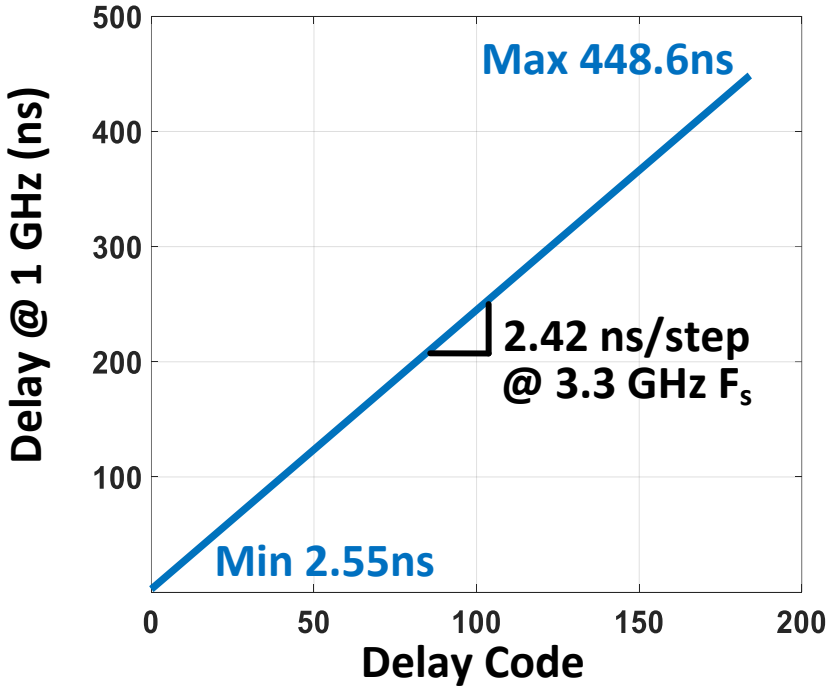

- Same $V_{ds}/V_{gs}$ in LNA NMOS
  - No cap at low Z node
- 0.0016 mm$^2$ area with 3.5 dB NF at 3.5 mW

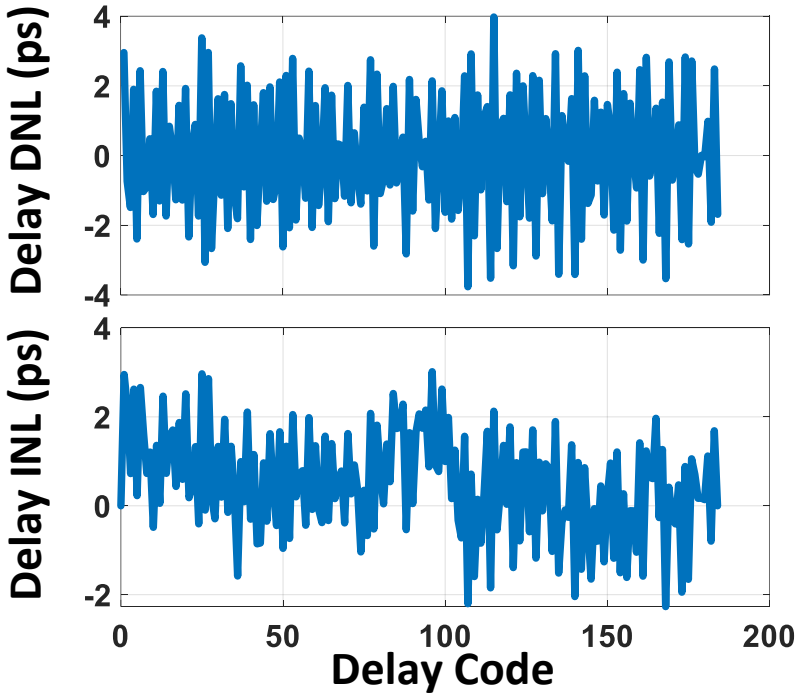
# Chip Micrograph




- 45 nm SOI CMOS process
- 4 $mm^2$ chip area
- 1.36 $mm^2$ active area
- Packaged in 5x5 $mm^2$ QFN
- Results shown at $F_s$ = 3.3 GHz

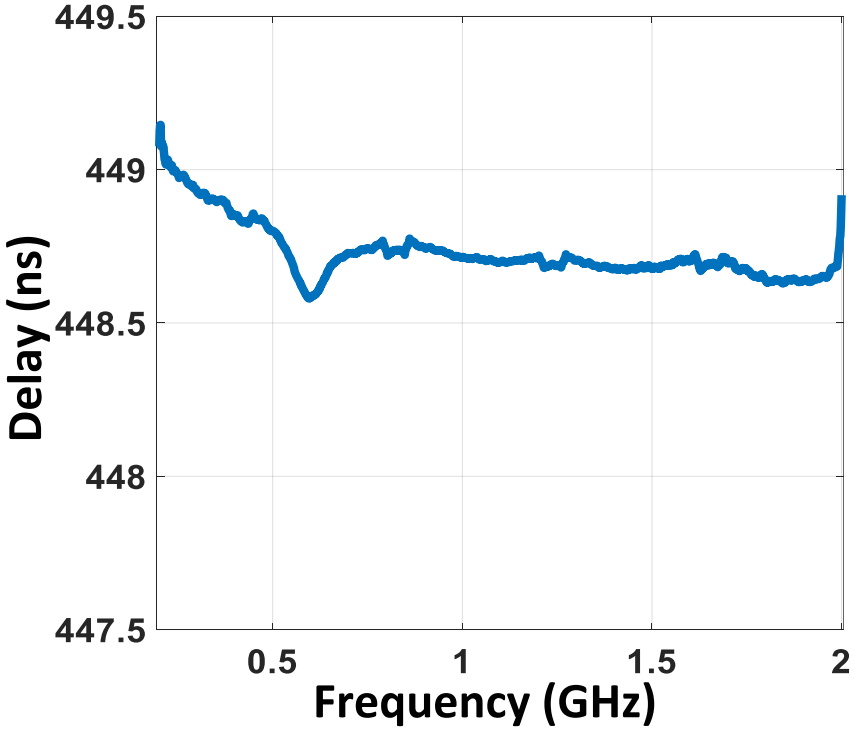
# Measured Delay at 1 GHz $F_{RF}$

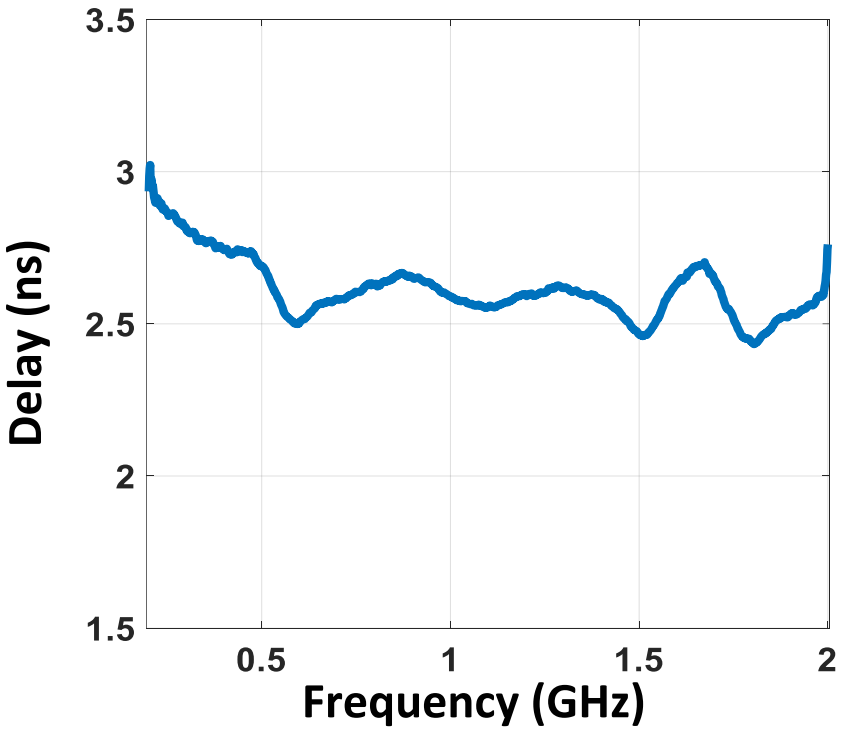



- DNL/INL < ± 4 ps
- Linear delay step of 2.42 ns ($8/F_s$)

# Measured Delay Across Frequency

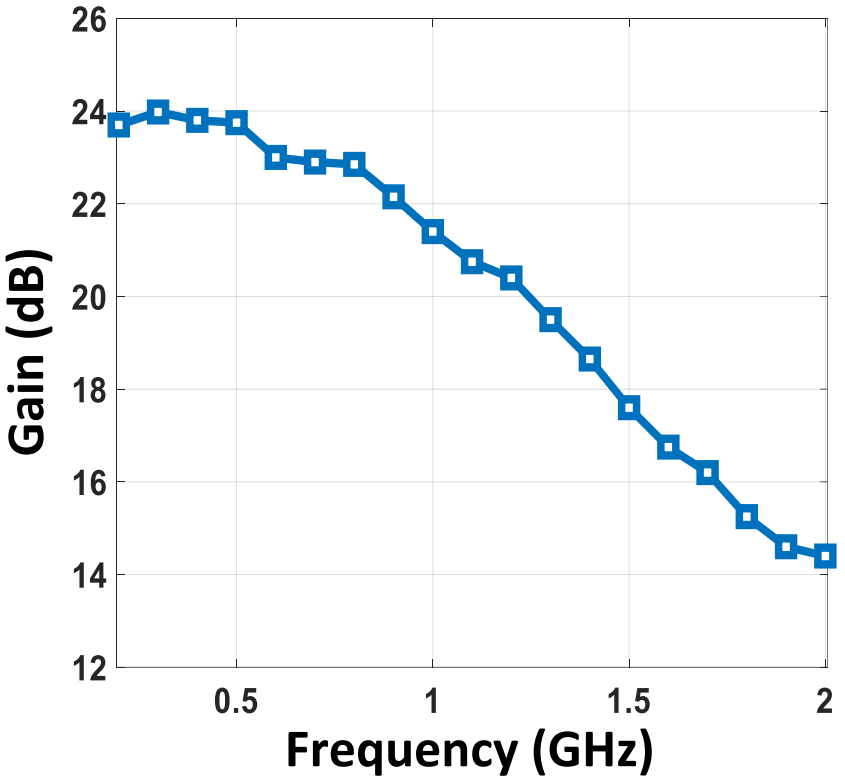


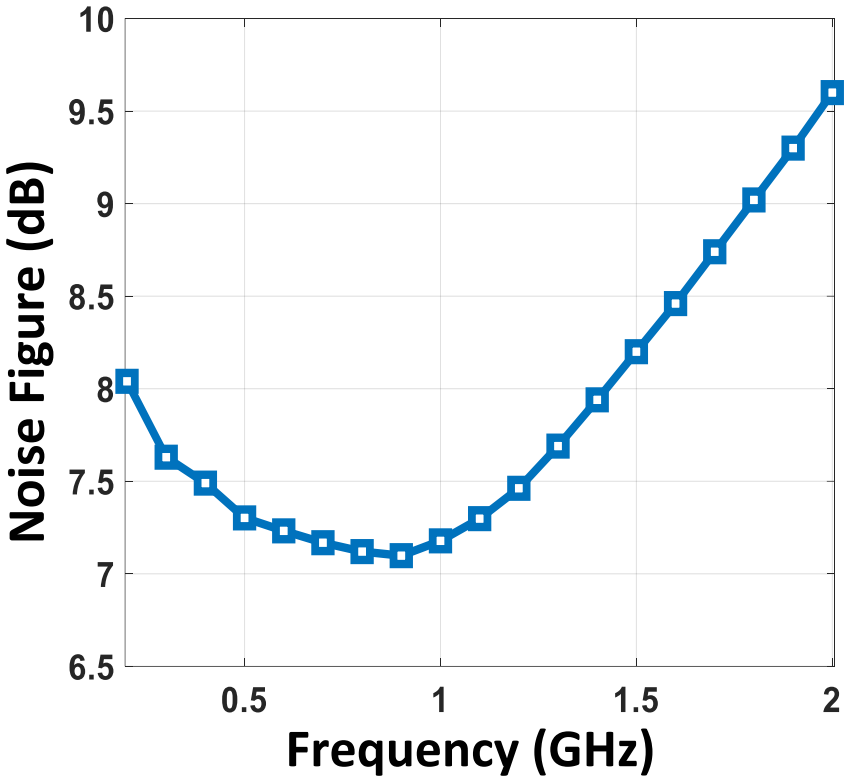




- 0.2-2 GHz flat delay range
- < 0.12 % variation at maximum delay

# Measured Gain and Noise Figure

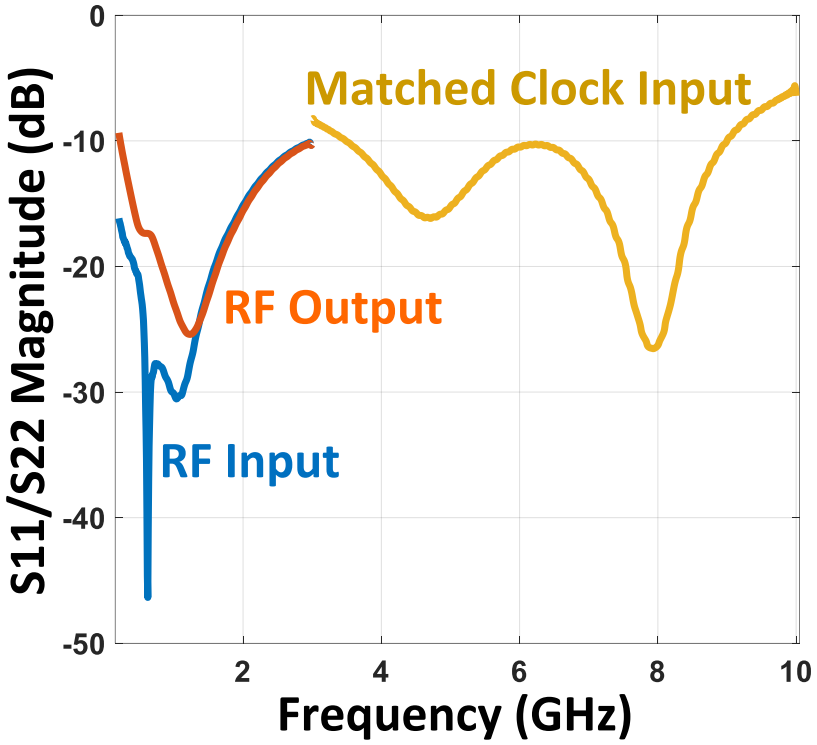
$$\text{ZOH} = \frac{\sin\frac{\pi F_{RF}}{F_S}}{\frac{\pi F_{RF}}{F_S}}$$

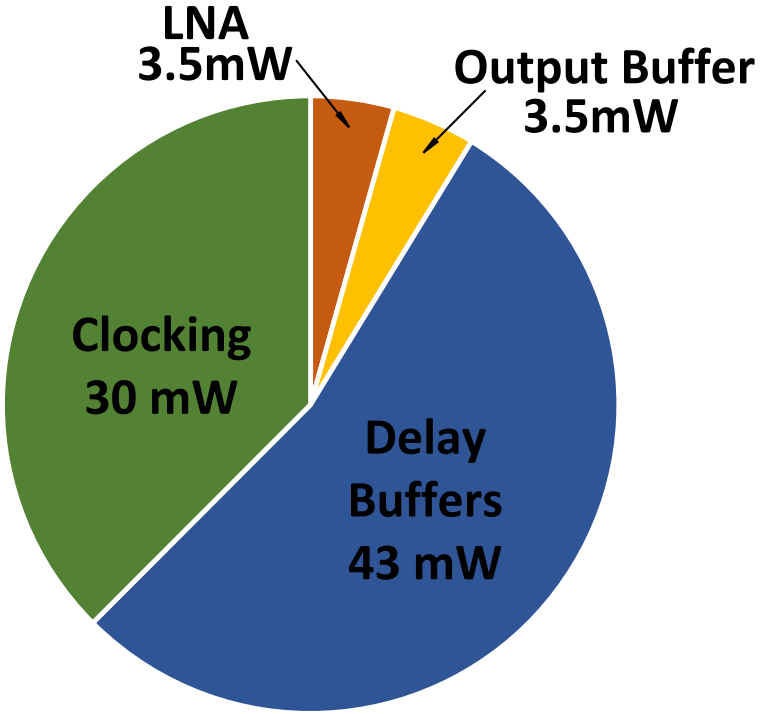



- < ± 0.5 dB gain flatness across any 100 MHz bandwidth
- < 0.1 dB variation across delay settings

# Measured S11/S22 and Power Consumption



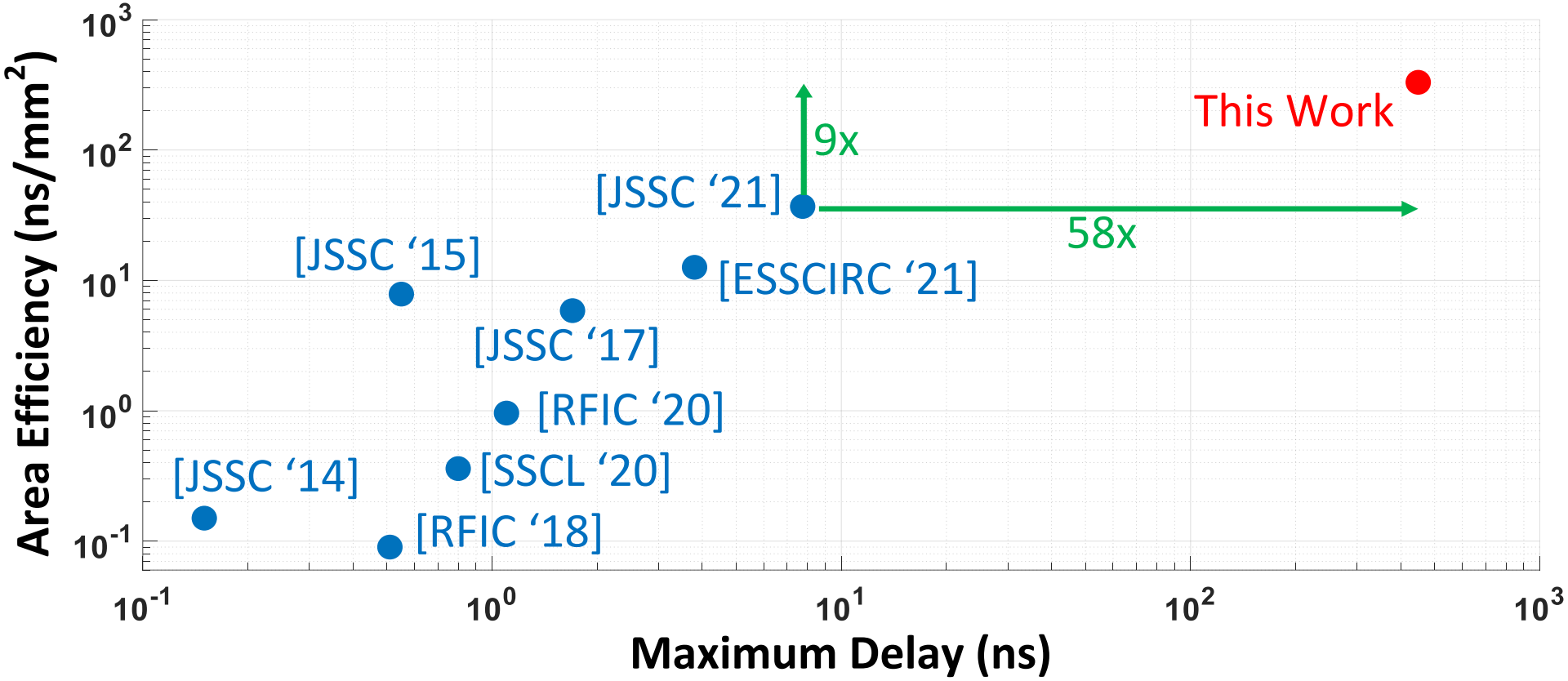

- 80 mW power consumption from 1V core supply

# Comparison with Prior Art

| | This Work | Nagulu et al., JSSC 2021 | Garakoui et al., JSSC 2015 | Mondal et al., JSSC 2017 |
|---|---|---|---|---|
| **Design** | Delay Element | SIC Receiver | 4 Channel Beamformer | Delay Element |
| **Architecture** | TI-MS Switched-Cap | Switched-Cap | Gm-C | Gm-C |
| **Delay Frequency Range** | 0.2GHz-2GHz | 0.1GHz-1GHz | 1GHz-2.5GHz | 0.1GHz-2GHz |
| **3-dB Bandwidth** | 0.2GHz-1.1GHz[a] | 0.1GHz-0.5GHz[b] | 1GHz-2.5GHz | 0.1GHz-2GHz |
| **Max Delay** | 448.6ns[a] | 7.75ns[b] | 0.55ns | 1.7ns |
| **Delay per Unit Area** | 330ns/mm$^2$[a] | 37ns/mm$^2$[b] | 7.9ns/mm$^2$ | 5.9ns/mm$^2$ |
| **Delay Range** | 175.9x | 31x[b] | 39.3x[c] | 6.8x |
| **Gain** | 24dB | -19dB[b] | 12dB | 0.6dB |
| **Noise Figure** | 7.1dB | - | 8dB | 23dB |
| **IP1dB** | -27dBm | - | -21dBm | -13dBm |
| **Power** | 80mW[a] | 7.4mW[b] | 90mW[d] | 364mW |
| **Technology** | 45nm SOI | 65nm | 140nm | 130nm |
| **Delay Active Area** | 1.36mm$^2$ | 0.21mm$^2$[b] | 0.07mm$^2$ | 0.29mm$^2$ |

[a]$F_s$=3.3GHz. [b]Max RF delay element extrapolated from publication. [c]Based on delay step. [d]Single Channel

# Comparison with Prior Art



# Conclusion

- Introduced a time-interleaved multi-stage switched-capacitor delay element technique
- Breaks < 8 ns programmable RF CMOS delay limit with 448.6 ns delay and state-of-the-art area efficiency
- Enables system miniaturization through CMOS delay replacement of non-programmable SAW and coaxial delays

# Acknowledgement

We Thank

- R. Llanes, J. Chiu, and I. Sobering for the board design and system integration support
- Laboratory Directed Research and Development program at Sandia National Laboratories for the funding support