SAND2022-2273C

Total Ionizing Dose and Single Event Effects on 12-nm bulk FinFETs

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HEART 2022

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Acknowledgments

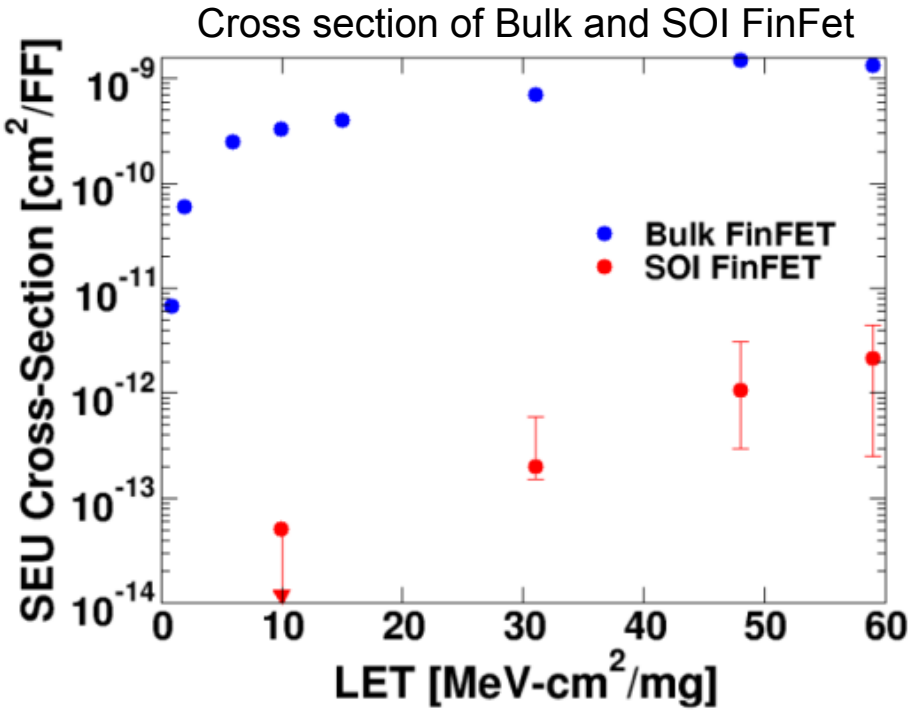
This work supported by the Navy Strategic & Spectrum Missions Advanced Resilient Trusted Systems (S2MARTS) program, Project No. S2MARTS 19-03 and the SEEEC Grand Challenge, part of the Laboratory Directed Research and Development program at Sandia National Laboratories.

This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

Outline

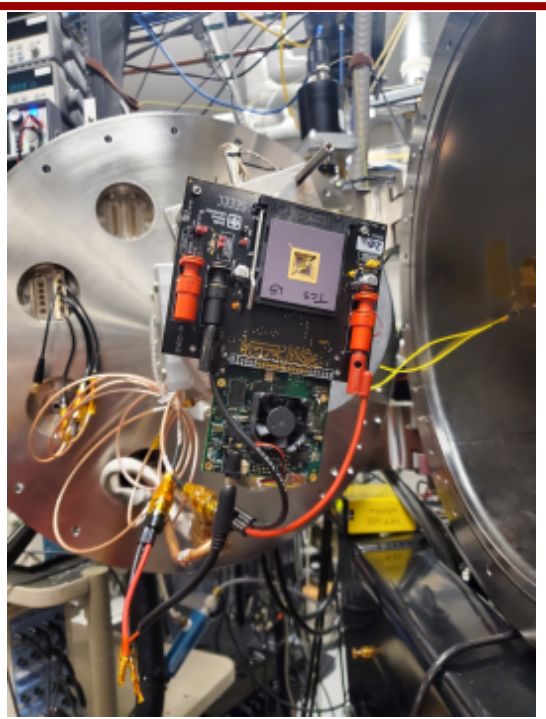
- Single event effects in 12 nanometer FINFET
- Total ionizing dose effects in 12 nanometer FINFET
- Conclusions

Prior SEE Results

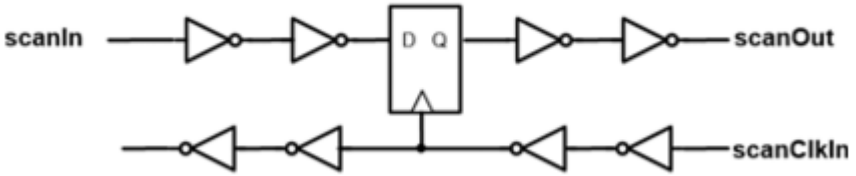


- **Data taken by Ball et al. show bulk FinFETs have a significant susceptibility to soft errors**
- **Error counts increase sharply as LET increases and begin to saturate at an LET of around 7**

SEE Test Structures

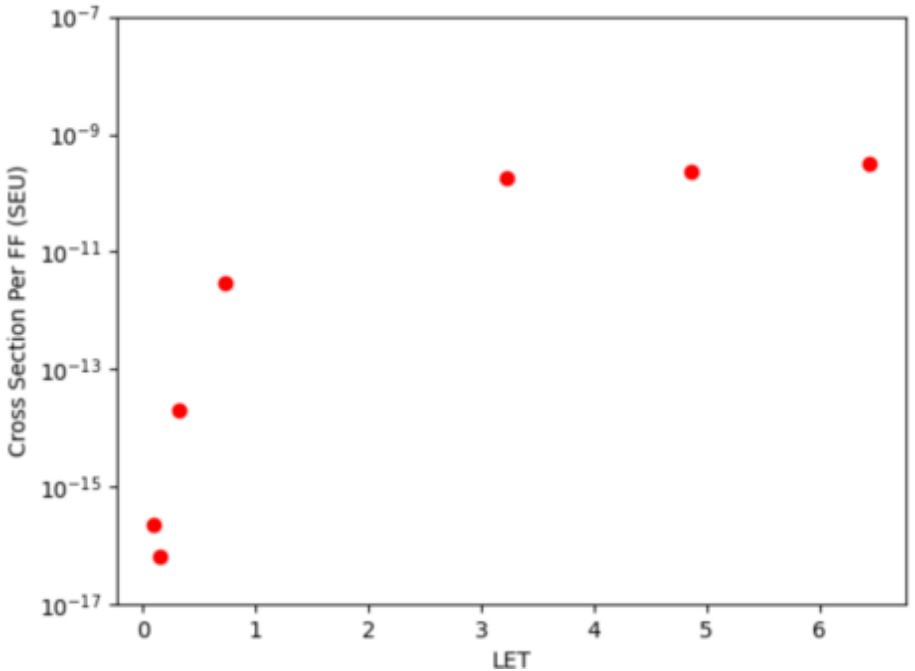


- Single event test structure is comprised of 19 scan chains each 15840 bits long
- Chip “TC3” containing test structures is placed into ether the Pelletron or Tandem beam at Sandia National Laboratories
- Data is scanned into the scan chain, irradiated with a beam, then read out
- Nominal voltage of 0.8 is used



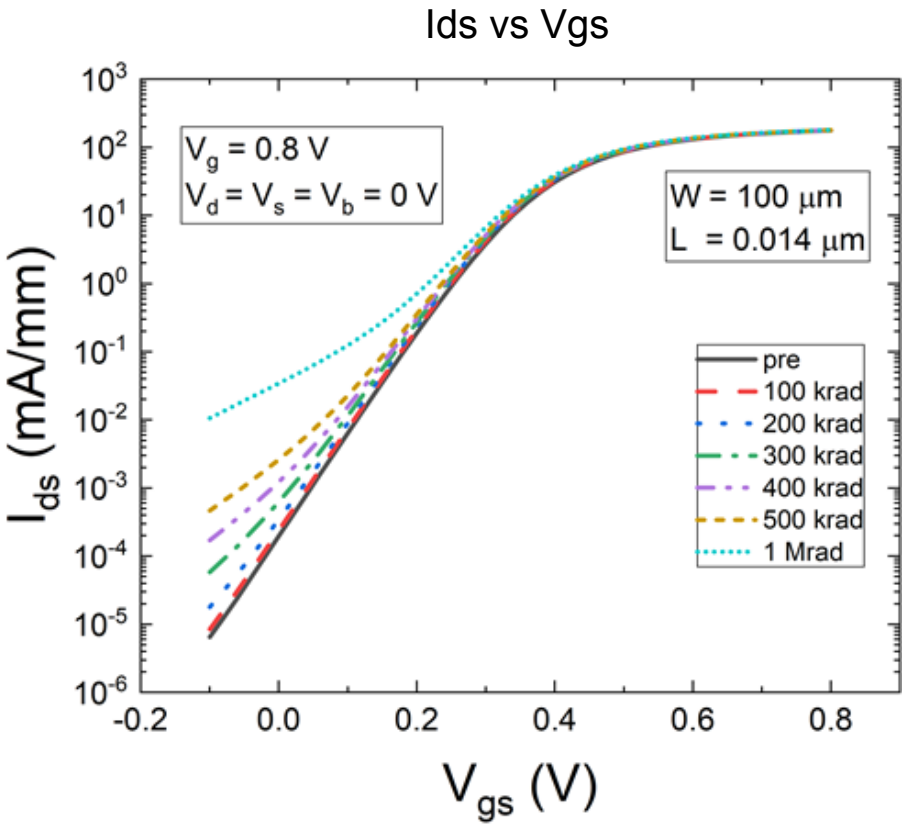
SEE Results

Representative cross section of scan chain



- **As expected error rate is very small at low LET and increases sharply with LET**
- **Similar to results published by Ball, cross section saturates at around 10^{-9}**
- **Saturation occurs quickly, around an LET of 3**

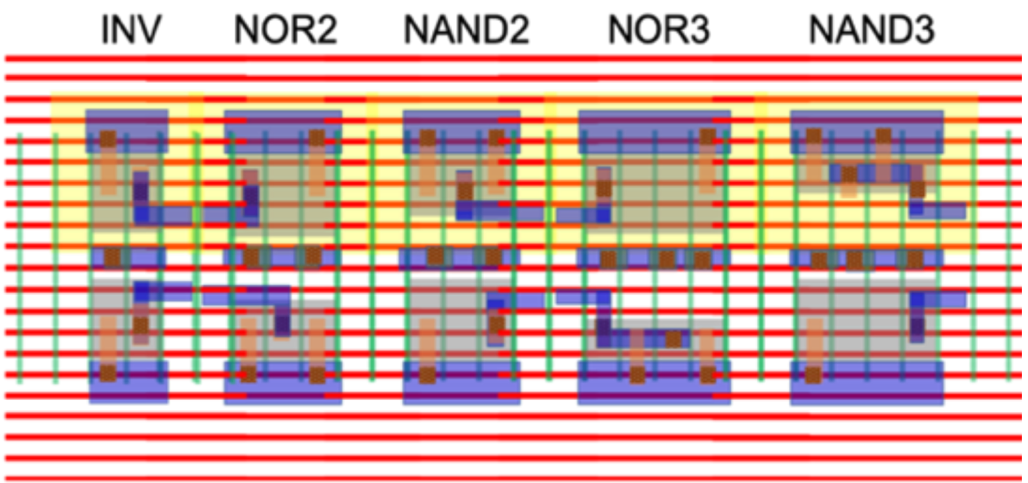
Prior TID Results



(after King et al., NSREC HI 2018)

- **Scaling of planar MOSFETs has generally lead to an increased tolerance of TID effects**
- **However, King et al. reported data showing a re-emergence of TID threats in bulk FinFETs**
- **Considerable off state leakage is shown with increasing dose**

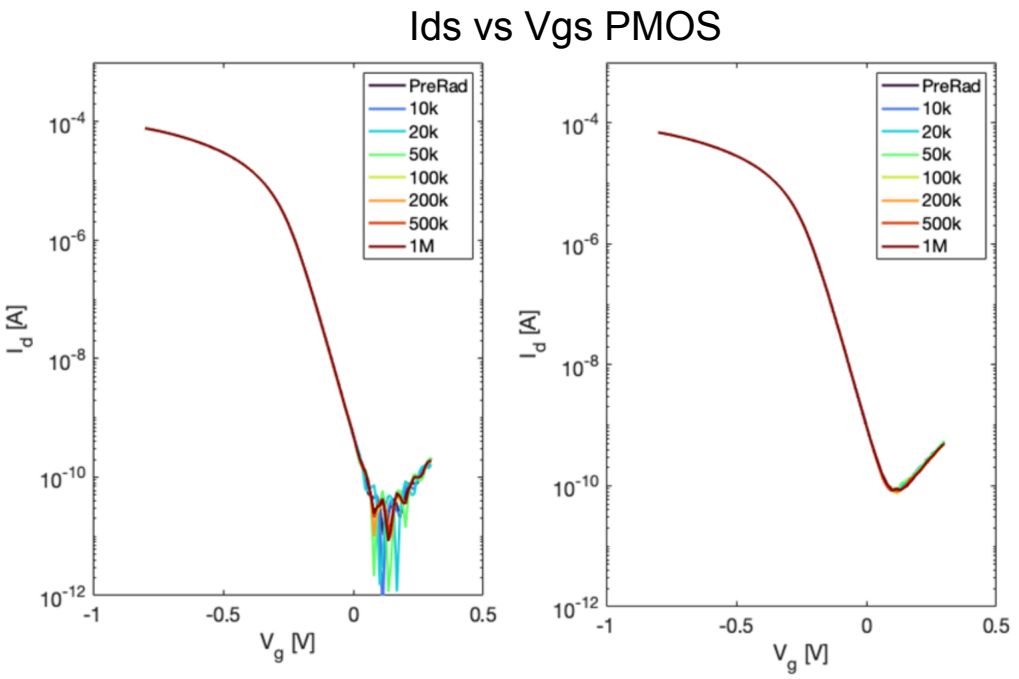
TID Test Structures



Representative layout of the TID test structure

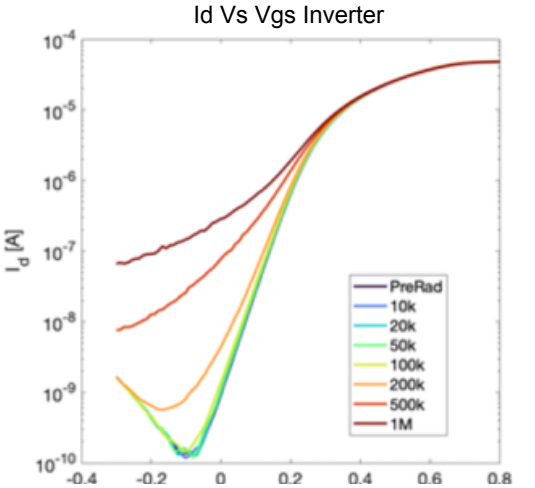
- Each cell is composed of 10 different transistor configurations
- Pull up network and pull down networks are disconnected via drain cuts while gates are shared
- PMOS utilizes shared VDD and n-well contacts, NMOS uses shared VSS and p-well contacts

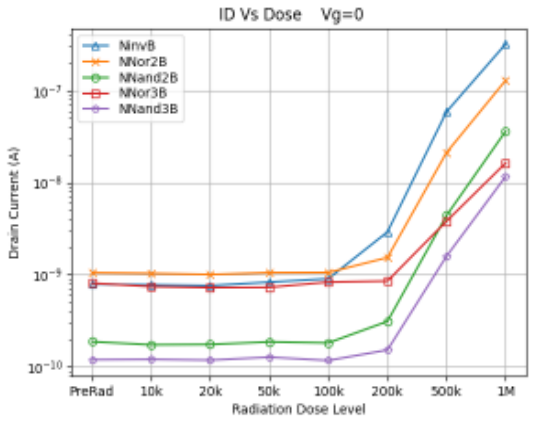
TID Experimental Results PMOS



- **PMOS transistors do not show significant degradation with radiation dose**
- **Plots are comprised of two tests from a single pull up network PMOS inverter**

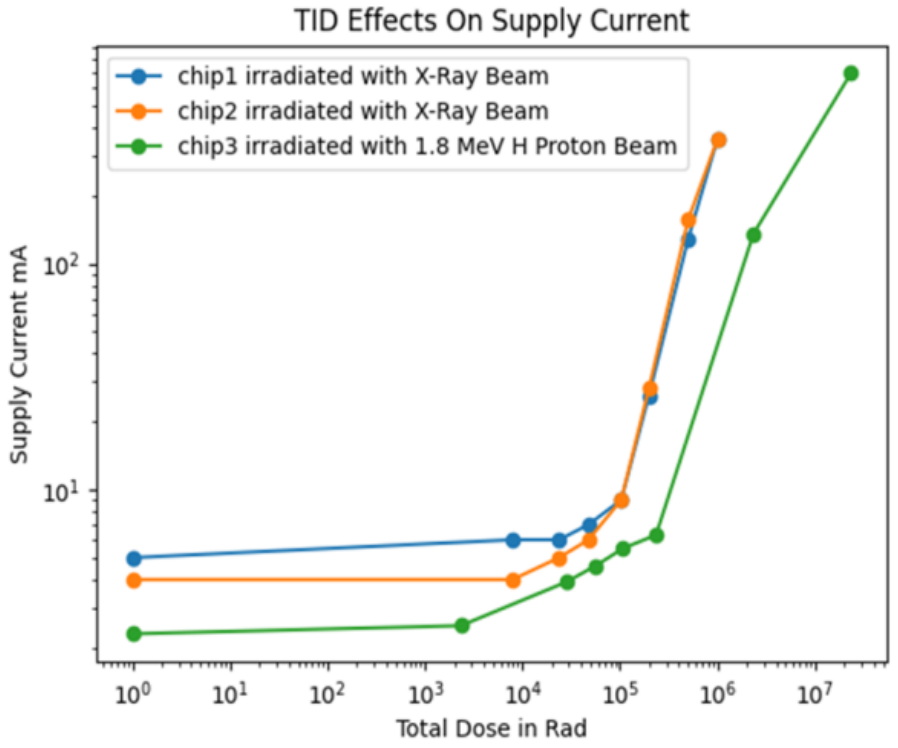
TID Experimental Results NMOS





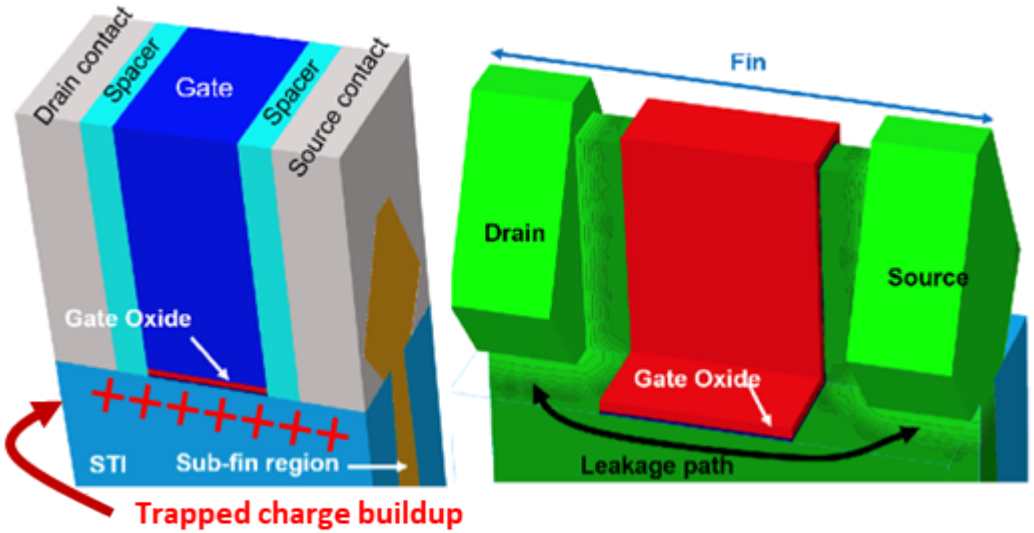
- NMOS pull up network shows significant leakage increase with dose level beginning at 200kRad
- Off-state leakage is consistent across all device pull down networks
- Threshold shifting with respect to dose is not observed

Supply Current Results



- TC3 power supply was monitored during high dose proton tests as well as X-Ray beams
- Proton data suggests that current increase is primarily a TID effect and not displacement damage

Possible TID Mechanism



- **Off-state current increases may be due to trapped charge buildup introducing a leakage path between source and drain**

Conclusion

- Single event upsets are a concern in 12nm FinFET technologies
- TID effects continue to be an issue in modern commercial CMOS technologies
  - Sub-threshold shift do not appear to be present
  - Dose dependent leakage paths increase off-state current