Analytical Expression for DC Link Capacitor Current in a Cascaded H-Bridge Multi-Level Active Front-End Converter

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***Abstract*—Medium-voltage grid-tied systems often use a cascaded H-bridge multi-level active front-end. In this converter, dc link bus capacitors play an important role in stabilizing the converter and enabling both active and reactive power injections. The present work provides analytical expressions for the capacitor current, which are essential for optimizing system design (especially capacitor size vs. lifetime). Then, the expression is incorporated into the grid connected bidirectional power system model. Consequently, this work contributes to the guiding principles to choose accurate dc link capacitor ratings against grid-side power delivery requirements. The analytical results have been validated with detailed simulations and hardware results.**

***Index Terms*—cascaded H-bridge, carrier-based PWM, dc-link capacitor lifetime, var compensation**

I. Introduction

A cascaded H-bridge ac-dc converter consists of more than one full-bridge, depending on the number of voltage levels needed on the ac side. Therefore, to begin with, the building block of the converter alone is illustrated in Fig. 1 and is referred to as a *module* in the cascaded system ahead.

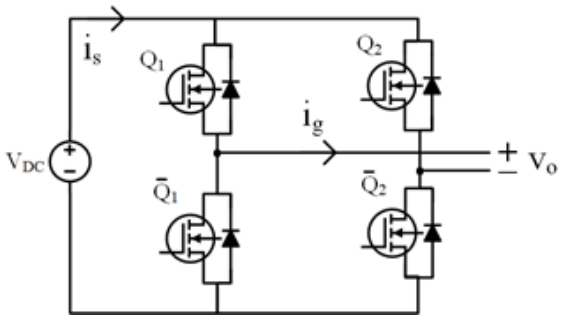


Fig. 1. Defined quantities in a full bridge circuit

Throughout this paper, the dc-link current is referred as i_s, the voltage of the ac side of the full-bridge as v_o and the current, also through the ac side of the full-bridge, as i_g. If i_g is modeled by a sinusoidal current source, then i_s depends on how the switches Q_1, Q_2, $\overline{Q_1}$ and $\overline{Q_2}$ are driven. It is valuable to accurately express i_s so that when such a system is realized on the dc side by a battery and a shunt aluminium electrolytic capacitor, to take a typical example, the amount of current going through the capacitor can be quantified. The portion of i_s going through the dc bus capacitor will inherently contain harmonics naturally caused by the switching.

These switching harmonics impact the lifetime of the capacitor. The frequency dependent ESR of the bus capacitor dictates the heat dissipated inside it causing the electrolyte to evaporate and the component itself to age. For typical aluminium electrolytic capacitors, the life of the capacitor halves for every $10\,^{\circ}\mathrm{C}$ rise above the rated temperature as dictated by Arrhenius Law [1], [2]. The capacitor lifetime's dependency on temperature has been an important concern for reliability of ac-dc converters both in literature as well as field operations [3]–[5].

Therefore, various approaches have been used in literature to quantify the dc-link current (instantaneous and rms). One method is to rely on a passive solution (i.e., simulations). While simulations are an effective way of finding the dc-link current in a particular circuit, the results do not reveal the underlying mathematical relationship which is essential for studying the overall system. Later in this paper, the results show how a mathematical framework helps choose the capacitor with optimal current ratings, instead of a trial-and-error approach.

In [6], the authors present expression for dc-link current for a three phase two-level voltage source converter in compressed integral form. Although the measurement and calculation results have been presented, the solution of integrals or a method of calculation is not reported.

Another approach to calculate dc-link current in H-bridge based converters is to use analytical estimation techniques, which can simplify analysis at the cost of accuracy and more importantly, are limited to associated application. A recent work in [7] evaluates dc-link current for a single phase H-bridge converter by ignoring high frequency harmonics for computational convenience. In the current paper, a mathematical argument illustrates that in a generic case, the rms sum

$$s_1(t) = \frac{1}{2} + \frac{M}{2}\cos(\omega_o t + \theta_o) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2}{m\pi}\left[J_n(m\frac{\pi}{2}M)\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])\right] \quad (5)$$

$$s_2(t) = \frac{1}{2} + \frac{M}{2}\cos(\omega_o t + \theta_o + \pi) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2}{m\pi}\left[J_n(m\frac{\pi}{2}M)\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o] + \pi)\right] \quad (6)$$

of the higher order harmonics can be equal, or even greater, than the rms of the highest magnitude harmonic.

Fundamental work by McGrath and Holmes [8] expresses the dc-link current in a carrier-based PWM driven half-bridge using the double Fourier Series analysis method introduced in [9]. The former reference applies the derived results of a cosine-triangle PWM based half-bridge converter under sinusoidal ac-side current on to two-level three phase VSI and on a three-level flying capacitor inverter. The same authors have utilized their framework to derive three-level flying capacitor converter's voltage balancing dynamics [10] and dc-link current harmonics in dual active bridge dc-dc converters [11].

In [12], the focus is on the dc link capacitor current for a three phase cascaded H-bridge converter connected with a diode rectifier. A closed form expression for the instantaneous dc link current is given for the three phase system but a (mathematical) argument of why it is applicable to their three phase application has not been discussed. For instance, the presented equation shows that in a three phase, multilevel cascaded H-bridge system, the dc-link current does not depend on modulator and carrier signals' phases. However, it does not reveal the dependence of dc-link current on the modulation and carrier phases in the individual H-bridge of the cascaded system. A modular relationship is useful in various ways including control for voltage balancing in unbalanced loads. Moreover, an expression for the dc-bus capacitor's rms current is also presented in the same paper. Even though an instantaneous dc-link current expression is available, it serves the authors better to use the formula proposed in [13]. The formula has been developed based on graphical observation method after drawing waveforms for a particular load angle and carrier frequency value, which can not be used arbitrarily in a closed form.

This paper presents a precise analytical model for calculating dc-link current in a multi-phase cascaded H-bridge multilevel converter on a modular level with detailed analysis and reporting. The modular results help mathematically explain behavior of the converter, such as the natural voltage balancing property of the converter, and also provide a framework that can be utilized in a straightforward manner to study its interaction on a system level. This leads to the second contribution which is in expressing dc-bus capacitor's rms current in terms of active and reactive power at the grid in a bidirectional configuration.

II. Analytical background

Consider a full-bridge circuit with a dc voltage source and ac load in Fig. 1. The first step is to accurately quantify the dc-link current in a single H-bridge and then apply the result to the cascaded system later. To solve for the exact dc-link current in Fig. 1, the modulated voltage on the ac-side of the H-bridge is defined as

$$v_o(t) = M\cos(\omega_o t + \theta_o) \quad (1)$$

where M is the modulation index, i.e., the percentage of the amplitude of maximum possible v_o that is targeted, while ω_o and θ_o are the modulation angular frequency and phase of v_o respectively. The current in the ac side of the H-bridge is modeled by a current source as,

$$i_g(t) = I_g\cos(\omega_o t + \theta_o + \phi) \quad (2)$$

where ϕ is the relative phase between i_g and v_o.

Next, the relationship between the switching functions of the respective half-bridges, $s_1(t)$ and $s_2(t)$, and the ac-side current, i_g, is explored. In this case, the dc-link current is a superposition of the products of switching function and the ac-side current. The dc link current can be expressed as

$$i_s(t) = [s_1(t) - s_2(t)]i_g(t) \quad (3)$$

where $s_1(t)$ and $s_2(t)$ are the switching functions of Q_1 and Q_2 respectively, as derived for naturally sampled phase shifted cosine-triangle PWM. $\overline{Q_1}$ and $\overline{Q_2}$ are complementary switches of the Q_1 and Q_2. These switching functions have been derived in [9] and are categorized into carrier and modulator harmonics in Eqs. (5)-(6) (at the top of the page for clarity). Here, m is the harmonic number for the fundamental carrier (triangle) frequency, w_c, and n is the harmonic number for the fundamental modulation (cosine) frequency, w_o. Moreover, θ_c is the carrier phase in radians, defined for a cascaded phase-shifted-carrier PWM system as follows.

$$\theta_c = \left[\frac{y-1}{(N-1)/2}\right]2\pi \quad (4)$$

In (4), y is the module number and N is the total number of levels in v_o. Here, the denominator in the bracketed term is equal to the number of modules in the cascaded N-level converter. Additionally, note that in (6), π is added to create the anti-phase for the modulation signal in the half-bridge on the right side in Fig. 1. π has been separated to avoid confusion in case the modulation signal is non-symmetric. This implies that

$$\mathcal{F}^{-1}\left[S_1(\omega) * I_g(\omega)\right](t) = \frac{MI_g}{4}\cos(\phi) + \frac{I_g}{2}\left[\cos(\omega_o t + \theta_o)\cos(\phi) - \sin(\omega_o t + \theta_o)\sin(\phi)\right] + \frac{MI_g}{4}\left[\cos(2\omega_o t - 2\theta_o)\cos(\phi) + \sin(2\omega_o t - 2\theta_o)\sin(\phi)\right] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{I_g}{2}\alpha \tag{7}$$

$$\mathcal{F}^{-1}\left[S_2(\omega) * I_g(\omega)\right](t) = -\frac{MI_g}{4}\cos(\phi) + \frac{I_g}{2}\left[\cos(\omega_o t + \theta_o)\cos(\phi) - \sin(\omega_o t + \theta_o)\sin(\phi)\right] - \frac{MI_g}{4}\left[\cos(2\omega_o t - 2\theta_o)\cos(\phi) + \sin(2\omega_o t - 2\theta_o)\sin(\phi)\right] - \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{I_g}{2}\alpha \tag{8}$$

$$i_s(t) = \frac{MI_g}{2}\cos(\phi) + \frac{MI_g}{2}\left[\cos(2\omega_o t - 2\theta_o)\cos(\phi) + \sin(2\omega_o t - 2\theta_o)\sin(\phi)\right] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} I_g\alpha \tag{9}$$

$$: \alpha = (K_{m,n+1} + K_{m,n-1})\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])\cos(\phi) + (K_{m,n+1} - K_{m,n-1})\sin(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])\sin(\phi)$$

$$: K_{mn} = \frac{2}{m\pi}J_n(m\tfrac{\pi}{2}M)\sin([m+n]\tfrac{\pi}{2}).$$

θ_o is not only defined as the modulation angle of the overall multilevel voltage on the ac-side, but also as the modulation angle of the left half-bridge in each module. Finally, J_n is the Bessel function of the first kind with order n. In a cascaded converter, each half-bridge would have its unique switching function. Therefore, the equations have been set up to obtain intra-modular dynamics to investigate the individual dc-link currents.

III. Derivation of DC-link Current in the Ideal Model and its Validation

The derivation strategy is as follows. To obtain the exact harmonic expression for the dc link current for the circuit in Fig. 1, first, the Fourier transform is applied to (3). The multiplication in the time domain indicated in (3) becomes convolution in the frequency domain. The inverse Fourier transform is applied to the subsequent result. This process is carried out for each half-bridge of the module separately and then the contributions are superposed. The contributions from the left and right half-bridges towards the dc-link current, i_s of Fig. 1 is summarized in (7) and (8) and then the results are substituted in (3) respectively, to obtain the dc link current for the module in (9) (again placed at the top of the page).

Each half-bridge generates a fundamental modulation frequency component which is effectively canceled in the superposition. Whereas, the dc component and remaining modulation and carrier harmonics add up to twice the magnitudes. The elimination of the fundamental modulator harmonic is because of the redistribution of harmonic energy (amplitude) to higher frequencies. Therefore, for dc-link capacitor, a full-bridge modulation is harmonically more efficient as compared to that in a half-bridge converter as the ESR of the capacitor is relatively lower at higher frequencies.

Eq. (9) is associated to dc-link current in one independent module. The topology of cascaded H-bridge converters is such that this equation can be applied to each module (due to the series connection) separately to provide information about all the modules. Therefore, this equation is applicable to any H-bridge as in Fig. 1 driven by a naturally sampled cosine-triangle pulse width modulation strategy.

TABLE I
Simulation Parameters for Section III

I_g (A)	ϕ (rad)	f_c (Hz)	M	N	f_o (Hz)
7	$\pi/3$	3000	0.9	5	60

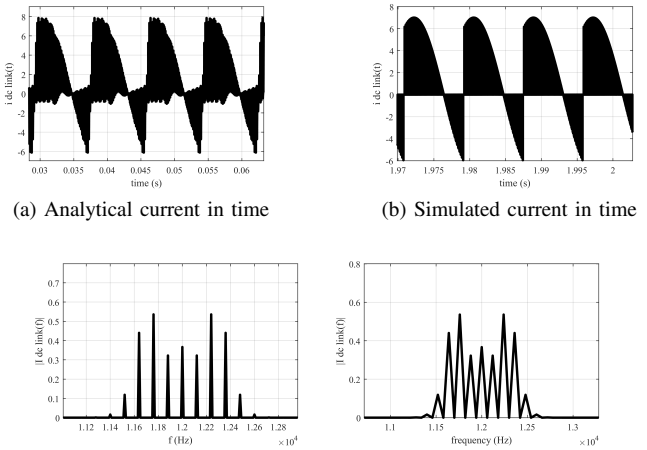
Now, the validity of the equation is carried using comparison with simulation of Fig. 1 by modeling i_g as a sinusoidal current source defined in (2) in a single phase five-level unidirectional system. The simulation parameter are mentioned in table I. In this table, I_g stands for the peak value of the ac-load current and other modulation parameters have already been defined.

Fig. 2 shows a comparison of the simulation and analytical results in time and frequency domain. The difference between Fig. 2(a) and Fig. 2(b) is because in numerical implementation of (9), the double series sum is for finite indices of m and n. In this implementation, maximum value of m = 10 and n ranges between -500 and 500. The waveform corresponding to the numerical implementation of the analytical result exhibits the Gibbs phenomenon. Note that this trade-off is more efficient than ignoring the higher order harmonics as observed in literature. A random frequency band is chosen for comparison in Fig. 2(c) and Fig. 2(d) and the results show a close match in all of the finite frequency bands up to three decimal places, thereby permitting to move ahead.

Next, a two-module (five-level) system is studied. It is observed that within one phase, each module has the same dc-link current even though each half-bridge is switched

$$I_{cap,rms}^2 = \left[\frac{1-\omega^2 L_f C_f}{2\left|\hat{V}_g\right|}\right]^2 \left[P_g^2 + \left(Q_g - \frac{\omega C_f \left|\hat{V}_g\right|^2}{1-\omega^2 L_f C_f}\right)^2\right] \left[\frac{\beta}{2V_{DC}^2} + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{4}{m\pi}\sin([m+n]\frac{\pi}{2}) J\left(\frac{m\pi}{V_{DC}}\sqrt{\beta}\right)^2\right]$$

$$: \beta = \left(\frac{P_g}{\left|\hat{V}_g\right|}(2\omega L_f - \omega^3 L_f^2 C_f)\right)^2 + \left(\frac{Q_g}{\left|\hat{V}_g\right|}(2\omega L_f - \omega^3 L_f^2 C_f) + \left|\hat{V}_g\right|(1-\omega^2 L_f C_f)\right)^2 \quad (10)$$



(a) Analytical current in time (b) Simulated current in time

(c) Analytical current harmonics (d) Simulation current harmonics

Fig. 2. (a)-(d) Validation of the ideal dc-link current model

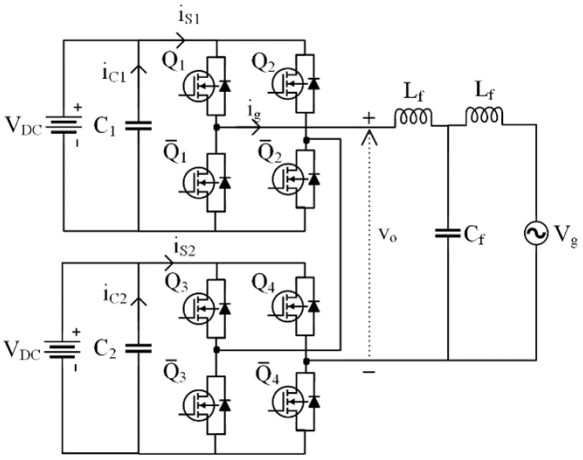


Fig. 3. The grid-tied cascaded H-bridge converter

differently from the three remaining half-bridges. In this way, the natural voltage balancing property is mathematically illustrated for the cascaded multilevel converter. These conclusions motivate hardware implementation and results are evaluated while studying a grid-tied system in the next section.

IV. Analysis of a Grid-Tied System, and Evaluation of Results in Three Domains

A. Mapping grid power to $I_{cap,rms}$

A system overview in Fig. 3 shows a typical active front-end configuration where the grid is modeled by a voltage source and a five-level cascaded H-bridge converter is connected to the grid through an LCL filter. It is now possible to map the the grid's active and reactive power flow (P_g, Q_g) to the dc-link current rms of the bus capacitor. Utilizing (9), the rms current flowing through the bus capacitors is obtained and is shown in (10).

In (10), $|\hat{V}_g|$ is the line-to-neutral rms of the grid voltage shown in Fig. 5. All other parameters are constant or running sum indices. L_f and C_f are the filter inductance and capacitance, J stands for the Bessel function as defined earlier, V_{DC} is the dc-bus voltage of each module, ω is the grid's fundamental frequency, while P_g and Q_g are the grid's active and reactive power using generator sign convention. Because of the symmetry within and between balanced phases, the equation is applicable to a multi-phase and multilevel system.

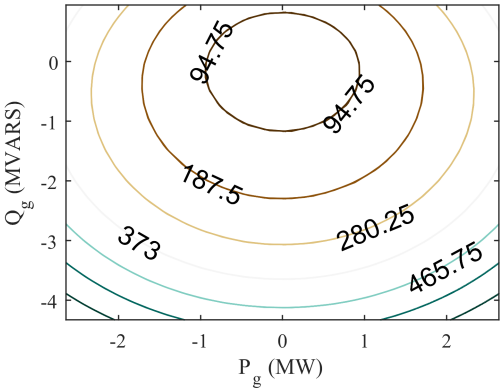


Fig. 4. DC link capacitor's rms current contours

A contour plot is shown for (10) in Fig. 4. Close examination shows that the round contours are not centered at the origin and do not form an exact ellipse, as is identified by the equation. For a specific contour, as P_g goes higher, the amount of Q_g decreases according to the described relationship. The area enclosed by a contour would depict the complex power operating points supported by the corresponding rms rating of the capacitor installed in the hardware.

The relationship between the dc-link capacitor's rms current and grid power P_g and Q_g is examined using a surface plot in Fig. 5. Using 10, the graph shows that as operating

TABLE II
CONFIGURATION PARAMETERS

Parameter		Value
V_{DC_a}	(V)	20
V_{DC_b}	(V)	1800
$f_{cut-off}$	(kHz)	6
L_f	(mH)	20.63
C_f	(nF)	34.11
R_f	(Ω)	22.35
f_c	(kHz)	3
L_h	(mH)	1.8
V_g l-n rms	(V)	7200

power levels are increased, the stress on the dc-link capacitor increases non-linearly. It is observed that this plot is not symmetric around the grid's active and reactive power. This fact is most visible by shifting the discussion focus back to the contours in Fig. 4. Consider the two points where the 94.75 A contour crosses zero P_g. In this case, the reactive power being supplied *to* the grid, positive Q_g, is 0.9 MVAR and in another operating scenario, the reactive power being drawn *from* the grid is around 1.2 MVAR, a point below the chosen contour. In other words, there is more stress on the capacitor when the same amount of reactive power is being consumed by the grid as compared to when it is being supplied by the grid. The LCL filter demands additional reactive power beyond the amount being fed to the grid.

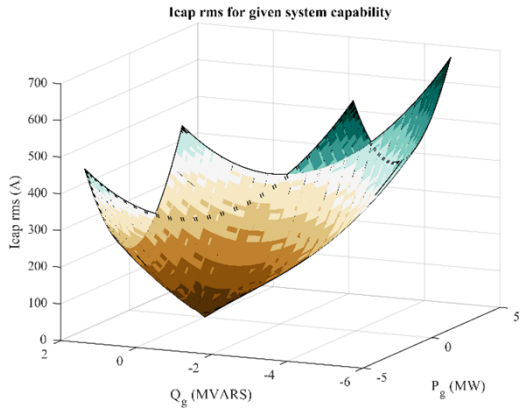


Fig. 5. Relationship of $I_{cap-rms}$ with grid power

B. Discussion of various results

A combination of hardware and simulation results were compared with analytical model to validate the derived equations. A single phase five-level cascaded converter was developed and its configuration parameters are shown in table II. This table contains specific parameters selected for corresponding discussion. Other parameters like modulation frequency, f_o, are not mentioned.

1) Evaluation of analytical and simulation results: The analytical model was compared with a simulation setup following the circuit in Fig. 3. All the parameters from table II were used except L_h, V_{DC_a} and R_f. V_{DC_b} was used in the analysis of analytical and simulation results of the grid-tied system. The analytical model has been developed based on a sinusoidal current source model whereas its results are to be compared with Fig. 3 which contains the LCL filter. The filter was designed for a cut-off frequency of 6 kHz to best accommodate the Bode gain and phase plots in the desired operating point. L_f was set to 0.05 p.u. of base impedance. Fig. 6 shows a comparison between the analytical model and the simulation results.

TABLE III
TEST POINTS TO COMPARE SIMULATION AND ANALYTICAL CAPACITOR STRESSES

	1	2	3	4	5	6	7	8
P_g (kW)	321	0	-321	0	-183	183	166	-167
Q_g (kVAR)	5	338	5	-363	168	168	-161	-141

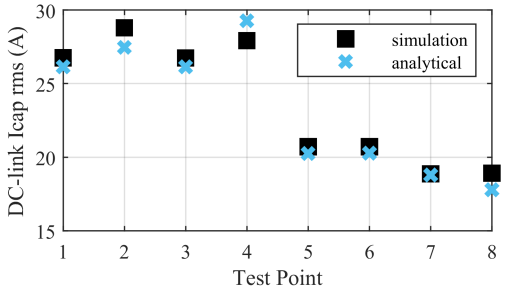


Fig. 6. Simulation and analytical comparison for the capacitor stresses

The worst case error in simulation and analytical comparison is noted to be about 4.8%. The difference can be explained based on a few factors. The first reason lies in the difference between the analytical model of (10), which assumes sinusoidal ac-side current, and the simulation which has an LCL filter with a cut-off frequency of 6 kHz. The 6 kHz range allows for multilevel voltage harmonics to propagate in the system, thus causing ac-side current harmonics. This in-turn effects the dc-link current which is a sampled version of the ac-side current. Therefore, the bus capacitor's rms current will have a different rms than the sinusoidal ac-load case. Another source of error is evident from the fact that the simulation implements regularly sampled PWM whereas the analytical model is based on naturally sampled PWM. Besides explaining errors, the results show that for all the sampled points in Table. III, the rms portion of the 120 Hz harmonic was close to the sum of rms contribution from non-120 Hz harmonics (i.e., within 1 A).

2) Hardware and simulation results evaluation: For hardware results, a single phase five-level H-bridge converter is operated in the inverter mode with an RL load. Therefore, V_{DC_a}, R_f, L_h and f_c are hardware and simulation parameters

in this case. For this setup, the dc-link current was measured and compared with simulations. The five-level voltage, the RL load current and the voltage output from both half-bridges of one module can be seen in Fig. 7.

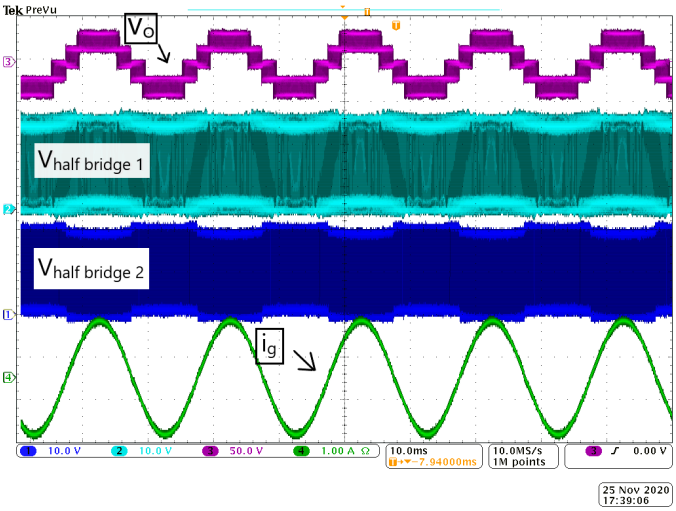


Fig. 7. Hardware results for the five-level cascaded H-bridge converter

The ac-side current through the RL load and the output voltage of the half bridges were measured directly as seen in Fig. 7. Since the dc-link current is of discontinuous nature, a regular Hall-effect based current probe cannot be used to measure it directly. Therefore, the method recommended in [14] was used. The method is described as follows. As illustrated in the referred work, the half-bridge outputs were multiplied with the ac-side load current to obtain the hardware dc-link current. This hardware result was then compared with the simulation results as shown in Fig. 8 and Fig. 9 respectively.

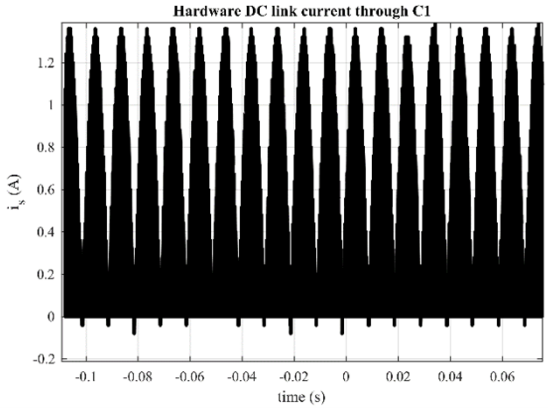


Fig. 8. Hardware dc-link current in one module

The rms current measured in the hardware and that in the simulation had a worst case difference of 9.2%. This difference is explained in two parts. The switching functions from the ideal simulation blocks are not the same as those coming from the microcontroller. The code implemented in the microcontroller contains deadtime which has not been incorporated in

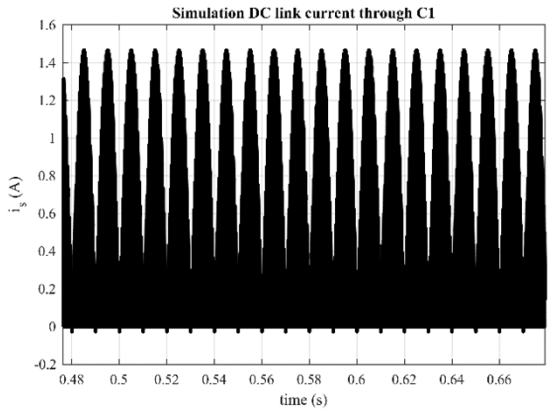


Fig. 9. Simulation dc-link current in one module

to the simulation blocks. This difference has direct impact on the hardware data-processing of the dc-link current as the pulse widths are not the same in the microcontroller as the simulation. However, this is only partially contributing to the deviation in pulse widths as it is a difference due to voltages but load current does not exist. When the load is turned on, a dynamic behavior between the body diode and IGBT-based half-bridge causes the pulse width to deviate as well. This deviation is evident from Fig. 7. The conduction of body diode is initiated during deadtime. Based on the polarity of the load current, corresponding body diodes will conduct. Due to the body diode's forward voltage drop, the pulses seen in Fig. 7 are slightly above and below V_{DC} as well as slightly below and above the 0 voltage level. Therefore, the overall pulse width profile in the hardware, which is used to calculate dc -link current, is significantly different than that in the simulation. The hardware prototype is finally shown in Fig. 10 with two modules for the five-level converter, micrcontroller and RL load.

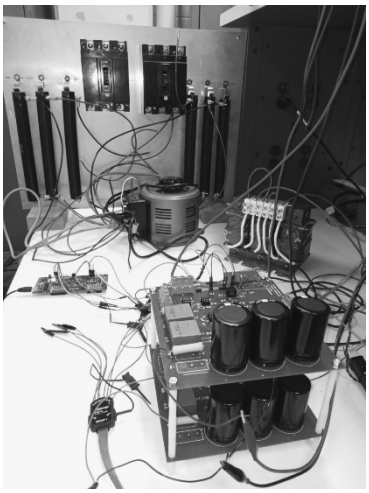


Fig. 10. Hardware prototype of the cascaded H-bridge system

V. Conclusion and future work

In this paper, a detailed and exact mathematical model has been developed for the dc-link current in a cascaded H-bridge multilevel converter. The detail of the model has been used to study the converter's interaction with a grid-tied system. The grid's active and reactive power commands have been mapped to the dc-link current stress in the bus capacitors. The analytical, simulation and hardware results have been evaluated in a variety of setups and these show a good match thereby validating the work. For future work, the derivations motivate deriving a framework for capacitor sizing against the dc-bus voltage specifications. Overall, this work contributes to estimating the lifetime of the dc-link capacitors in an accurate manner which in-turn adds to system reliability by avoiding contingency outages and improving scheduled outages in power systems.

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