Design and Demonstration of an 850 V dc to 13.8 kV ac 100 kW Three-phase Four-wire Power Conditioning System Converter Using 10 kV SiC MOSFETs

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***Abstract*—In this paper, an 850 V dc to 13.8 kV ac 100 kW modular multilevel three-phase four-wire dc/ac converter based on 10 kV SiC MOSFETs is designed and demonstrated. The design considerations of key components, including the dc-link, device cooling, gate driver, isolated gate driver power supply (GDPS), medium voltage (MV) ac filter inductor, MV and medium frequency transformer, and the mechanical design are discussed. Two converters are designed, and two prototypes are developed, to study the converter paralleling operation and scalability. Both converters are fully tested up to their voltage and power ratings. However, the two converters are not identical. Based on the design and test results of the first converter, the MV power stage, transformer design, GDPS, as well as the low voltage power stage in the second converter are improved for smaller size and/or higher efficiency. Compared to the version 1 converter, the version 2 converter achieves 49% volume reduction and 2 percentage point efficiency improvement, with a peak efficiency of 98.4% at the rated power.**

Keywords—medium voltage (MV), 10 kV SiC MOSFET, modular, multilevel converter

I. Introduction

High voltage (HV) SiC devices (>3.3 kV) provide small size, high-efficiency, and enhanced functionality solutions for medium voltage (MV) high-power converters in grid applications [1, 2]. Their high blocking voltage simplifies the converter topology and control system. Their high switching speed and low switching loss enable the application with high efficiency and high switching frequency so that the passive size can be reduced and the high control bandwidth can be achieved, which brings system-level benefits, such as stability and harmonic filtering.

HV SiC devices, mainly the 10 kV SiC MOSFETs, have been studied for a decade [3-7]. There is also some research work with these devices, including device characterization and modeling [8-10], solid-state transformers [2, 11, 12], solid-state circuit breakers [13], PV integration into the MV grid [14, 15], off-shore wind farm HVDC [16], and power conditioning system converter for asynchronous microgrids [17]. However, because of the high voltage and high dv/dt of these MV SiC devices, there are still many challenges in their applications, including the gate drive and protection design considering the high dv/dt [18-20]; gate drive power supply (GDPS) design considering the high insulation requirements and low coupling capacitance [21-23]; electric field management to realize high and reliable insulation [24]; the impact of parasitic capacitances on the device DPT-based dynamic characterization [25] and on the converter loss [26, 27]; sensor design considering the high dv/dt noise [28]; the MV converter testing approach [29]; and the insulation considerations [30-33].

In this paper, a MV grid-connected modular multilevel three-phase four-wire dc/ac converter using 10 kV SiC MOSFETs is designed and demonstrated. The design considerations for the gate drive, device cooling, GDPS, passives, sensors, and mechanical are discussed. To study the converter paralleling operation and scalability, two converter prototypes are developed. However, compared to the first converter, the second converter follows an improved design. Therefore, two versions of the design and demonstration are discussed in this paper. In the version 1 design and development process, the development of the MV power stage and magnetics are mainly focused on. With the experience obtained in the version 1 converter, the version 2 converter is designed and developed with significant volume and efficiency improvement. Two prototypes for the two design versions, respectively, are also presented.

The rest of the paper is organized as follows. In Section II, the converter topology and design parameters are introduced. Then, the detailed converter design of the first version is discussed in Section III, followed by the converter prototype and experimental test in Section IV. In Section V, the improved design of the second version of the converter is discussed, followed by the prototype and experimental test results in Section VI. Finally, Section VII concludes this paper.

II. Converter Topology

As shown in Fig. 1, the power conditioning system (PCS) converter is used in a flexible combined heat and power system(F-CHP), enabling flexible energy management and advanced grid support functions for the F-CHP system [34]. It connects the 850 V dc to the 13.8 kV ac without low-frequency power transformers. It consists of a dual active bridge (DAB)-based dc/dc stage, which boosts the 850 V dc to 6.7 kV dc, and a cascaded H-bridge (CHB)-based dc/ac stage, which interfaces the MV ac grid. It is a three-phase four-wire converter, featuring a modular design. In the grid-connected mode, it controls the power exchange with the grid; in the islanded mode, it operates in the voltage control

mode, to support the ac side external balanced or unbalanced loads. Cree 1.7 kV/80 mΩ and 10 kV/300 mΩ SiC MOSFETs are used for the LV side and MV side, respectively.

The major specifications of the PCS converter are summarized in Table I. In addition to the normal operation range, this converter also needs to consider grid requirements, including the voltage ride through, frequency ride through, voltage and frequency support, grid faults, lightning surge, different operation modes, as well as unbalance supports. Since the key technical challenge is the MV SiC application, converter design, and implementation, this paper focuses on the HV SiC-based converter design.

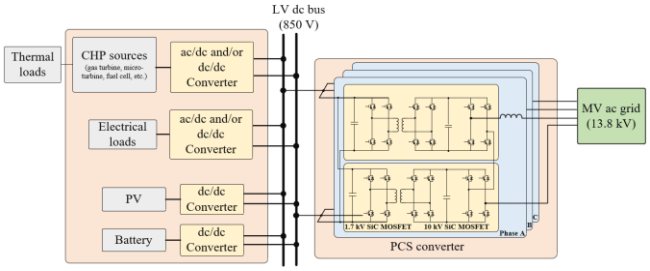


Fig. 1. The system configuration.

TABLE I. TABLE TYPE STYLES

Parameter	Value
LV side dc	850 V dc (±5%)
MV side voltage	13.8 V ac (-12% ~ +10%)
Power rating	100 kVA
Power factor	Four quadrant operation
Ambient temperature	-25ºC ~ 55ºC
TDD	<5%
Ac side control bandwidth	Voltage control bandwidth >300 Hz Current control bandwidth > 1 kHz
Other requirements	1) Voltage ride through, frequency ride through, frequency and voltage support required in IEEE Std 1547 2) grid faults 3) Lightning surge 4) Grid-connected mode and islanded mode operation and seamless transition 5) unbalance support

III. CONVERTER DESIGN: VERSION 1

A. 10 kV SiC MOSFET Cooling

The 10 kV/300 mΩ devices with the same package provided in [8] are used, and the device characteristics are obtained with the curve tracer and double pulse test (DPT). Then, the device losses are estimated, and device cooling is designed. As shown in Fig. 2, four 10 kV SiC devices (a half bridge in the dc/dc stage and a half bridge in the dc/ac stage) are in one air duct, and two fans are put at the two sides of the air duct to push and pull the air, respectively. Since the baseplate of the 10 kV SiC MOSFET is also its drain terminal, sharing one heatsink among different devices requires high insulation capability between the device and the heatsink, which results in a large thermal resistance. Besides, a large heatsink with multiple devices enlarges the parasitic capacitance, which leads to more power losses. Therefore, each device has its own heatsink, and different heatsinks are isolated from each other. A clearance distance of 20 mm is adopted considering the maximum voltage stress (14 kV). Ansys Icepak simulation is conducted to estimate thermal performance. The maximum heat sink temperature rise is about 38 ºC, and the estimated junction temperature is 75 ºC at the ambient temperature of 20 ºC.

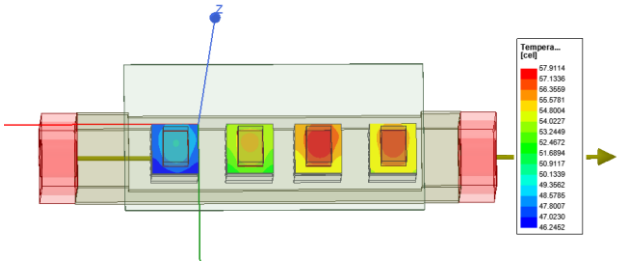


Fig. 2. Cooling design of the10 kV SiC MOSFETs.

B. DC-link Design

Four TDK 1.98 kV/40 µF (B25620B1406K981) film capacitors are connected in series to withstand the 6.7 kV MV dc-link voltage and provide sufficient energy buffer to limit the 2nd-order voltage ripple to ±5%. Because of the capacitance tolerance, the capacitance value of each capacitor is measured first, and then four capacitors with the most closed capacitance values are picked out for one power stage to minimize the voltage unbalance. The PCB-based dc-link design is adopted, considering the current rating, as shown in Fig. 3. The clearance and creepage distances are following with the IPC-2221 standard. The total stray inductance of the switching commutation loop, which is mainly estimated with Ansys/Q3D, is 528 nH. The dc-link PCB contributes 288 nH, the capacitors contribute 240 nH, and others are contributed by the power loop on the gate drive board and the connection. Since the di/dt is only around 0.2 A/ns, the switching voltage overshoot is about 97 V, which is quite small compared to the high dc-link voltage. Therefore, decoupling capacitors are not considered.

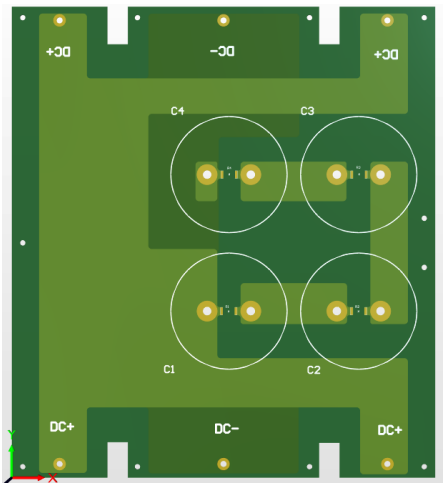


Fig. 3. The dc-link PCB design.

C. Gate Driver and Gate Driver Power Supply

Compared to the gate driver for LV devices, the MV gate driver needs to pay more attention to fast protection and noise immunity. The gate drive voltages are selected to be +15 V and -5 V, considering the tradeoff between conduction loss and the short-circuit saturation current. The turn-on and turn-

off gate resistances are 15 Ω and 3 Ω, respectively, which are the tradeoff results between the switching loss and the dv/dt.

Short-circuit protection, under voltage lockout, as well as PWM signal feedback are implemented to enhance the performances of the gate driver. To improve noise immunity, the gate driver board components are put as close as possible. The parasitic capacitances between the switching node and the sensitive components are minimized by using small traces and/or maximizing the distance. Also, shielding is utilized with a PCB polygon. More considerations can be found in [18].

The isolated GDPS needs to achieve high insulation capability. In addition, low coupling capacitance is critical to achieve low common mode current, which can be caused by the high dv/dt. The GDPS discussed in [21] is used. The GDPS has a similar transformer design as discussed in [21], but the topology has been changed from fly-back to fly-buck considering the noise immunity. It outputs 24 V dc, with a maximum power rating of 2.5 W, and features a coupling capacitance of 1.85 pF and an insulation capability of 20 kV.

D. MV Filter Inductor

The MV ac filter inductor is determined at 44 mH, considering the power quality and the grid requirements. To fully utilize the benefits of HV SiC devices, the filter inductor needs to be as small as possible. However, due to the high switching frequency, high dv/dt, and high insulation requirements (considering both normal and abnormal conditions), the ac filter design is also a big challenge.

Three different versions of the inductor are designed and implemented with epoxy or silicone elastomer encapsulation [33, 35]. Shielding is adopted to fully stress the high voltage on the insulation material and avoid partial discharge in the air between the winding and the core. The final version of the design passes the 12 kV RMS partial discharge test, 46 kV (>1 minute) dc hi-pot, and 1-hour full voltage and current rating continuous test, achieving the design requirements.

E. MV Medium Frequency Transformer

The MV medium frequency transformer is another big challenge in this MV converter. A nanocrystalline core-based 850 V/6.7 kV transformer is designed and developed [36]. To realize high power density, the leakage inductance is designed to be the resonant inductance and the leakage flux-related loss is minimized with additional ferrite sheets. Electrical shielding similar to the MV inductor is also adopted in the MV winding design to achieve high insulation.

F. The MV Power Stage

The MV power stage is shown in Fig. 4. Considering the modularity and ease of testing and debugging, the gate driver dc/dc converter and desaturation diodes are located in two separate daughterboards, respectively. The gate driver dc/dc converter board converts the 24 V output from the GDPS to -5 V, +15 V, and 30 V, supplying the gate drive circuit and the desaturation protection circuit. The dc-link sampling board is located on the gate driver board, and it shares the same GDPS with the low-side 10 kV SiC MOSFET.

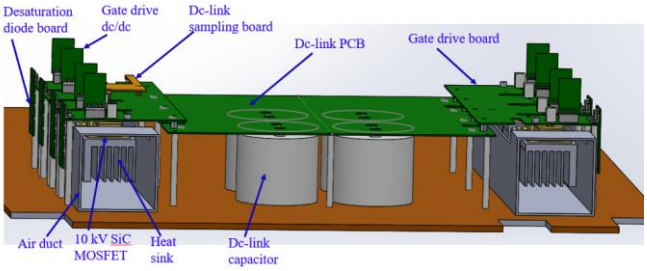
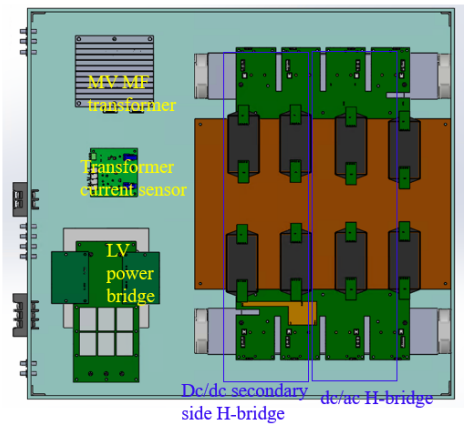


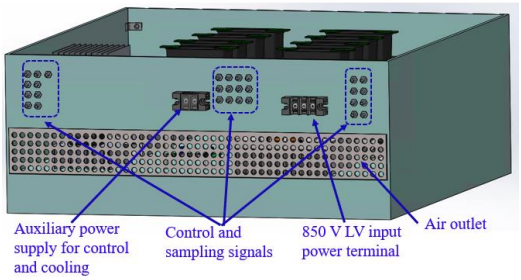
Fig. 4. The MV power stage

G. The Power Unit

Modular design is realized. As shown in Fig. 5(a), each power unit consists of a DAB-based dc/dc stage and an H-bridge in the CHB dc/ac stage. As shown in Fig. 5(b), the LV power terminal, the control fiber optic signals, sampling signals, and the auxiliary power supply connectors are located at the front panel. The MV ac power terminals are led out from the rear panel, as shown in Fig. 5(c). The dimensions of one power unit are 27.5 inches × 11 inches × 30 inches. The clearance and creepage distances between the MV and the LV and between different potentials on the MV side must be considered.



(a)



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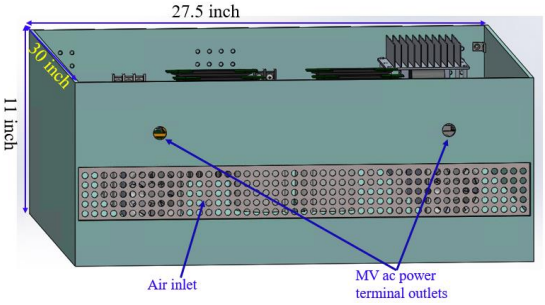

(c)

Fig. 5. The (a) top, (b) front, and (c) rear view of the power unit.

IV. Version 1 Converter Prototype and Experimental Test Results

The 13.8 kV/100 kW converter prototype with version 1 design is shown in Fig. 6, and its dimensions are 33.562 inches × 36.875 inches × 87.625 inches. The ac side three-phase voltage and current waveforms under the full rating test with three-phase RC loads are shown in Fig. 7. The LV dc side input power and the MV ac side output power are measured with the power analyzer WT3000E under the single-phase full active power test, and the efficiency is measured to be 96.4% at the rated output power.

The ac voltage and current control bandwidth are tested to be 300 Hz and 1.1 kHz, respectively, meeting the requirements. The grid requirements, including voltage ride through, frequency ride through, voltage support, and unbalance supports are tested with the setup discussed in [29].

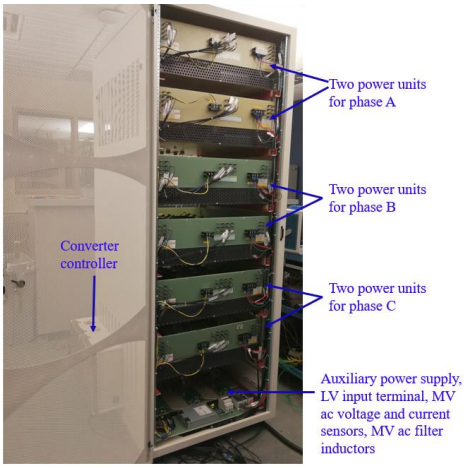

Fig. 6. The version 1 converter prototype.

Fig. 7. The ac-side voltage and current waveforms of the PCS converter.

V. Design Improvements in the Version 2 Converter

To study the paralleling and scalability of the MV PCS converter, another converter needs to be built, and it is a good chance to improve the first converter. Based on the experience and testing results obtained from the first converter, significant size and efficiency improvements are achieved in the second converter (version 2 converter) through improving design for several components and better mechanical design. Since this paper focuses on the converter design, the paralleling and scaling work is not included.

A. MV Power Stage Improvement

The dc-link capacitors are changed to AVX FFVE6N0356K7X, which does not have the bottom stud so the space can be saved. The dc-link layout is also improved. As shown in Fig. 8, the four dc-link capacitors are physically located in a line, and the large dc-link PCB in the version 1 design is divided into two smaller PCBs. One PCB is used to connect the four capacitors in series and mount the voltage balancing resistors, and the other one is used to connect the dc-link to the devices and gate driver boards. Because of the better flux cancellation effect and the smaller internal stray inductance of the dc capacitors, the commutation loop inductance reduces from 528 nH to 397 nH. Through these changes, the volume of the MV power stage is reduced by 66%.

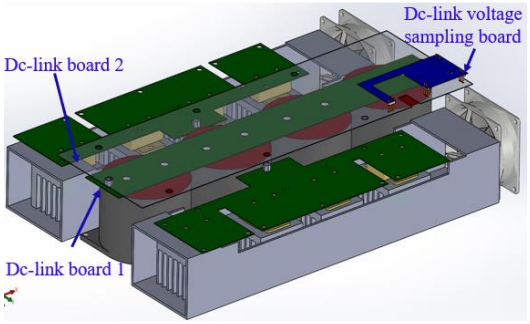

Fig. 8. The improved dc-link design.

B. Isolated GDPS Improvement

The isolated GDPS design is also improved, as shown in Fig. 9. Primary-side regulated fly-buck topology is adopted, considering the common mode noise immunity and control simplicity. A toroid core is used to achieve the required inductance with minimized size. The GDPS transformer is encapsulated with SilGel 613, which has good electric strength so that the insulation distance can be reduced, and the transformer size can be small. The creepage distance is achieved with bushing surrounding the two side terminals and bushing on the PCB board standoffs, which further minimizes the volume of the GDPS. With the improved design, the GDPS volume is reduced by 70% keeping the same insulation capability and power rating. Also, the coupling capacitance is reduced from 1.85 pF to 1.0 pF by adopting a new winding structure - putting the winding turns as closely as possible.

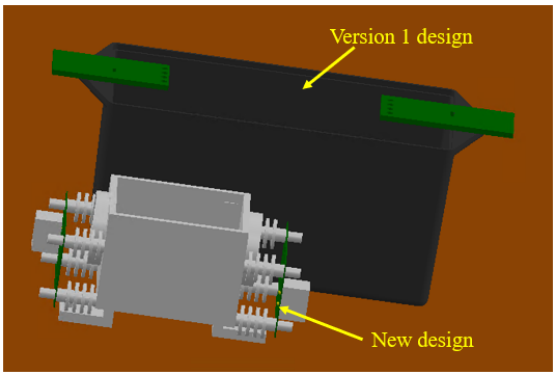

Fig. 9. The improved GDPS.

C. Other Improvements

The MV medium frequency transformer is also improved with partial shielding, having smaller parasitic capacitance, therefore the parasitic capacitance-related losses are reduced [27]. In the modified MV transformer, the leakage field related to the nanocrystalline core has been minimized, so that

the intrinsic leakage inductance and leakage related loss can be reduced, while the ferrite bridges have been inserted into the transformer core to achieve the desired leakage inductance value [36].

The LV power stage is also improved from the layout and heatsink size shrink, which achieves a 30% volume reduction. Moreover, the LV power stage devices are changed to Microchip 1.7 kV/35mΩ SiC MOSFET (MSC035SMA170B4) to reduce the conduction loss.

D. The New Power Unit

The improved power unit is shown in Fig. 10, and its dimensions are 15.5 inches × 8 inches × 27 inches. Compared to the version 1 power unit, the improved power unit volume is reduced by 64%.

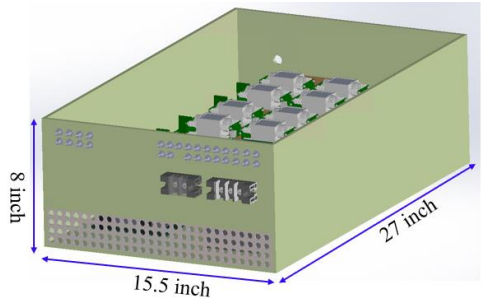

Fig. 10. The improved power unit.

VI. Version 2 Converter Prototype and Experimental Test Results

The second 13.8 kV/100 kW PCS converter prototype developed following the improved design is shown in Fig. 11, and its dimensions are 40 inches × 31.562 inches × 43.875 inches. Compared to the first version, the second version achieves a volume reduction of 49%. The three-phase tests have been conducted with three-phase RC loads, achieving the full voltage and power ratings, and the ac side PWM voltage and ac current waveforms are shown in Fig. 12.

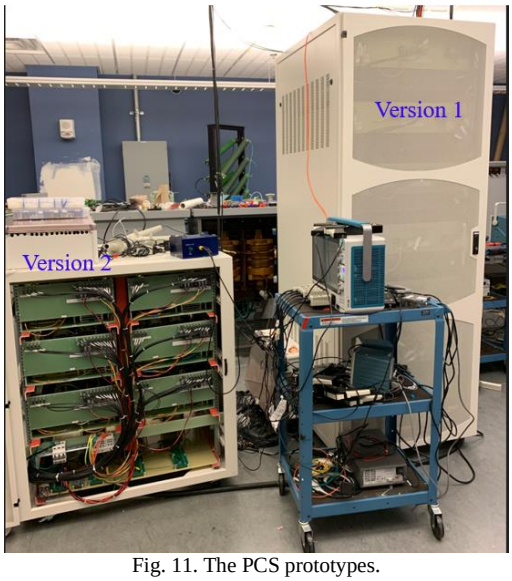

Fig. 11. The PCS prototypes.

The converter efficiency is measured with the same approach as the version 1 converter, and the peak efficiency is 98.4% at the rated output power. Therefore, compared to the first converter, the efficiency of the second one is improved by 2%. The efficiency improvement mainly comes from three parts:

a) 10 kV SiC MOSFETs with less loss are used. Two different versions of devices are used in the two converters. Compared to the 10 kV devices used in the version 2 converter, the devices used in the version 1 converter have a similar turn-off loss but a 2x turn-on loss.

b) The smaller parasitic capacitance-related loss is because of the smaller parasitic capacitance from the MV transformer and the GDPS.

c) The smaller leakage flux-related power losses in the MV transformers because of the adoption of optimized leakage integration strategy.

d) The smaller LV power stage loss because the 1.7 kV SiC MOSFETs with lower on-resistance are used.

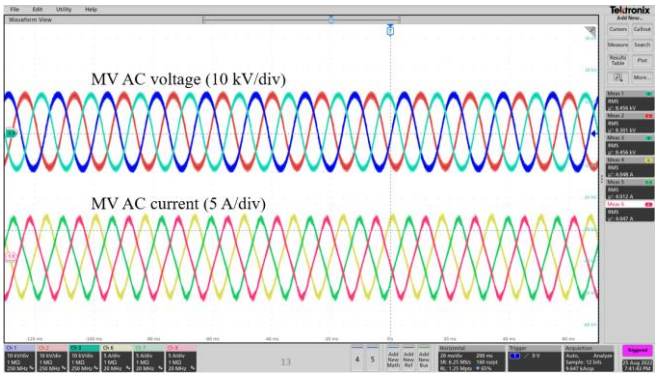

Fig. 12. The ac side voltage and current waveforms in the three-phase 13.8 kV/100 kVA test.

VII. Conclusions

This paper discusses the design and demonstration of two 13.8 kV/100 kW two-stage modular multilevel three-phase four-wire dc/ac converters. The design considerations of the main parts, including the device cooling, dc-link, GDPS, magnetics, and mechanical systems are presented. The design improvement in the version 2 converter is also discussed. Compared to the version 1 converter, the version 2 converter achieves 49% volume reduction through the design improvement of the MV power stage, MV GDPS, and LV power stage, and the efficiency is improved from 96.4% to 98.4% through using a better 10 kV SiC MOSFET with lower loss, parasitic capacitance reduction of the MV MF transformer with partial shielding, leakage flux-related loss reduction with better ferrite bridge structure, and better LV power stage devices with lower conduction loss. The design of both two converters is verified with experimental tests under the full voltage and power ratings.

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REFERENCES

[1] S. Ji, Z. Zhang, and F. Wang, "Overview of high voltage sic power semiconductor devices: development and application," *CES Transactions on Electrical Machines and Systems*, vol. 1, no. 3, pp. 254-264, 2017.

[2] A. Q. Huang, "Medium-Voltage Solid-State Transformer: Technology for a Smarter and Resilient Grid," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29-42, 2016.

[3] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, and A. Agarwal, "Characterization, Modeling, and Application of 10-kV SiC MOSFET," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1798-1806, 2008.

[4] D. Johannesson, M. Nawaz, and K. Ilves, "Assessment of 10 kV, 100 A Silicon CarbidemosfetPower Modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5215-5225, 2018.

[5] V. Pala, E. V. Brunt, L. Cheng, M. O. Loughlin, J. Richmond, A. Burk, S. T. Allen, D. Grider, J. W. Palmour, and C. J. Scozzie, "10 kV and 15 kV silicon carbide power MOSFETs for next-generation energy conversion and transmission systems," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 449-454.

[6] J. B. Casady, V. Pala, D. J. Lichtenwalner, E. V. Brunt, B. Hull, G. Wang, J. Richmond, S. T. Allen, D. Grider, and J. W. Palmour, "New Generation 10kV SiC Power MOSFET and Diodes for Industrial Applications," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1-8.

[7] A. H. Wijenayake, T. McNutt, K. J. Olejniczak, B. Passmore, A. Lostetter, J. Hayes, Y. Liu, and H. A. Mantooth, "Next-generation MVDC architecture based on 6.5 kV / 200 A, 12.5 mΩ SiC H-bridge and 10 kV / 240 A, 20 mΩ SiC dual power modules," in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, 2017, pp. 598-604.

[8] S. Ji, S. Zheng, F. Wang, and L. M. Tolbert, "Temperature-Dependent Characterization, Modeling, and Switching Speed-Limitation Analysis of Third-Generation 10-kV SiC MOSFET," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4317-4327, 2018.

[9] S. Ji, M. Laitinen, X. Huang, J. Sun, W. Giewont, F. Wang, and L. M. Tolbert, "Short-Circuit Characterization and Protection of 10-kV SiC <sc>mosfet</sc>," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1755-1764, 2019.

[10] A. N. Lemmon, R. C. Graves, R. L. Kini, M. R. Hontz, and R. Khanna, "Characterization and Modeling of 10-kV Silicon Carbide Modules for Naval Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 309-322, 2017.

[11] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% Efficient 10 kV SiC-Based 7 kV/400 V DC Transformer for Future Data Centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753-767, 2019.

[12] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3343-3360, 2015.

[13] X. Song, C. Peng, and A. Q. Huang, "A Medium-Voltage Hybrid DC Circuit Breaker, Part I: Solid-State Main Breaker Based on 15 kV SiC Emitter Turn-OFF Thyristor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 278-288, 2017.

[14] R. Chattopadhyay, S. Bhattacharya, N. C. Foureaux, S. M. Silva, F. B. Cardoso, H. d. Paula, I. A. Pires, P. C. Cortizio, L. Moraes, and J. A. d. S. Brito, "Low voltage PV power integration into medium voltage grid using high voltage SiC devices," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 3225-3232.

[15] F. Wang and S. Ji, "Benefits of high-voltage SiC-based power electronics in medium-voltage power-distribution grids," *Chinese Journal of Electrical Engineering*, vol. 7, no. 1, pp. 1-26, 2021.

[16] T. Lagier, P. Ladoux, and P. Dworakowski, "Potential of silicon carbide MOSFETs in the DC/DC converters for future HVDC offshore wind farms," 2017.

[17] R. Chen, F. Wang, L. M. Tolbert, X. Huang, D. Li, C. Nie, M. Lin, S. Ji, L. Zhang, J. E. Palmer, and W. Giewont, "10 kV SiC MOSFET Based Medium Voltage Power Conditioning System for Asynchronous Microgrids," *IEEE Access*, vol. 10, pp. 73294-73308, 2022.

[18] X. Huang, S. Ji, C. Nie, D. Li, M. Lin, L. M. Tolbert, F. Wang, and W. Giewont, "Comprehensive Analysis and Improvement Methods of Noise Immunity of Desat Protection for High Voltage SiC MOSFETs With High DV/DT," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 36-50, 2022.

[19] A. Anurag, S. Acharya, Y. Prabowo, G. Gohil, and S. Bhattacharya, "Design Considerations and Development of an Innovative Gate Driver for Medium-Voltage Power Devices With High <inline-formula><tex-math notation="LaTeX">dv/dt</tex-math></inline-formula>," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5256-5267, 2019.

[20] D. Rothmund, D. Bortis, and J. W. Kolar, "Highly compact isolated gate driver with ultrafast overcurrent protection for 10 kV SiC MOSFETs," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 4, pp. 278-291, 2018.

[21] L. Zhang, S. Ji, S. Gu, X. Huang, J. E. Palmer, W. Giewont, F. Wang, and L. M. Tolbert, "Design Considerations for High-Voltage-Insulated Gate Drive Power Supply for 10-kV SiC MOSFET Applied in Medium-Voltage Converter," *IEEE Transactions on Industrial Electronics*, pp. 1-1, 2020.

[22] K. Sun, Y. Xu, J. Wang, R. Burgos, and D. Boroyevich, "Insulation Design of Wireless Auxiliary Power Supply for Medium Voltage Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4200-4211, 2021.

[23] N. Yan, D. Dong, and R. Burgos, "A Multichannel High-Frequency Current Link Based Isolated Auxiliary Power Supply for Medium-Voltage Applications," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 674-686, 2022.

[24] Y. Xu, J. Stewart, H. Song, L. Cheng, I. Cvetkovic, R. Burgos, and D. Boroyevich, "High Power Density Medium-Voltage Converter Integration via Electric Field Management," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 1, pp. 895-905, 2022.

[25] H. Li, Z. Gao, R. Chen, and F. Wang, "Improved Double Pulse Test for Accurate Dynamic Characterization of Medium Voltage SiC Devices," *IEEE Transactions on Power Electronics*, pp. 1-11, 2022.

[26] X. Huang, S. Ji, J. Palmer, L. Zhang, L. M. Tolbert, and F. Wang, "Parasitic Capacitors' Impact on Switching Performance in a 10 kV SiC MOSFET Based Converter," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 311-318.

[27] H. Li, Z. Gao, and F. Wang, "A PWM Strategy for Cascaded H-bridges to Reduce the Loss Caused by Parasitic Capacitances of Medium Voltage Dual Active Bridge Transformers," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, p. (Accepted).

[28] J. Palmer, S. Ji, X. Huang, L. Zhang, W. Giewont, F. F. Wang, and L. M. Tolbert, "Improving Voltage Sensor Noise Immunity in a High Voltage and High dv/dt Environment," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 107-113.

[29] H. Li, Z. Gao, Z. Yang, C. Nie, and F. Wang, "A Medium Voltage Testbed for the Performance and Function Tests of a 13.8 kV Power Conditioning System Converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021.

[30] T. Batra, G. Gohil, A. K. Sesham, N. Rodriguez, and S. Bhattacharya, "Isolation design considerations for power supply of medium voltage silicon carbide gate drivers," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 2552-2559.

[31] S. Ozdemir, N. Altin, A. Nasiri, and R. Cuzner, "Review of Standards on Insulation Coordination for Medium Voltage Power Converters," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 236-249, 2021.

[32] J. P. Meadors and F. Wang, "Partial Discharge Testing Platform for PWM Voltage Source Converters in Electric Aircraft," in *2021 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, 2021, pp. 1-9.

[33] H. Li, P. Yao, Z. Gao, and F. Wang, "Medium Voltage Converter Inductor Insulation Design Considering Grid Requirements," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 2339-2350, 2022.

[34] H. Li, D. Li, Z. Gao, Y. Ma, Z. Yang, J. Wang, and F. Wang, "Development of a Power Electronics-based Testbed for a Flexible Combined Heat and Power System," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 764-770.

[35] H. Li, P. Yao, Z. Gao, and F. Wang, "Medium Voltage Converter Inductor Insulation Design Considering Grid Insulation Requirements," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2120-2126.

[36] Z. Gao, H. Li, and F. Wang, "A Medium-Voltage Transformer with Integrated Leakage Inductance for 10 kV SiC-Based Dual-Active-Bridge Converter," in *2022 IEEE 9th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2022.