I.1.1 High-Efficiency, Medium-Voltage-Input, Solid-State-Transformer-Based 400-kW/1000V/400A Extreme Fast Charger for Electric Vehicles ((Delta Electronics)

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Project Introduction

Range anxiety and long battery charging time continue to be critical challenges to mass adaptation of EVs. A major identified gap to wider adoption of BEVs is the ability and availability to refuel quickly or to fast charge. Studies have shown that in areas where drivers have access to 50-kW or 120-kW fast charge stations, annual electric vehicle (EV) miles traveled (i.e., eVMT) increased by over 25%, even in cases where fast charging was used for 1% to 5% of total charging events [1]. Charge stations of higher power not only alleviate the "range anxiety" and reduce the driver's waiting time, but also requires less investment. Michigan Energy Office completed a study in early 2019 titled "Electric Vehicle Charger Placement Optimization in Michigan: Phase I – Highways". This study finds a system with 150kW chargers, though more expensive individually, actually has lower total system cost when compared to a 50kW charging system when serving the same battery size EV [2]. To be truly competitive to the ICEV refueling experience, even higher power stations are necessary. However, high power charge stations would create large power draws from the grid. If this occurs during peak demand periods, grid capacity could be overloaded. This problem needs to be addressed to reduce the impact on the electric utility infrastructure.

The main goal of this project is to develop a 400-kW/400-A XFC system targeting total efficiency of 96.5 percent from the MVAC grid to a vehicle. The novel SST power cell topology, combined with a new silicon carbide (SiC) MOSFET device, enables a 3.5 percent improvement in system efficiency, a 50-percent smaller equipment footprint, and four times less weight than today's DCFC systems. The SST technology would directly utilize MVAC at 4.8-kV or 13.2-kV. This would eliminate the line frequency transformer (LFT), which steps down medium-voltage AC to 3-Phase 480-V line-to-line voltage in current DCFC systems.

Objectives

The objectives of the program are:

To design and test a high-efficiency, medium-voltage-input, solid-state-transformer-based 400-kW Extreme Fast Charger (XFC) for electric vehicles, achieving better than 96.5 percent efficiency.

To demonstrate extreme fast charging with a retrofitted General Motors' light-duty battery electric vehicle at 3C or higher charging rate for at least 50 percent increase of SOC.

To achieve a 180-mile charge within 10 minutes.

Approach

The team developed the XFC system specification and module specifications. It includes the System architecture, SST specification, DC charger specification, charge interface specification, communication architecture, fault protection specification, and installation specification. The system block diagram is illustrated in Figure I.1.1.1.

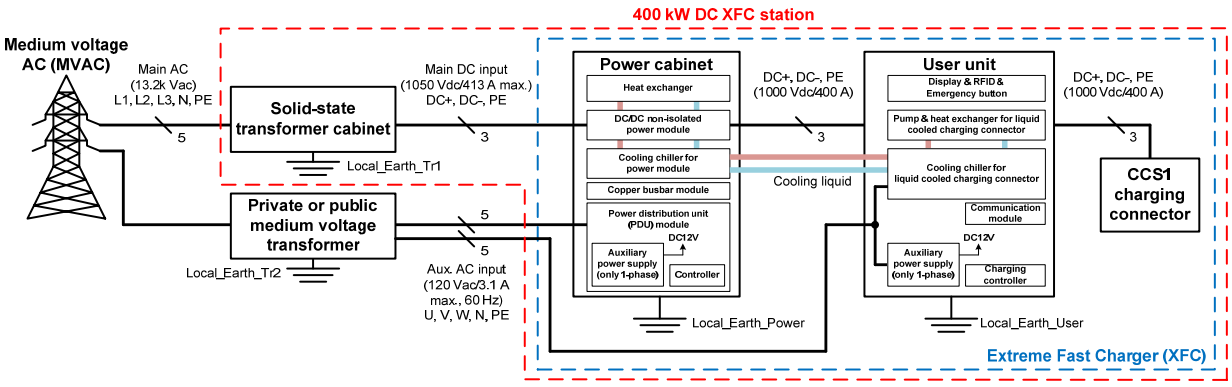


Figure I.1.1.1 XFC System Architecture

The XFC system consists of a Solid-State Transformer (SST), a Charge Controller (in power cabinet), and a Charge Dispenser (A.K.A. User Unit). The SST is the key component in the whole system because it has multiple functions such as voltage step-down, AC/DC conversion, MV insulation, and grid interface. Of all the possibilities of medium voltage levels, the standard voltages most often used in the United States are 4.16-KV, 4.8-KV, 12.47-KV, 13.2-KV, 13.8-KV, etc. The team selected modularized architecture to accommodate the various voltages. For the 4.8-kV AC medium-voltage applications, each phase has twelve modules connected in a four-series and three-parallel configurations. Alternatively, for a 13.2-kV medium-voltage application, nine power cells in each phase are connected in series for the higher voltage. For both voltage levels, the outputs of all the power cells are connected in parallel to provide total 400-kW power to the 1-kV intermediate DC bus. Each SST module is rated at 15-kW, which is optimized for the transformer thermal dissipation. Cascaded H-bridge (CHB) topology is used in system level, which lowers the voltage stress on semiconductor devices, reduces the filter size with more voltage level, and improves the power quality and electromagnetic interference (EMI) performance on grid side. The power module's circuit diagram is illustrated in Figure I.1.1.2.

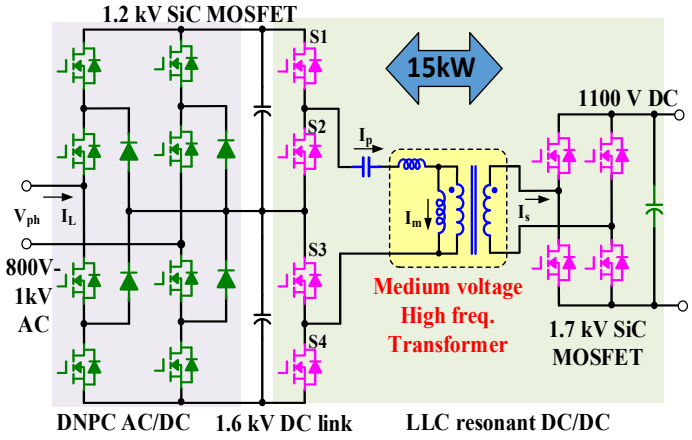


Figure I.1.1.2 Circuit Diagram of Power Module

Silicon Carbide (SiC) power switches are more suitable for high voltage, high frequencies and high-temperature operation compared to the Si counterparts due to the superior properties [3]-[5]. For the SST and charge controller in the XFC system, high-efficiency and high-power density design is expected while the system operates at high voltage and high-switching frequency. As a result, SiC switches are the key technology to achieve the challenging design target.

The transformer winding structure design with medium voltage insulation capability was analyzed in the context of SST converter topology to assess the best system performance. Different insulation material were compared. The transformer loss was simulated to achieve the best balance between winding loss and core loss. Electrical circuit, mechanical package and control software were developed around the power switch circuit and the isolation transformer. Two sets of version 1.5 SST cells have been built and tested. The picture of SST module is shown in the left half of Figure I.1.1.3.
The 400-kW charging controller has a modularized design as well. The power modules, each capable of outputting 200-A, are connected in parallel. The maximum output power of each module is determined by the power dissipation and thermal design. Based on the original design target of 120-kW, four charge controller modules will be needed to provide 400-kW. Detailed analysis and simulation shows that the module has potential to output 135kW through design optimization. The charging controller module is based on Buck topology, thus also called Buck module. The buck converter runs at continuous conduction mode (CCM) with 50-kHz switching frequency. A full-bridge SiC MOSFET module with 1.2-kV, 50-A rating is used as the switching device. Two sets of version charging controller modules were built and tested. The picture of charging controller module is shown in the right half of Figure I.1.1.3.

Figure I.1.1.3 Picture of an SST Module at left, and Charging Controller (Buck) Module at right

The SST module, the charging controller module and the SST controller were integrated into a 15-kW charge system and tested.
Each SST module is capable of handling 1-kV AC input voltage. Four SST modules were connected in series for single phase of 4.8-kV system, which has 2.77-kV phase voltage. The output of the SST modules are connected in parallel. The output voltage of the SST modules is 1050V, to allow the charging controller to further step down to 1000V or less.
In parallel to the XFC development, General Motor has been developing the vehicle Rechargeable Energy Storage System (RESS), Charge Inlet, and Vehicle Integration Control Module (VICM). The team tested RESS candidate battery cell and verified the cells can take 3C charge and even higher rate for short time. The battery package is configured to receive 400-kW charge power, supporting the program objectives.

Results

Test Results from Delta's Livonia Lab

The SST module was tested on bench. The test result matches the design calculation very well and meets the specification. The peak efficiency is 97.8%. Figure I.1.1.4 shows one of the operation waveforms of the SST's AC/DC stage and Figure I.1.1.5 shows the operation waveforms of the SST's DC/DC stage.

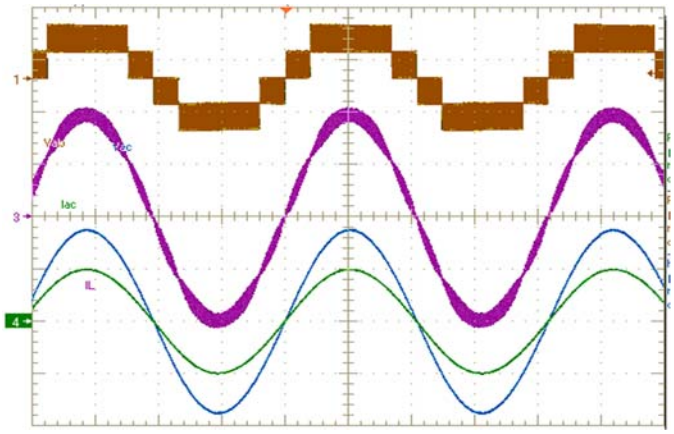


Figure I.1.1.4 SST's AC/DC Stage Waveforms (CH1 brown: Vph, CH2 blue: V_{AC}, CH3 purple: V_L, CH4 green: I_{AC})

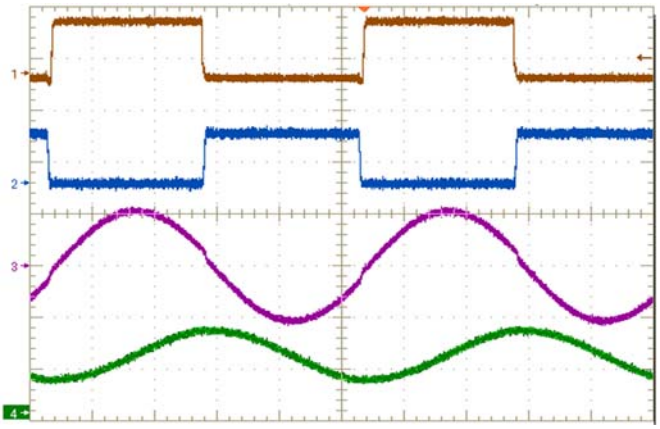


Figure I.1.1.5 SST's DC/DC Stage Waveforms (CH1 brown: V_{GS}, CH2 blue: V_{DS}, CH3 purple: I_{Lr}, CH4 green: V_{Cr})

Buck Module

The Buck module was tested on bench. The result matches the design calculation and meets the specification. The peak efficiency is 99.2%.

1-Phase Series SST and Buck Module Integrated Test

The four SST modules are integrated into the SST cabinet at center. The cabinet at left contains the line filter inductors, line voltage sensors and current sensors. The cabinet at right contains the SST controller and output filter. Figure I.1.1.6 shows the test system.

Figure I.1.1.6 1-Phase Series SST and Buck Module Test Setup (up to 45-kW)

This system was tested from 4.5kW to 45-kW and in a wide range of input voltage and output voltage. Figure I.1.1.7 shows the efficiency test result.

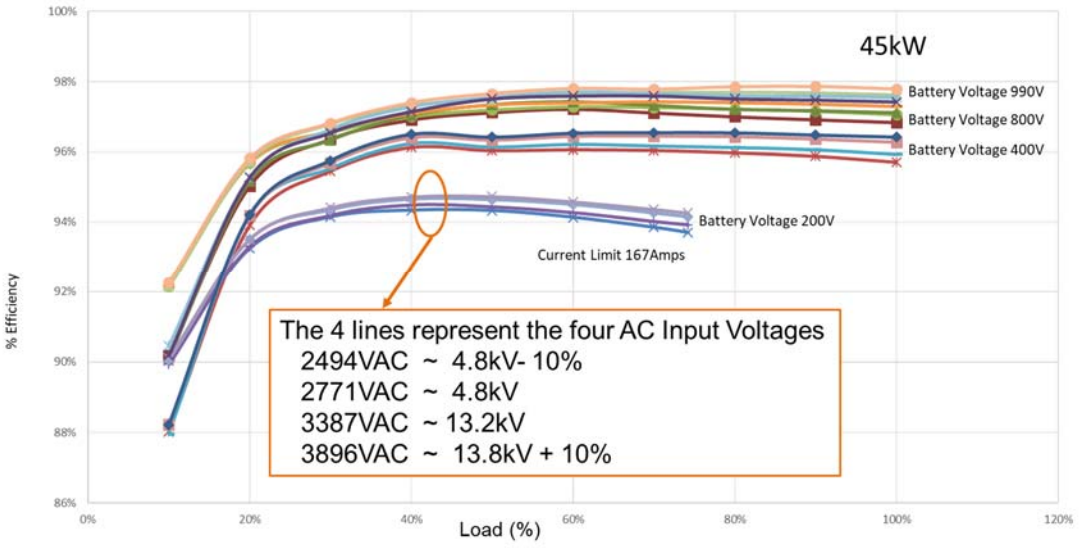


Figure I.1.1.7 1-Phase Series SST and Buck Module Efficiency Test Result (up to 45-kW)

Simulation and Study Results from Virginia Tech

High frequency transformer with medium voltage insulation capability

Transformer core material evaluation and selection.

In high frequency applications, a good core material can provide high permeability as well as low core loss density. Three main material candidates for high frequency transformer are: amorphous, nanocrystalline, and ferrite. The core loss density of the three material candidates are compared at different frequency, as shown in Fig. 8 We can see that when the frequency is higher than 200 kHz, ferrite material is a very good candidate, especially considering that as the working frequency increases, the reasonable working flux density will decrease.

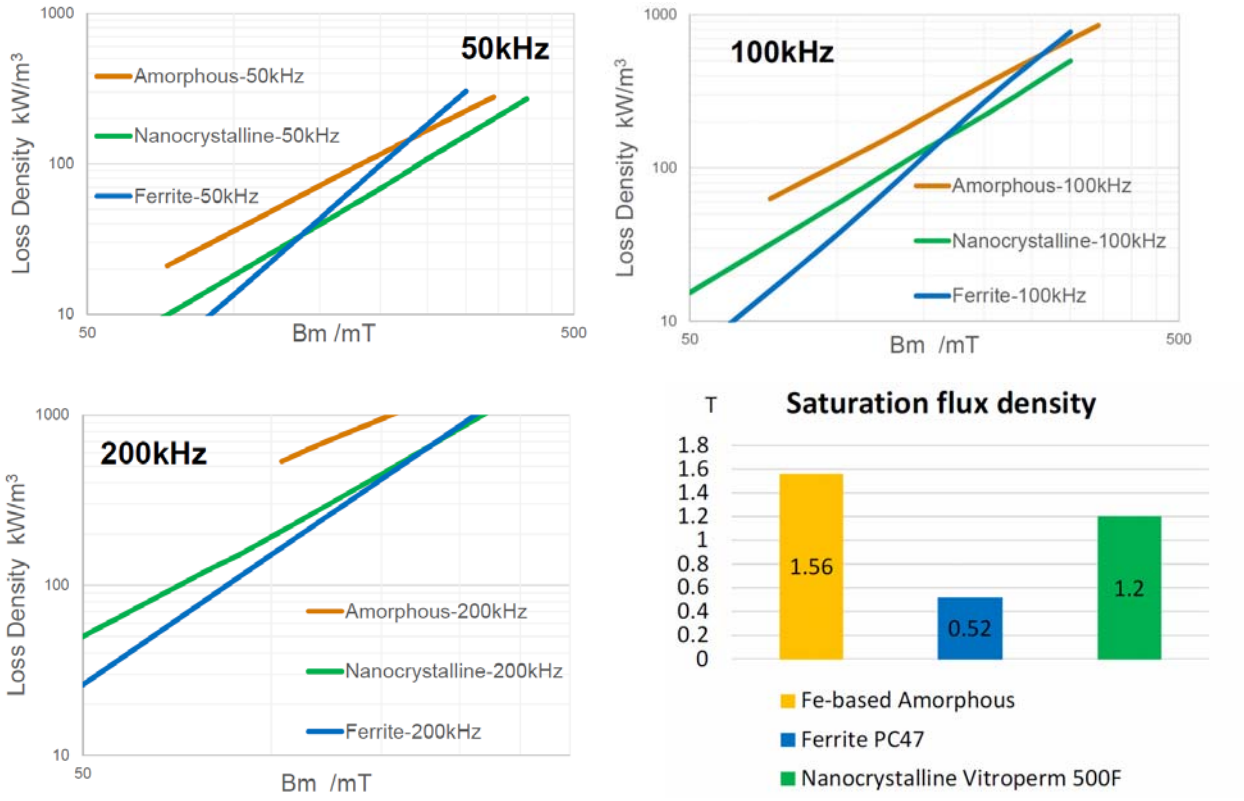
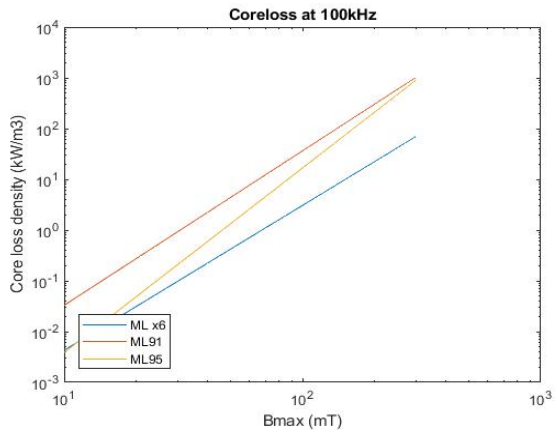


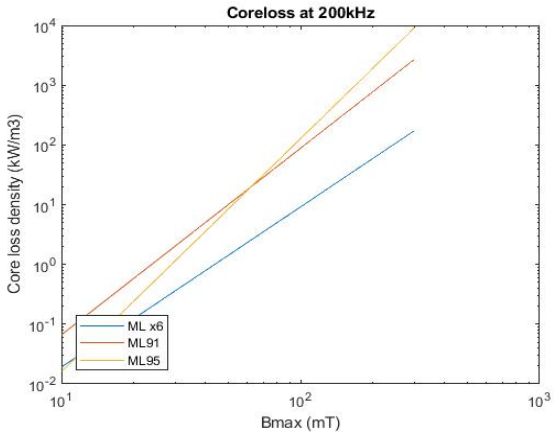
Fig. 8 Core material comparison

The newest materials we can have at this moment are: MLx6, ML91, and ML95. A comparison between these MnZn ferrite materials is also made. The test result is shown in Fig. 9 for different working frequencies.

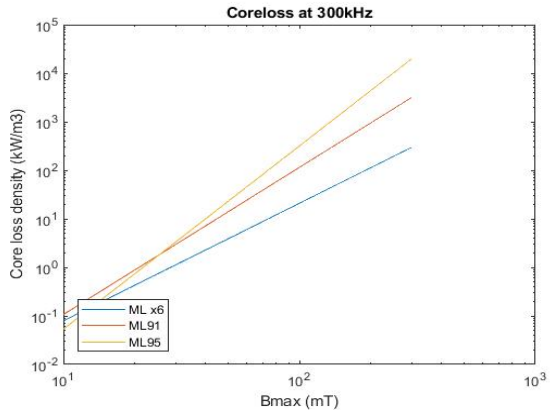
Based on the test results, we will choose MLx6 as the core material for working flux density under 300mT and working frequency between 100 kHz and 500 kHz.



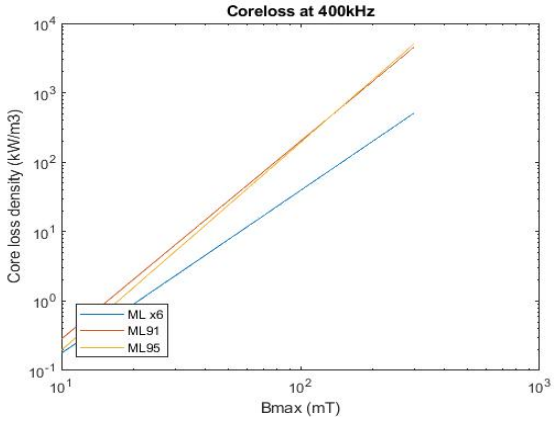
(1) f=100kHz



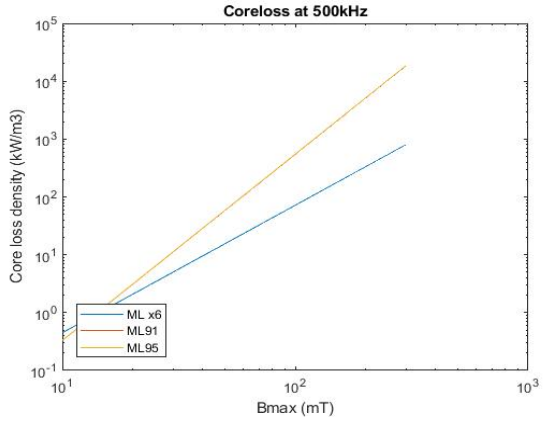
(2) f=100kHz



(3)300kHz



(4)400kHz



(5) 500kHz

Fig. 9 Core loss density comparison between different MnZn ferrite material at 100~500kHz

Transformer winding structure design with medium voltage insulation capability.

System and module structure

The whole fast charger system is shown in Fig. 10 with a medium voltage (13.2kV) input and 1.1kV output voltage. The detail dc-dc circuit of one of the cascaded submodules is shown in Fig. 11. It is obvious that only the high frequency isolated transformer can provide insulation for overall system and it should be designed based on the input medium voltage. Insulation between primary high voltage winding and secondary low voltage winding and transformer core should be designed based on 13.2kV insulation requirement. However, insulation between secondary winding and core only need to be designed based on 1.1kV level.

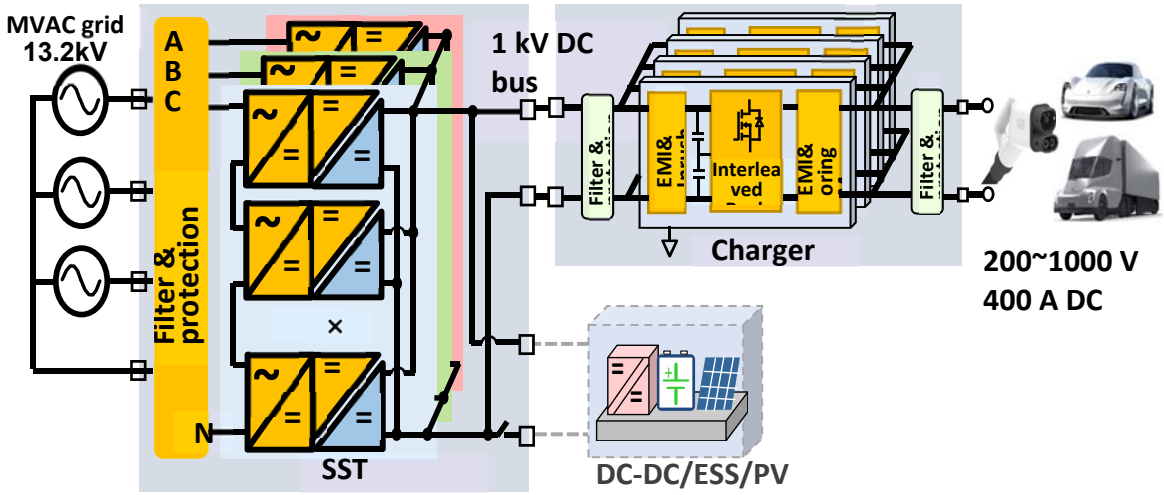


Fig. 10 System Structure

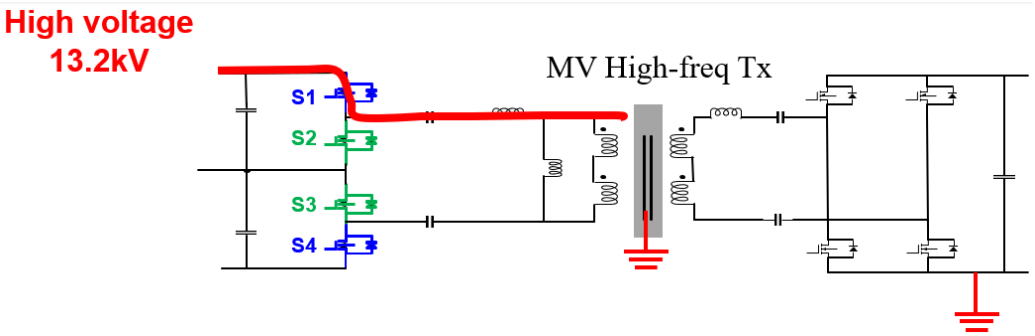


Fig. 11 DC/DC module

Transformer structure

In this transformer design, UI core is selected and both primary and secondary windings on the two legs are connected in series.

Partial discharge (PD) is the most severe electrically driven degradation mode for ac insulation due to trapped air voids in the insulation system. If air is present inside or around the insulation, PD may happen in the air. The discharge will cause slow damage to the insulation that's next to the air volume. So, it is important to eliminate air voids around the high voltage insulation.

In previous transformer design, bobbin, tape, and epoxy are applied, as shown in Fig. 12. However, with this structure, there's many air voids around the primary side winding and it's almost impossible to eliminate these air voids. To eliminate the air voids between primary side winding and the insulation structure around it, we remove the bobbin and tape structure and then capsule the primary side winding with only epoxy.

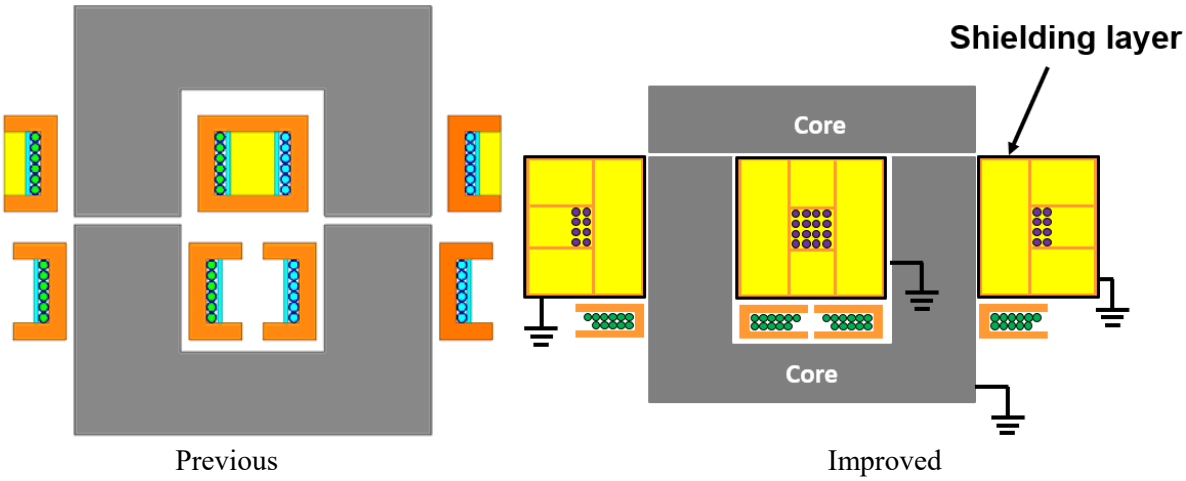


Fig. 12 Transformer Design (a) Previous design (b) Improved design

To avoid partial discharge in the air between primary side winding/epoxy and core, we apply a shielding layer outside the epoxy. The shielding layer is also grounded and provides an electrical field shield. So, the electric field strength in the air is almost 0 and no partial discharge will happen.

Proper material is the key to the insulation encapsulation. For the dielectric strength, most insulation materials are at almost the same level (around 20kV/mm). Viscosity, thermal conductivity, curing time, and hardness are more crucial. From electric performance point of view, the insulation material should be with high thermal conductivity to avoid thermal issue. However, high thermal conductivity material always has high viscosity (e.g., 50-3182NC with 15000 cps and 1.66W/mK). It is hard for the air bubble to escape from the high viscosity insulation material. Partial discharge level will be higher than expectation with air bubble trapped in the insulation material. With low viscosity material, air voids can be easily eliminated from the insulation layer, which is beneficial to creating a partial discharge free insulation structure. Curing time is another important factor. The air bubble will not have enough time to escape from the insulation material with short cure time, which is harmful for the insulation manufacturing. From hardness point of view, gel is preferred rather than the hard epoxy after curing to avoid cracking which will damage the fragile insulation encapsulation.

The epoxy material candidates are listed in Table I. SilGel 612 is selected considering dielectric strength, thermal conductivity, and Viscosity. For a given material, the dielectric strength is a function of the thickness and can be estimated as:

$$\frac{E}{E_{ref}} = \left(\frac{D_{ref}}{d_{epoxy}}\right)^{0.4}$$

where E is the dielectric strength in Epoxy at given thickness d_{epoxy}, and E_{ref} is the dielectric strength at given testing thickness D_{ref}.

Insulation thickness is determined for 13.2kV application according to IEEE standard. Assume that the electric field in the epoxy is uniform. Then the thickness of epoxy can be calculated as:

$$\frac{48kV/d_{epoxy}}{23kV/mm} = 0.3 \times \left(\frac{3.175mm}{d_{epoxy}}\right)^{0.4}$$

Table I. Epoxy Material Candidates

Insulation Material Candidate	50-3182 NC	EPIC Resin R1055/H5083	SilGel 612
Dielectric Strength	22 kV/mm	22.6 kV/mm	23 kV/mm
Cure time	85°C for 3-4 hours or 100°C for2-3 hours	25°C for 2 hours or 50°C for 100 mins	25°C for 8 hours or 100°C for 15 mins
Thermal conductivity	1.66 W/mK	0.42 W/mK	0.3 W/mK
Viscosity	15,000	3,300	1,900
Hardness after curing	Hard	Hard	Soft

Insulation capability is preliminary verified in Finite Element Analysis (FEA) electric field simulation, as shown in Fig. 13.

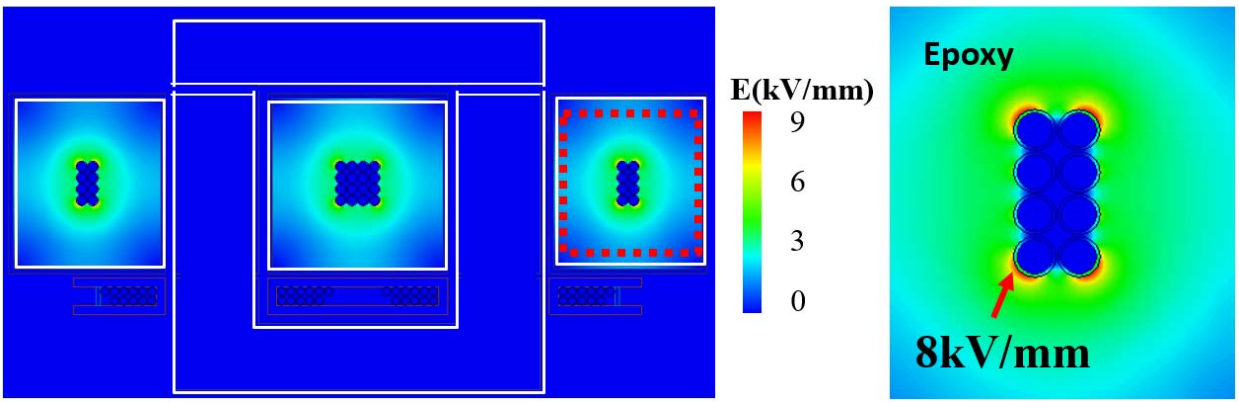


Fig. 13 Electric field simulation result

From the simulation result, the highest electric field in the insulation material is no more than 8kV/mm, which satisfies the requirement of insulation.

Termination Design

By applying the shielding layer, zero voltage potential is built on the surface of the winding encapsulation. Safe creepage and clearance distance is required between the high voltage primary side and the zero-voltage shielding, as shown in Fig. 14. However, the shielding layer's sharp fringes cause equipotential lines concentrating at the edge of the shielding layer on the termination sleeve, causing high electric field stress, as shown in Fig. 15(a). That also increases the possibility of generating partial discharge. A high permittivity layer is applied on the surface of the termination sleeves to solve this problem. This stress grading layer can be modeled as a series of RC network. Such method makes the equipotential line more uniform on the termination sleeve and lowers the electrical stress at the point of shield discontinuity by refracting the electrical stress. The stress grading layer allows the equipotential lines to spread out along the insulation interface of the termination sleeves, as shown in Fig. 15(b). By doing this, the surface stress of the termination is greatly reduced, which improves termination performance.

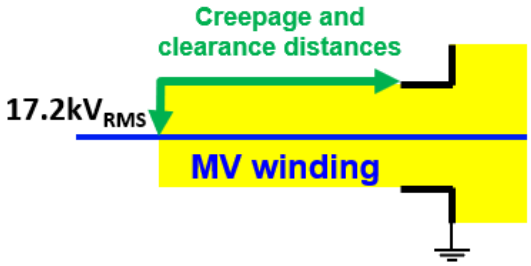


Fig. 14 HFT Termination Design

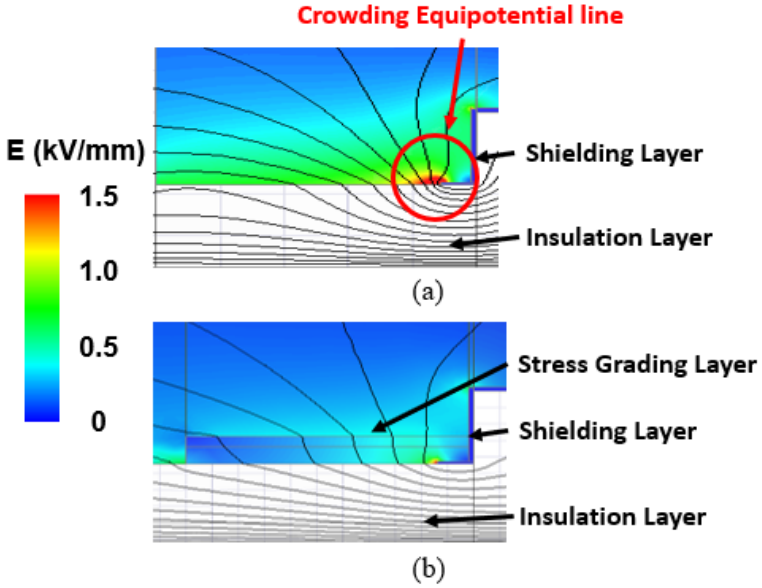


Fig. 15 Simulation result for termination design

(a) without stress grading layer, (b) with stress grading layer

Litz wire's impact on partial discharge

The air trap inside litz wire is another concern in this application and has a huge impact on the partial discharge test. Recently we noticed that the selection of litz wire insulation makes a big difference on the partial discharge inception voltage (PDIV). Fig. 16 shows the structure of the primary-side medium voltage winding with insulation capability.

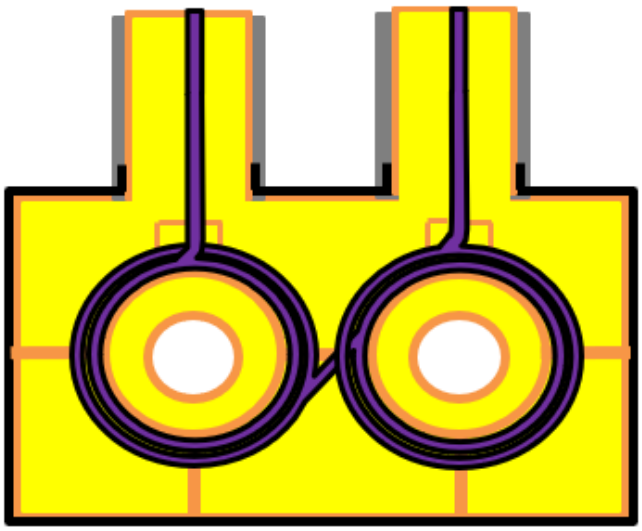


Fig. 16 Structure of primary-side medium voltage winding with insulation

The tested PDIV is 8.2kV, which is far below 17.2kV as the standard indicates. Then several test results are compared to exclude two suspected reasons for partial discharge, either the sleeve of stress grading layer on termination or the air voids inside the insulation material (silicone). Finally, measurement results show that it is the insulation layer of the litz wire that makes a big different. Previously we use the litz wire covered by a Teflon layer, as shown in Fig. 17(a). This kind of insulation layer has a high insulation level (1000V). However, also due to this Teflon layer, air voids are inevitable in the litz wire bundle. Then this air voids trapped in litz wire become the weak point when the whole medium voltage winding is under partial discharge test. By using another soft coating litz wire, as shown in Fig. 17(b), the air voids inside the litz wire bundle no longer exist because the liquid insulation material can now immerse through the soft coating and fill up the air voids inside a litz wire bundle. Experimental result shows that the medium voltage winding using the soft coating litz wire is partial discharge free at 17.2kV.

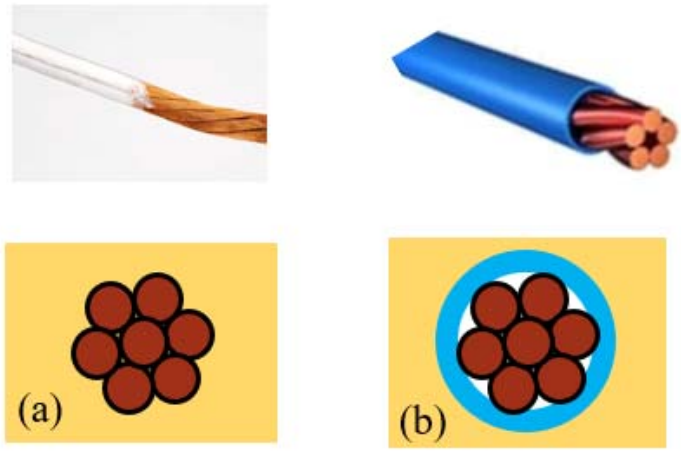


Fig. 17 (a)Litz wire with silk coating (b) Litz wire with FEP jacket

Design and optimization of high frequency transformer

Transformer loss and size trade-off at given switching frequency

Previously, we have determined the core material, transformer structure, insulation material and litz wire gauge for a given switching frequency (f_s), 200 kHz. Then the core loss (P_{core}), winding loss ($P_{winding}$), and transformer total volume (V_{Tr}) can be calculated for each number of turns with given core loss density (P_v).

Core Loss Model

To estimate the core loss, Steinmetz Equation is used as follows:

$$P_v' = k \cdot f_s^{\alpha} \cdot B_m^{\beta}$$

where P_v' is the core loss density under sinusoidal excitation. k, α, β are constants from curve fitting data. f_s is the switching frequency of the sinusoidal waveform. B_m is the peak flux amplitude. For CLLC topology, the excitation on the transformer core is the square waveform, and the Rectangular Extension Steinmetz Equation is proposed to exactly predict core loss under the rectangular voltage excitation as follows:

$$A_e = nV_0/(4N \cdot B_m \cdot f_s)$$

$$P_v = \frac{8}{\pi^2} k \cdot f_s^{\alpha} \cdot B_m^{\beta}$$

For cross section area of the core A_e, it is derived from the Faraday's Law. And the core loss is calculated by core loss density times core volume as shown below:

$$P_{core} = P_v \cdot A_e \cdot l_c$$

where V_o is the DC output voltage. n is the turns ratio. N represents the primary side turns number. l_c means magnetic loop length in the core. B_m is a function of P_v and f_s. Note that l_c is a function of A_e and N. Therefore, in order to calculate core loss, there are three design variables: turns number N, core loss density P_v, and switching frequency f_s.

Such a method assumes magnetic flux distributes uniformly inside the core. To verify this assumption, an FEA simulation is built with $N = 16$, $P_v = 300\ kW/m^3$, and $f_s = 200\ kHz$. The simulation and the result are shown in Fig. 18. Core loss is 24 W in the simulation and the calculated core loss is 25 W. The error between the calculation and simulation is negligible, which means the model is accurate and can be used for further analysis.

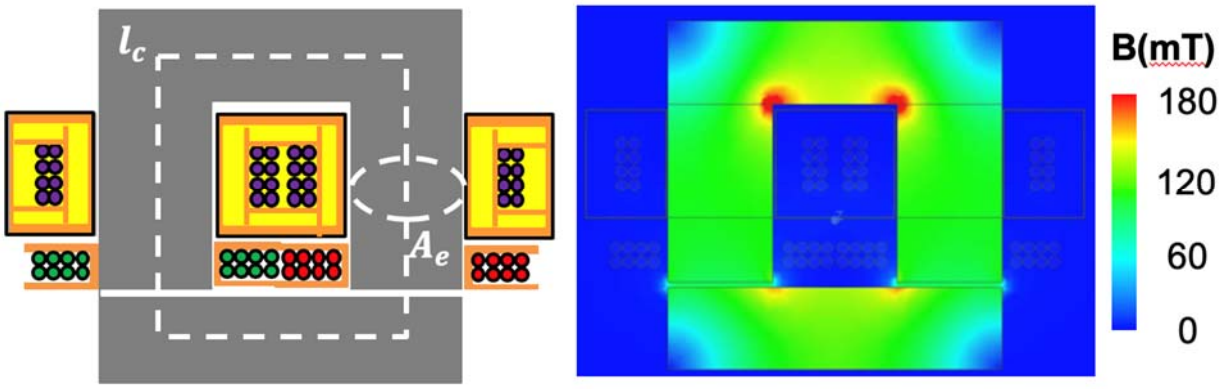


Fig. 18 Magnetic field distribution in the core.

Winding Loss Model

Litz wire is widely used for the high frequency transformer. Litz wire strand AWG is selected based on operating frequency and manufacture's recommendation. AWG 42 is

chosen for the 200-kHz application as an example. The equivalent AWG is selected as AWG 15 according to NPFA 70 National Electrical Code for a 15-kW 22-A RMS current application.

The winding insulation material is another critical component in medium voltage transformer design. The high dielectric strength is the first priority to achieve compact transformer winding design. For high frequency applications, the dissipation factor is also important for relatively low dielectric loss. High thermal conductivity is required to extract winding loss from insulation encapsulation. Material viscosity cannot be ignored during the fabrication process; it is easy for air cavity to be trapped inside high viscosity material. That increases the possibility for partial discharge. Three winding insulation material candidates are listed in TABLE II. SilGel 612 is finally selected for its low viscosity and high dielectric strength.

TABLE II WINDING INSULATION MATERIAL CANDIDATE COMPARISON

Material candidate	**R1055/H5083**	**50-3182NC**	**SilGel 612**
Dielectric Strength	22.6kV/mm	22kV/mm	24kV/mm
Dissipation Factor	0.022	0.018	0.008
Thermal Conductivity	0.42W/(mK)	1.66W/(mK)	0.2W/(mK)
Viscosity	3,000cps	15,000cps	1,900cps

To calculate Litz wire winding loss, the squared field derivative (SFD) method is used for eddy current power dissipation in turn j, with assumptions that the magnetic field remains constant inside each Litz wire strand and no eddy current flows between different strands.

$$P_{eddy,j} = \frac{\pi N_s l_j d_s^4}{64\rho_c} \langle \overline{\left(\frac{dB}{dt}\right)^2} \rangle_j$$

where N_s is the strands number, l_j is the winding length for turn j, d_s is the strand diameter, ρ_c is the conductivity for copper, $\langle \cdot \rangle_j$ is the space average for turn j, and $\bar{x}$ is the time average. dB/dt can be obtained from the simulation, as shown in Fig. 19.

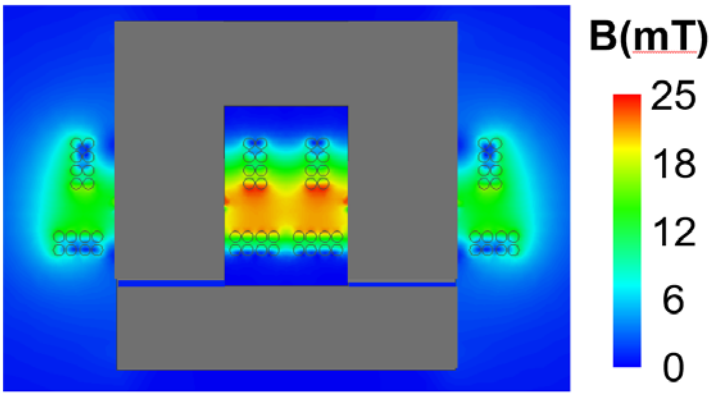


Fig. 19 Magnetic field distribution in the core.

The winding loss with non-eddy current effect can be calculated easily with I^2R , and the total winding loss is the sum of eddy current loss and non-eddy current loss as below.

$$P_{non-eddy,j} = \frac{4\rho_c l_j}{N_s \pi d_s^4} I_{rms}^2$$

$$P_{winding} = \sum_{j=1}^{N} \left(\frac{\pi N_s l_j d_s^4}{64\rho_c} \left\langle \overline{\left(\frac{dB}{dt}\right)^2} \right\rangle_j + \frac{4\rho_c l_j}{N_s \pi d_s^4} I_{rms}^2 \right)$$

In winding loss, dB/dt is a function of switching frequency f_s. l_j is a function of cross section area A_e, which is related to turns number N and core loss density P_v. N, P_v, and f_s are still the design parameters for winding loss. To verify this model, a transformer prototype is built, and the winding resistance is measured through an impedance analyzer. Fig. 13 indicates that the calculated winding resistance matches with the measurement.

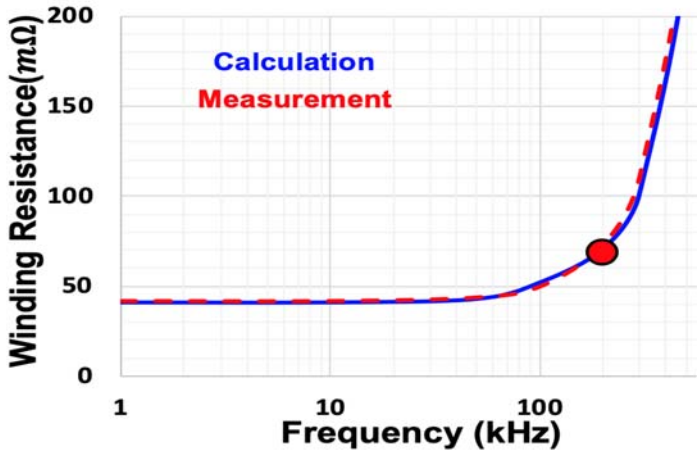


Fig. 20 Winding Resistance verification.

Then the transformer loss (P_{Tr}) is the sum of core loss and winding loss.

$$P_{Tr} = P_{core} + P_{winding}$$

After selecting the core material, winding AWG, winding equivalent AWG, and insulation material, there are still three design variables, including turns number N, core loss density P_v, and switching frequency f_s. Based on the core loss and the winding loss model, a transformer optimization method is proposed for multiple design objectives, including core loss, winding loss, and transformer volume. In order to have a clear picture on the impact of each design variable, a 3-step optimization method is utilized.

Transformer Optimization Steps

Step #1: Sweep turns number (N) with given $P_v = 300\ kW/m^3$ and $f_s = 200\ kHz$

The transformer core loss, the winding loss, and the transformer volume with a swept N are plotted in Fig. 21. With given P_v and f_s, core loss will decrease when N increases. We learn that A_e will shrink with the increment of N, and thus core loss reduces. For winding loss, a larger turns number will increase the total length of the winding, leading to higher winding loss. From the volume point of view, the height of the transformer will be higher with the turns number increasing; however, the width and the length will decrease due to smaller A_e. The transformer volume will be smaller with larger turns numbers in the interested turns number range (8-24) obtained from the loss calculation.

Step #2: Sweep N and P_v with given $f_s = 200\ kHz$

*Fig. 16*Fig. 21 shows the design result when considering only the one parameter N. Adding core loss density and switching frequency information to the same plot will be complicated to read; therefore, a plot with total loss as the vertical axis and volume as the horizontal axis is proposed for better clarity. The transformer loss and device loss are both taken into consideration in this plot. That is because switching frequency will impact device loss. Bearing this in mind, total loss will be unbiased when switching frequency impact is taken into consideration. Two trade-offs are considered in the design process. The first trade-off is to find the best total loss and transformer volume. This is followed by the trade-off between core loss and winding loss. Insulation encapsulation always has lower thermal conductivity, which means lower winding loss is favored. Because of this, 24 turns cases will be ignored in the following analysis.

Core loss density from $100\ kW/m^3$ to $600\ kW/m^3$ are taken into consideration in order to evaluate the core loss density impact. A further simplification is made by hiding detailed design points. The result is shown in Fig. 22. Each line represents one core loss density. For a given core loss density, the turns number decreases from the left side to right. At the low core loss density region ($P_v = 100\ kW/m^3$), the transformer volume increases while there is almost no benefit on loss. At the high core loss density region ($P_v = 600\ kW/m^3$), the total loss is higher but the transformer volume is almost the same. According to such a phenomenon, the design region is restrained to $P_v = 200 - 600\ kW/m^3$. Among these four curves, the valley point for each curve is selected to have

smaller loss. Another curve can be drawn based on these four valley points, and the design region can be finally selected around such curve.

Step #3: Sweep N, P_v and f_s

To explore the impact of switching frequency from $100\ kHz$ to $300\ kHz$, the same methodology is utilized based on Step #2, as shown in Fig. 23 and Fig. 24. For each switching frequency, a design region could be selected. Five design regions can be plotted in the same plot to have a better understanding of how switching frequency impacts transformer design. This is shown in Fig. 25. One point can be selected for each frequency, and the final design region can be figured out. It is clear to see that when switching frequency is less than $200\ \mathrm{kHz}$, the volume increases with almost the same loss. At high frequency region ($\mathrm{f_s} > 300\ \mathrm{kHz}$), total loss increases rapidly; however, there is no benefit from the transformer volume point of view. At $100\mathrm{kHz}$, the core volume impacts the total volume a lot. Although low frequency will lead to lower eddy current loss and smaller core loss density with certain $\mathrm{B_m}$, the core volume increases due to low frequency and winding length also increases. Thus, there is almost no benefit on loss reduction. For higher frequency range, both winding loss and core loss will increase at such a switching frequency. Although the core volume will decrease with the increasing switching frequency, the insulation volume cannot be compressed.

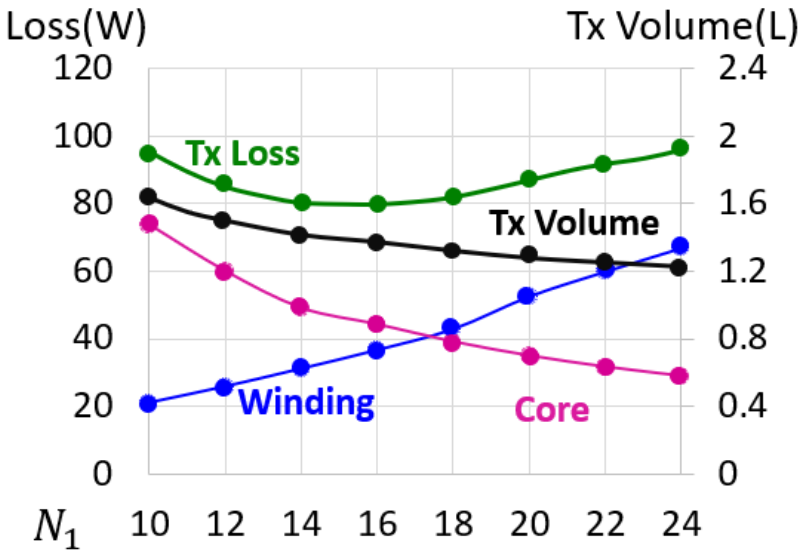


Fig. 21 Transformer loss and volume for given frequency and given core loss density

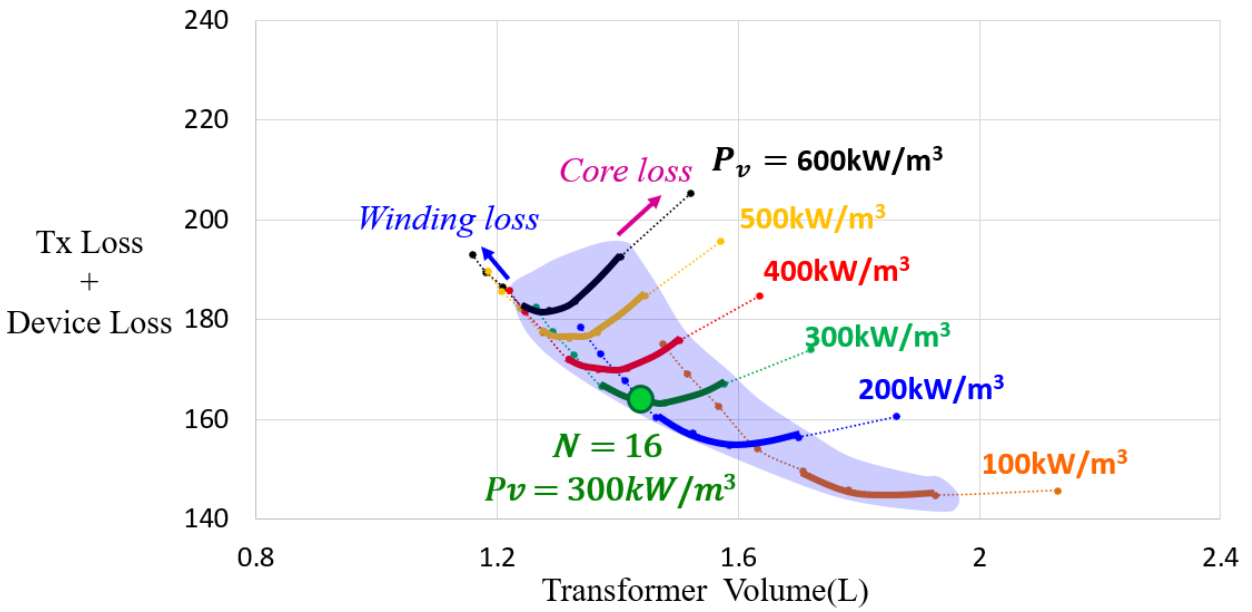


Fig. 22 Transformer loss and size trade-off at 200k Hz

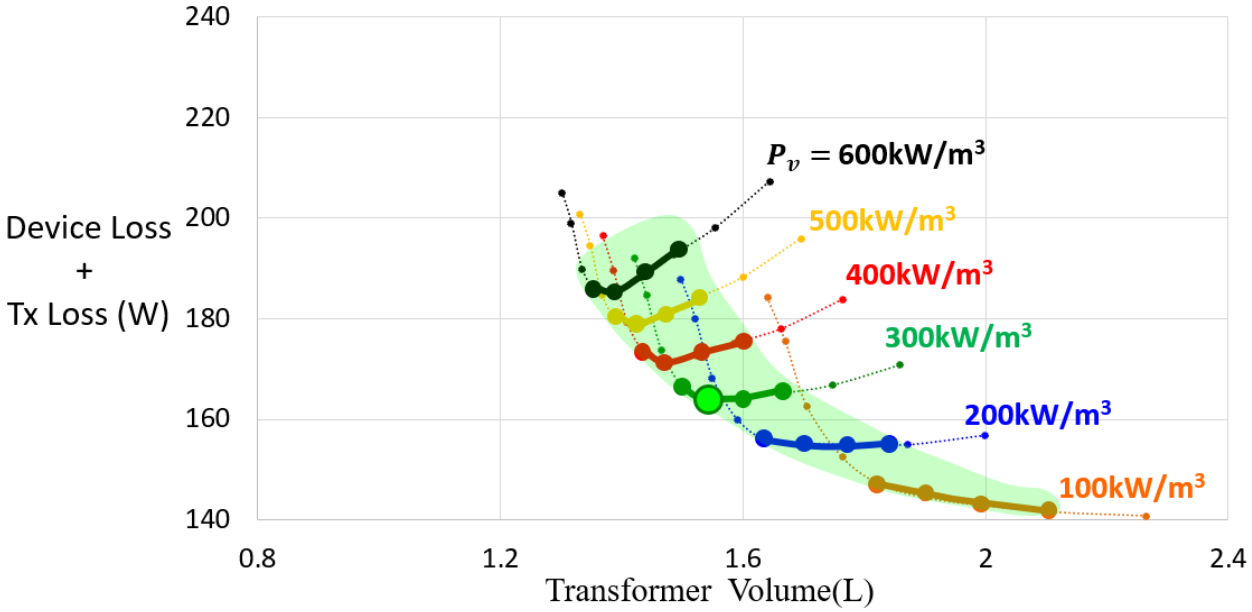


Fig. 23 Transformer loss and size trade-off at 100k Hz

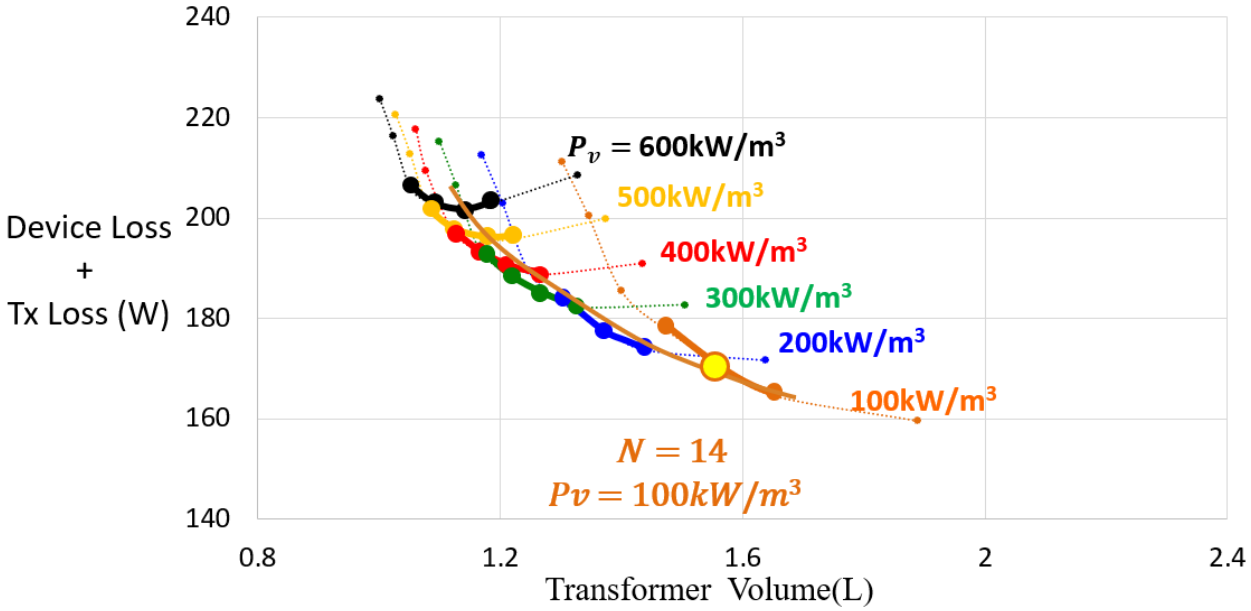


Fig. 24 Transformer loss and size trade-off at 300k Hz

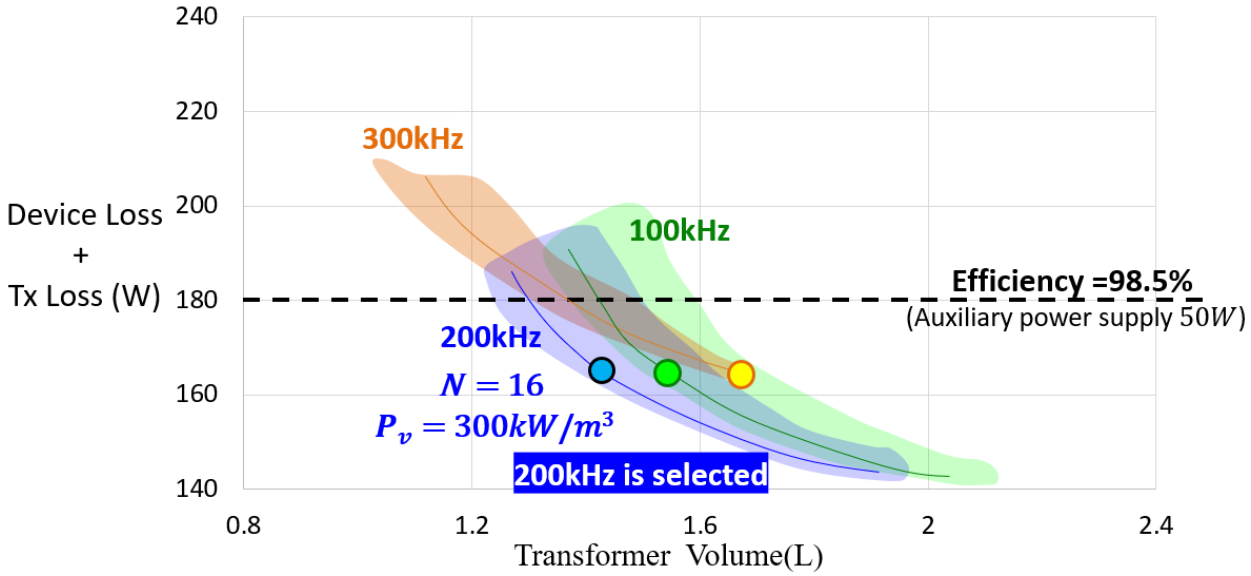


Fig. 25 Transformer loss and size trade-off at different frequencies

Transformer design result

To determine the design point, the transformer loss and device loss are added together to get the total loss of the DC/DC converter, as shown in Fig. 25. The design point is picked according to total loss and transformer volume tradeoff.

To achieve a total efficiency of 98.5% and considering that the loss of auxiliary power supply is around 50W, the maximum total loss shall be less than 180W. If we further

increase the transformer volume, the total loss will drop. But the benefit on loss becomes very limited while the transformer volume increases significantly. Thus, the design point is selected to be $P_{Tr} = 80W$ and $V_{Tr} = 1.37L$. Table III shows the result of this transformer design.

Table III. Transformer design result

Design Parameter		**Values**
Switching frequency (fs)		200kHz
Device Loss		100W
Core material		MLx6
Core Loss Density		300 kW/m3
Magnetic Flux Density		153mT
Litz wire	**AWG**	42
	Strands Number	525
Number of Turn	**N1**	16
	N2	22
Tx	**Winding Loss**	36W
	Core Loss	44W
	Total Loss	80W
	Total Volume	1.37L
Magnetizing Inductance (Lm)		100uH

Manufacturing Process and Special Consideration For The Insulation Encapsulation

Besides the insulation structure design, the manufacturing for the insulation is also essential to creating an PD-free winding encapsulation. Different from the line frequency bulky transformer, the HFT has a much smaller volume. It is hard to use commercially available manufacturing process to make the insulation due to volume restrict. Many researchers

provide manufacturing process solution which are complicated. A relatively simple method is purposed in this chapter to create a PD-free insulation encapsulation.

A 3D-printed bobbin is used as the fixture to leave enough insulation thickness between the primary side winding and the zero potential grounded shielding. After wind the winding on the bobbin, the winding and bobbin are placed in another 3D-printed mold to create a sealed winding encapsulation. Insulation

material Wacker SilGel 612 is filled up the winding unit from two terminals of the transformer. To create a partial discharge free transformer, vacuum pressure impregnation (VPI) process is applied. The winding unit with insulation material is placed in a vacuum chamber, as shown in Fig. 26. The air bubble in the insulation material will be squeezed out with the pressure gradually down to 50mbar in the vacuum chamber. If the pressure is too low in the vacuum chamber, the air bubble in the insulation material escapes fast and flows out from the winding unit. Also, a small vibrating table is placed in the chamber to vibrate the winding unit in order to eliminate air cavity inside the winding unit to achieve partial discharge free. The vacuum chamber is heated to 60 °C in half an hour. Which makes the air bubble easy to escape from the winding units with relatively high temperature. After the air cavity is removed, the winding unit is cured for 1 hours at 60 °C. Semi-conductive shielding layer is sprayed on the surface of the winding encapsulation with desired thickness except termination sleeves. Finally, the stress grading tape should be coated on the surface of the termination sleeves with minimized air cavities. The assembled transformer is shown in Fig. 27.

Hardware Prototype and Experimental Evaluation

The transformer prototype is shown in Fig. 27. The secondary side winding is inside the white bobbin on the top. The primary side winding and the insulation silicone gel is covered by the black shielding. A copper tape is used to ground the shielding layer and the core. Thanks to the grounded shielding (in Black), there is no space between the primary side winding and the secondary side winding. The space between winding can core is also minimized. In this case, the space utilization is as much as possible and the volume can be shrunk from insulation point of view. The other black parts on the termination sleeve is the stress grading tape.

Fig. 26 Vacuum chamber for VPI

The applied voltage test as the overvoltage test is conducted based on IEEE C57.12.01. For the applied voltage test, the secondary side winding, shielding, and the core are all grounded. The primary high voltage winding is firstly shorted and then gradually applied 34 kV RMS line frequency medium voltage. The test setup is shown in Fig. 28. The voltage level is kept at 34kV RMS for 60 second in the test. During the test, there is no voltage breakdown in the HFT. The transformer prototype can pass such test.

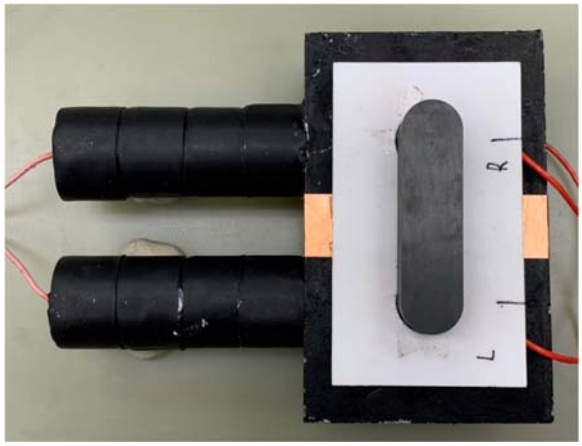


Fig. 27 Transformer prototype for the 15kW CLLC with 13.2kV input level

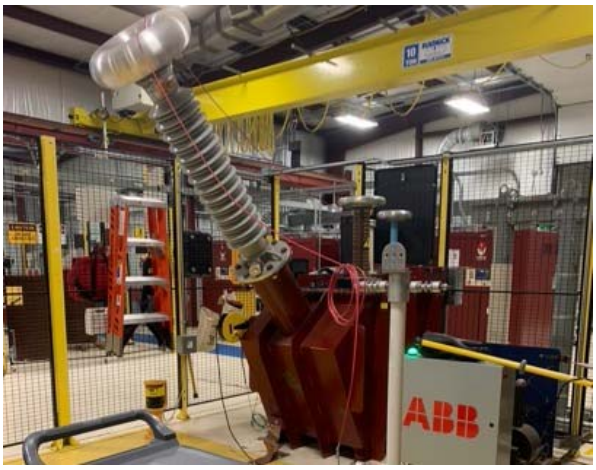


Fig. 28 Line frequency transformer for 34kV applied voltage test

The partial discharge test is done to verify the partial discharge level for the HFT. The partial discharge test setup is shown in Fig. 29 and the equivalent circuit is shown in Fig. 30. In the partial discharge test, the different between transformer with different Litz wire types is shown in Fig. 31 and Fig. 32. The test result for the transformer with FEP jacket is shown in Fig. 31. The partial discharge inception voltage occurs at 11.4kV peak (8.2kV RMS). However, using silk coating Litz wire instead of FEP jacket can lift the partial discharge inception voltage to 29.6kV peak (20.8kV RMS) under same manufacturing condition. The experimental result indicates that the silk coating Litz wire is more suitable for such medium voltage high frequency applications. Based on the standard, the partial discharge level at 17.2kV RMS ($1.3V_o$) after 210 second is less than 10pC. The HFT can pass the partial discharge test.

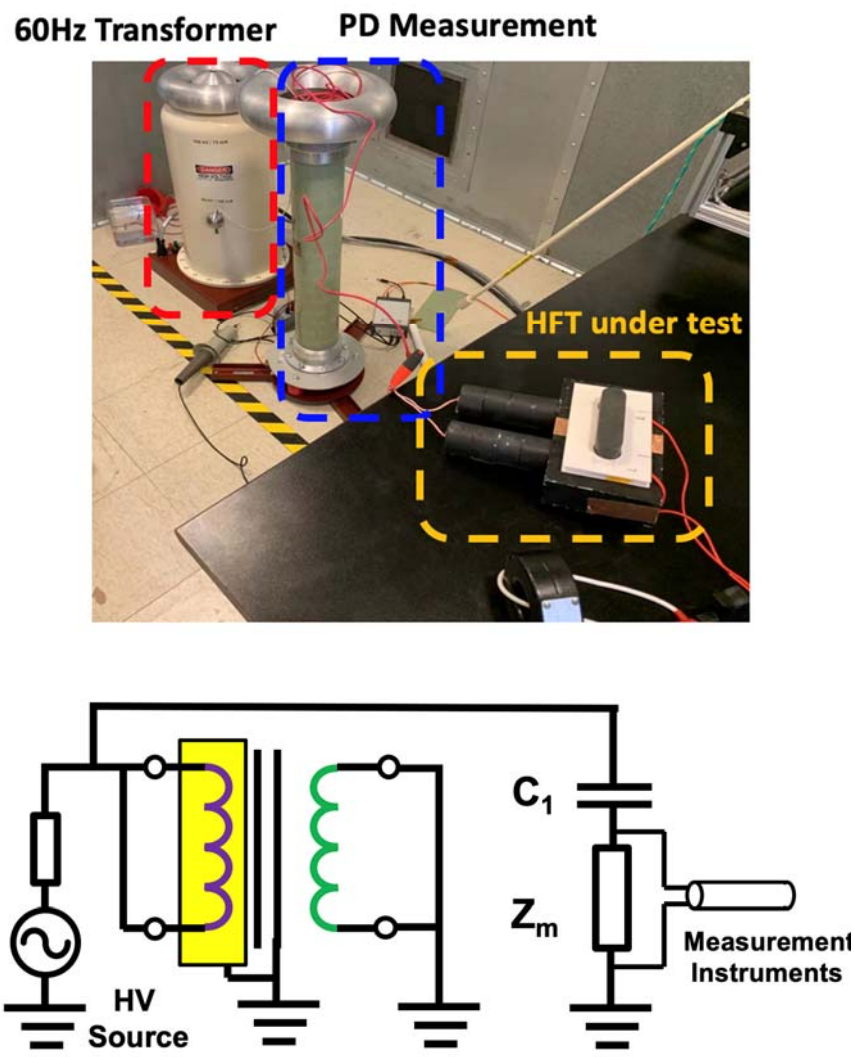


Fig. 30 Equivalent circuit for partial discharge test

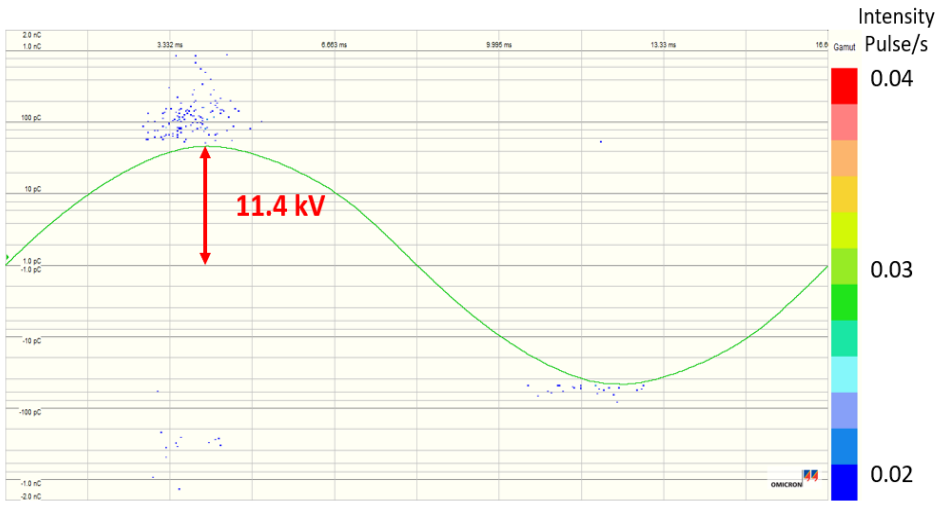


Fig. 31 Partial discharge test result for transformer with Litz wire with FEP jacket

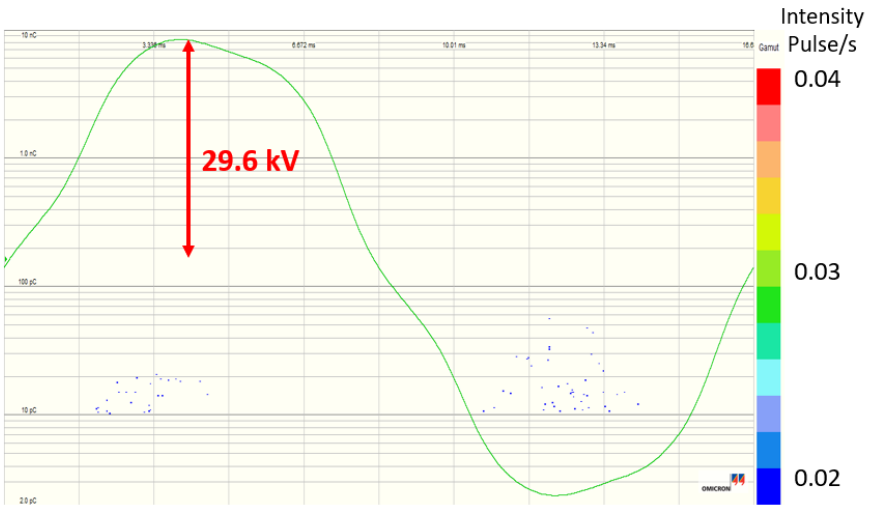


Fig. 32 Partial discharge test result for transformer with Litz wire with silk coating

High frequency high voltage three-level resonant converter with SiC MOSFET

High frequency driving circuit with high dv/dt immunity

One of the most challenging aspect of the gate driving circuit design for SiC device is its ability to deal with the noise issue related to high dv/dt due to the ultra-fast switching capability of SiC devices. The noise path will be identified and special technique will be used to minimize noise amplitude. The gate drive solution for SiC device will achieve high dv/dt

immunity, high driving capability, and small propagation delay. The device we will use is FF23MR12W1M1_B11 for the primary side and C3M0030090K for the secondary side. (See details in the last section about device selection.)

1EDI20H12AH Driver

The 1EDI20H12AH is a 1200-V galvanically isolated single-channel wide body gate driver with a small footprint for quick design-in cycles. It can deliver ± 2.0 A output current for high speed devices, like the FF23MR12W1M1_B11.

The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its wide input voltage supply range supports the direct connection of various signal sources like DSPs and microcontrollers. The separated rail-to-rail driver outputs simplify gate resistor selection, save an external high current bypass diode and enhance dv/dt control. Based on Infineon's coreless transformer technology, the driver enables a benchmark-setting minimum common mode transient immunity (CMIT) of 100kV/us

Switching performance evaluation for SiC MOSFETs

Device loss evaluation and device selection

Since that in CLLC resonant converters, we can always achieve ZVS turn on for both primary and secondary sides, and ZCS turn off for secondary side, the total device loss will be the sum of conduction loss and driving loss on both sides, and turn-off loss on primary side, as shown below:

$$P_{total} = P_{conduction} + P_{driving} + P_{turnoff}$$

$$P_{conduction} = 4 \times (I_{dev\_pri}^2 \times R_{dson\_pri} + I_{dev\_sec}^2 \times R_{dson\_\mathrm{sec}})$$

$$P_{driving} = 4 \times f_{sw} \times (Q_{g\_pri} \times V_{gs\_pri} + Q_{g\_sec} \times V_{gs\_sec})$$

$$P_{turnoff} = 4 \times f_{sw} \times E_{off(eq)}$$

where,

I_{dev} is the RMS value of the current through a device;

R_{dson} is the Drain-source on resistance;

f_{sw} is the switching frequency;

Q_g is the total gate charge of a device;

V_{gs} is Gate-source voltage of a device;

$E_{off(eq)}$ is the compensated turn off energy of a device;

pri and sec stands for the primary side and secondary side respectively.

Assume that:

1) i_{Lr} is a sinusoidal waveform
2) i_{Lm} has a constant value during the dead-time t_d and has a constant slew rate in other time.

With the assumptions above, we can get the I_{dev_pri} and I_{dev_sec} as shown below:

$$I_{dev\_pri} = \frac{V_o}{8nR_L}\sqrt{\frac{n^4R_L^2T_s^2}{L_m^2} + 4\pi^2 + \frac{16\pi^2(T_0t_d + t_d^2)}{T_0^2}}$$

$$I_{dev\_sec} = \frac{\sqrt{3}V_o}{12\sqrt{2}\pi R_L}\sqrt{\frac{(5\pi^2 - 48)n^4R_L^2T_o^3}{L_m^2(T_0 + 2t_d)} + \frac{12\pi^4T_0}{T_0 + 2t_d} + \frac{48\pi^2(T_0t_d + t_d^2)}{T_0(T_0 + 2t_d)}}$$

$$i_{Lm\_max} = \frac{nV_oT_s}{4L_m}$$

Then, the total loss is a function of td. For a given switching frequency, if td is too large, conduction time will decrease, leading to a higher conduction current and so is the conduction loss. If td is too small, then there will be large circulating energy, which also reduces the whole efficiency. So, we can minimize the total loss by choosing an appropriate t_d.

For the secondary side device, there is no switching loss. So, we will choose the device with the minimum R_{dson} value. Based on our most recent survey, we choose *C2M0045170D* from CREE. For the primary side, Table IV shows the three primary side device candidates and secondary side device selection according to our most recent survey:

Table IV: A Specification Three Level Resonant Converter

	Part No.	Vds(V)	Rdson (@100oC)	Qg (nC)	Coss(pF)
Primary	C3M0075120K	1200	86 m ohm	51	58
	FF23MR12W1M1_B11	1200	30 m ohm	124	220
	IMZ120R045M1	1200	55 m ohm	62	115
Secondary	C2M0045170D	1700	80 m ohm	188	171

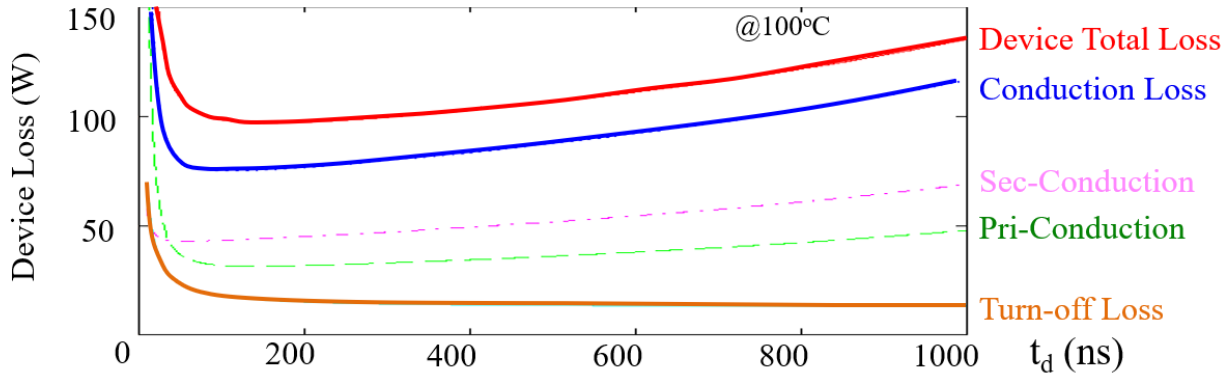


Fig. 33 Device losses versus deadtime

At fs=200kHz, device loss is calculated versus deadtime t_d. The result is shown in Fig. 33 and Fig. 34. We can see that conduction losses dominate. Thus, we also pick the lowest R_{dson} device for the primary side. Loss breakdown is as shown below in Fig. 34.

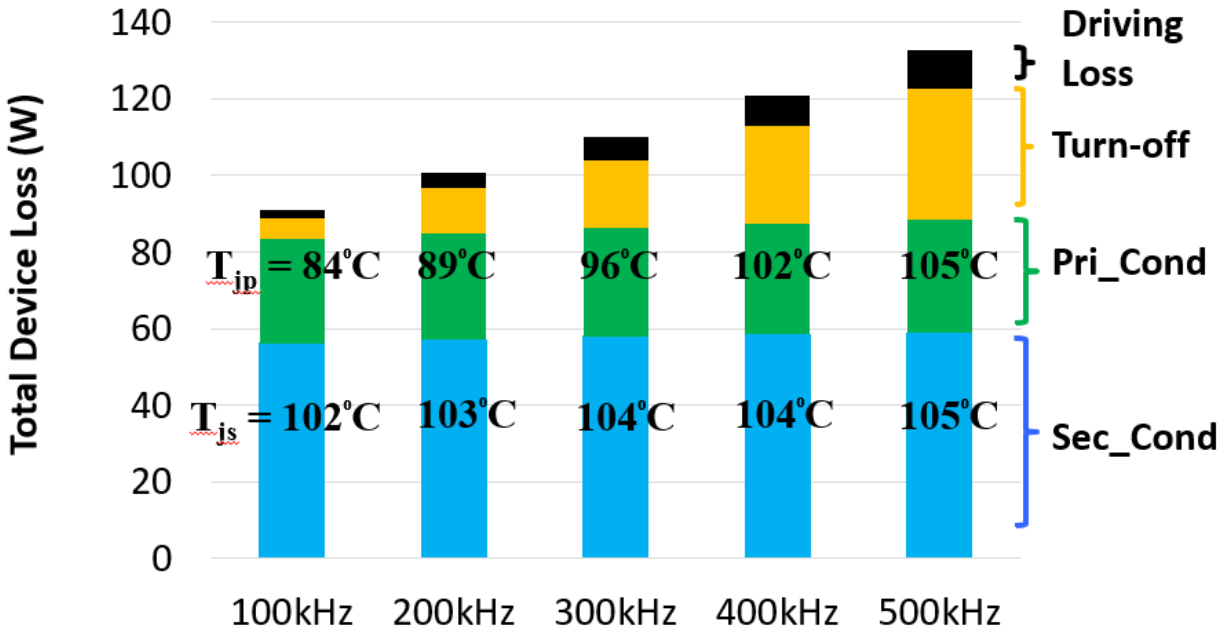


Fig. 34 Device loss distribution at different switching frequency

Considering the auxiliary power supply loss of 45W and transformer loss of 80W, a total efficiency of 98.5% can be reached. Also, device temperature is estimated based on selected thermal sink.

G1 prototype development for high voltage three-level resonant converter

The Three Level Resonant Converter Design

At this moment, each part of this Three level resonant converter has been designed. Devices for both primary side and secondary side are selected based on device loss evaluation. Magnetizing inductance L_m and deadtime t_d are selected based on the requirement of zero voltage switching (ZVS). Transformer core material candidates are evaluated using the specialized core-loss measurement techniques developed at CPES and the core material is selected based on the switching frequency. Litz wire is also selected based on the switching frequency. Considering the insulation requirement, the insulation materials and winding structures are evaluated and selected to minimize the transformer volume. The

transformer loss is then calculated using the magnetic core loss model and litz wire winding loss model developed in CPES. Finally, all the transformer design parameters, such as number of turns, core loss density, and switching frequency are optimized based on the trade-off between the volume and converter total loss, as well as winding loss and core loss. The design result is summarized below as shown in Table V.

Table V: Three Level Resonant Converter Design Result

Item	Spec.
Pri-side SiC MOSFET	FF23MR12W1M1
Sec-side SiC MOSFET	C2M0045170D
Insulation material	SYGARD 3-6605
Core material	ML27D
Litz wire	TXXL525/42T2XX-2
Number of turns ($N_1 : N_2$)	16:22
Switching frequency	200 kHz

A. The Three Level Resonant Converter Prototype Development

In circuit design stage, RECOM R24P series DC/DC brick type converter are selected as auxiliary power supplies for gate drivers and control circuits. The PCB layout and a photo of the prototype are shown in the Fig. 35 below. The width of primary and secondary PCB is the same, 170mm (6.69”), and the length of primary and secondary PCBs are 182mm (7.16”) and 125mm (4.92”), respectively.

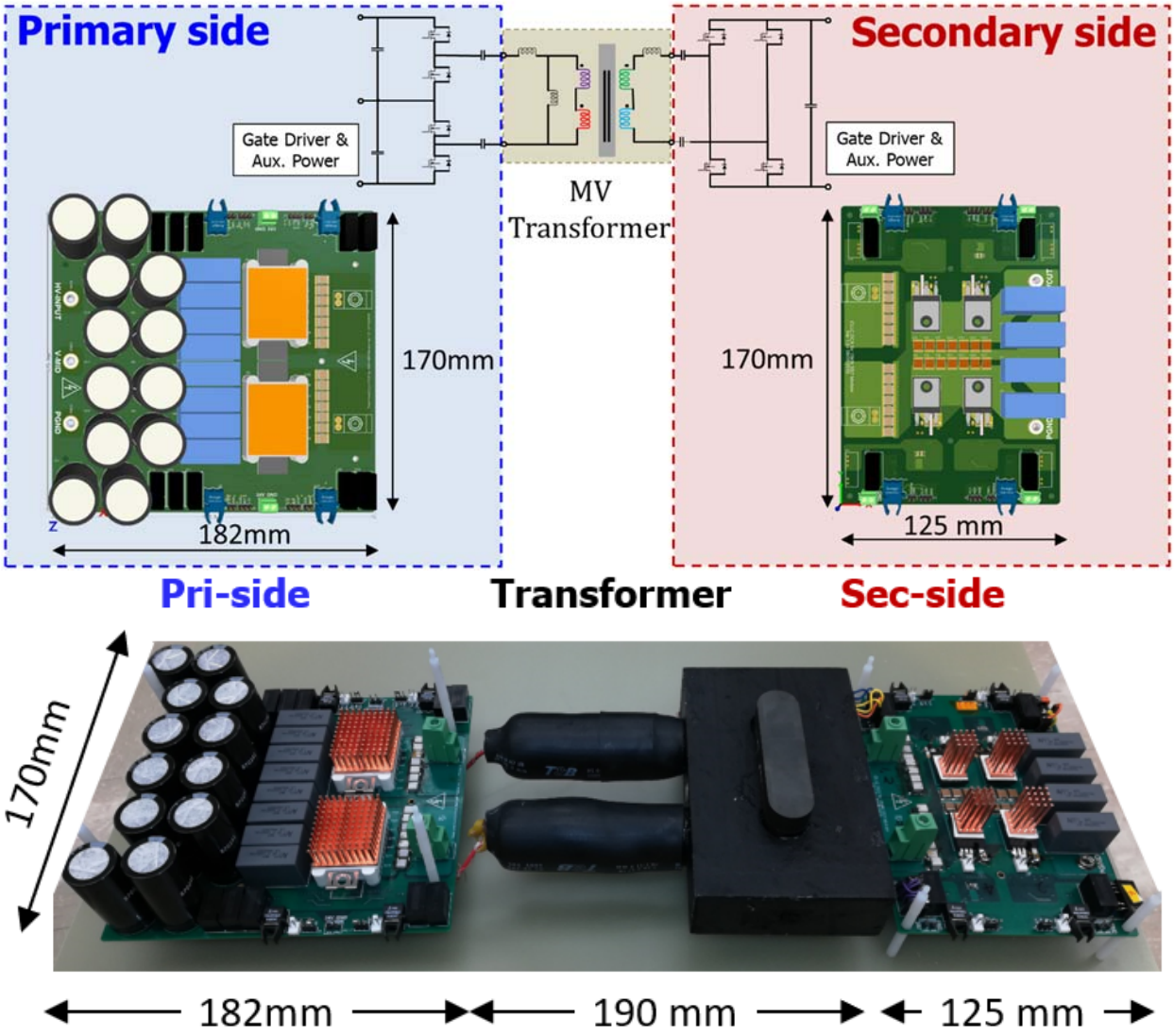


Fig. 35 Hardware layout and prototype

Test Results

The prototype circuit is tested under the conditions as designed. During the test, the converter input DC voltage is increased gradually. To achieve ZVS, the converter is operating at a switching frequency slightly lower than the resonant frequency. The working waveforms are shown in Fig. 36. Primary side can achieve zero voltage turn on (ZVS) and low current turn off. While the secondary side can achieve both ZVS and zero current turnoff (ZCS). Under full load condition, the efficiency is 98.6%. And the efficiency curve under different load conditions is plotted in Fig. 37.

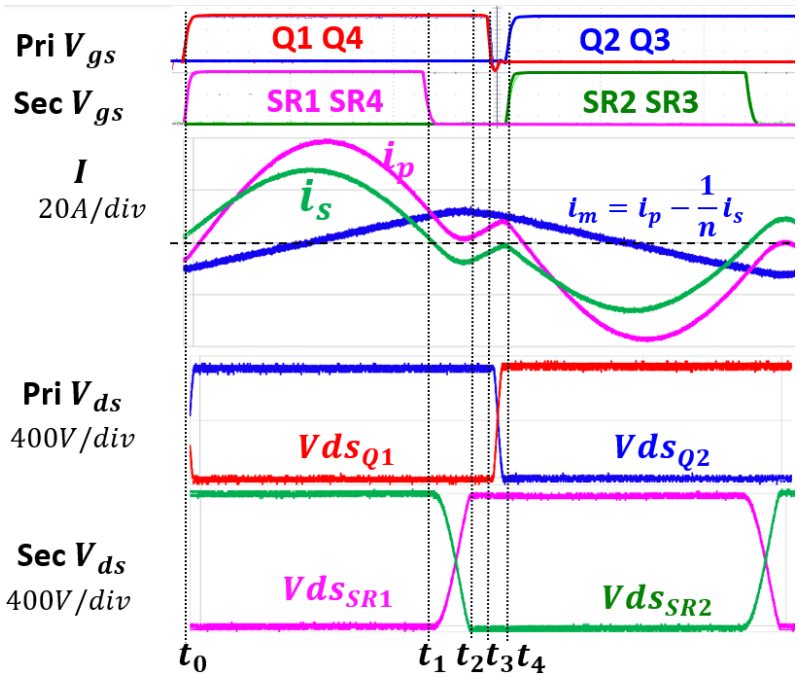


Fig. 36 Main working waveforms of G1 tests

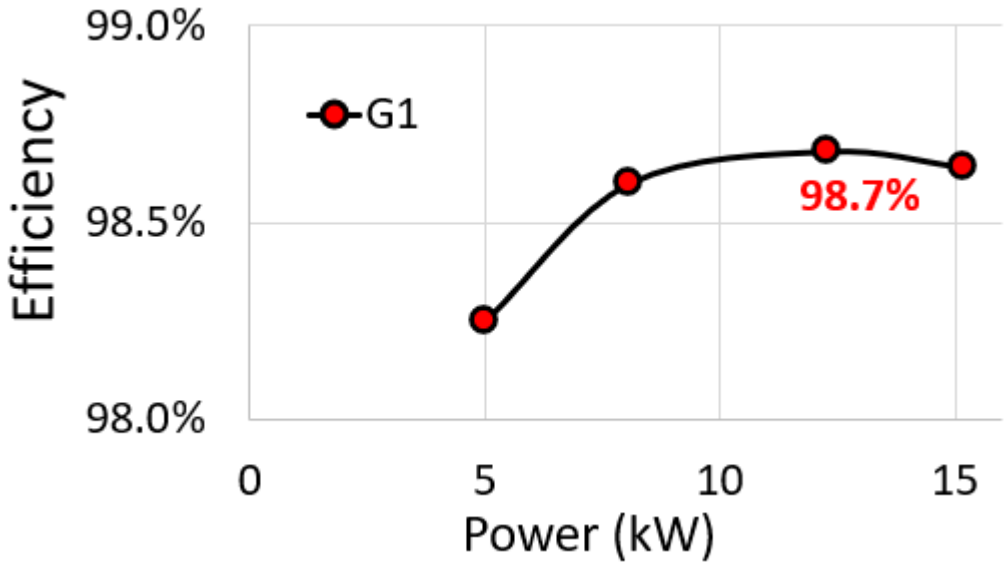


Fig. 37 Tested Efficiency

Further improvement of high frequency high voltage three-level resonant converter with SiC MOSFET

Design optimization for DC/DC stage

According to the G1 tested waveform, one minor issue is that the primary side has to wait until t_3 to turnoff to achieve ZVS. And the interval of $t_1 \sim t_3$ is determined by a high

frequency resonance, with leakage inductance, secondary side devices' junction caps, and parasitic caps on the PCB involved.

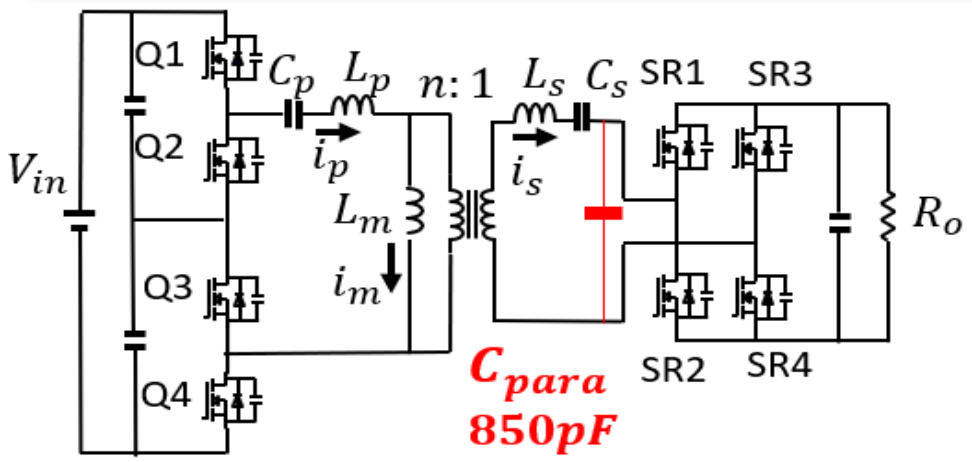


Fig. 38 Large parasitic capacitor in G1 secondary side PCB

On the secondary side PCB, there's too much overlap area between different copper layers of the main circuit. And this brings a huge parasitic capacitance (almost 850pF) between the two AC terminals on the secondary side, as shown in Fig. 38. This parasitic capacitance makes a huge impact on the waveform between t_1 and t_2 as shown in Fig. 36. During the commutation period, the parasitic cap is parallel to the junction caps on the secondary side and it will sink a lot of current from the primary side. Thus, if the primary side MOSFETs are turned off at the same time, the primary side current is not enough to discharge the junction cap on the primary side to realize ZVS. Then a time delay is applied to the primary side MOSFETs before the turn-off such that the primary side current is high enough to do ZVS. Since this parasitic capacitance is paralleled to the junction caps, it will also significantly increase the resonant period during the secondary side communication process. And due to no power is delivered during this t_1 to t_2 interval, the longer this interval is, the higher current RMS will be, and thus the higher conduction loss. In G2 design, to reduce the parasitic caps of PCB, the layout is improved to reduce the overlapped area of the power stages as shown in Fig. 39. And the parasitic cap is reduced from 850pF to 50pF.

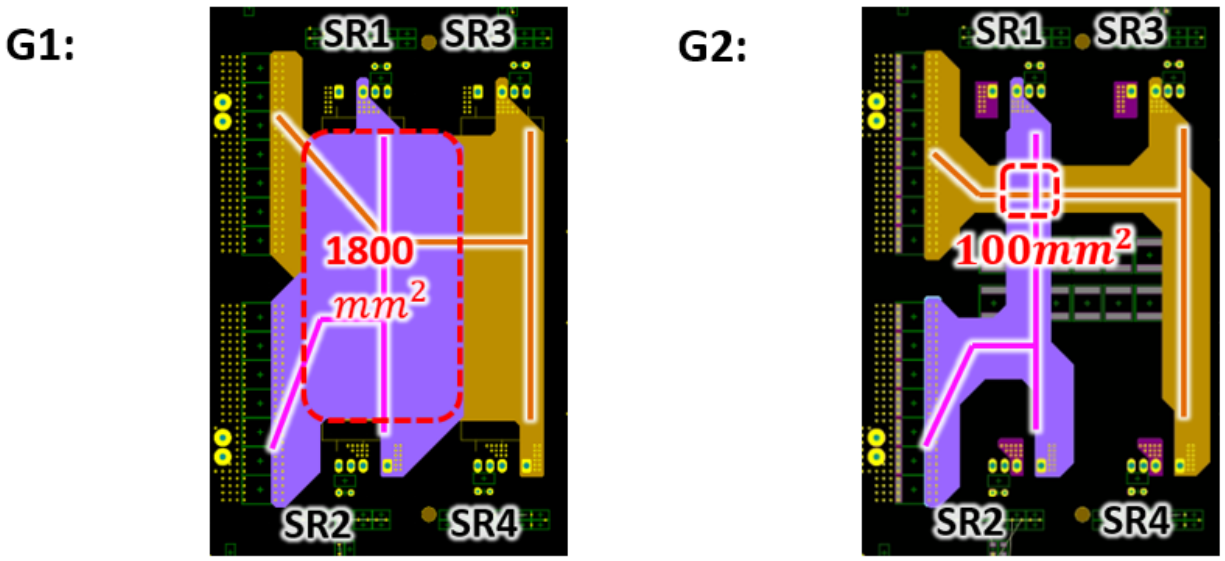


Fig. 39 PCB layout improvement

	G1	G2
Overlap area	$\mathbf{1800mm^2}$	$\mathbf{100mm^2}$
Parasitic cap	$\mathbf{850pF}$	$\mathbf{50pF}$
$I_{pri}(RMS)$	$\mathbf{26.7A}$	$\mathbf{21.9A}$
$I_{sec}(RMS)$	$\mathbf{18.6A}$	$\mathbf{15.3A}$

Demonstration of G2 Prototype

Test Result of G2 Prototype

In G1 prototype, the secondary side PCB has a large parasitic cap (850pF) due to too much overlap area of the power path between two layers. The layout is improved in the G2 prototype, and the parasitic capacitor is reduced to 50pF, which is negligible. Fig. 40 shows the waveform of G2 after improvement. Compared to Fig. 36, it can be observed that the primary side current drops slowly after t1. Now it's enough to realize ZVS for both primary side and secondary side MOSFETs at the same time. So, the switching frequency is determined by the resonant frequency and an adequate deadtime. In G2 prototype test, both the primary side and secondary side current are reduced compared to G1. And this reduction of RMS currents totally saves the conduction loss of 30W.

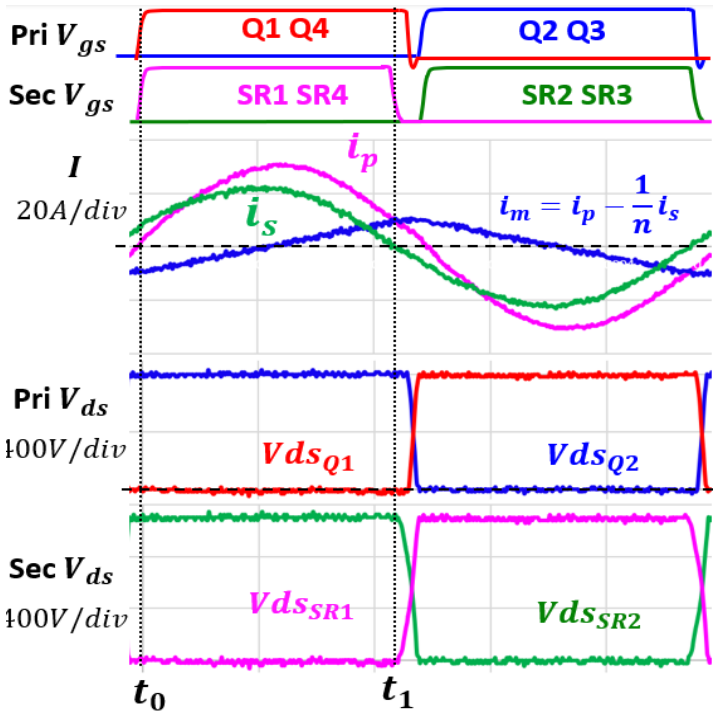


Fig. 40 Main working waveforms of G2 tests

Fig. 41 shows measured efficiency curves at different load conditions. The peak efficiency of the 15kW DC-DC converter is increased from 98.7% in G1 tests to 98.9% in G2 tests.

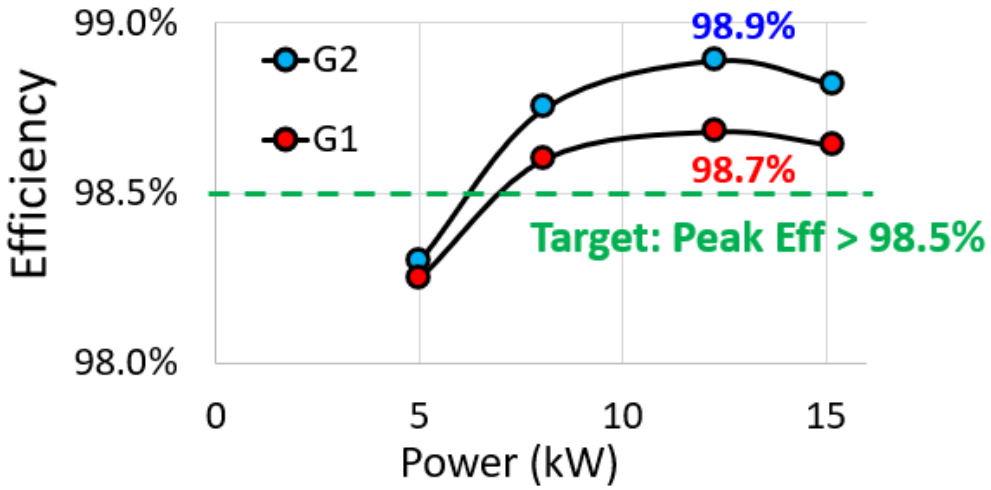


Fig. 41 Measured Efficiency of G1 and G2

System level control development for both AC/DC and DC/DC stages

High-Frequency Simplified Optimal Trajectory Control development for high voltage resonant converter-based DC/DC stage

Start-up Process Consideration

The resonant converter is very difficult to control due to the dynamics of the resonant tank. Conventional frequency control cannot achieve good transient performance, and there is very large dynamic oscillation during the transient, which may damage the converter due to the large current and voltage stresses. For the Solid-State Transformer in EV charger application, there are three stages, AC/DC stage, DC/DC stage, and following Buck converter stage as shown in Fig. 42. Take one phase system as the example. The start-up process should be charging the AC/DC stage first. And when the output capacitor of the AC/DC stage is fully charged, DC/DC stage will start to be charged until rated voltage (e.g. 1.1kV). Finally, Buck converter will start up from 0V.

At this moment, CPES develops a high-frequency simplified optimal trajectory control for the proposed CLLC converter for DC/DC stage to precisely control the state trajectory of the resonant tank components at start-up condition. The short circuit protection the inverse process of start-up. For AC/DC start-up and short circuit protection, CPES will develops in the future.

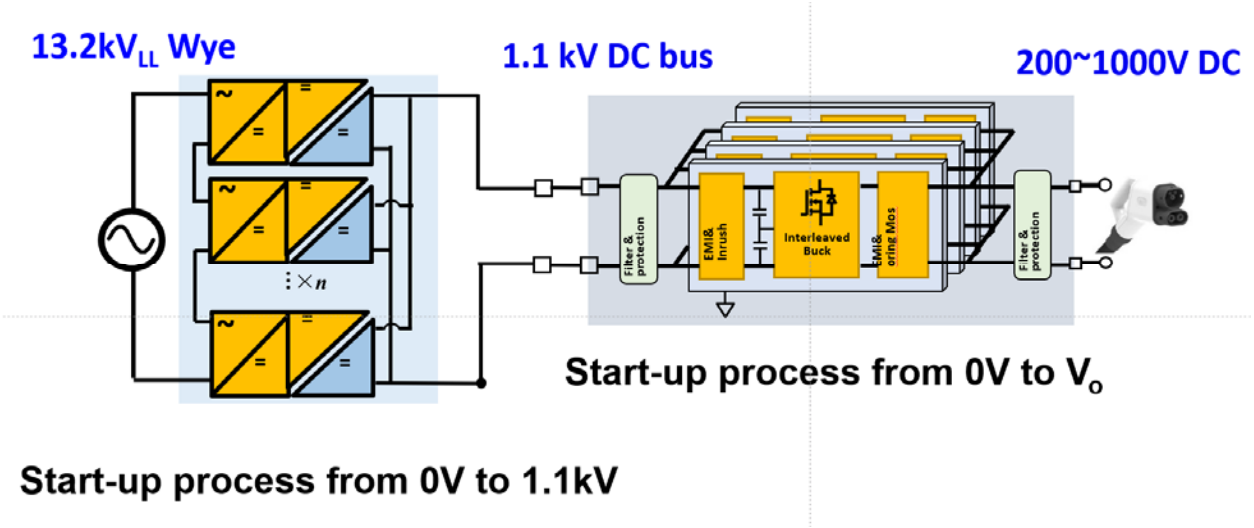


Fig. 42. System schematic and start-up consideration

Review of Previous SOTC Achievements in CPES

Two version of SOTC is proposed in previous CPES achievements. The basic idea of the soft start-up process for the LLC resonant converter is to investigate and optimize based on a graphical state-trajectory analysis. By setting a current limitation band, several optimal switching patterns are proposed to settle the initial condition. After that, by sensing the output voltage, the optimal switching frequency is determined within the current limiting band. This virtually guarantees that there will be no current and voltage stress in the resonant tank during the soft start-up process and

over-load protection. Meanwhile, the output voltage is built up quickly and smoothly. When it comes to the over-load protection, it is a reverse operation of the soft start-up. By applying the similar switching pattern, the resonant current and voltage stress is limited under the over-load condition.

In the version I design, the whole startup process is divided into three stages, as illustrated in Fig. 43. Stage 1 sets an asymmetrical current-limiting band, $+I_{maxN}$ and $-I_{LmN}$ (the suffix N means normalized), to settle V_{Cr} to half of input voltage V_{in} (for 3 level CLLC configuration). Stage 2 sets a symmetrical current-limiting band, $+I_{maxN}$ and $-I_{maxN}$, to optimize the energy delivery. Stage 3 decreases f_s gradually until V_o reaches steady state, which is 12 V in this case.

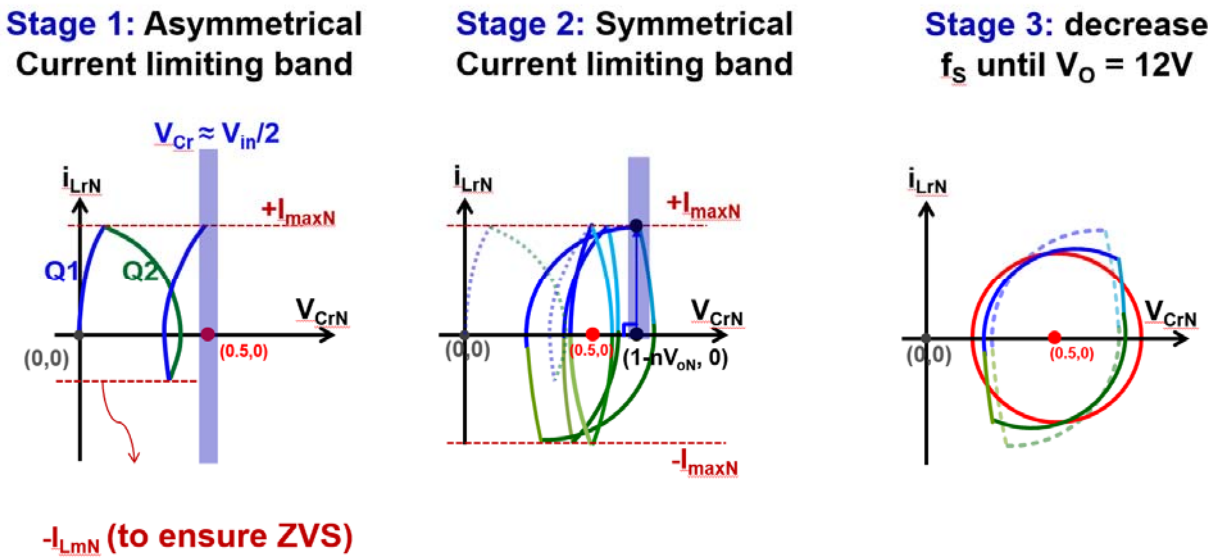


Fig. 43. OTC control process in version I

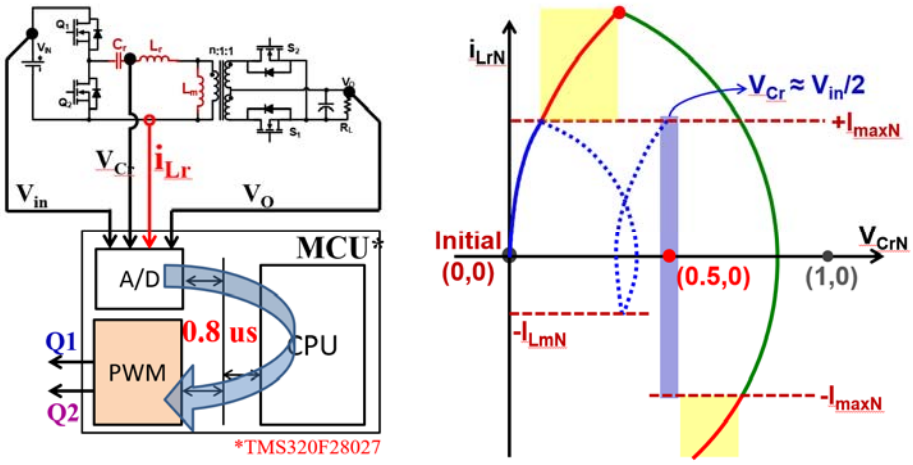


Fig. 44. Issue for OTC control with MCU Implantation

However, All the required state variables are sensed through the analog-to-digital converter (ADC) and processed by the CPU, as shown in Fig. 44(a). If the MCU senses i_{Lr} and compares it with I_{maxN}, there would be a digital delay of at least 0.8 μs. The impact of this 0.8 μs digital delay will cause very large i_{Lr} stress in Stage 1 as shown in Fig. 44(b), where the dashed line represents the desired trajectory and the solid line represents the actual trajectory with digital delay. Since the initial f_s for start-up should be very high, even a very small digital delay will cause a large i_{Lr} stress. Specifically, the 0.8 μs digital delay will cause twice as large as the full-load current stress for a 200-kHz LLC converter and more than three times the full-load current stress for a 500-kHz LLC converter.

To solve this issue caused by digital delay in ADC and calculation, MCU-based implementation with lookup tables is proposed, which only requires sensing V_o. In Stage 1, V_o is considered to be approximately 0 V because the output capacitor is very large and there are only a few switching pulses in Stage 1. The initial condition is: $V_{Cr} = 0$ and $i_L r = 0$ because there is no energy in the resonant tank before start-up. The trajectories to calculate ΔT1 and ΔT2 are shown in Fig. 45 And ΔT1 and ΔT2 are calculated based on the angle. The values for ΔT1 , ΔT2 … ΔTn are calculated step by step until it comes to the step at which V_{Cr} comes into the region around V_{in} /2, which is the last switching action in Stage 1.

In Stage 2, f_s can be determined based on the precalculated f_s versus V_o table. This is because for a given V_{in} and V_o, f_s can be determined based on the i_{Lr} stress requirements when operating at above f_o . During start-up, V_{in} and V_o can be considered to be constant within several switching cycles because there is a large input capacitor for the hold-up time and a large output capacitor for the load transient. Under these conditions, the corresponding f_s can be obtained for different values of V_o to guarantee i_{Lr} is within I_{max} under the nominal input voltage V_{in} nom based on the corresponding trajectory shown in Fig. 45. The switching period is then calculated based on the angle to derive the f_s versus V_o table for Stage 2, which then linearized piece-wise and stored in the MCU. Stage 3 for this method is the same as that of the OTC for soft start-up, just decreasing f_s gradually until $V_o = 12\,V$ and then merging with closed-loop control.

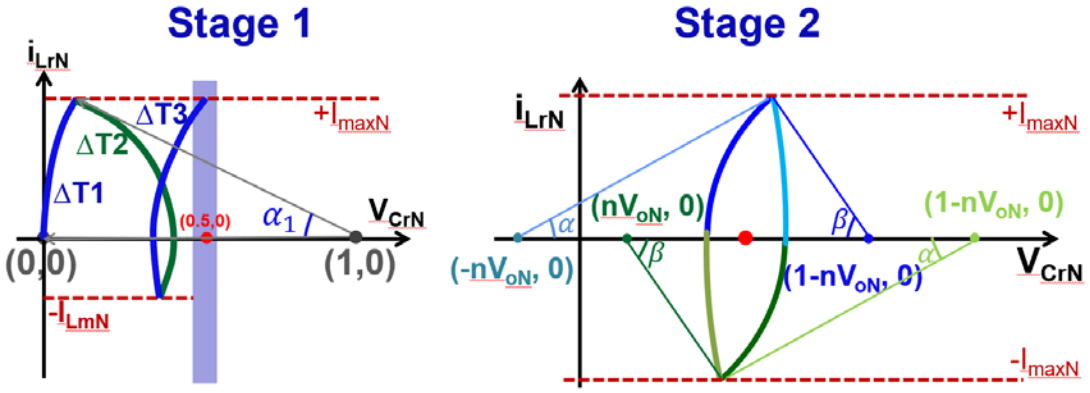


Fig. 45. Modified SOTC control to apply digital control

SOTC Control in CLLC Application

To utilize the SOTC control in the CLLC converter in SST application. The difference between LLC and CLLC should be considered. Compared with LLC, the CLLC has 4 resonant component and it is really hard to analysis CLLC performance. However, an approximation can be applied in CLLC to find an equivalent LLC circuit in the start-up process. As shown in Fig. 46, at stage 1, the output voltage is 0. Compared with L_m, the impedance of L_s and C_s is smaller. There is almost no impact from the I_m, which means we can consider L_p, L_s, C_p, and C_s in series. In this case, an equivalent LLC circuit can be proposed. From the trajectory point of view, the solid line are the CLLC trajectory and the dash line are the equivalent LLC trajectory. These two lines overlaps well, which means we can use the equivalent LLC trajectory to determine the turn on time of each devices. For stage 2, the equivalent LLC trajectory can be also utilized for the CLLC circuit with almost no error. For stage 3, the feedback control will be applied to deal with the error in the stage 2., exactly same as what we proposed in LLC applications, as shown in Fig. 47.

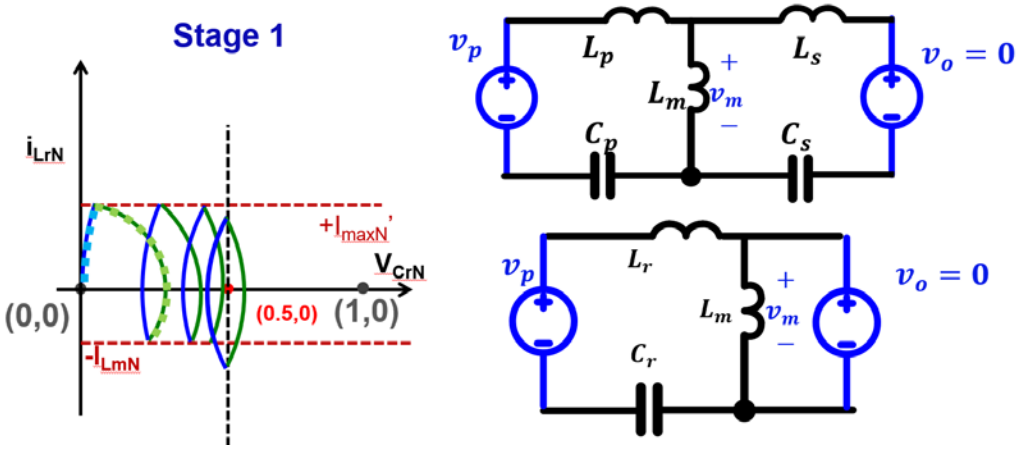


Fig. 46. Approximation in CLLC for start-up

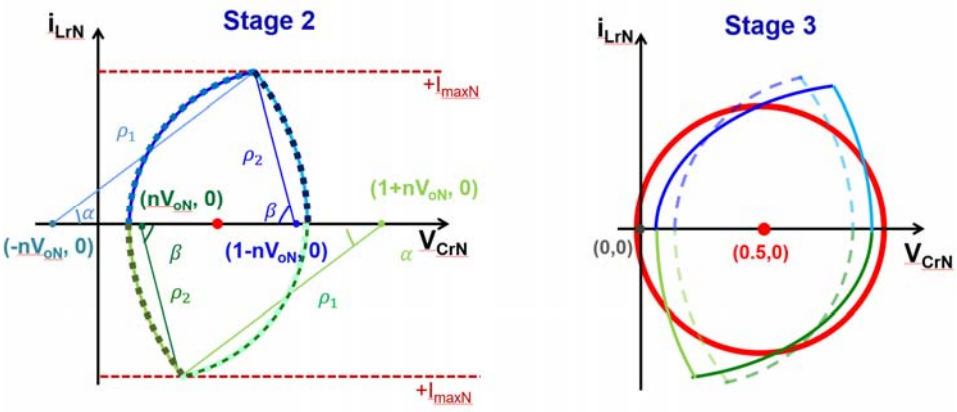


Fig. 47. Approximation trajectory for stage 2 in CLLC for start-up

Fig. 41 shows the simulation of the whole start-up process of the CLLC converter. As the figure indicates, the V_o increase from 0V to 1.1kV smoothly without overshoot in 1.3ms. The highest peak current stress on the inductance is around 40A and the highest capacitance voltage stress is 1.8kV.

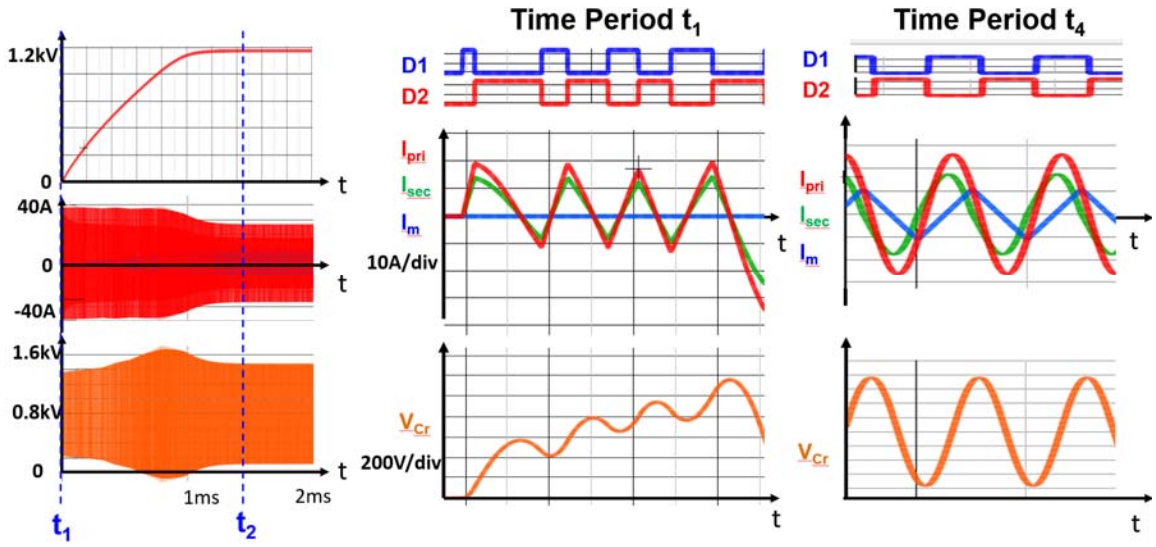


Fig.48. Simulation result for the CLLC converter

Cascaded multi-level rectifier control for AC/DC stage

Modulation Method Comparison

The modulation method is critical for the SST system, because such method determines the simulation complexity for the entire system. Consider the switching frequency difference, two modulation method are surveyed for comparison.

The first method is modules in each phase balance the voltage together. There are two voltage loops. The first one is to compare voltage information v_{cx} and the reference voltage $v_{c,ref}$ for each module, as shown in Fig. 49. The second voltage loop is to compare the previous signal with the voltage command v_m from PFC to achieve the voltage balance. Every module has its own switching performance based on this method. To regulate the voltage, the switching frequency is high and fast communication is required but the voltage is more accurate. So this method cannot handle too many modules.

The second method is to add some phase shift in the modulation systems as shown in Fig. 2. Compared with method 1, the voltage command from PFC will pre-modulation to divide into m part. The switch of different modules will operate at certain input voltages and then compare with voltage information v_{cx}. Due to phase shift, each module can have relatively

low switching frequency. Although the voltage cannot be controlled very accurate at each time period, the communication demand will not high and it can handle more modules compare with method 1.

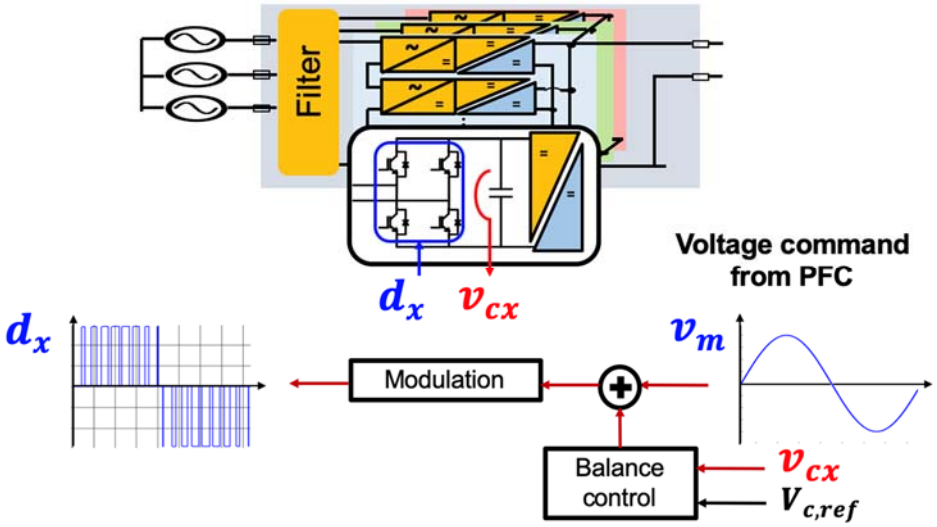


Fig. 49. Method 1: For high switching frequency with less modules

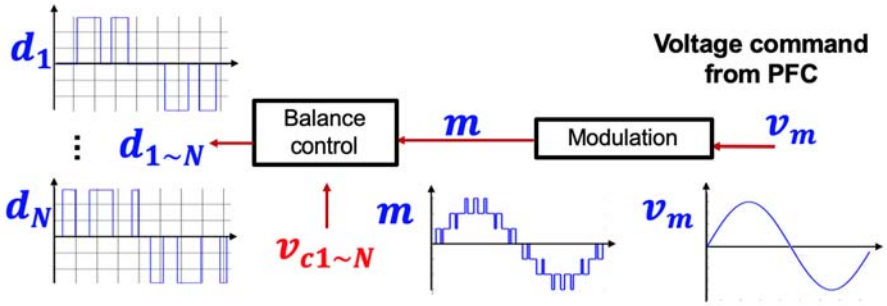


Fig. 50. Method 2: For low switching frequency with more modules

Simplified Cascaded H Bridge Simulation Model

For the Solid-State Transformer system level simulation, the most essential challenge is the simulation speed. The SST system is a three-phase system with 9 modules per phase. As we can see from Fig. 44, for one module, there are 7 energy storage components (2 bulk capacitors, 2 resonant capacitors, 2 resonant inductors, and 1 magnetizing inductance). It is a 7-order system for even one module. Such resonant behavior will dramatically slow down the simulation. Consider only one module per phase, this simulation will take 1 hour to finish 1 line cycle. For the entire SST system, there are 193 order. To finish the entire system simulation, the Simulink should continuously run over 24 hours. This time cost is too much to accept.

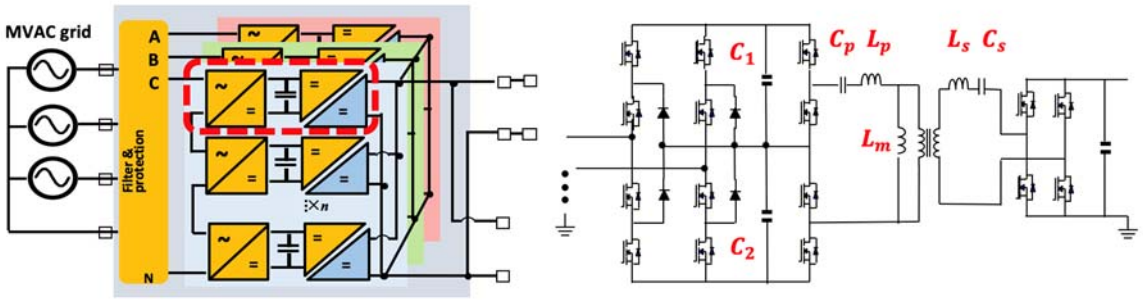


Fig.51. SST system architecture and the topology for 1 module

To make some improvement, we can regard the DC/DC stage as the constant power load, which can well regulate its output power. Based on such assumption, the CLLC converter can be regarded as a 3-order component instead of a 7-order component. The entire system order can be reduced from 193 to 57, as shown in Fig. 45. However, 57-order system is still a high order system. In addition, the constant power load is also a non-linear component. Its simulation speed is relatively low. Considering even more modules should be introduced to the system in the future to handle more power, this simulation system is not what we prefer. The research goal for the SST simulation is to further reduce the system order and to speed up the simulation progress.

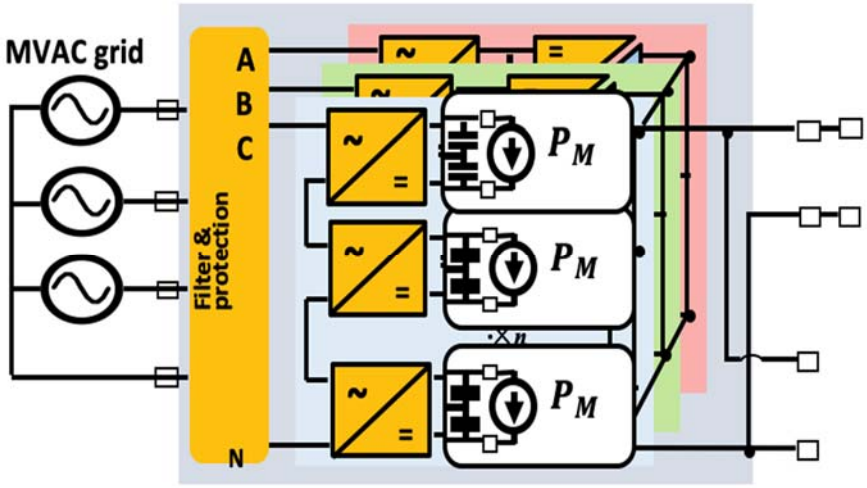


Fig. 52. SST system architecture with simplified DC/DC stage

To make some improvement, the priority is to find out which components affect the simulation speed most. In the simplified SST system architecture in Fig. 45, there are still 4 kinds of non-linear components, which are 3 input inductances, switches in each AC/DC modules, two bulk capacitors per module, and 1 constant power load per module. To speed up the simulation, all these non-linear components should be converted to linear components by some way. That is the motivation for this AC/DC simulation simplification research.

For the switches in the AC/DC module, in the simulation, we can regard these devices as ideal devices. In this case, devices only have three switching performances, forward turn on, turn off, and reverse turn on. These three states can be presented by duty cycle $d = 1, 0, -1$, as shown in Fig. 5. Under this assumption, we can simplify the real switch model into simplified switches. The switch network can be simplified to two voltage-controlled current sources. The AC/DC stage can be regarded as a linear system to reduce the simulation time.

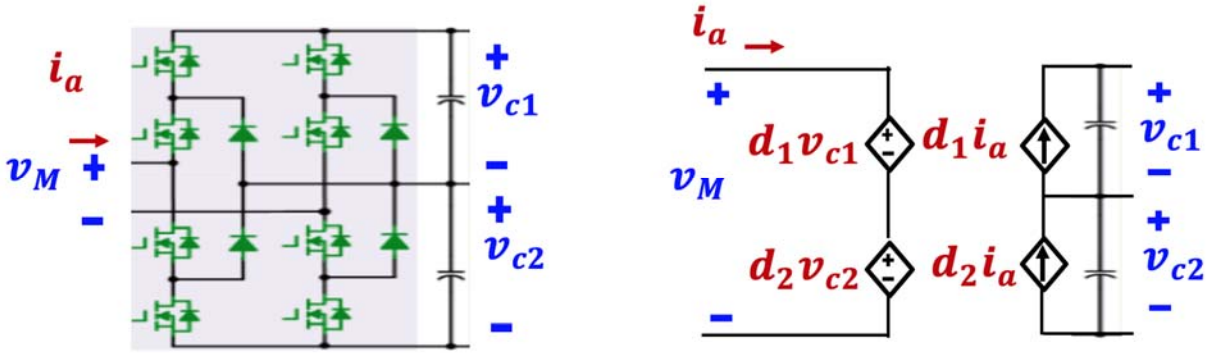


Fig 53. AC/DC stage real switching model and simplified switches model

For the capacitors and inductors simplification, the piecewise linear model is applied. The idea for the piecewise linear model is the capacitor current and voltage is almost linear at a very small Δt during the charging time for one capacitor, as shown in Fig. 47. If we know the initial state i_{c1} and v_{c1} at t_0, we can calculate the i_{c2} and v_{c2} at $t_0 + \Delta t$. From the capacitor charging definition,

$$v_{c2} = v_{c1} + \frac{1}{C}\int_{\Delta t} i_c dt$$

Assuming a very small Δt, the previous equation could be simplified as,

$$v_{c2} \approx v_{c1} + \frac{1}{C}\frac{i_{c1} + i_{c2}}{2}\Delta t$$

In this equation, i_{c1} and v_{c1} is known as initial state, i_{c2} information is known from previous AC/DC switching models. We can rewrite this equation into the following manner,

$$v_{c2} \approx V_{eq} + R_{eq} i_{c2}$$

where $V_{eq} = v_{c1} + R_{eq} i_{c1}$, and $R_{eq} = \frac{\Delta t}{2C}$. The non-linear capacitor can be represented by a voltage source and a resistor in series. So we can solve the v_{c2} information by a linear equation, whose simulation speed is much faster than simulating a capacitor. Same concept can also be applied to simulate input inductors.

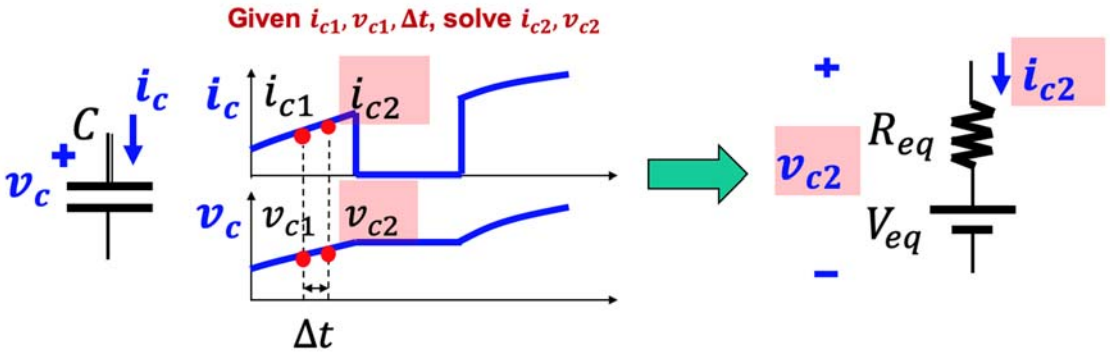


Fig. 54. Piecewise linear model of Capacitor

For constant power load, we can also apply piecewise linear method, as shown in Fig. 48. If we know the initial state i_{M1} and v_{M1} at t_0, we can calculate the i_{M2} and v_{M2} at $t_0 + \Delta t$. From the power definition with a very small Δt,

$$i_{M2} = \frac{P_M}{v_{M2}} = \frac{P_M}{v_{M1} + (v_{M2} - v_{M1})} \approx \frac{P_M}{v_{M1}}\left(1 - \frac{v_{M2} - v_{M1}}{v_{M1}}\right)$$

In this equation, i_{M1} and v_{M1} is known as initial state, v_{M2} information is known from the input voltage. We can also rewrite this equation into the following manner,

$$i_{M2} \approx I_{eq} - \frac{v_{M2}}{R_{eq}}$$

where $I_{eq} = 2P_M/v_{M1}$, and $R_{eq} = -\frac{v_{M1}^2}{P_M}$. The non-linear constant power load can be represented by a current source and a resistor in parallel. So we can solve the i_{M2} information by a linear equation, whose simulation speed is much faster than simulating a constant power load.

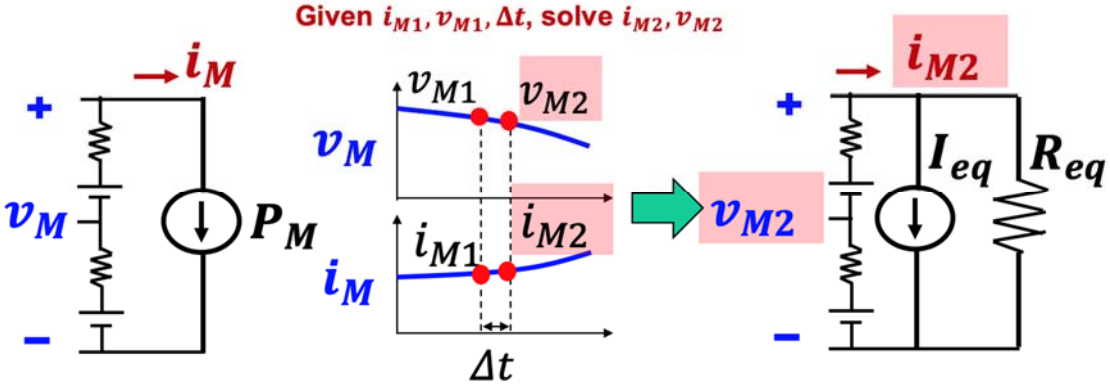


Fig. 55. Piecewise linear model of Constant Power Load

With all components are linear, the entire system becomes a 0-order system. We can run the simulation much faster than previous mentioned 193-order system. To further increase the simulation speed, MATLAB is utilized instead of Simulink. A simulation flow chart is shown in Fig. 49. In the simulation, the input is the voltage and current information at t_0. With the constant

power information, V_{eq}, I_{eq}, and R_{eq} can be calculated based on the piecewise linear model. Together with the feedback and balance control, the current and voltage information can be calculated at $t_0 + \Delta t$. Repeat the same process, the simulation can be done within 2 minutes, which much faster than Simulink simulation. The simulation results are also shown in Fig. 50.

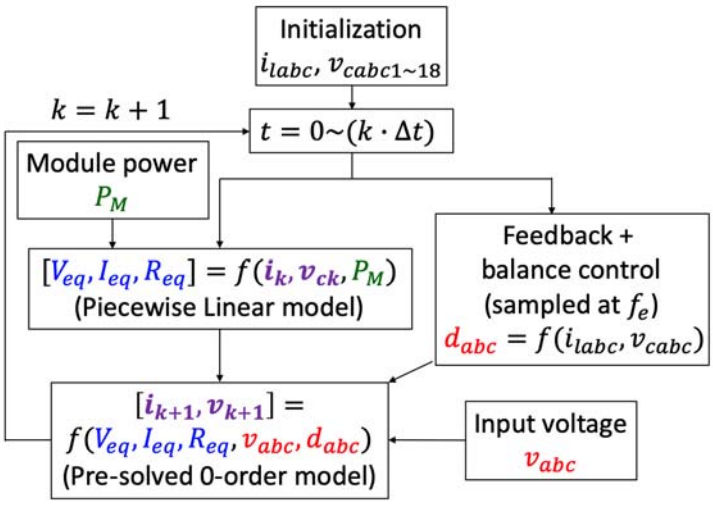


Fig.56. Simulation flow chart

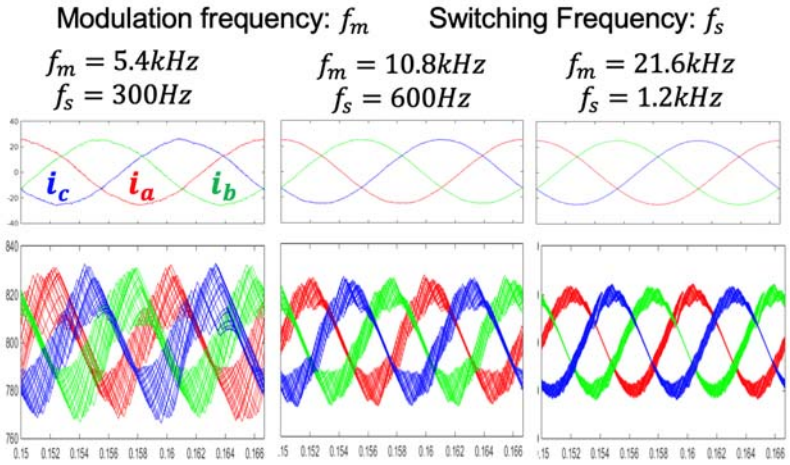


Fig. 57. simulation results

System level control simulation model development

Centralized or Distributed Control Method Comparison for Solid-State Transformer (SST) systems.

Due to medium-voltage requirement, the Cascaded-H-Bridge (CHB) circuit will be applied as the AC/DC rectifier as the first stage of the SST system. While the DC/DC stage, which provides the isolation, plays the role as the second stage. Because of and high-power and modularity, for one phase, multi-cell will be used to handle such high power. From control point of view, multi-cell topology will lead to issues of voltage balance and power balance

between different modules. This will be solved by control methods. If we consider the synchronization between each module, one controller would be the simplest solution. However, for such a huge system, the controller should be strong to process all the input signal and generate the output commands. In addition, due to the medium-voltage input, the signal transmission will be under high voltage insulation and high bandwidth which increases the cost. Considering these disadvantages, distributed control, which control signals generate from local controller to lessen the control burden of the strong central controller, is more and more popular at this moment.

Based on the SST architecture, the first stage is the CHB. We will use CHB as the starting point to compare advantages and disadvantages of centralized control and distributed control. For the centralized control of the CHB, the control schematic is shown as Fig. 51. The input line frequency voltage and current are sensed to the central controller. The bus voltage of each bridge cell is also sensed. Sensed signals are processed in the central controller. PWM signals are generated based on the voltage balance and power balance control and then transferred to each bridge cell. For the centralized control, only one strong controller is needed and no synchronization issue should be considered. The communication between each module are simple and easy to achieve. However, as we mentioned before, the central controller should be powerful enough. The sensing signal for bus voltage requires high voltage insulation and the PWM signal requires not only high voltage insulation but high bandwidth.

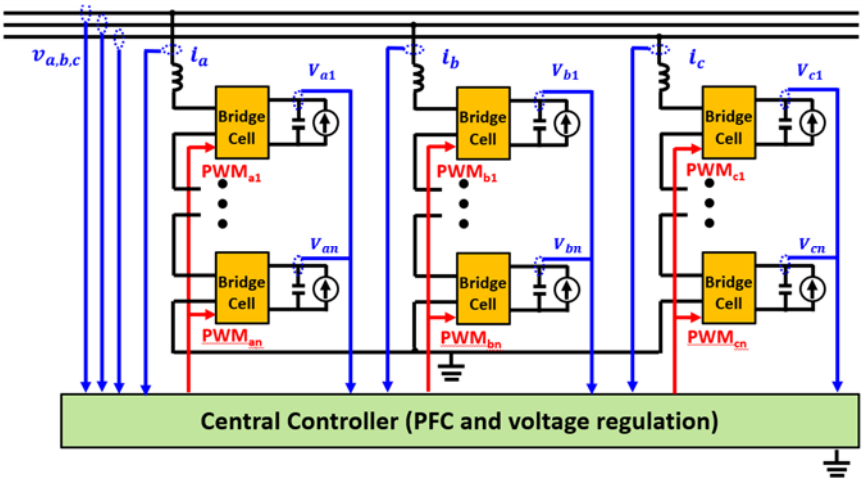


Fig. 58. centralized control method for CHB

For the distributed control for CHB, local controllers are required for each bridge cells, as shown in Fig. 52. The central controller is still required to sense the input line frequency voltage, current and the bus voltage. The average voltage control and PFC is achieved in the central controller and the control signal v_{c-a} is transferred to the local controller. In the local controller, the bus voltage will also be sensed and compared with reference voltage to achieve the voltage regulation for each module. The PWM signal, as the output of the local controller, control the power device of the converter. Compared with the central controller, no high frequency high bandwidth signal transfer in the distributed control loop. Only high bandwidth low voltage transmission and low bandwidth high voltage transmission are required.

Extend the CHB to the SST, DC/DC module as the second stage is added to the system, as shown in Fig. 53. The AC/DC stage control method is the same and the only difference occurs at DC/DC stage. The central controller plays a role for output voltage regulation in the DC/DC stage. The reference power signal generates from the central controller and convey to each local controller of the DC/DC stage. DC/DC controller senses input current and voltage information and generate PWM signal after processing. In this method, the primary side PWM signal is high-bandwidth low-voltage and the secondary side PWM signal is high-bandwidth high-voltage.

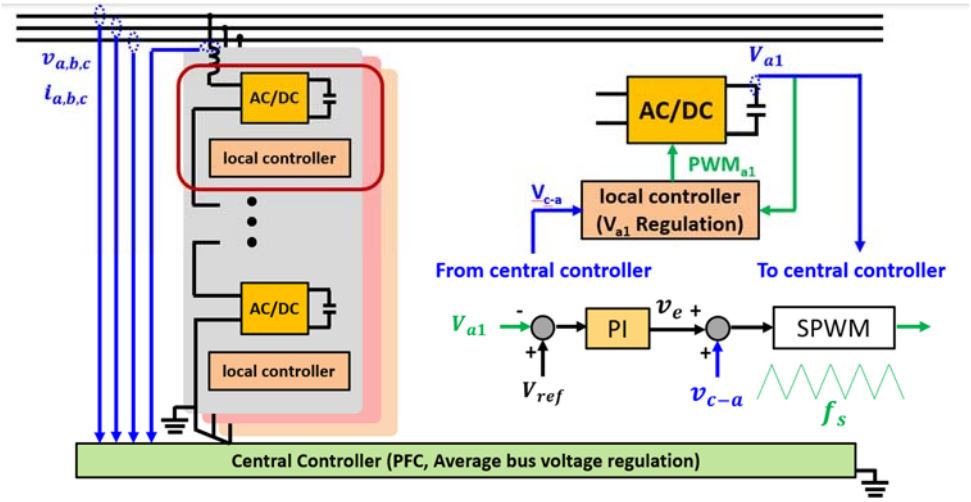


Fig. 59. CHB control with local voltage regulation

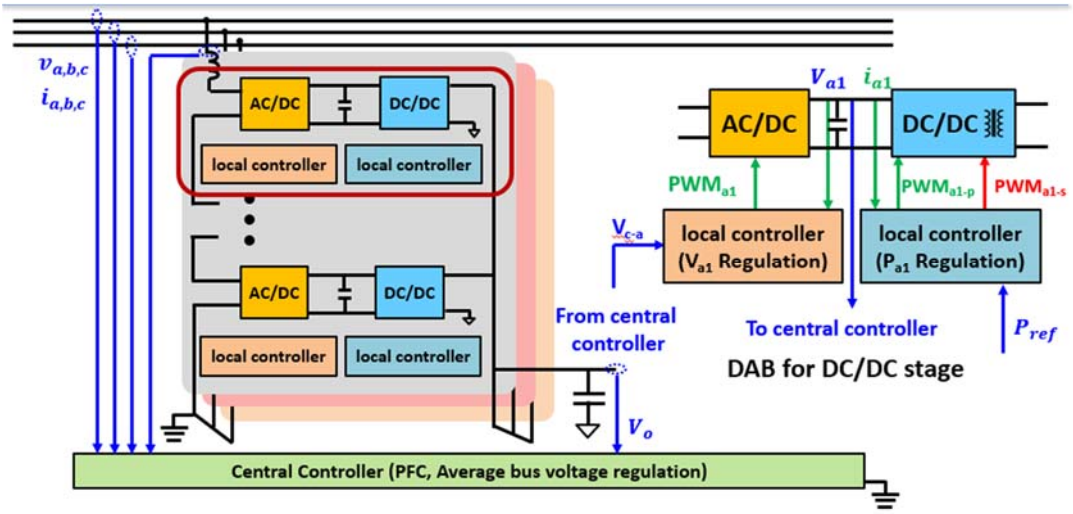


Fig. 60. SST control with local voltage and power regulation

In the aforementioned SST control method, lots of sensing is required. Another control method for the SST with less sensor is shown in Fig. 54. In this case, the DC/DC stage works under open loop control and there is no sensor for the bus voltage. The system only needs to sense 7 signals,

3 input line frequency voltage, 3 input line frequency current and the output voltage. The bus voltage is ensured by DCX operation and the power balance is ensured by the same control signal v_{c-a}. In this control method, we can eliminate the high-bandwidth, high-voltage control command for the secondary side devices in the first SST control method.

Compare these two control methods from communication point of view, the first method and the second method all sense 7 signals, 3 input line frequency voltage, 3 input line frequency current and the output voltage. For the first method, it needs $3n \times 3$ low-bandwidth high-voltage signal, $3n \times 4$ high-bandwidth low-voltage signal, and $3n$ high-bandwidth high-voltage signal. For the second method, it needs $3n$ low-bandwidth high-voltage signal and $3n \times 3$ high-bandwidth low-voltage signal. There is no high-bandwidth high-voltage signal needed in the second method.

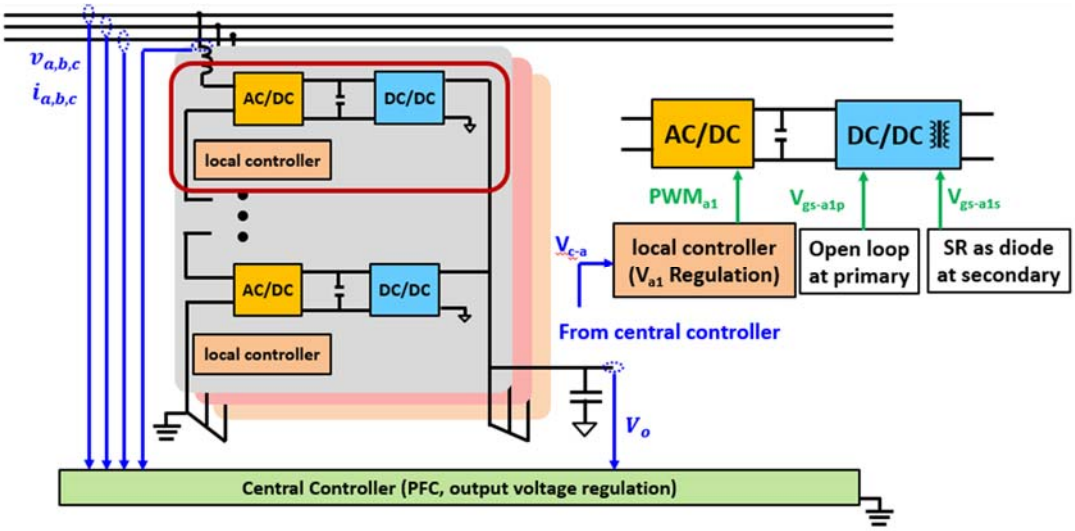


Fig. 61. SST control with DC/DC open loop control

System level simulation to evaluate different operation methods with the impact of power flow.

Constant power flow control method for DC-DC stage in SST

The SST system consists of N models per phase with input series output parallel structure. The input side will directly be connected to the MVAC grid and the output will be series connected with another interleaved Buck circuits as the fast charger for electrical vehicle application. The prototype of the SST is rated as input AC-voltage of 13.2kV, output DC-voltage of 1.1kV, bus voltage of 1.6kV, 9+1 modules per phase, and the output power of 405kVA. The modeling and control of the SST, for both CHB stage and CLLC converter with constant power flow as DC-DC stage is introduced in this section.

1. *Modeling and control for CHB stage*

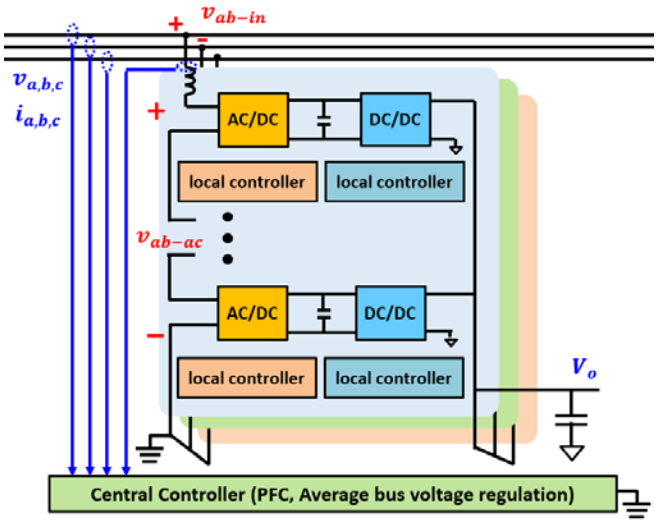


Fig. 62. Three phase SST with constant power control in DC-DC Stage

The AC-DC stage has 3 goals, power factor correction, bus voltage balance, and bus voltage regulation. A 2-step control strategy is applied to achieve these control goals. The first step is a conventional d-q control to achieve power factor correction and bus voltage regulation. And the second step is the individual voltage balance. Based on Fig. 55, the CHB stage voltage current equations can be written as

$$\begin{bmatrix} v_{ab-in} \\ v_{bc-in} \\ v_{ca-in} \end{bmatrix} - \begin{bmatrix} v_{ab-ac} \\ v_{bc-ac} \\ v_{ca-ac} \end{bmatrix} = L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

where v_{ab-in}, v_{bc-in}, v_{ca-in} are the grid line voltage; v_{ab-ac}, v_{bc-ac}, and v_{ca-ac} are CHB AC-side voltage; i_a, i_b, and i_c are inductor current.

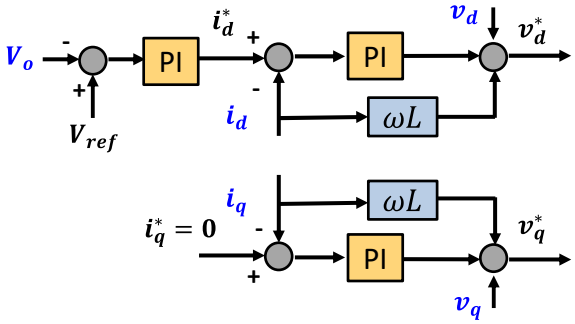


Fig. 63. Scheme for dq decoupled control

With, d-q transformation on (1), the equation in dq coordinate can be re-written as

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} - \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} = L \begin{bmatrix} \frac{d}{dt} & -\omega \\ \omega & \frac{d}{dt} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix}$$

where v_d, v_q are the d- and q- axis component of grid line voltage; v_d^* and v_q^* are CHB AC-side voltage under dq coordinate; i_d and i_q are inductor current in the same coordinate. The scheme of the dq control is shown as Fig. 56. Bus voltage for each module will be sensed and the average bus voltage v_{ave} will be calculated in the central controller. The reference bus average voltage $v_{ref-ave}$ is set based on the designed system bus average as 1.6kV. The error voltage will go through the proportional-integral (PI) controller to get the reference active current i_d^*. To get unity power factor, the i_q^* should be set as 0. With such dq control, the control signal for average value of the bus capacitor v_{c-ai}, v_{c-bi}, and v_{c-ci} can be got and the power factor correction can be achieved. Here, i means ith module per phase.

Due to the parasitic components in the circuit and the small error of duty cycle, the individual voltage balance should be taken into special consideration. For the individual voltage, the voltage balancing control should occur in the local controller and the control scheme is shown in Fig. 57. The local controller senses the individual bus voltage (v_{ai}) and compare with the reference bus voltage (V_{ref}). The error of these two voltages come into another PI controller to generate the compensation signal v_e. The individual voltage balance can be obtained by the sum of the compensation signal v_e and the control signal v_{c-ai}, v_{c-bi}, and v_{c-ci}.

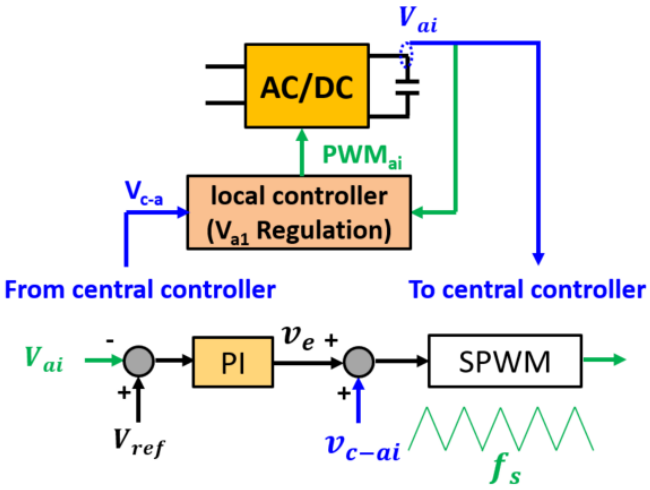


Fig. 64. Control scheme for individual voltage balance control

2. Modeling and control for DC-DC stage

With the CHB stage control, the power factor correction, the voltage regulation, and the voltage balance are achieved. Other control goals are the current sharing between modules, the power regulation, and the output voltage regulation. The power regulation method has been proposed for Dual Active Bridge (DAB) circuit. For the CLLC circuit, the control concept is similar. The difference is using the frequency control instead of the phase shift angle. The control scheme is shown in Fig. 58. One module is used as an example to illustrate how the control concept works. The control loop includes two parts. For the voltage loop control, the sensed output voltage V_o is compared with the reference voltage V_o^{ref} and generates the

constant power reference P_{ref}. In the controller, such P_{ref} will be divided by the bus voltage V_{ai} to get the input current reference I_{ref} for the CLLC converter. For the current loop, the sensed input current I_{ai} compares with the reference current. The error current comes into the PI controller to get the control signal of the CLLC converter. In this way, the current sharing between modules and the power regulation can be realized in the system.

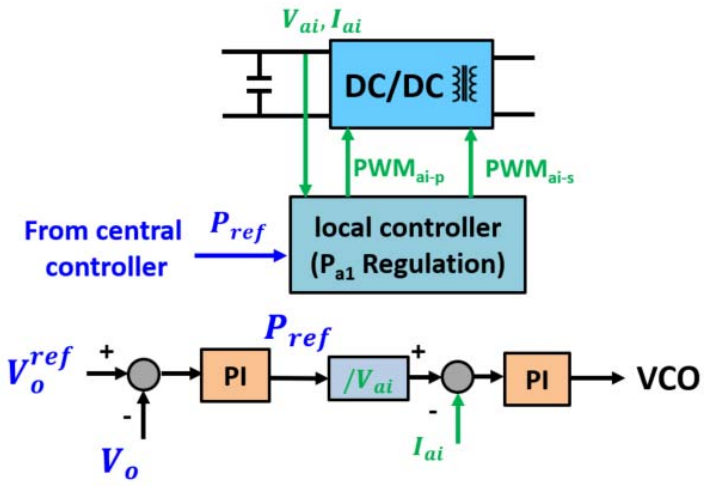


Fig. 65 Control scheme for power regulation control

3. Bus Capacitor Design

From the aforementioned analysis, the output power for the CLLC stage is a constant power. For the input stage of the CHB stage, under the unity power factor assumption, there is a double line frequency component power as shown in the Fig. 59. Due to the mismatch of the input and output power, bus capacitor should be put between the CHB stage and CLLC stage to achieve the goal for power regulation.

$$v_a = Vsin(\omega t)$$

$$i_a = Isin(\omega t)$$

$$P_a = \frac{VI}{2} - \frac{VI}{2}\cos(2\omega t)$$

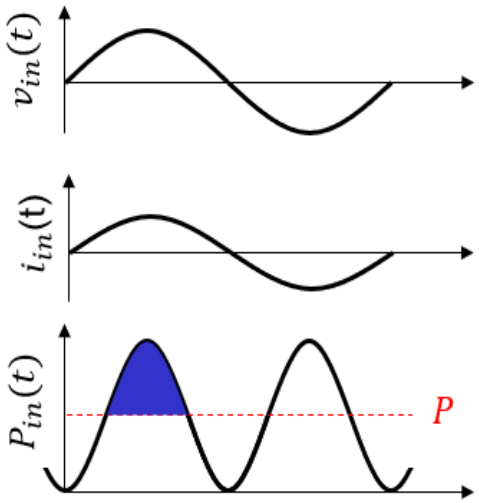


Fig. 66 Input voltage, current, and power waveform

Because the CLLC converter has a constant power flow, a simplification can be made on the 3-Phase system. In Fig. 60, the DC-DC stage is regarded as a constant power. Consider one module a_i of Phase A, assume the voltage ripple ΔV_{ai} is much smaller than the DC voltage V_{ai}. So that the input current of the DC-DC stage is

$$I_{ai} \approx \frac{P_o}{V_{ai}}$$

where P_o is the power per module.

For the output current for the CHB stage,

$$i_{ai}^{a/d} \approx \frac{p_{ai}(t)}{V_{ai}} = P_o[1 - \cos(2\omega t)]$$

where $p_{ai}(t)$ is the output power per module.

For the bus capacitor,

$$i_{ai}^{a/d} - I_{ai} = C\frac{dv_{ai}(t)}{dt}$$

Solve the equation, the bus voltage is

$$v_{ai}(t) = V_{a1} + \frac{P_o/V_{ai}}{2\omega C}\sin(2\omega t)$$

For certain voltage ripple ΔV_{ai}, the minimum capacitor value is

$$C = \frac{P_o}{2\omega V_{ai}\Delta V_{ai}}$$

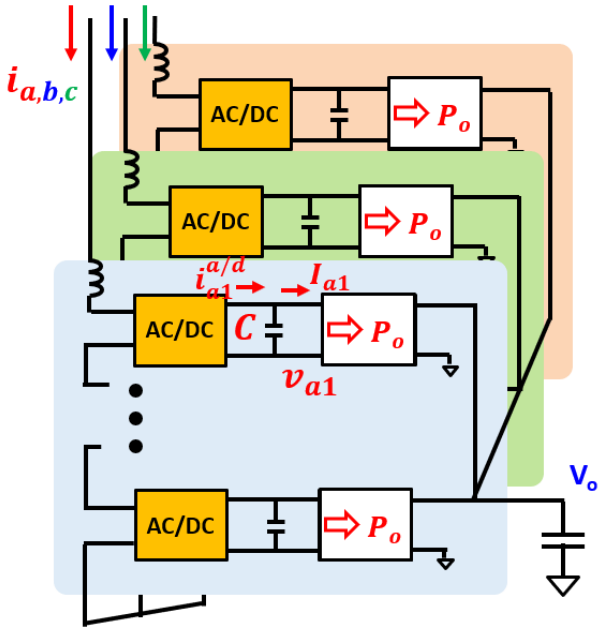


Fig. 67 System scheme with simplified DC-DC stage as constant power flow

Consider the bus voltage as 1.6kV, output power as 15kW, and 5% of voltage ripple, the bus capacitor should be larger than $155\mu F$.

Fluctuating power flow control method for DC-DC stage in SST

Although aforementioned constant power flow method in the DC-DC stage is popular in many researches, one of the drawbacks of this control method is the bus capacitor. Film bus capacitor occupies more than 20% volume in the DC-DC converter. If using electrolytic capacitor, the volume will be smaller. However, the lifetime of the electrolytic capacitor will be another bottleneck. Some researchers proposed another control method for the SST system with the DC-DC stage work with fluctuating power flow. The idea for such control method is easy to understand. There is double line frequency power flow in each phase in the CHB stage. If the SST system allows no matter how much power flows in, the same amount of power flows out from the output. There is no requirement of the capacitor usage. Due to the three-phase system, the double line frequency for the three phases can be cancelled with each other at the output terminal. The output power will still be a constant value.

1. *Modeling and control with DC-DC fluctuating power flow*

One of the easiest methods to achieve such DC-DC fluctuating power flow control is to use the DC-Transformer (DCX) concept at the DC-DC stage. The CLLC converter works as a transformer. There is no control ability in the converter to regulate the power flow. The control scheme is shown in Fig. 61.

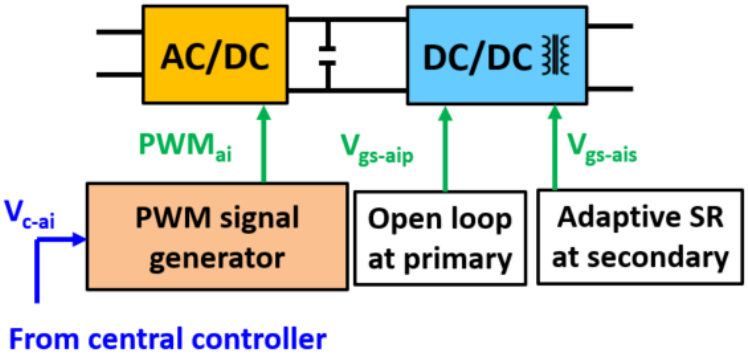


Fig. 68 Control scheme with fluctuating power flow control in DC-DC stage

Compared with the control method with constant power flow in DC-DC stage, the control method with fluctuating power flow is much easier. The central controller only needs to sense 7 signals, input signals v_a, v_b, v_c, i_a, i_b, i_c, and output voltage V_o. The control goals for fluctuating power flow control includes PFC, bus voltage regulation, bus voltage balance and output voltage balance. In the fluctuating power flow control, output voltage is sensed for dq control to achieve PFC and bus voltage regulation instead of bus voltages in the constant power control. Consider one module as an example. Due to DCX,

$$V_{bus} = \frac{1}{n} V_o$$

where n is the transformer turns ratio.

The bus voltage regulation and balance are ensured by the DCX operation under fluctuating power flow. In this case, all the bus voltage in the system equals to V_{bus}. For the CHB stage, the control can be achieved by different control signal v_{c-ai}, v_{c-bi}, and v_{c-ci}. For the DC-DC stage, it is easy to control such DCX by using open loop control at the primary side and the adaptive SR control at secondary side.

2. Bus Capacitor Design

Still consider the unity power factor in this system. As the equation indicates, the output of the CHB stage is still a fluctuating power flow with double-line frequency. Due to DCX, the DC-DC stage can be simplified as a transformer, as shown in Fig. 62.

The CHB stage output current for the module a_i at phase A is

$$i_{ai}^{a/d} = p_{ai}(t)/v$$

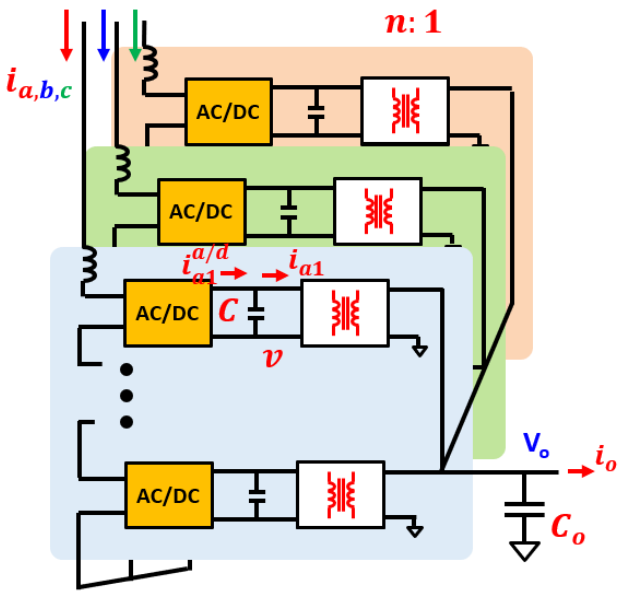


Fig. 69 System scheme with simplified DC-DC stage as transformer

where $p_{a1}(t)$ is the output power per module.

For the bus capacitor in 3-Phase

$$i_{ai}^{a/d} - i_{ai} = C\frac{dv}{dt}$$

$$i_{bi}^{a/d} - i_{bi} = C\frac{dv}{dt}$$

$$i_{ci}^{a/d} - i_{ci} = C\frac{dv}{dt}$$

Where i_{ai} is the DC-DC input current per module.

For the output capacitor

$$n(\Sigma i_{ai} + \Sigma i_{bi} + \Sigma i_{ci}) - i_o = C_o\frac{dv/n}{dt}$$

Add these equation together,

$$\left(\Sigma i_{ai}^{a/d} + \Sigma i_{bi}^{a/d} + \Sigma i_{ci}^{a/d}\right) - \frac{i_o}{n} = 3NC\frac{dv}{dt} + C_o\frac{dv/n}{dt}$$

For a three-phase balanced system,

$$\left(\Sigma i_{ai}^{a/d} + \Sigma i_{bi}^{a/d} + \Sigma i_{ci}^{a/d}\right) - \frac{i_o}{n} = 0$$

which means there is no voltage ripple in the three-phase system. And also, the conclusion is regardless of bus capacitor value. For a balance three-phase system, only decoupling capacitors need to put between the CHB and CLLC stages.

However, control with DC-DC fluctuating power flow has its own drawback. Because of $dv/dt = 0$,

$$i_{ai} = i_{ai}^{a/d} = P_o[1 - \cos(2\omega t)]/V_{bus}$$

$$i_{bi} = i_{bi}^{a/d} = P_o[1 - \cos(2\omega t - \pi/3\ )]/V_{bus}$$

$$i_{ci} = i_{ci}^{a/d} = P_o[1 - \cos(2\omega t + \pi/3\ )]/V_{bus}$$

The DC-DC stage will see double-line-frequency input current ripple with the fluctuating power flow in DC-DC stage.

Compare these two DC-DC stage control methods. For the constant power flow control in the DC-DC stage, large bus capacitors should be selected based on the voltage ripple. The current ripple is small. From system-level control point of view, bus voltage should be regulated for each module. For the fluctuating power flow control in the DC-DC stage, only decoupling capacitors and small bus capacitor is required for the high frequency ripple and unbalance three-phase grid. The space of the bulky capacitor can be saved. However, due to DCX, large current ripple can be seen in the CLLC converter, which will bring additional conduction loss and winding loss. From system level control point of view, DCX is much easier to control compared with voltage regulation.

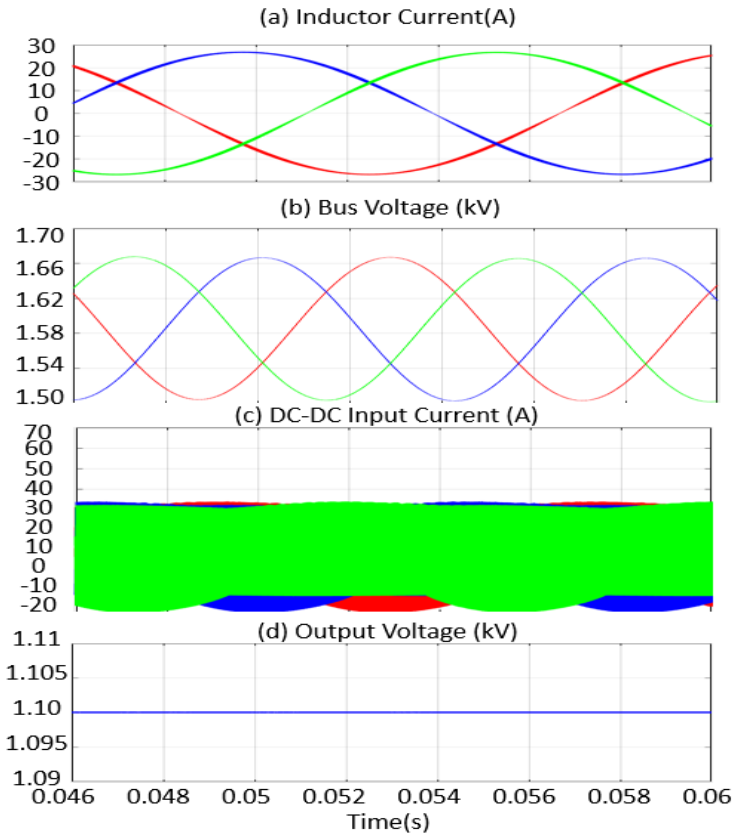


Fig. 70 Simulation result with constant power flow control in DC-DC stage

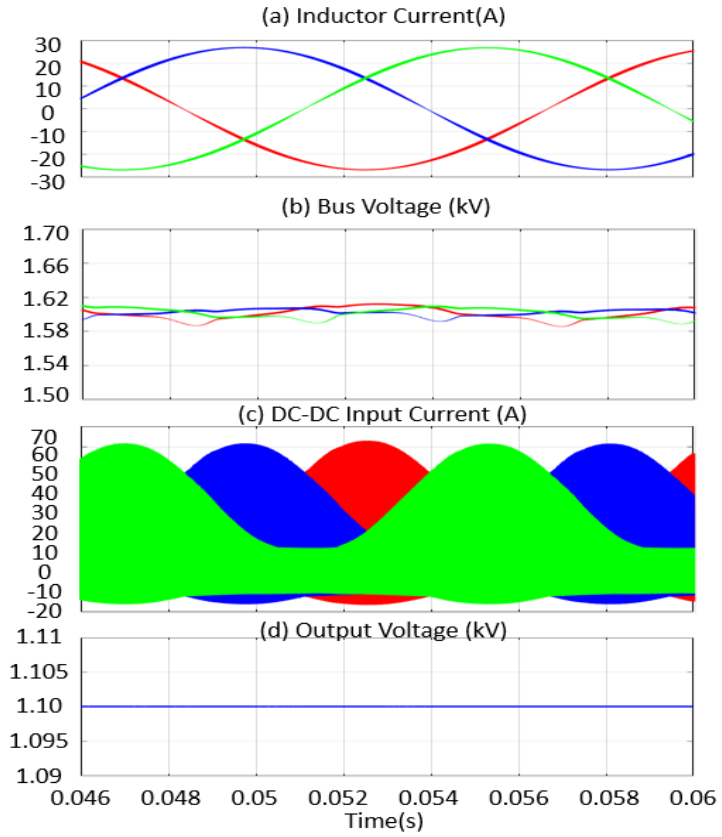


Fig. 71 Simulation result with fluctuating power flow control in DC-DC stage

Compare these two control methods from communication point of view, the first method and the second method all sense 7 signals, 3 input line frequency voltage, 3 input line frequency current and the output voltage. For the first method, it needs $3n \times 3$ low-bandwidth high-voltage signal, $3n \times 4$ high-bandwidth low-voltage signal, and $3n$ high-bandwidth high-voltage signal. For the second method, it needs $3n$ low-bandwidth high-voltage signal and $3n \times 3$ high-bandwidth low-voltage signal. There is no high-bandwidth high-voltage signal needed in the second method.

Simulation Result and potential methods to improve the performance

With the purpose to verify the operation principle, a simulation model is built with one module per phase. The AC-DC stage is a H-Bridge rectifier and the DC-DC stage is a 3-level half-bridge CLLC converter. The input voltage is 1.32kV, the bus voltage is 1.6kV and the output voltage is 1.1kV.

Fig. 63 shows the results for the constant power flow control in the DC-DC stage. Fig. 63 (a) demonstrates the inductor current waveform of the CHB stage. In the waveform, the red curve represents the Phase A inductor current, while the blue and green curve represent the Phase B and Phase C inductor current. The peak current for all these three inductor current is 27.8A. The bus voltage shows in Fig. 63 (b), based on the capacitor calculation, $155\mu F$ capacitors will have 5% (80V) ripple. The DC-DC stage input current is simulated in Fig. 63 (c). With the constant

power flow control, there is no double-line-frequency current ripple. The DC-DC input current has a peak value as 33.4A. The last simulation is the output voltage simulation. Due to the output voltage regulation in the CLLC converter, the output voltage is a constant

1.1kV. Compared with the constant power flow control in the DC-DC stage, the inductor current of the fluctuating power flow control is the same, which indicates the control for the CHB stage has the same effect. However, the DC-DC stage simulation waveform is totally different. For the bus voltage, the ripple for the bus voltage is less than 20V, can be regarded as a constant voltage. The huge difference occurs at the DC-DC input current. The peak current under fluctuating power flow control reaches 56.6A, which is almost two times higher than the current under constant power control. The loss of these two control methods can be evaluated based on the simulation. Use the device and transformer loss information, the loss breakdown for constant power flow control and fluctuating power flow can be calculated. Results are shown in Fig. 65.

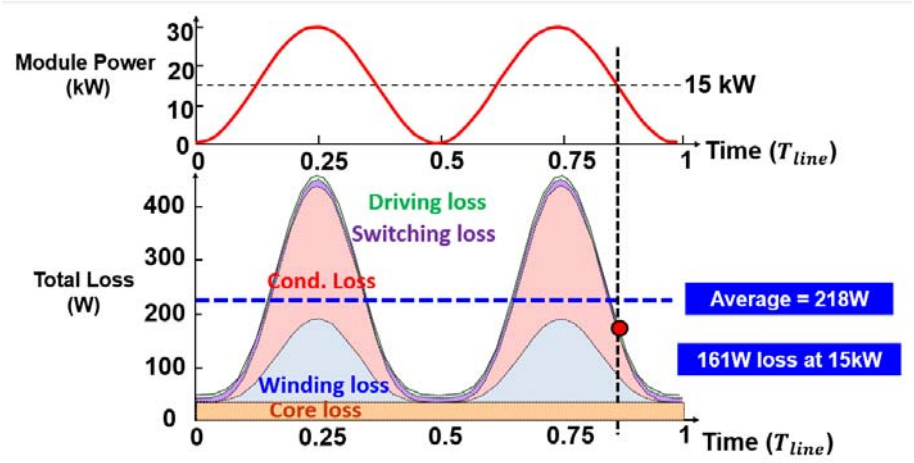


Fig. 72 Loss Breakdown of two control methods

From the loss breakdown, it is clear that both conduction loss and transformer winding loss are dominant in the fluctuating power flow control. That is because the input power fluctuates from0W to $2P_o$ (30kW). When the input is $2P_o$ (30kW), the conduction loss and the winding loss will be proportional to I^2, where the loss significantly increases. Compare the constant power flow control, whose loss is 161W, 57W loss (0.4% efficiency) increment happens with the fluctuating power flow. Consider the prototype volume as shown in Fig. 66.

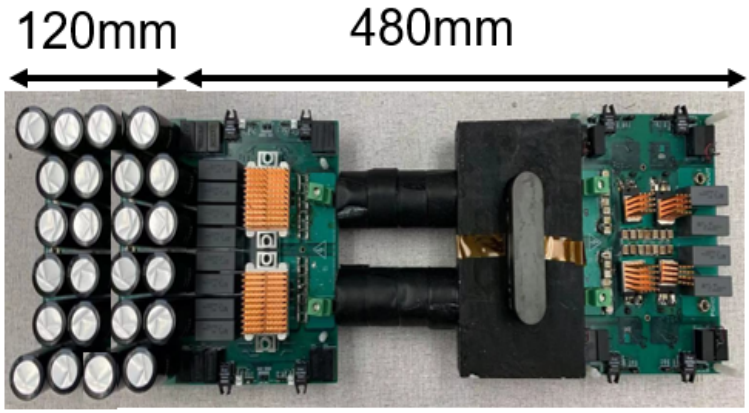


Fig. 73 15kW, 200kHz, CLLC converter prototype

The 0.4% efficiency sacrifice will gain 20% volume reduction in the DC-DC stage. However, from system point of view, such 20% volume reduction in DC-DC stage is neglectable while the 0.4% efficiency will lead to huge loss. It is hard to apply fluctuating power flow control in the SST system. From loss breakdown, the conduction loss and winding loss are dominant. If it is possible to use better devices to gain more benefit on fluctuating power flow control? For 15kW constant power flow control, the primary side and secondary side device are selected based on the current, 22A and 15A. Based on such criteria, FF23MR12_W1M1 from Infineon and C2M0045170D from Cree are selected. If do not consider the current level, devices can be chosen simply according to the R_{dson}. Based on such criteria, UF3SC120009K4S from UnitedSiC and G3R20MT17K from GeneSiC are the lowest R_{dson} devices in the market. The detailed comparison is shown in Table. VI. By using lower R_{dson} devices, both control methods will have a lower loss. The loss information for the fluctuating power flow control reduces to 173W, which is comparable with the constant power flow control method (161W), as shown in Fig. 67.

Table VI

Parameters of different devices

	FF23MR12 W1M1	UF3SC120009K4S	C2M0045170D	G3R20MT17K
V_{ds}	1.2kV	1.2kV	1.7kV	1.7kV
I_{ds} @100°C	50A	77A	48A	88A
R_{dson} @100°C	29.5mΩ	13mΩ	70mΩ	34mΩ
Q_g	124nC	234nC	188nC	400nC
C_{oss}	220pF	395pF	171pF	261pF

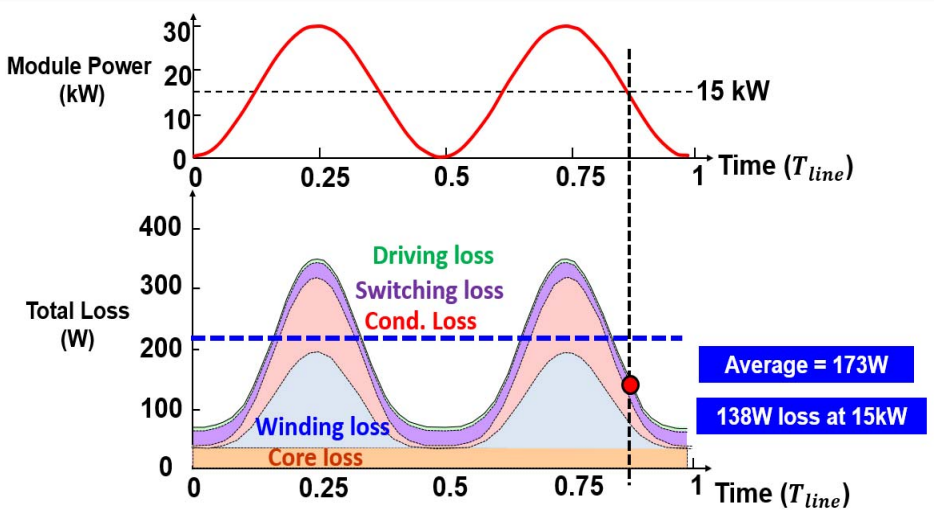


Fig. 74 Loss Breakdown of two control methods with lower R_{dson} Devices

For the efficiency curve in Fig. 68, the measured data is close to the simulation and calculation data. The highest error is smaller than 0.2%. In this case, the simulation prediction and the analysis based on the simulation is convincing. From the simulation result, the fluctuating power flow gains more benefit with lower R_{dson} devices.

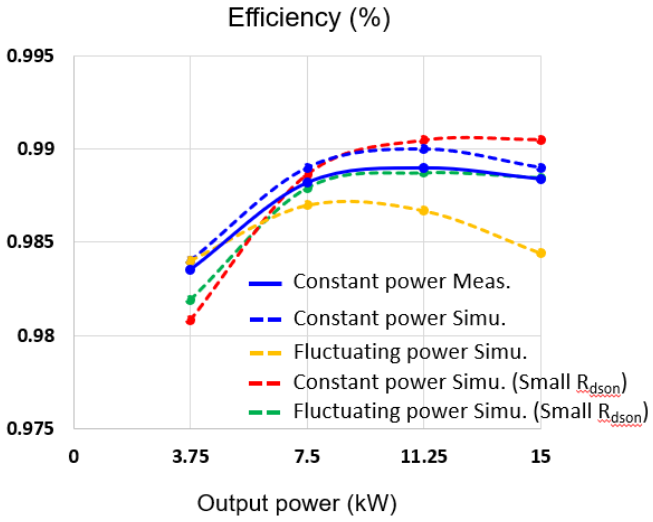


Fig. 75 Efficiency measurement with different conditions

Constant power flow control loss model for DC-DC stage in SST

The modeling and control of the SST, for both CHB stage and CLLC converter with constant power flow as DC-DC stage is introduced in last report. In this report, the loss model is introduced in detail. The control scheme for the DC-DC stage with constant power control is shown in Fig. 69.

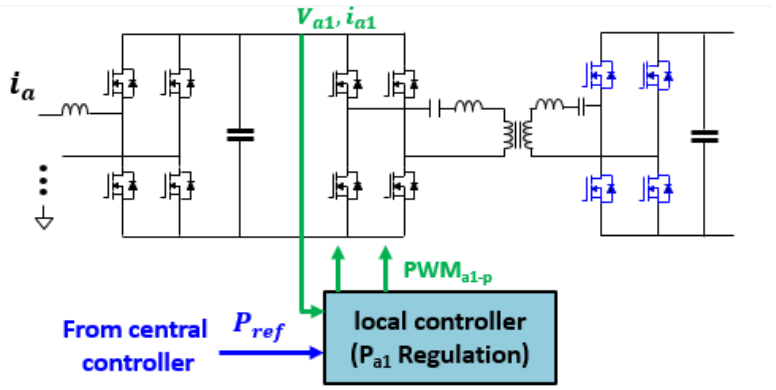


Fig. 76 Control scheme SST with constant power control in DC-DC Stage

Compared with traditional two stage SST system, the topology of the DC-DC stage is selected as CLLC rather than DAB for a lower turn-off current with less switching loss. In addition, the CLLC topology use synchronous rectifier (SR) at the secondary side, which can be decoupled with the primary side high voltage potential with less insulation burden at secondary side. The power going through the DC-DC stage is regulated by the input current. To achieve the constant power flow, huge bus capacitor will be required to handle double-line-frequency ripple.

To calculate the loss breakdown for the constant power flow control method, different parts of loss will be analyzed. For device conduction loss, the device current can be calculated based on the CLLC circuit working principle.

For primary side device current,

$$I_{p,rms} = \frac{I_o}{4\sqrt{2}n}\sqrt{\frac{64C_{oss}^2 n^4 R_o^2}{t_d^2} + 4\pi^2 + \frac{16\pi^2(t_d^2 + t_d T_o)}{T_o^2}}$$

where I_o is the output current, n is the turns ratio, R_o is the output load, t_d is the deadtime and T_o is the resonant period.

For secondary device current,

$$I_{s,rms} = \frac{\sqrt{6}}{24\pi} I_o \sqrt{\frac{64(5\pi^2 - 48)C_{oss}^2 n^4 R_o^2 T_o}{t_d^2 T_s} + \frac{12\pi^4 T_o}{T_s} + \frac{48\pi^4(t_d^2 + t_d T_o)}{T_o T_s}}$$

where T_s is the switching period.

And the conduction loss can be written as

$$P_{cond}(t_d) = I_{p,rms}^2 \cdot 4R_{dson_{pri}} + I_{s,rms}^2 \cdot 4R_{dson\_sec}$$

As we can see, the conduction loss will be a function of the circuit deadtime with certain I_o and T_o.

Consider the circuit parameters in this project. For one module, the input and output voltage are 1.6 kV / 1.1 kV. The power level is 15kW. And the switching frequency is 200kHz. Select FF23MR12W1M1 from Infineon as the primary side device and C2M0045170D from Cree as the secondary device. We can get the conduction loss for primary and secondary devices as shown in red curve and green curve in Fig. 70.

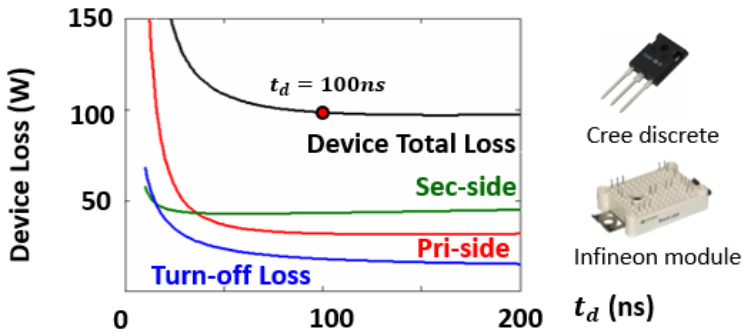


Fig. 77 Device loss calculation for the constant power flow control

For the turn-off loss, it is determined by the turn-off current and the turn-off energy for the primary side devices.

For the turn-off current

$$I_{off}(t_d) = \frac{1}{2}\frac{nV_o \times (T_s/2 - t_d)}{L_m}$$

where V_o is the output current and L_m is the magnetizing inductor.

For the E-off information, we can get that from the datasheet with

$$E_{off}\ (\mu J) \approx 0.6\, I_{off} + 10$$

Based on aforementioned information, we can get the turn-off loss with different t_d as shown in Fig. 70 with blue curve. The turn-off loss is only related with the output voltage and the switching frequency. With the sum of all the device loss, $t_d = 100ns$ is selected as the design point.

For the transformer loss, it can also be separated as core loss and winding loss. For core loss, it can be simply calculated by

$$P_{core} = P_v \times V_{core}$$

where P_v means core loss density and V_{core} is the core volume. With the rectangular waveform, Modified Steinmetz Equation is utilized to calculated the core loss density,

$$P_v = \frac{8}{\pi^2} k f_s^{\alpha} {B_m}^{\beta}$$

From the equation we will see the core loss density will be impacted by the magnetizing current and the switching frequency with the impact of f_s and B_m.

For the winding loss, we can also separate it as DC winding loss and AC winding loss. We can write the winding loss equation as follow

$$P_{winding} = I_{rms}^2[R_{dc} + R_{ac}(f_s)]$$

In the equation, $R_{dc} = \sum_{j=1}^{N} R_{turn,j}$ and $R_{ac} = \sum_{j=1}^{N}(2\pi f_s k)^2/G_{eddy,j}$, $k = \frac{1}{I_{rms}}\frac{1}{A}\int_A B(\sigma)\, d\sigma$. The winding loss is also proportional to the I_{rms}^2 with given structure.

With all the loss model, the transformer can also be optimized and the optimization process has been shown in the previous report. Finally, a 16-turn, 300kW/m^3 core loss density, 200-kHz transformer is designed with the loss and size trade-off.

The loss breakdown for the constant power flow control is shown in Fig. 3. The power profile for the output of the AC-DC stage is the red sine curve and the power flows through the DC-DC stage is the blue curve. Due to the constant power flow, the loss in the DC-DC stage will be constant 161W during one-line-frequency cycle.

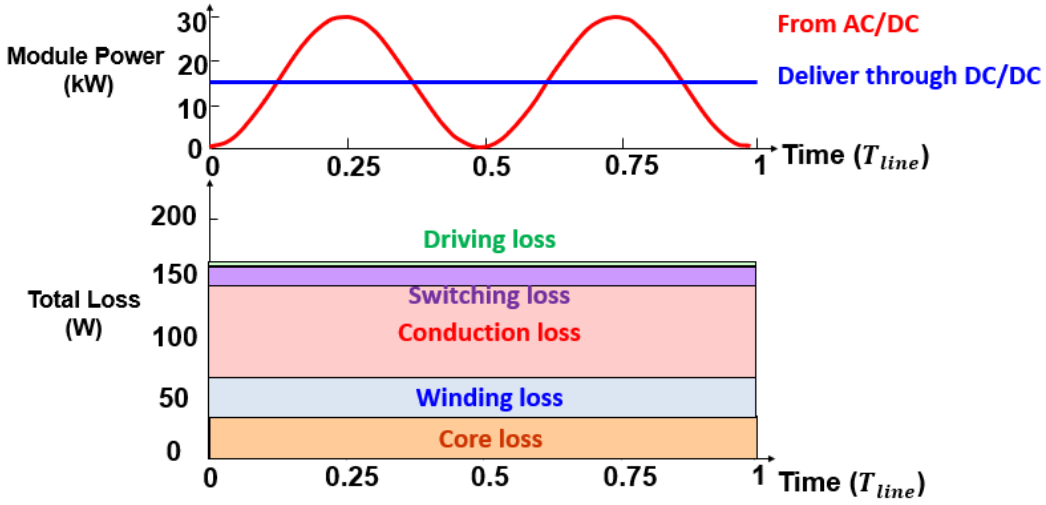


Fig. 78 Device loss breakdown for the constant power flow control

Fluctuating power flow control loss model for DC-DC stage in SST

In the constant power flow control method, huge bus capacitor is required to handle double-line-frequency ripple. The bus capacitor will lead to additional burden from BOM and volume point of view. To eliminate the bus capacitor, a fluctuating power flow control method is proposed. In the fluctuating power flow, the DC-DC stage will work as a transformer (DCX). Due to no control function in the DC-DC stage, no matter how much power comes out of the AC-DC stage will totally flow through the DC-DC stage. By using this control scheme, bus capacitor can be eliminated due to the balanced 3 phase system. However, the drawback is the current ripple. Because all the power will deliver through the DC-DC stage, the DC-DC stage will see the double-line-frequency power. Which lead to high current stress with double line frequency. The circuit diagram is shown in Fig. 72.

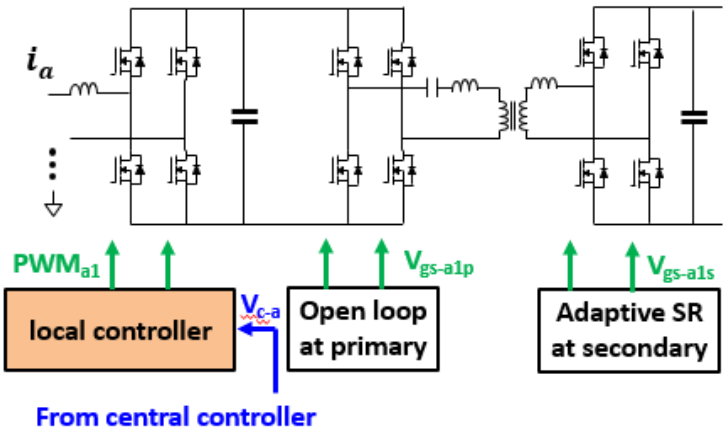


Fig. 79 Control scheme SST with fluctuating power control in DC-DC Stage

To calculate the loss breakdown for the fluctuating power flow control method, conduction loss, switching loss, core loss and winding loss will also be evaluated. For device conduction loss, compared with the constant power flow control, a double-line frequency ripple should be added to the current profile.

For primary side device current,

$$I_{p,rms} = \frac{I_o[1 + cos(2\omega t)]}{4\sqrt{2}n} \sqrt{\frac{64C_{oss}^2 n^4 R_o^2}{t_d^2} + 4\pi^2 + \frac{16\pi^2(t_d^2 + t_d T_o)}{T_o^2}}$$

where $[cos(2\omega t)]$ represents the double line frequency ripple

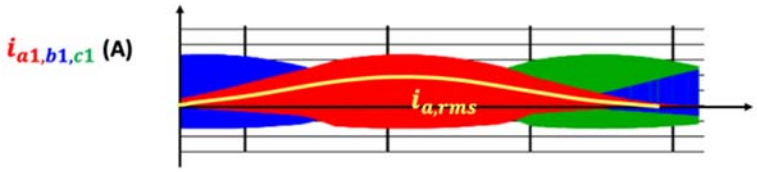


Fig. 80 Current profile with fluctuating power control in DC-DC Stage

For secondary device current, we have the same conclusion,

$$I_{s,rms} = \frac{\sqrt{6}}{24\pi} I_o[1 + cos(2\omega t)] \sqrt{\frac{64(5\pi^2 - 48)C_{oss}^2 n^4 R_o^2 T_o}{t_d^2 T_s} + \frac{12\pi^4 T_o}{T_s} + \frac{48\pi^4(t_d^2 + t_d T_o)}{T_o T_s}}$$

And the conduction loss over one-line cycle can be written as

$$P_{cond}(t_d) = \frac{1}{T_{line}} \int_0^{T_{line}} (I_{p,rms}^2(t) \cdot 4R_{dson_{pri}} + I_{s,rms}^2(t) \cdot 4R_{dson\_sec}) dt$$

$$P_{cond,FP} = \frac{3}{2} P_{cond,CP}$$

As we can see, the conduction loss for the fluctuating power flow will be 1.5 times higher than the conduction loss for constant power flow with the same design criteria.

For turn-off loss, it is only related with the output voltage and the switching frequency. With the same output voltage and the switching frequency, the turn-off loss in the fluctuating power flow control should be the same with the loss in the constant power flow control.

The same conclusion can be drawn to the core loss. Due to the same output voltage and the switching frequency, the core loss for the fluctuating power flow control will be also the same with the loss in the constant power flow control.

For the winding loss, based on the previous analysis, the winding loss is proportional to the I_{rms}^2. Due to the fluctuating power flow, the winding loss over one-line cycle is

$$P_{winding} = \frac{1}{T_{line}} \int_0^{T_{line}} [I_{rms}(1 + cos2\omega t)]^2 [R_{dc} + R_{ac}(f_s)] dt$$

The winding loss for the fluctuating power flow will also be 1.5 times higher than the winding loss for constant power flow with the same design parameters.

To compare the loss difference with these two control methods, the loss breakdown for the fluctuating power flow control is shown in Fig. 74. The power profile for the output of the AC-DC stage is the red sine curve and the power flows through the DC-DC stage is the dash blue curve, which overlapped with the output power for the AC-DC stage. Due to the double-line-frequency current ripple flow, the loss in the DC-DC stage will be a fluctuating power with 218W average loss during one-line-frequency cycle. As we can see, the core loss and the switching loss remain the same. However, the winding loss and the conduction loss has a huge variation during one cycle.

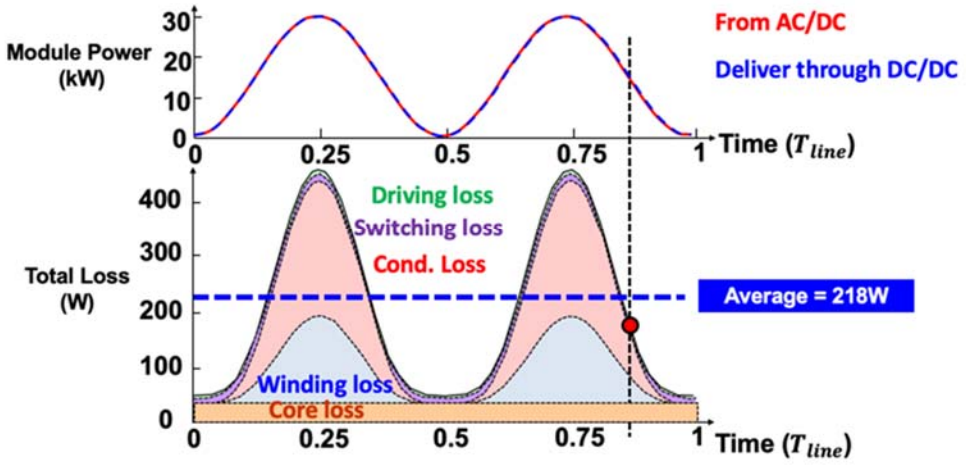


Fig. 81 Device loss breakdown for the fluctuating power flow control

The benefit for the fluctuating power flow control is the save on the bus capacitor. Because there is no bus capacitor required, the volume of the DC-DC converter will have a 20% reduction. As shown in Fig. 75. However, the sacrifice is the loss. With peak power comes to $2P_o$, the efficiency for the DC-DC stage will have a 0.4% drop. In the high-power

application, 0.4% efficiency means a lot. And we do not want to pay such a price in the efficiency.

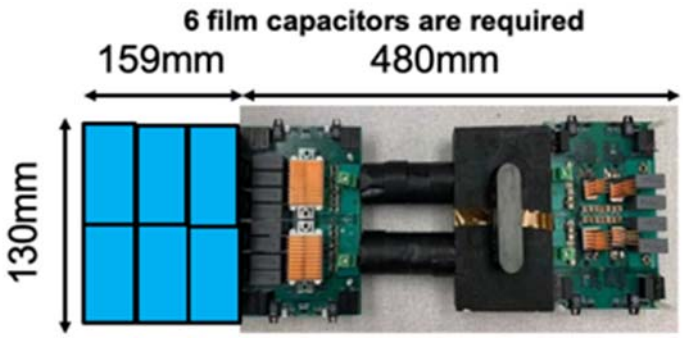


Fig. 82 Hardware prototype with huge bus capacitor

Partial fluctuating power flow control loss model for DC-DC stage in SST

As we mentioned above, the constant power flow control requires huge bus capacitor with lower loss. The fluctuating power flow control eliminates all the capacitors with a 35% loss increment. These two control methods represent two extreme cases from no fluctuating power to full fluctuating power. To make some trade-off between the bus capacitor and loss, a partial fluctuating power flow control is proposed. The AC-DC stage control will be same as the fluctuating power flow control. However, the input current of the DC-DC stage will be regulated. With the same output voltage, we can control the power profile going through the DC-DC stage by regulating the input current. The control scheme is shown in Fig. 8. With the red curve as output for the AC-DC stage and the blue curve as the input of DC-DC stage.

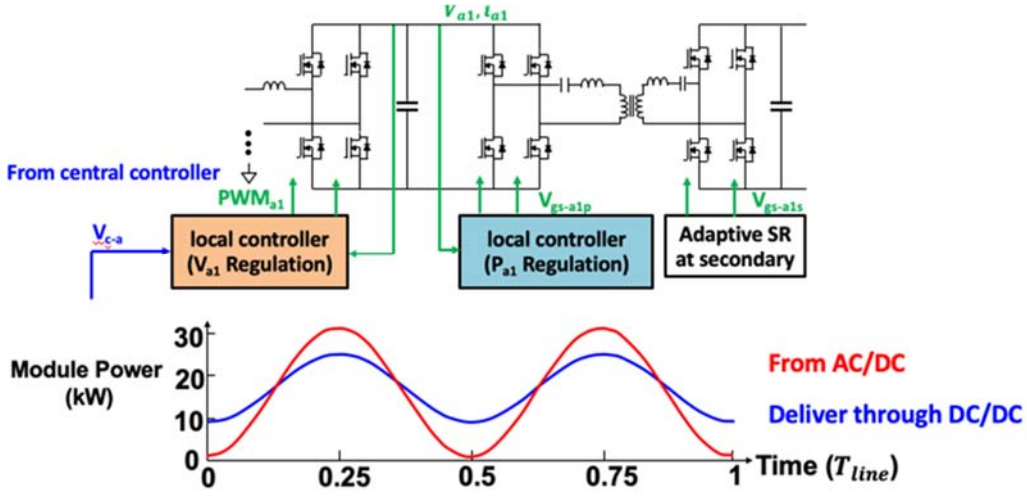


Fig. 83 Control scheme SST with partial fluctuating power control in DC-DC Stage

The loss model for the partial fluctuating power flow control method is shown below.

For primary side device current,

$$I_{p,rms} = \frac{I_o[1 + kcos(2\omega t)]}{4\sqrt{2}n}\sqrt{\frac{64C_{oss}^2 n^4 R_o^2}{t_d^2} + 4\pi^2 + \frac{16\pi^2(t_d^2 + t_d T_o)}{T_o^2}}$$

where $[kcos(2\omega t)]$ represents the partial double line frequency ripple. k is the percentage of the power deliver through the DC-DC stage.

For secondary device current, we can also have the similar conclusion,

$$I_{s,rms} = \frac{\sqrt{6}}{24\pi} I_o[1 + kcos(2\omega t)]\sqrt{\frac{64(5\pi^2 - 48)C_{oss}^2 n^4 R_o^2 T_o}{t_d^2 T_s} + \frac{12\pi^4 T_o}{T_s} + \frac{48\pi^4(t_d^2 + t_d T_o)}{T_o T_s}}$$

And the conduction loss over one-line cycle can be written as

$$P_{cond}(t_d) = \frac{1}{T_{line}}\int_0^{T_{line}} (I_{p,rms}^2(t) \cdot 4R_{dson_{pri}} + I_{s,rms}^2(t) \cdot 4R_{dson\_sec})dt$$

$$P_{cond,PFP} = (1 + \frac{k^2}{2})P_{cond,CP}$$

As we can see, the conduction loss for the fluctuating power flow will be $(1 + \frac{k^2}{2})$ times higher than the conduction loss for constant power flow with the same design criteria.

For turn-off loss and core loss, it is still related with the output voltage and the switching frequency. With the same output voltage and the switching frequency, the turn-off loss and core loss in the partial fluctuating power flow control should be the same.

For the winding loss, based on the previous analysis, the winding loss is proportional to the I_{rms}^2. Due to the partial fluctuating power flow, the winding loss over one-line cycle is

$$P_{winding} = \frac{1}{T_{line}}\int_0^{T_{line}} [I_{rms}(1 + cos2\omega t)]^2[R_{dc} + R_{ac}(f_s)]dt$$

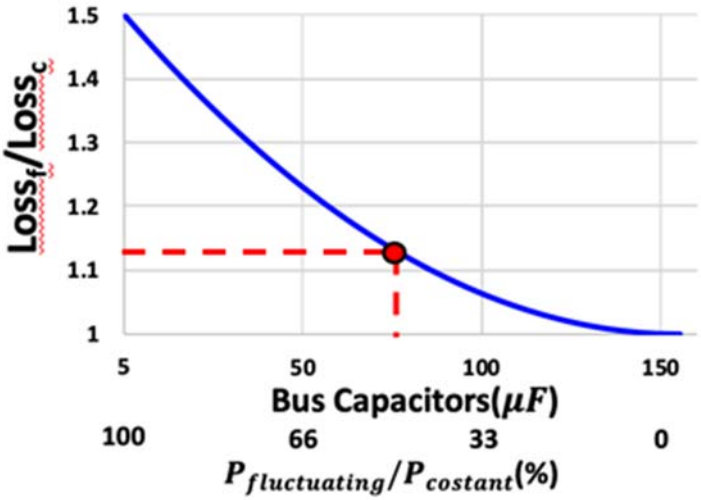


Fig. 84 trade-off between the bus capacitor and the converter loss

The winding loss for the fluctuating power flow will also be $(1+\frac{k^2}{2})$ times higher than the winding loss for constant power flow with the same design parameters. With the loss model, we can play the trade-off between the bus capacitor and the converter loss. The result is shown in Fig. 77. As we can see, if we choose $k = 0.5$, 50% of the fluctuating power flow will go through the DC-DC stage. With the same voltage ripple, 50% of the bus capacitor can be saved with only 12.5% of conduction loss and winding loss increase. In other words, we pay 8% total loss and save 50% of bus capacitor and 10% of total volume. This trade-off is worth to trying.

The loss breakdown for the partial fluctuating power flow control is shown in Fig. 78. Due to 50% of double-line-frequency current ripple flow, the loss in the DC-DC stage will be 186W, much smaller than the fluctuating power flow control.

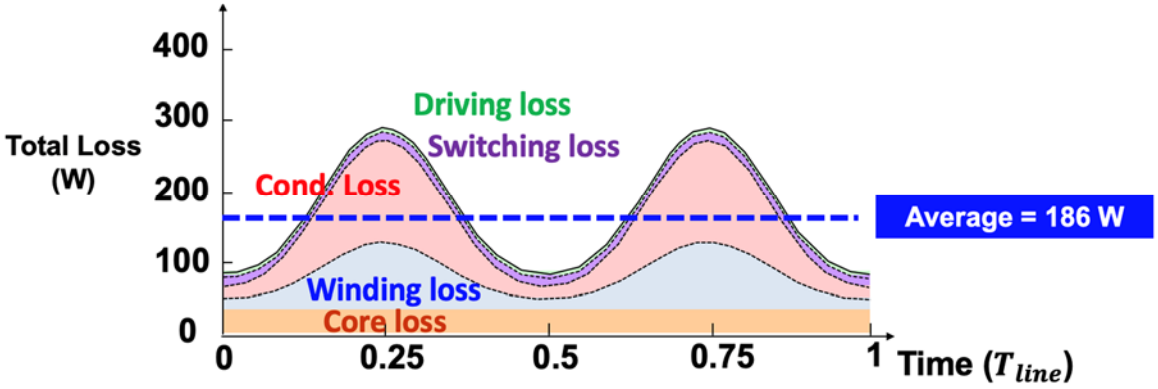


Fig. 85 Device loss breakdown for the partial fluctuating power flow control

The efficiency comparison is shown in Fig. 86. As we can see, the method 3 represents the partial fluctuating power flow control. The efficiency is close to the constant power control as method 1 with only 0.1% efficiency difference. However, method 3 can save 50% of the bus capacitor, which might be attractive from BOM and power density point of view.

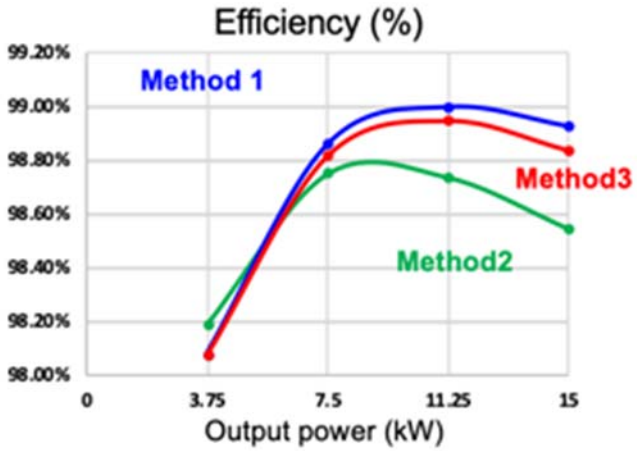


Fig. 86 Efficiency comparison for different control methods

Hardware test result

Based on the design parameters with 1.6 / 1.1 kV input and output voltage, 15kW rated power, and 200kHz switching frequency. The hardware prototype is built as shown in Fig. 82. The open loop test result is shown as below with 7.5kW, 11kW, 15kW, 18kW, and 22kW, as shown from Fig. 80-84.

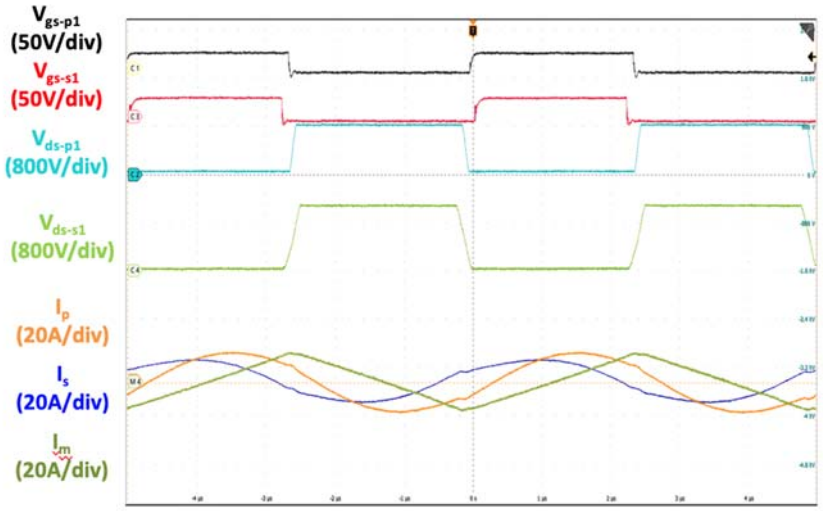


Fig. 87 Test waveform at 7.5kW

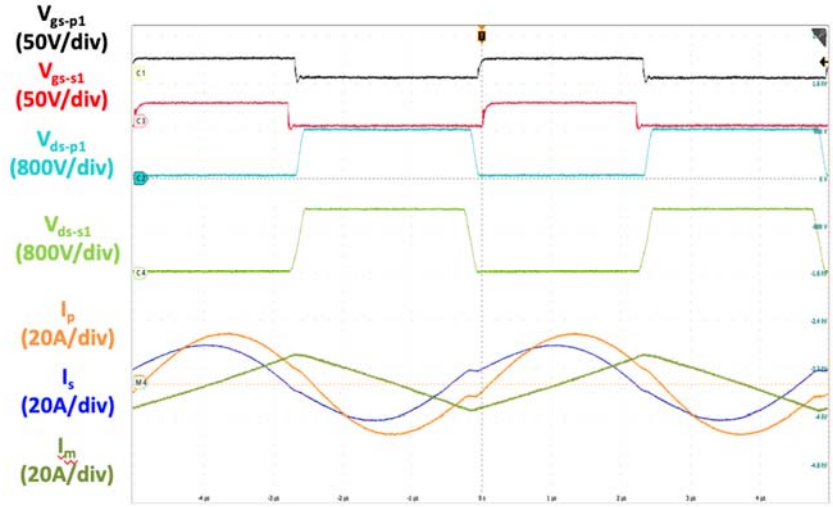


Fig. 88 Test waveform at 11kW

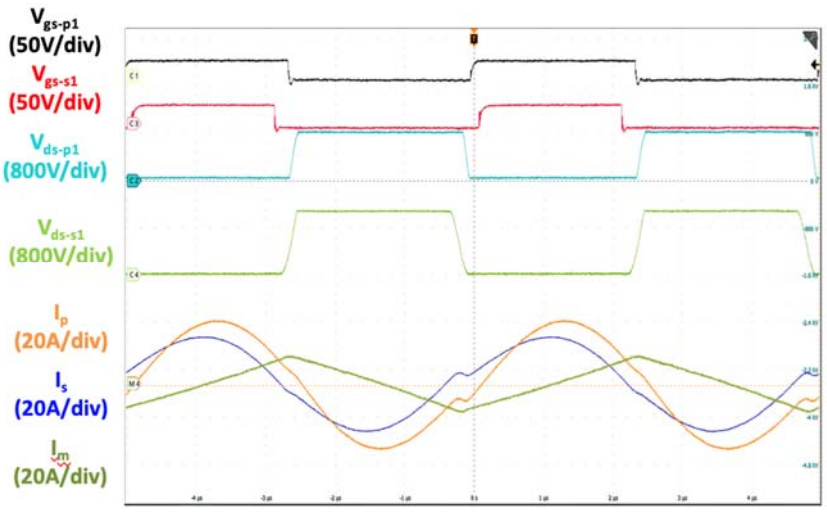


Fig. 89 Test waveform at 15kW

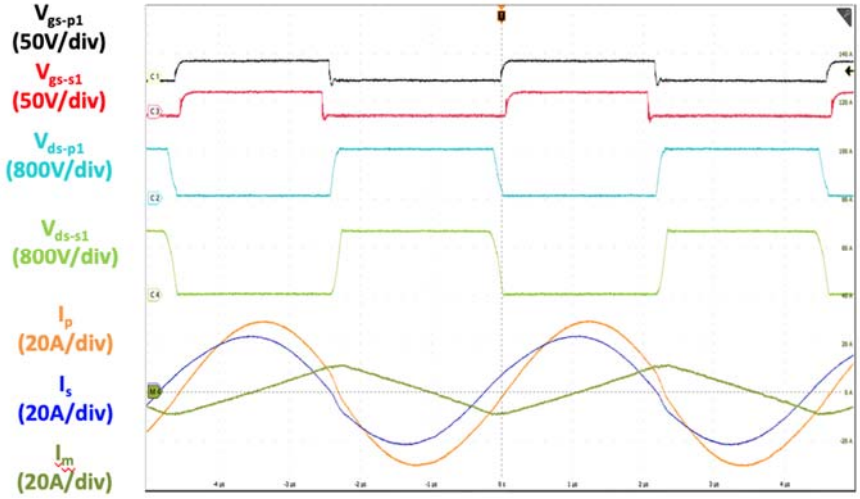


Fig. 90 Test waveform at 18kW

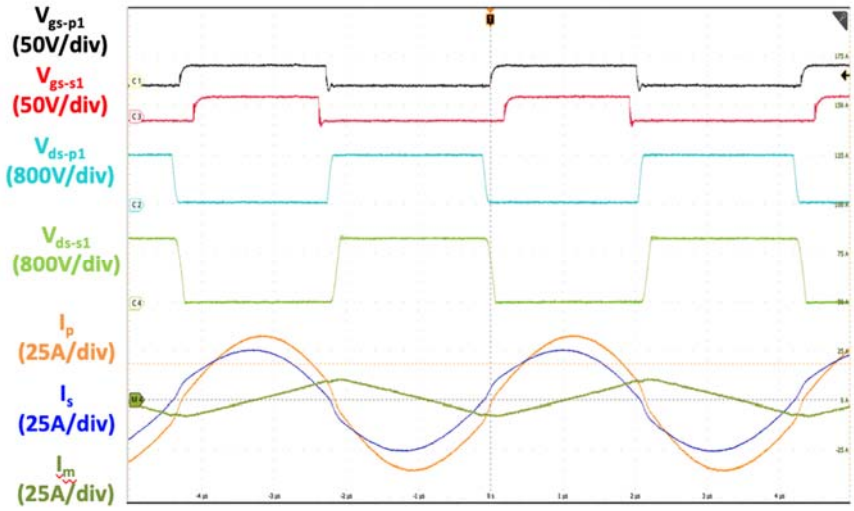


Fig. 91 Test waveform at 22kW

The efficiency curve is shown in Fig. 85. From the efficiency curve, the measured loss is quite close to the calculated result, which means the calculation result is convincing.

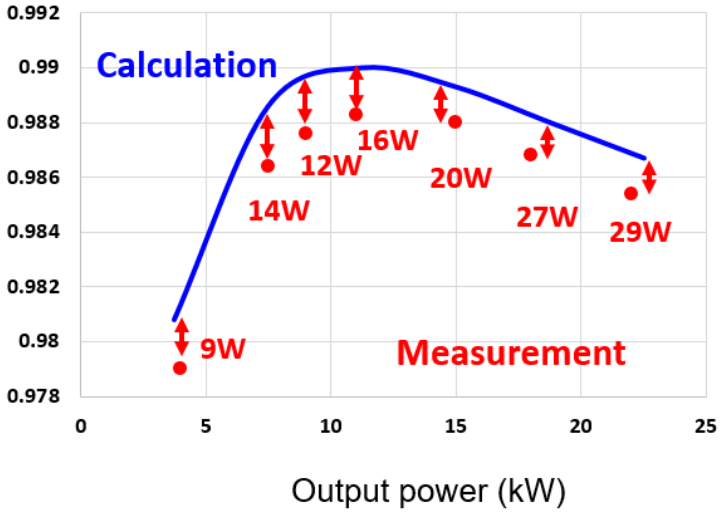


Fig. 92 Test waveform at 22kW

A comparison is made between the constant power control (15kW) and the partial fluctuating power control within a power range of 7.5-22.5 kW. The experimental results for the constant power control at full load are shown in Figs. 86. The black and red waveforms are the gate signals for the primary- and secondary-side devices. The light blue curve and the green curve are the Vds signals for the primary- and secondary-side devices. The orange and blue curves are the current waveforms for the transformer's primary and secondary

sides. With constant power control, the power profile over one-line cycle is a constant value. There is no fluctuation in the waveform.

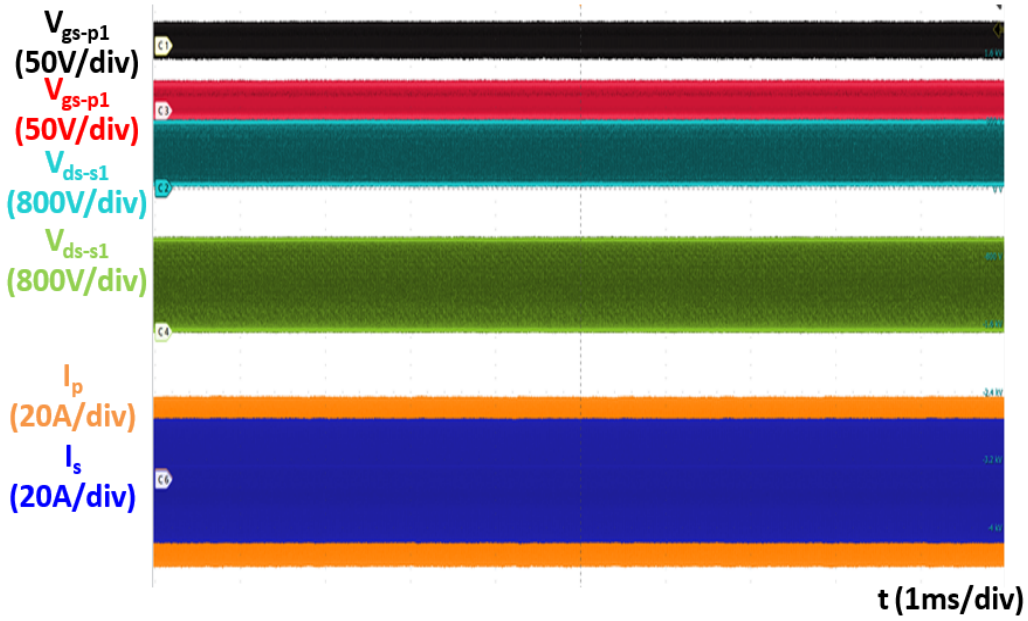


Fig. 93 Experimental waveform for constant power control in a half-line cycle.

Experimental results for the partial fluctuating power control at full load are shown in Figs. 87. From the experimental waveform, there is a 50% fluctuation in power flow in the DC-DC stage. To verify the concept, a huge bus capacitor (1mF) is placed at the output together with the load to absorb the single-phase power ripple. And the output voltage is a constant 1.07kV in the pink line as shown in Fig. 87. The current ripple has a 50% fluctuation compared with the constant power control method.

The tested efficiency is shown in Fig.88, in the light-blue dotted curve for the constant power (CP) control. The blue solid curve is the predicted efficiency based on calculation. Compared with the constant power control in blue, the partial fluctuating power control will have a 0.1% efficiency reduction but with 10% overall converter volume reduction by the decrease in bus capacitors. Compared with the calculated full fluctuating power control (0-30kW) in green, the partial fluctuating power control will have a better efficiency performance. The biggest error between the prediction and the test in the constant power control approach and the partial fluctuating approach are both less than 0.2%. If the measurement error is taken into consideration, the result is pretty close which means the loss model for the partial fluctuating power control is convincing.

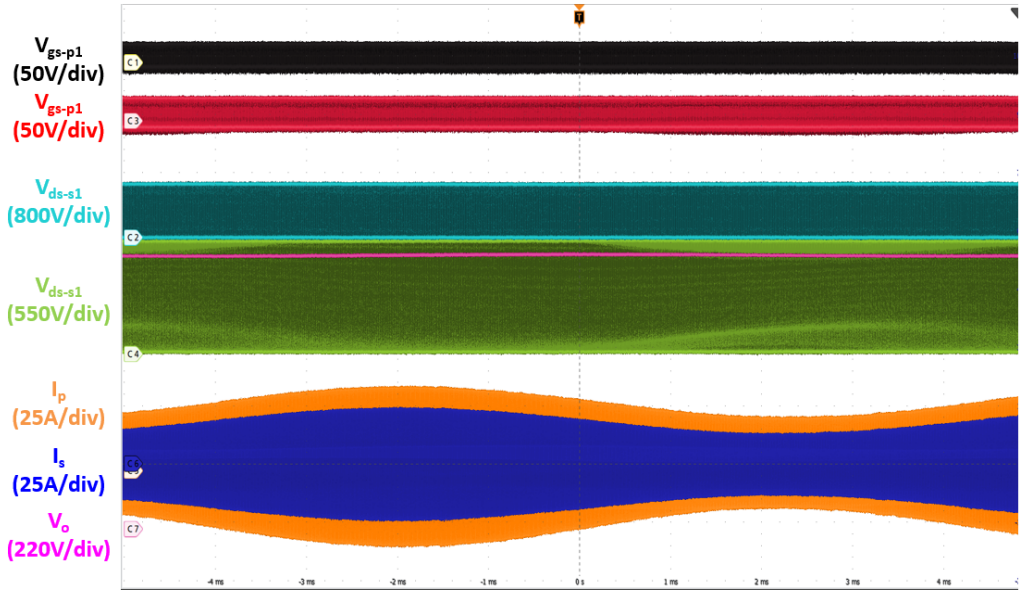


Fig. 94 Experimental waveform for fluctuating power control in a half-line cycle.

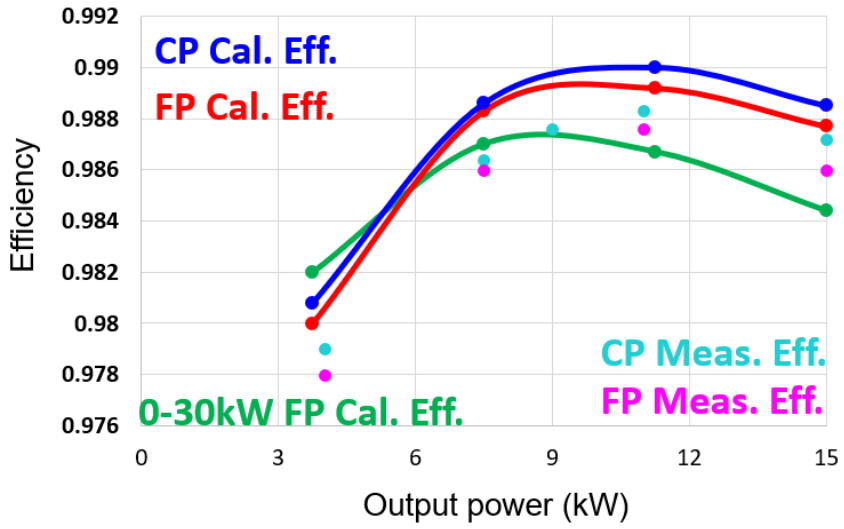


Fig. 95 200 kHz CLLC converter efficiency test result

References

Test Results from NextEnergy's Power Pavilion

For a 13.2-kV medium-voltage application, nine SST power cells in each phase are connected in series for the higher voltage. The outputs of all the power cells in three phases are connected in parallel to provide total 400-kW power to the 1050-V intermediate DC bus. Total 27 cells are installed in three cabinets. The SST also includes an AC input cabinet and a control/DC cabinet. The dimensions of the SST are 3100x1300x2100mm.

The weight is approximately 3000 -kG. It is cooled by forced air. The cabinet is rated for NEMA 3R outdoor usage. Figure I.1.1.4 shows the complete 13.2-kV 400-kW SST.

Figure I.1.1.4 Front View of 13.2kV/400kW SST Design

Three Buck power modules are connected in parallel to handle 500-A 400-kW charging power. The supporting plant includes a control module and a chiller. The dimensions of the power cabinet are 1318 x 1280 x 1432 mm. The weight is 800-kG. It is cooled by forced air with an internal chiller. Figure I.1.1.5 shows the complete 400-kW charger power cabinet.

Figure I.1.1.5 3-D View of the 400-kW Charger Power Cabinet

The dispenser features a 500A CCS1 vehicle charging interface, an LCD user interface and a charging cable chiller. The dimensions of the power cabinet are 600 x 400 x 2400 mm. The weight is 800-kG. It is cooled by forced air with an internal chiller. Figure I.1.1.6 shows the dispenser design.

Figure I.1.1.6 3-D View of the Charging Dispenser

The 400kW power system and supporting infrastructure has been installed at NextEnergy's Microgrid Power Pavilion. This includes a step-up transformer, a 15kV switch, power distribution panels, contactor, surge suppression equipment, and all cabling. Final inspection of the XFC test setup was conducted on September 28, 2020. Figure I.1.1.7 and Figure I.1.1.8 are the pictures of the 400kW XFC setup at NextEnergy.

Figure I.1.1.7 400kW XFC Setup Front View (SST, Charger Power Cabinet, Dispenser, and DCE from left to right)

Figure I.1.1.8 400kW XFC Setup Rear View (DCE Cooling System, Buck charger, SST from Left to Right)

To verify the interoperability charging power, vehicle charging tests were conducted with Chevy Bolt EV, Cadillac Lyriq EV, Volkswagen ID.4, GMC eHummer and Ford Mach-E EVs. Figure I.1.1.11 and Figure I1.1.12 show the pictures of testing with Chevy Bolt and Ford Mach-E, respectively.

Figure I.1.1.11 Charging Test with Chevy Bolt

Figure I.1.1.12 Charging Test with Ford Mach-E

Results

XFC Full System Efficiency Test Result

The function and efficiency of 400kW XFC system was tested at full voltage and power range at total 44 points. The test result matches the design calculation very well. It meets and exceeds the specification. The peak efficiency is 97.6%. The efficiency curves have been reported in last year's report.

The AC input waveforms looks clean. Figure I.1.1.13 shows the typical AC input waveforms. The

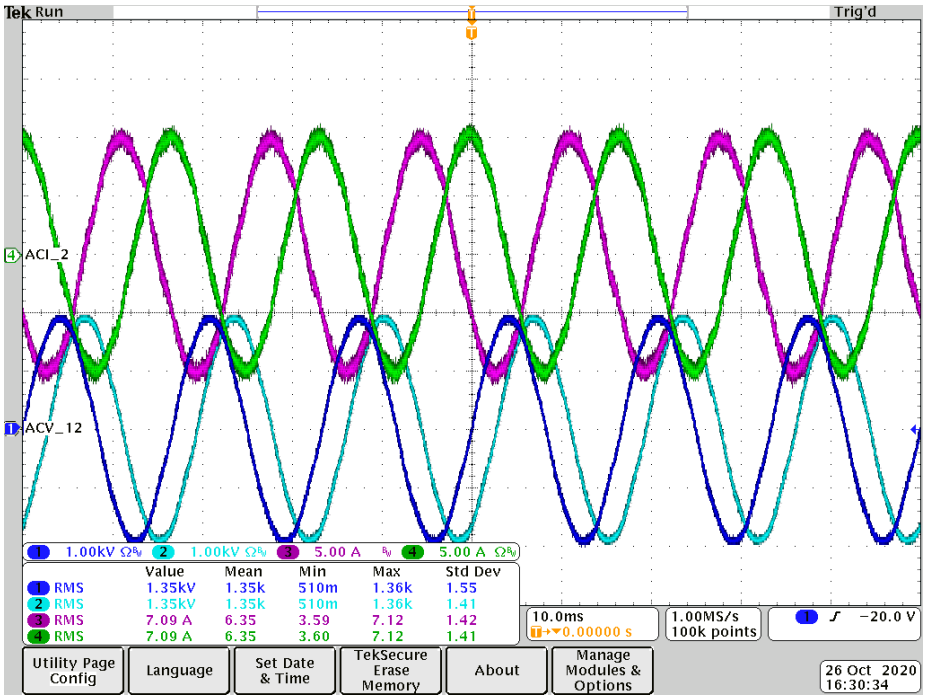


Figure I.1.1.13 AC Input Waveforms (CH1: VAB, CH2: VBC, CH3: IA, CH4: IB)

The power factor is above 95% when input power is above 50kW, and above 99% when the input power is above 100kW. Figure I.1.1.14 shows the power factor vs. input power.

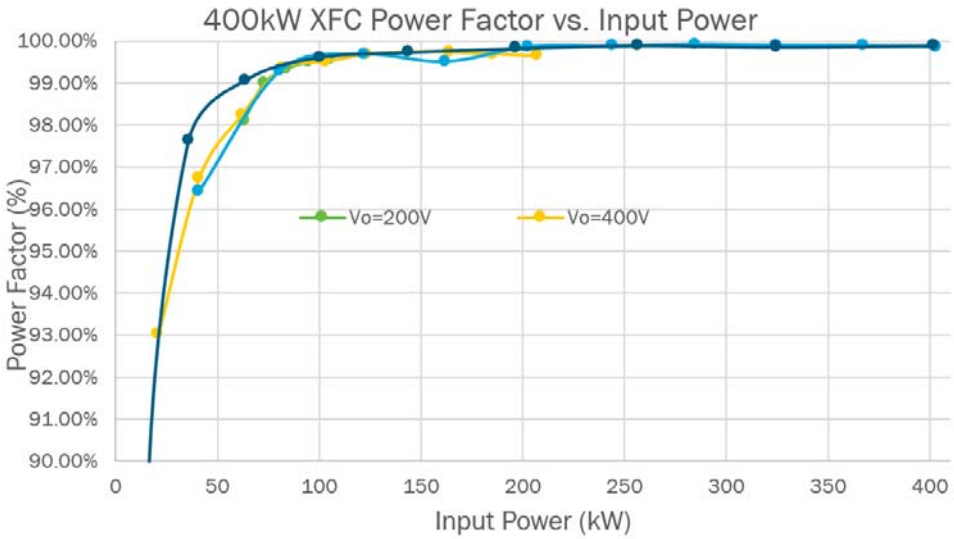


Figure I.1.1.14 Power Factor vs. Input Power

Vehicle Charging Test Result

Vehicle charging tests were conducted with Chevy Bolt EV, Cadillac Lyriq EV, Volkswagen ID.4, GMC eHummer and Ford Mach-E EVs. When charging Cadillac Lyriq EV, the maximum charging current of 500A lasted for approximately 10 minutes, accumulated in 5 sections. This shows that the XFC's maximum charging current exceeds the original objectives.

Conclusions

The test result shows that the 13.2kV 400kW SST, the 400kW Buck charger power cabinet and the dispenser meet the specification. The integration of the 13.2kV 400kWXFC system is successful and the performance of simulated load meets and exceeds the target specification. The program objects of FY 2020 is completely met. The next step is to install an XFC system at DTE site and test full power charging with GM's retrofit vehicle.

Analyses and Testing Results from General Motors

List of Acronyms

ACCM	Air Conditioning Compressor Module
APM	Auxiliary Power Module
BC	Battery Controller
BDU	Battery Disconnect Unit
CAE	Computer Aided Engineering
DCFC	Direct Current Fast Charge
DOE	Department of Energy, Design of Experiments
GM	General Motors
HIL	Hardware-in-Loop
HV	High Voltage
HVJB	High Voltage Junction Box
MIL	Model-in-Loop
MY	Model Year
PIM	Power Inverter Module
RESS	Rechargeable Energy Storage System
SiC	Silicon Carbide
SM	Sensor Module
SS	Solid-state
SSSw	Solid-state Switch
XFC	Extreme Fast Charge

Executive Summary

Fast charging capability is expected to be a key enabler for adoption of electric vehicles by the public. Due to the electrochemical storage of energy in batteries, charging of an electric vehicle is an inherently slower process than refueling of an internal combustion vehicle with a similar range. To achieve fast recharge, a vehicle must have sufficient electric power available from a charger, as well as a battery capable of accepting sufficient power to recharge quickly. For this project, the goal was to achieve a charge rate capable of 50% recharge of the battery within 10 minutes from a low state of charge.

The overall project was led by Delta Electronics, with General Motors as subrecipient being responsible for the vehicle portion of the project which is described in this report. The project developed a 73 kWhr battery pack capable of meeting the charge rate goal of 50% recharge for an automotive traction application. This battery pack was designed to be installed in a large sport utility vehicle which had been previously converted to all-wheel-drive electric propulsion with 400V nominal components. The vehicle was designed to use the combined charging system coupler; however, to transfer the required charging power without exceeding the maximum current limit of the coupler and charger, an 800V charging mode was required. To enable this, the system employed a reconfigurable series-parallel arrangement to provide the 800V charging capability. Since the installed base of charging infrastructure is of both 400V and 800V variety, it is desirable for a vehicle to be interoperable with both types of chargers, and a series-parallel architecture is one way to provide this capability. The system also employed silicon-carbide (SiC) power modules for switching between the 400V and 800V modes. SiC is an emerging technology that may allow smaller, faster switching devices as compared to the typical mechanical contactors which are used for high voltage switching in electric vehicles.

A complete battery pack composed of 4 independent subpacks was built during the project, along with a junction box housing the SiC modules for series-parallel reconfiguration and other mechanical contactors and sensors for power distribution. Both components were tested and characterized, and a detailed electrical model of the system was created based on test data. A control system was also developed for the battery pack, switches, and vehicle under a separate internally project, leveraging GM's existing battery control hardware and software. After hardware characterization, the control system and junction box were integrated with the system model of the batteries, vehicle, and charger, and experiments were performed with the system to investigate the effect of temperature and current limits on charging time and efficiency. Experimental results showed the battery pack to be capable of meeting the charge rate goal when charged at a constant rate of 312A for 10 minutes and exceeding the goal when higher current up to 500A was available from the charger. Separate cases were run with battery cooling system enabled and disabled to investigate the effect of the battery cooling on charging time and efficiency, and it was found that with appropriate thermal conditioning the large thermal mass of the battery pack was able to absorb the heat generated during the short duration of high current charging without relying on the cooling system. Results of the testing are summarized in this report.

Project Introduction

The goal of the project was to develop and demonstrate a vehicle and charging system capable of high power DC fast charging at a 3C rate or greater. GM was responsible for developing and testing a rechargeable energy storage system (RESS) capable of meeting the charge rate target, and then integrating the RESS into a vehicle to support a demonstration of the completed charging system at an installation site in southeastern Michigan.

Battery capacity is typically measured in Amp-hours, which is the total amount of electrical charge required to charge a battery from 0 to 100% of state of charge. "C rate" is a standard figure of merit for a battery that expresses a rate of charge or discharge relative to its capacity. Since this rating is independent of the total energy, it is useful when comparing charge or discharge rates between batteries of different technologies or capacities. "C rate" is also inversely proportional to the time required to recharge a battery as follows: Since a 1C charge rate will recharge a battery completely in 1 hour, it follows that a 3C charge rate will recharge in 20 minutes if the battery is able to accept the current for the entire duration. Allowable charge and discharge rates are generally state-of-charge dependent, with charge acceptance, i.e., maximum charging current, being limited by thermal and electrochemical constraints, decreasing as state of charge increases. Due to this, the rated capacity of a battery is achievable only at very low charge and discharge rates, and the usable portion of the capacity is typically restricted to a fraction of the rated capacity where it can meet the power demands of the application. Due to these limitations inherent in a battery system, it is difficult to achieve a high C rate all the way to the maximum usable state of charge, and metrics for fast charging generally specify a minimum charging rate and charging energy starting at a low state of charge. For this project, the goal is to recharge 50% of total battery capacity in 10 minutes, i.e., 3C rate.

Constraints on DC fast charging power to be transferred to the vehicle can be separated into two types, both of which are important to the vehicle customer; for this project, the goal was to design a system that enabled improvement in each of these areas:

- Constraints that are independent of battery energy or state-of-charge, such as system voltage or current limits; these determine the peak and sustained power requirements for the charging system and, for a vehicle of given efficiency, limit the vehicle range that can be supplied to the vehicle per unit time of recharge

- Constraints that depend on the battery energy on-board the vehicle, such as battery charge acceptance; these are a major factor determining the time to recharge the vehicle from empty to full

This project focused on designing a high-power charging system that also achieved a fast recharge time on the vehicle. For vehicle system design, this presented the opportunity to investigate whether design tradeoffs could be made to take advantage of the fact that a requirement for fast recharge time inherently increases the ratio of power to energy, that is; the demand for power is increased for short durations but reduced for long durations.

Objectives

The project had the following objectives:

1. Vehicle and charging system shall be capable of increasing battery state of charge by at least 50% with a 3C or greater rate of charging.

2. Charging the battery system at a 3C rate shall not require more than 400A.

Approach

GM was responsible for the vehicle portion of the project, which had the following elements:

1. Selection of a cell capable of charging at a 3C rate
2. Design of battery pack (module configuration, thermal and cooling system design, and mechanical design) to meet project objectives
3. Design of electrical mechanization (series/parallel cell and module configuration, high voltage distribution, switching and protection circuitry) to interface to DC fast charger and to existing propulsion components in the vehicle
4. Build and test of components specific to the project
5. Build of a system model to support component design and control system testing
6. System test, including control system and software which was funded by GM under a separate project
7. Vehicle retrofit
8. Support of charger testing, including demonstration of vehicle charging at the final charger site

To ensure that the vehicle portion of the charging system could meet the 3C target, performance requirements were defined for the on-vehicle system as a whole; subsequently requirements were set for the individual components to enable the system to meet high level requirements. As a result of this process, enabling features were identified and implemented in the components making up the charging system. Figure 1 summarizes the enablers implemented throughout the system.

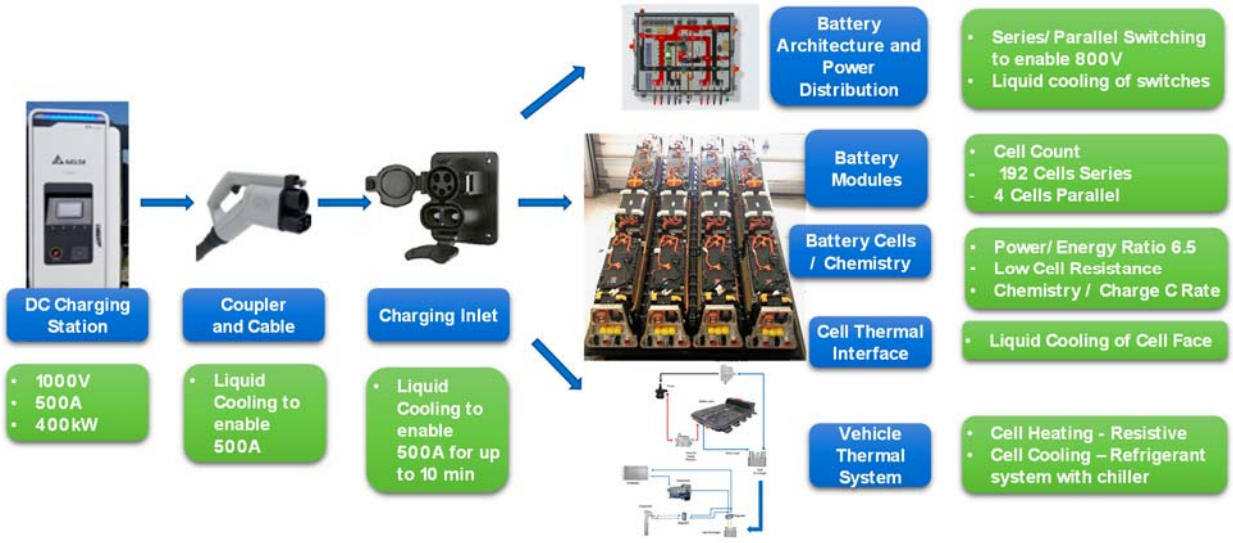


Figure 1: System Enablers for 3C Charge Rate in Extreme Fast Charge Vehicle

Development of the vehicle and components involved the following phases to design, build, and test the system:

- System design, including requirements definition and trade studies to select design concepts
- System optimization and initial performance prediction

- Component build and functional test
- Component high voltage/current characterization testing
- Development of plant model to support control HIL bench and software development
- Integration testing of components with control system
- Vehicle retrofit
- System testing and charging demonstration
- Virtual demonstration of 3C charging rate

System Design

Design of the system began with definition of overall system requirements. Next, a coarse-to-fine approach was taken with trade studies conducted to select concepts and define the components of the system. In the first stage of concept selection, the cell and pack configuration were selected. In the second stage, the battery disconnect mechanization, physical layout in the vehicle, and accessory power / thermal system were chosen, then in the last stage the details of the controller and sensing hardware were defined.

System Requirement Definition

The current profiles shown in Figure 2 were established as a starting point for system design. The minimum required capability, Profile 1 shown in red, was defined based on a maximum charger current of 400A for a charging time of 10 minutes to meet the project goal of a 3C charging rate. Since the DC charger and inlet connector were expected to support up to 500A a second current vs. time profile, Profile 2 shown in blue, was also established to represent the additional expected charger capability for initial thermal design of the RESS, HV distribution components, and charge inlet. The required current beyond 10 minutes was established based on charge test data for one of the cell candidates that had been previously characterized in the lab. Since the number of cells in parallel was not finalized at that time, cell configurations of 3 and 4 parallel cells were looked at in combination with initial charging currents from 300 to 500 amps to determine an envelope profile (Profile 2) with severity at short and long durations to cover the possible range of RESS designs and take full advantage of charger capability. This profile exceeds the minimum required to meet the 3C charging requirement (Profile 1) shown in the chart below.

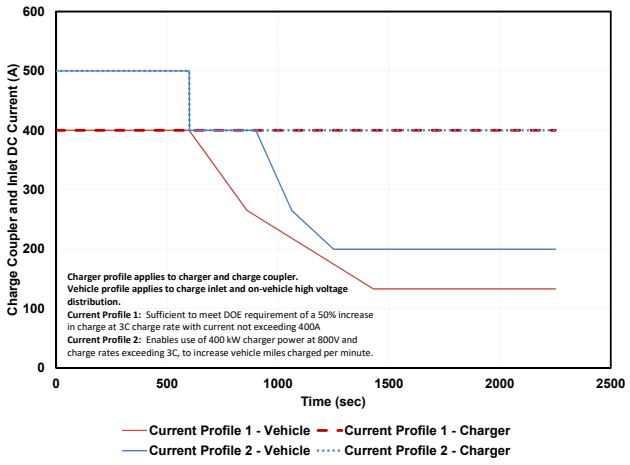


Figure 2: Current Profiles for Vehicle and Charger Design

Key System Design Decisions

During the system design, trade studies were conducted in order to make the key design decisions which are summarized in Table 1. The design criteria and rationale for each of these are described in the following section.

Table 1: Summary of Selected Concepts at Each Stage

1st Stage	**Cell Selection**	LG P2.7 cell (Chevrolet Volt reuse)
	Cell Configuration	768 total cells arranged in a 192 series, 4 parallel cell configuration for 800V charging and 96 series, 8 parallel cell configuration for 400V propulsion and charging
2nd Stage	**RESS Battery Disconnect HV Mechanization**	Reconfigurable concept which can be set up to use either solid-state or electromechanically switch circuits. Includes: 10 electromechanical contactors 2 pre-charge circuits with electromechanical contactors 4 solid-state switches 2 removable bus bars allowing reconfiguration
	RESS Physical Layout	Single layer pack using 4 sets of Volt pack sections arranged side-by-side, with battery disconnect and connectors in upper rear of RESS. Vehicle will be full-size SUV, with RESS mounted in rear. Charge inlet location on right-hand side of vehicle.
	HV Accessories	Dual accessory circuits (APM and Thermal System Compressor) each connected to 400V subpacks during 800V charge
3rd Stage	**Controller and sensing hardware**	Prototype controller acting as master controller interfaced to existing control and cell sensing hardware from the Volt RESS

Stage 1: Cell Selection

Electrochemical Performance Evaluation

Since the Chevrolet Volt was designed as an extended range electric vehicle having lower electric range but equivalent performance requirements compared to a pure electric vehicle, cells from the Volt were looked at as potential candidates for this application. Two feasible cells were identified: LG P2.7 cell (MY 2016-2019 Volt), and a second cell with slightly more energy capacity. A third cell option was investigated but was found to have unacceptable risk for the project. Both candidate cells had been previously characterized at individual

cell level in the GM battery lab for fast charging at high rates. Figure 3 shows the lab test data for the P2.7 cell.

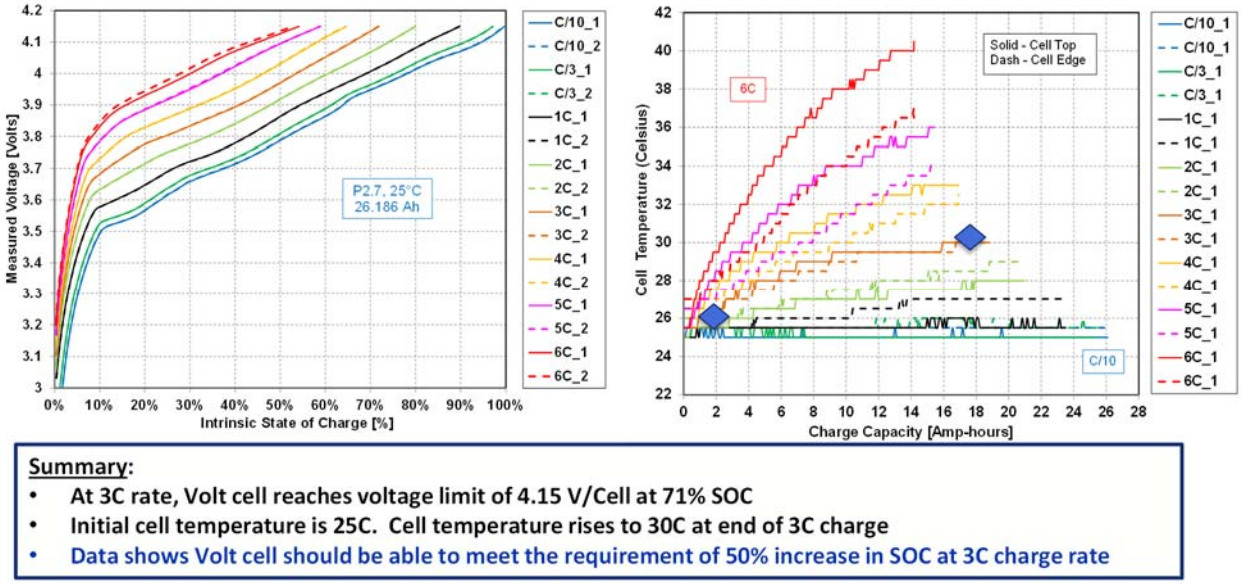


Figure 3: Lab Characterization Test Result of P2.7 Cell for Various Charging Rates

Based on review of the test data, it was determined that:

1. The Volt cell could meet the requirements of the project, with cell test data showing significant margin to meet or exceed the project goal of demonstrating 50% increase in SOC in 10 minutes at a current of 400A or less in terms of headroom to maximum charger current, cell charge acceptance, and cell thermal capability.

2. The second cell candidate showed more temperature rise and reduced ability to accept charge at high C rates. This cell was deemed marginal in terms of being able to meet project requirements.

After the leading concept (Chevy Volt cell in 192 series, 4 cell parallel configuration) was identified, the GM battery lab cell test data was used to develop the charge interface current profiles 1 and 2 to specify RESS, charge inlet, and cable requirements as described in the System Requirement Definition section.

Evaluation of Cell Module Design and Thermal Performance

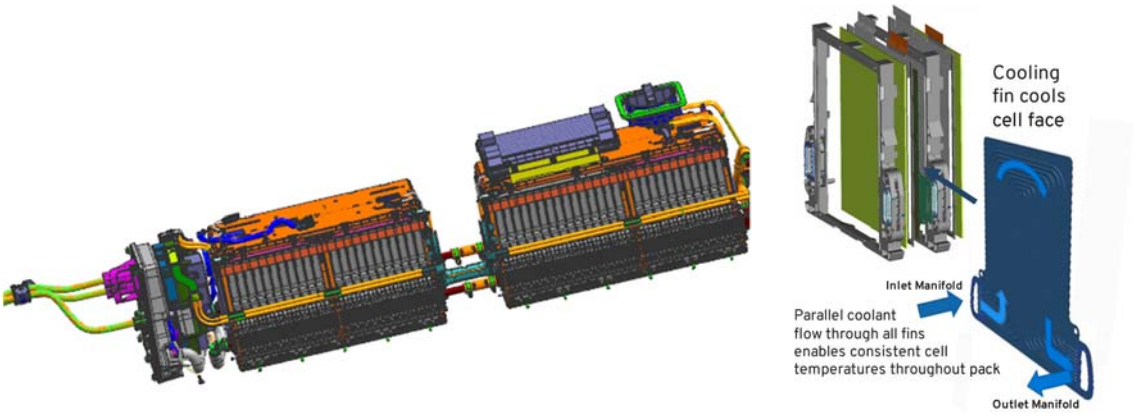
The Chevy Volt cell was designed to be stacked into sections which are liquid cooled, as shown in Figure 4. Coolant flows from the inlet coolant manifold, in parallel through cooling fins stacked between cells, to the outlet coolant manifold. The cooling fins positioned between cells in the stack provide cooling to the cell face, which allows a large surface area for heat transfer.

To assess the capability of the cell-to-coolant thermal interface, a thermal CAE simulation study was run using an existing section model (group of cells with coolant manifolds) which had previously been developed from cell/section test data. The section model was scaled to 768 cells in a 4P configuration. The analysis assumed the following conditions:

- Pack ambient condition: adiabatic
- Inlet coolant temperature: 25C
- Inlet coolant flow rate: 10, 15, 20 LPM

- Pack current: 500A Pack (250A / Parallel Pack String) = 4.8C rate (constant SOC)

Plots of cell temperature from analysis run at 3 different coolant flow rates are shown in Figure 5,



(a) Assembled Modules

(b) Details of Cell Stacking and Coolant Flow

Figure 4: Chevrolet Volt Battery Module – (a) Assembled Modules, (b) Details of Cell Stacking

and the outputs of the analysis are summarized in Table 2.

Table 2: Thermal CAE Analysis Outputs

Design Factor: Coolant flow level	Low	Med	High
Coolant Flow Rate (L/min)	10	15	20
Cell Temperature Rate of Increase (deg C/sec)	4	3.5	3.25
Final Cell Temperature Rise vs. Coolant (deg C)	18	14	12

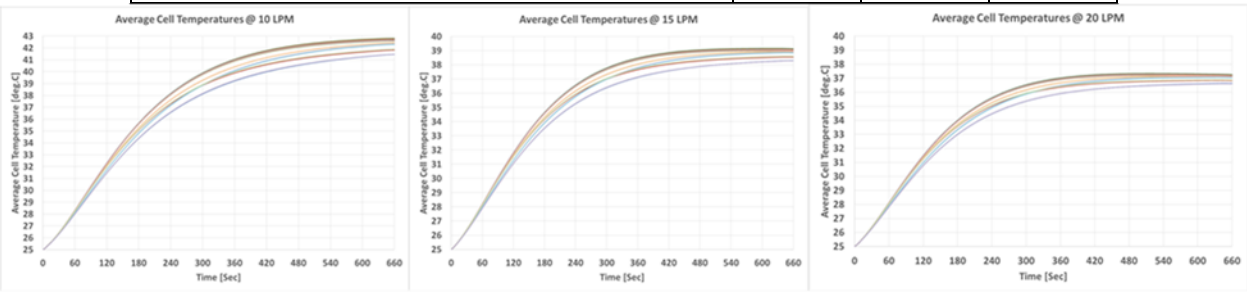


Figure 5: Thermal CAE Analysis Result, Average Cell Temperature vs. Time for 10, 15, and 20 LPM

The following conclusions were drawn based on the study results:

- The cell-to-coolant thermal interface was expected to be capable of removing all heat generated by a 500A total charge current with acceptable cell thermal rise.
- In steady state, the maximum thermally limited steady state charging current would be constrained by the cell temperature limit as well as cell voltage constraints and thermal system cooling capacity. If cell temperature limit were the active constraint, two coolant pumps (10 L/min each) would enable up to a 6 degree C reduction in maximum cell temperature as compared to a single pump.
- At a 3C charge rate, no significant limitation due to RESS thermal system cooling capability was expected within the ten minute charge time to achieve 50% SOC increase. At higher charge

rates up to 500A/4.8C and steady state temperature, the cell heat rejection exceeded the capacity of the liquid cooling system to remove heat from the coolant; therefore, coolant inlet temperature would be expected to rise unless the charging current was reduced.

The LG P2.7 cell was selected for the project based on acceptable electrochemical and thermal performance as demonstrated by the cell test data and thermal analysis. Since these cells were used in the MY 2016-2019 Volt vehicle in a 96 cell in series, 2 cell in parallel configuration, this allowed significant potential to use cells, cell modules, and other pack hardware within the project.

Stage 1: Cell Configuration

Current and Voltage Study

In order to determine the configuration of the cells which would best meet the requirements of the project, arrangements of 2, 3, and 4 cells in parallel and 192 and 240 cells in series were considered. Table 3 shows a comparison of the potential configurations.

Table 3: Comparison of Cell Configuration Options

Potential Configurations with Volt P2.7 Cells	2P 192S	2P 240S	3P 192S	3P 240S	4P 192S	4P 240S
Base Cell Capacity (AH)	26	26	26	26	26	26
Number of Cells in Parallel	2	2	3	3	4	4
Number of Cells in Series	192	240	192	240	192	240
Module Configurations	2 X 96S2P	3 X 80S2P	3 X 64S3P	3 X 80S3P	4 X 96S2P	6 X 80S2P
1C Charge Rate (A)	52	52	78	78	104	104
3C Charge Rate (A)	156	156	234	234	312	312
Max Charger Current	400	400	400	400	400	400
Max C Rate Charger Limited (C)	7.7	7.7	5.1	5.1	3.8	3.8
Charge Energy in 10 Minutes (kWhr)	47.2	59.0	47.2	59.0	47.2	59.0
% of Max Charger Energy Available (66.7 kWh in 10 minutes @ 400kW)	71%	88%	71%	88%	71%	88%
Total Pack Energy (kWhr)	36.8	46.0	55.2	69.0	73.6	92.0
Pack Mass (kg)	362	452	543	679	724	905
Allows Series/Parallel	Yes 2:1	Yes 3:1	Yes 3:1	No	Yes 2:1	Yes 3:1

The selected configuration is a total of 768 cells arranged in a 192 series, 4 cell parallel configuration. This configuration was selected based on mass, charging performance and power, compatibility with vehicle operating voltage ranges, and compatibility with 2:1 parallel switching. Each cell has a capacity of 26 AH, with 4 cells in parallel having 104 AH total capacity. Consequently, the 3 C charge rate current for this RESS is 312A, which meets the requirement of not exceeding 400A. Moreover, because the cell is capable of charging at a rate greater than 3C, the design has the potential of charging at faster rates i.e. >3C, without exceeding the charger current limit.

The cells were arranged into 4 subpacks each consisting of 192 cells connected as parallel groups of 2 cells arranged in series. Each subpack contains the same cell content and arrangement as a pack from a Chevrolet Volt vehicle, which allowed the XFC RESS to be built from Volt pack sections.

In order to utilize sections from Volt packs, the 4 subpacks were designed to be connected in parallel groups of 2 to provide 2 larger 400V subpacks which are then configured in series for fast charging at 800V, or parallel for propulsion or charging at 400V.

Inrush Analysis

To understand the effect of connecting cell strings in parallel, simulations were conducted to model the potential inrush current between two strings of cells which could occur if strings of different state of charge were to be connected together in parallel. The electrical model for the cell was based on

previously characterized cells. Figure 6 shows a comparison of modeled and tested cell open circuit voltage. Overall plant model development is described in more detail elsewhere in the report. A design of experiments (DOE) was conducted to understand inrush variation as a function of cell temperature, state of charge, and state of charge difference between the two strings. From the result it was concluded that the potential inrush current would be within the design range of either solid-state or mechanical contactors available for the system. As shown in Figure 7, the largest inrush occurred at 4% state of charge, and inrush current magnitude was correlated to the voltage difference before closing the switch. The cell charge test data showed increasing open circuit voltage slope vs. SOC between 5 and 10% SOC and very steep slope near 0% SOC. Based on these results, a minimum bound on the initial state of charge for demonstration of the 3C rate was set at 5%.

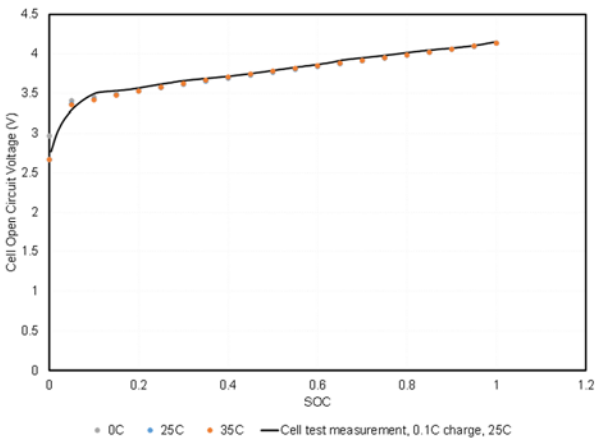


Figure 6: Cell Open Circuit Voltage, Model vs. Test

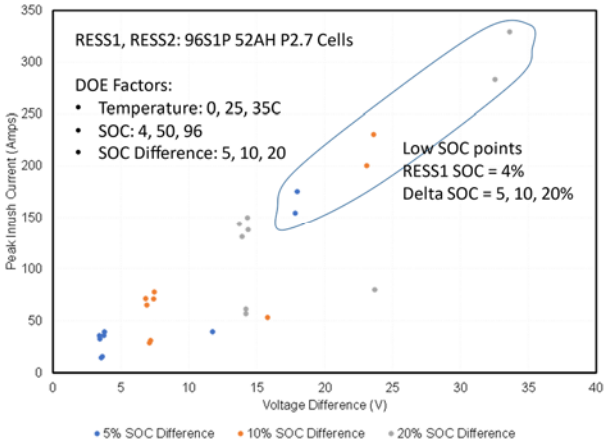


Figure 7: DOE Result, Peak Inush Current

Comparison of Selected Pack Concept vs. Example Electric Vehicle Battery Pack

Table 4 shows the specifications of the selected battery pack concept compared to an example electric vehicle battery pack (published Chevrolet Bolt specifications). The XFC vehicle battery pack trades off energy for power as seen by the higher power-to-energy ratio vs. electric vehicle pack, being about 28% less Whr/kg but 3 times W/kg. The XFC pack also uses about 3 times more cells with a different cooling system to support the higher power density.

Table 4: Specifications of XFC Vehicle Pack Compared to Example Electric Vehicle Pack

Parameter	XFC Vehicle Pack (Chevrolet Volt Modules)	Example Electric Vehicle Pack (Chevrolet Bolt[1])
Battery Energy (kWhr)	73.2 kWhr (100 Whr/kg)	60 kWhr (137 Whr/kg)
Battery Power (kW)	480 kW (656 W/kg)	150 kW (344 W/kg)
Power-to-energy Ratio	6.5	2.5
Battery Mass (kg)	732 kg	436 kg

Nominal Voltage	350V propulsion (parallel), 700V charging (series)	350V
Total Number of Cells	768	288
Battery Chemistry	NMC-LMO	Li-Ion (Nickel-rich)
Battery Pack Cooling	Active thermal liquid cooling, Cooling fin with coolant passages between each module	Active thermal liquid cooling, Cooling fin between each module

[1]Liu, J., Anwar, M., Chiang, P., Hawkins, S. et al., "Design of the Chevrolet Bolt EV propulsion system," SAE Int. J. Alt. Power. 5(1):79-86, 2016

An initial estimate of charging performance, shown in Table 5, was made based on cell data which indicated that the program target of 50% increase in SOC at 3C or greater rate could be met with the proposed configuration.

The selection of battery cell and cell arrangement completed the first stage of concept selection, allowing work to begin on the second stage of concept development focused on electrical mechanization and physical arrangement of cells or cell groups.

Table 5: Initial Estimate of Charging Performance Based On Selected Cell Data

Available Charge Current (Amps)	Equivalent C Rate	SOC Increase After 10 Minutes (%)	Energy Increase After 10 Minutes (kWhr)	Temperature Rise (deg C)
312	3C	50	36	5
400	3.85C	64	47	8
500	4.8C	72	53	10

Stage 2: Battery Disconnect Unit High Voltage Mechanization Selection

Battery Disconnect Unit Requirements

A main goal of the project was to design a system that could operate at 800V for DC fast charging, and at 400V for vehicle propulsion. Since development of a new propulsion system was beyond the scope of the project, the decision had been made during project scoping to use existing propulsion components which were designed to operate at 400V. This required that the system implement series/parallel switching of the two 400V subpacks to realize the desired propulsion and charging voltages. Figure 8 shows the configurations that were needed to support the following 3 required modes of operation:

1. Series DC Charge with Solid-state Switch, 800V

   This mode supported DC fast charge at the necessary voltage and current to charge the batteries at the maximum rate without exceeding voltage or current limits, and was planned to be the focus of the project to be used to demonstrate the project goal of charging at a 3C rate.

2. Parallel Discharge with Solid-state Switch, 400V

   This mode was included to support repeated cycles of charge/discharge testing during development testing. It allowed the two 400V battery subpacks to be connected in parallel and discharged through the charge inlet connector to an external controllable load. This would provide a faster and more convenient alternative than driving the vehicle for the purpose of discharging the battery pack between DC charging tests. This mode also provided the secondary function of being able to equalize state-of-charge between the two 400V subpacks if needed.

3. Independent Drive / On Board Charge Module AC Charge, 400V

This mode was identical in function to the existing vehicle all-wheel-drive propulsion system, which included separate front and rear electric traction drives, each with an on-board charge module for AC charging. This mode was intended for driving the vehicle and also allowed maintenance charging of either of the two subpacks at low power (7.2 kW) through the on-board charge modules. Both systems were controlled by a single control system which controlled front/rear torque split as a means for discharging both subpacks at the same rate. Normally, tractive power was split equally between the front and rear systems to maintain both battery packs at the same states of charge.

The following fail-safe criteria were used to evaluate candidate mechanizations for unacceptable potential single point failures of solid-state or mechanical switches in the system:

1. System mechanization shall not include a single point failure of a HV switch that can cause a short between + and – HV rail, and shall have diagnostics to detect latent faults in HV switches that could lead to shorts.
2. System shall include HV switches to provide 2 independent means of disconnecting the RESS during charging or discharging, with diagnostics to detect latent faults.

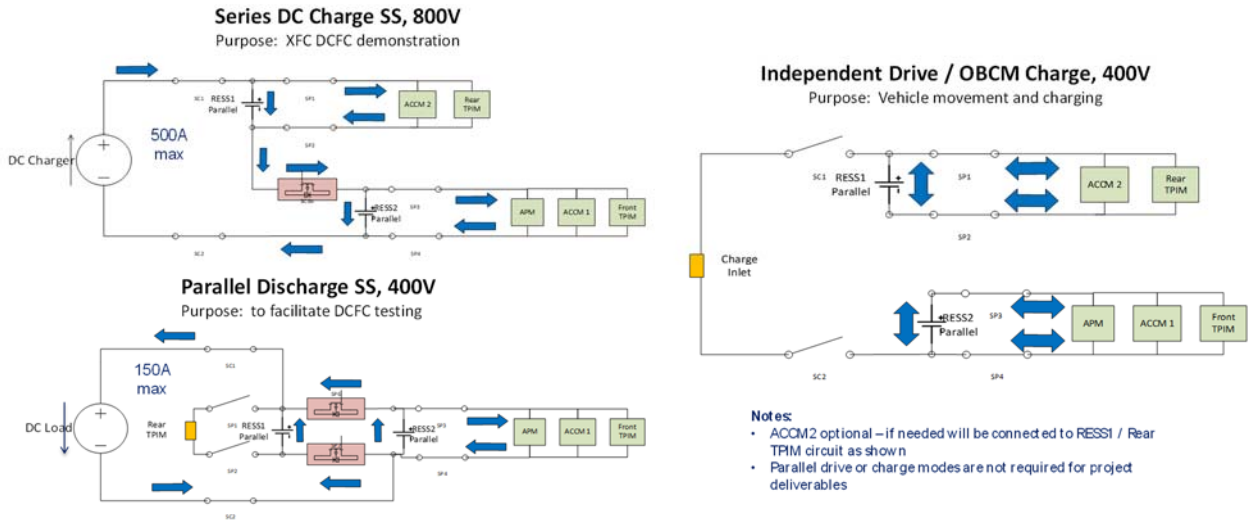


Figure 8: Battery Pack Modes of Operation and Current Paths

To select the mechanization, a trade study was conducted which initially included 10 separate variants. As solid-state switch technology is potentially of interest in battery pack applications, some of the options included semiconductor power modules in place of electromechanical contactors for some of the switch functions. Concepts were first evaluated to ensure they met the fail-safe criteria; in some cases modifications were required. Requirements for solid-state switch modules were defined and reviewed with experts within GM to establish estimates for size, mass, and power loss for appropriately sized modules to allow comparison between solid-state switches and electromechanical contactors. The designs were then evaluated for trade study criteria which included mass/size, part count, hardware availability to meet program timing, technical risk for hardware and controls, power loss and cooling required in charging and propulsion modes. Data was summarized in a Pugh matrix and a weighted ranking was calculated to rank the options.

Out of the initial concepts, several were identified that provided significant advantage in one or more of the trade study criteria. Table 6 shows metrics for 3 of the leading concepts, identified as 1A, 1B, and 2D in the trade study.

- Concept 1A utilized solid-state switches for series/parallel switching and separate mechanical contactors for switching combined front/rear propulsion component and charging circuits. This concept was the smallest and lightest; however, it had high losses during propulsion mode and was also not compatible with the selected accessory power strategy.
- Concept 1B utilized solid-state switches for series/parallel switching and separate mechanical contactors for switching front propulsion component, rear propulsion component, and charging circuits. It had significantly lower losses during propulsion mode than concept 1A and was also slightly smaller and lighter than concept 2D.
- Concept 2D was the best ranked concept overall. Due to using all mechanical switches, it had low losses in both propulsion and charge modes.
- The final selected concept was a combination of concept 1B and 2D which allowed series/parallel switching to be realized via either solid-state switches or mechanical contactors via appropriate switch commands and removable busbars. Technical risk was deemed higher for the solid-state devices due to the earlier stage of development and use of prototype parts, so by implementing an all-mechanical backup option the selected concept mitigates the potential risk due to use of solid-state switches.
- The selected concept implements two solid-state devices in the series path, in order to be able to block current in either direction via use of back-to-back devices. Since there is no requirement for discharging current flow in the 800V series mode, it is possible to use either a diode or a second solid-state switch (SiC MOSFET) to block current flow out of the series connected 800V battery pack. For this project, a semiconductor power diode was used in place of a second SiC MOSFET switch. The diode has a higher voltage offset which produces more power loss at currents and less at higher currents, with a crossover at about 300A. While the diode is reverse biased when the two 400V packs are connected in parallel, it must be provided with sufficient forward biasing current to allow the two packs to be charged in series, which occurs as the charger voltage exceeds the total series-connected battery voltage. During system integration testing, it was found that the diode affected the measured system voltages during initial contactor closure sequence and DC fast charge pre-charge, causing diagnostic-related issues that required changes to resolve.
- Due to issues with availability of the originally selected parts, the junction box was redesigned midway through the project to utilize alternate mechanical switches and driver circuitry to the box. When the box was redesigned, it implemented concept 1B with solid-state switches, and retained the ability to also implement series/parallel switching as electromechanical contactors to provide a lower loss and risk alternative. Figure 9 shows the final mechanization after redesign.

Table 6: Comparison of Leading Concepts for Junction Box Mechanization

Estimates	Part Count for Estimating Mass and Volume					Metrics					
Mass (g)	780	400	450	200	200						
Volume (L)	0.57	0.187	0.187	0.037	0.2						
Concept	Main Fuse	Small Contactors, 250A Continuous	Large Contactors, 400A Continuous	Solid-state Switches	Pre-charge Contactor and Resistor	Total Mass (kg)	Total Volume (L)	AWD Propulsion Mode Continuous Losses @ 255A (watts)	AWD Propulsion Mode Peak Losses @ 835A (watts)	400V Discharge Mode Losses (watts)	800V Charge Mode Losses (watts)
1A	1	0	4	4	1	**3.6**	**1.7**	338	3626	325	575

1B	2	4	2	4	2	5.3	2.8	78	837	575	575
2D	2	0	8	0	2	5.6	3.0	**39**	**418**	**113**	**150**

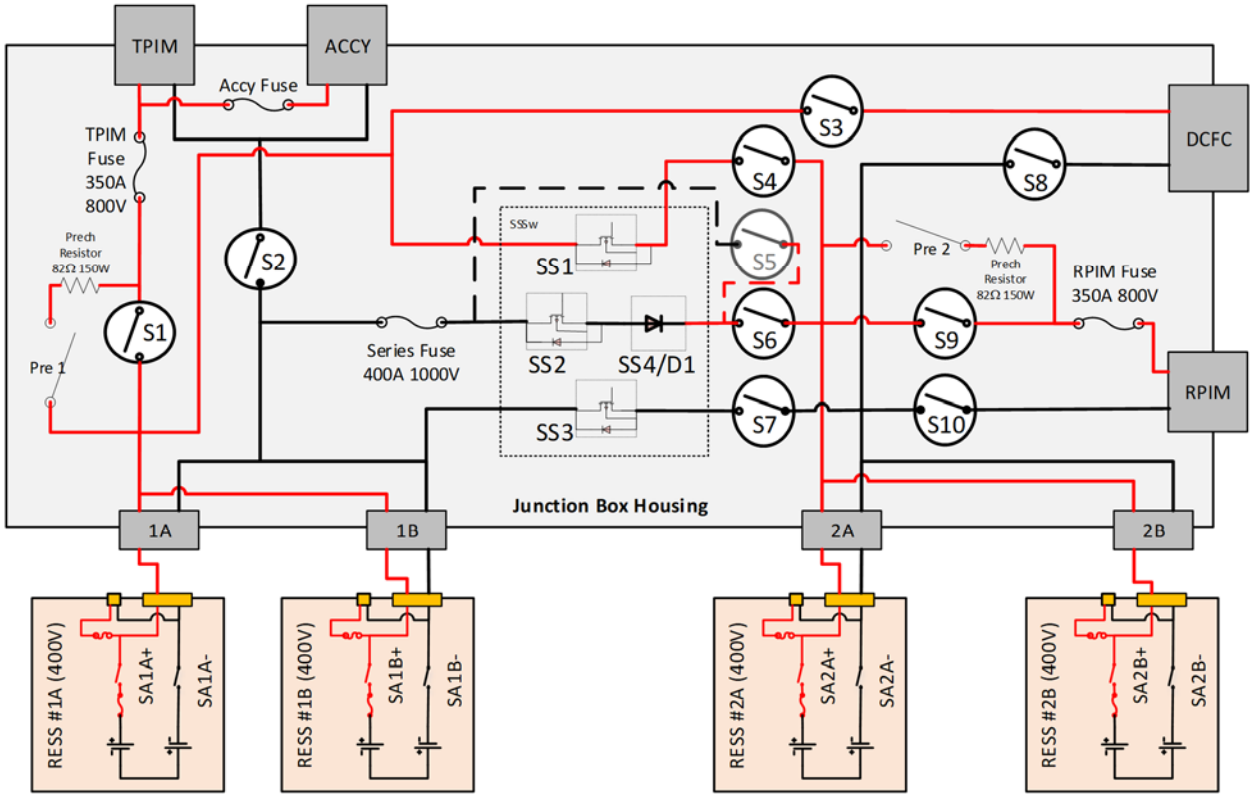


Figure 9: Final Junction Box Mechanization Supporting Solid-State and Mechanical Switching Options

Stage 2: System Physical Layout and Vehicle Packaging

To accommodate the RESS size and mass, a large SUV was planned to be used for the project vehicle, with the RESS mounting in the rear of the vehicle. Based on the selected target vehicle and battery pack concept, the RESS would be constructed from 4 sets of Volt pack sections arranged on a metal platform/frame. The RESS would be constructed on a frame and should accommodate a forklift for installation into vehicle. The RESS should be structurally self-sufficient to allow movement between lab and vehicle for testing. The junction box would mount to the top of the RESS and incorporate connections to the 4 subpacks at the rear of the vehicle. The front propulsion system would connect on the left side of the junction box, the high voltage accessories at the front, and the rear propulsion system at the right rear. The DC fast charge inlet would be installed on the right side of the vehicle to the rear of the passenger door, and would connect to the junction box on the right side near the front of the box.

Both single and double layer concepts were evaluated against decision criteria summarized in Table 7. The single layer RESS layout was selected primarily to reduce project risk due to the simpler design and more straightforward vehicle modifications. Mass analysis showed that the vehicle could meet the rear axle load limit of 2400 kg could be met with the 735 kg RESS installed in the rear offset by removal of the rear seat which removed 40 kg. Figure 10 shows the selected design concept packaged in the rear of the project vehicle.

Table 7: Comparison of Single vs. Double Layer RESS Options

Criteria	Single Layer RESS	Double Layer RESS
RESS approximate dimensions (LxWxH)	2133mm x 1067mm x 406mm	1524mm x 1067mm x 711mm
RESS approximate mass	735 kg	735 kg
Vehicle packaging	Requires removal of 2nd row seat for packaging, requires added bracket to support front	Fits in rear of vehicle
Vehicle mass	Meets overall vehicle mass limit and individual axle mass limits	Meets overall vehicle mass limit but exceeds rear axle mass without modification
RESS complexity	Allows simple, rigid design	Additional frame complexity to support second layer, likely reduced structural rigidity
Other considerations		Poor vehicle handling due to rear weight distribution

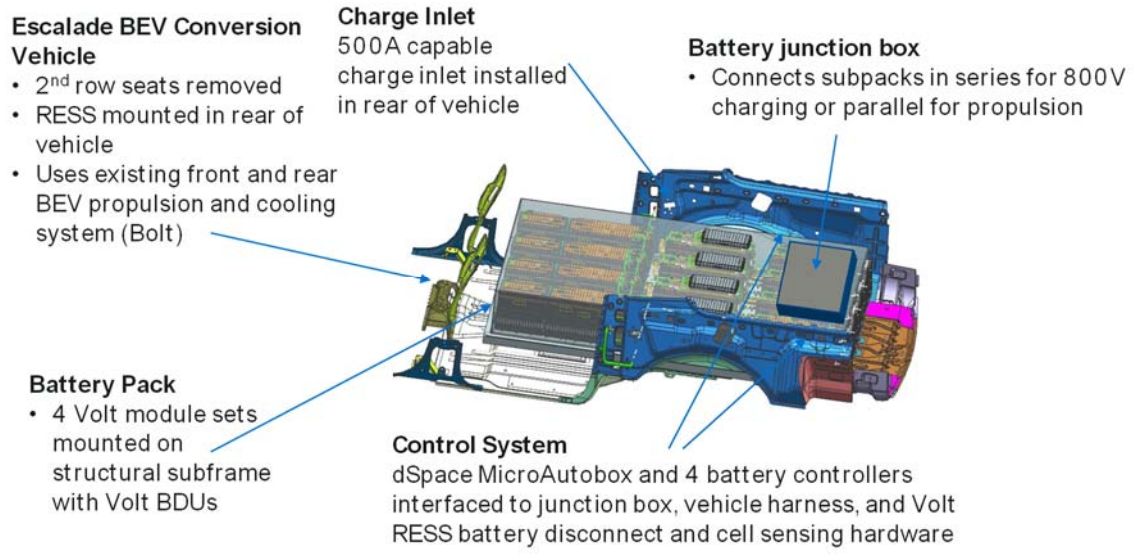


Figure 10: Selected RESS Physical Layout Packaged in Rear of Project Vehicle

Stage 2: High Voltage Accessories and Thermal System

Based on initial steady state thermal analysis, capacity and flow rate of the RESS cooling system was expected to limit the charge rate at high currents and low states of charge. However, transient thermal analysis had yet to be conducted to show that the temperature of the cells would reach the limit before electrochemical limits of the cell became active. Also, the project vehicle had an existing liquid cooling system including compressor and chiller for the batteries integrated with the front propulsion system and had the option of adding a second system to the rear of the vehicle.

The existing vehicle accessories, including 12V DCDC converter and compressor loads, were designed to operate at 400V. Since these were required to operate during DC fast charging as well as 400V charging and propulsion, there was a need to provide power to these loads during 800V charging when the vehicle battery was configured in series mode. Several options for providing HV power to 400V vehicle accessories were considered, and were assessed against the criteria in Table 8.

One option that was considered was the use of AC pins to supply power to the vehicle for accessories. In theory, use of offboard power for accessories via the existing AC on board charger through either a separate AC charge inlet or the unused AC pins on the DC inlet could increase charge rate by about 6%. From a vehicle design perspective, this solution has some advantage as it makes use of AC charging hardware already on the vehicle. However, this option was not pursued after brief investigation since it would likely introduce significant issues with charger interoperability.

Table 8: Comparison of Accessory Power Options

	Accessory Power Options			
Criteria	**Dual Accessories Each Connected to 400V Subpacks**	**Single Accessory Connected to 400V Subpack**	**Separate DCDC Converter for Accessories**	**Offboard Power via AC EVSE and Existing On Board Charge Module**
Accessory Power Available for RESS Cooling and Loads	10kW	5kW	Up to 10 kW	Up to 7.2 kW
Cell imbalance during 10 minute charge	Minimal	up to 5%	Minimal	Minimal
SOC Increase in 10 min @ 400A, 72 kWhr RESS	60.0%	62.0%	59.6%	64.1%
Compatible with existing infrastructure	Yes	Yes	Yes	No, requires additional AC EVSE and action by user
Effect on vehicle	Requires dual accessories	Minimal	Additional DCDC component	Requires additional AC charge inlet

A dual accessory system, with each system connected to 400V subpacks during 800V charging, was selected based on expected RESS cooling benefit and relative ease of implementation with existing BEV components. This choice also retained the option to delete the second compressor later in the project, and in the end only a single cooling system was needed as the more detailed analysis showed that some warming during the initial part of the charging process was beneficial as it increased the charge acceptance of the battery.

Following completion of the 2nd stage of concept selection, the complete high voltage and thermal systems were defined. Figure 11 shows the thermal system, and Figure 12 shows the high voltage components and interconnections.

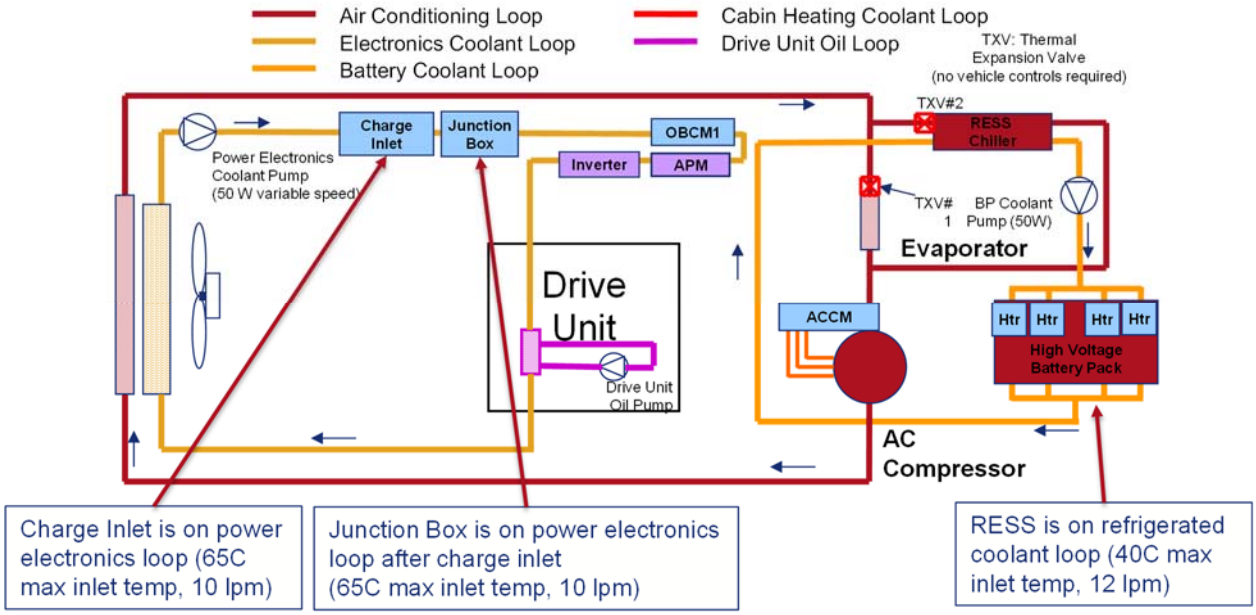


Figure 11: Vehicle Thermal System Mechanization

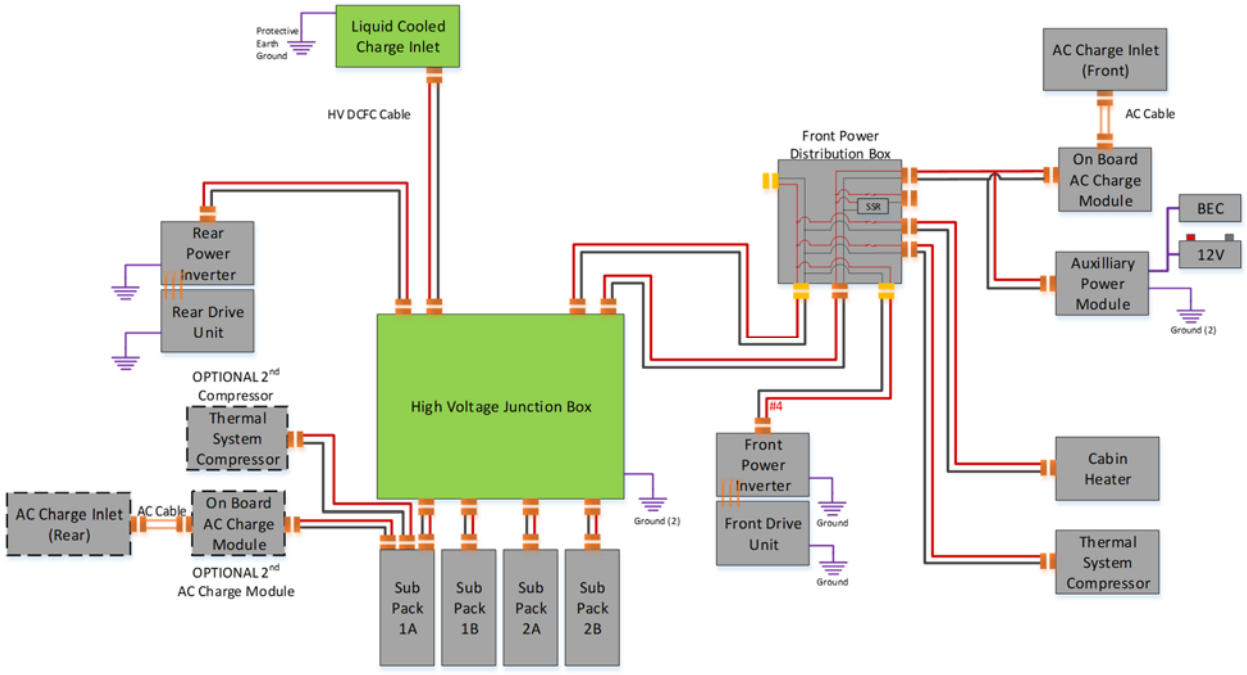


Figure 12: High Voltage Mechanization Diagram Showing Components and Interconnections

Stage 3: Controller and Sensing Hardware

In order to support the required input/output channels for the components in Figure 12, the control system for the DC fast charge hardware and battery pack used a prototype controller (dSPACE MicroAutoBox) acting as master controller interfaced to existing GM battery controllers and cell sensing hardware associated with the 4 battery packs.

Sensor and Actuator Definition

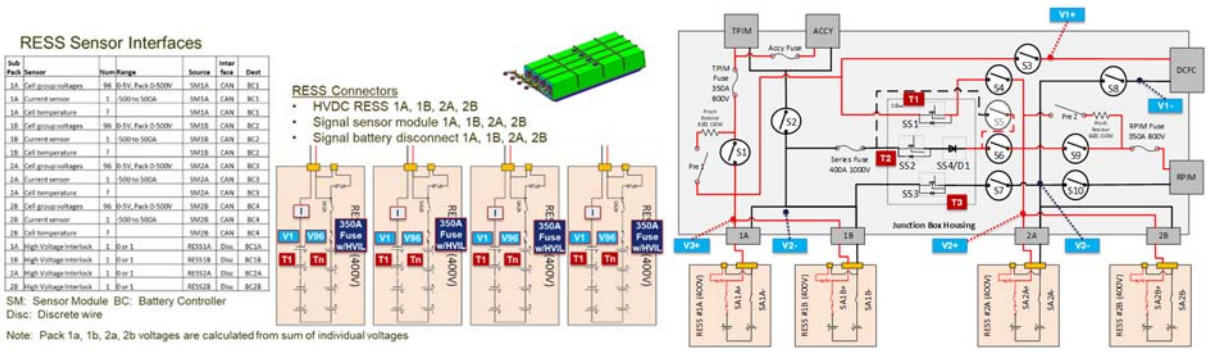
Once all the components had been defined, a list of required sensors and actuators to implement the required control functions and diagnostics was initially defined based on carryover of control system mechanization from existing vehicles which implemented the DC fast charge function, with modification for the specific features of this system such as multiple subpacks. Control signals and interfaces were maintained in a spreadsheet, as shown in Figure 13. A fault analysis was then performed on the system in order to review the system response to loss of function of any component, sensor, actuator, or interface, and to identify any additional sensors required to diagnose failures. An example section from the fault analysis is shown in Figure 14. Battery pack and junction box sensors are shown in Figure 15. The junction box incorporated isolated voltage measurement of subpack 1, subpack 2, and DC fast charge connector voltage. Each solid-state switch module also incorporated a temperature sensor.

XFC	Signal Abbreviation	I/O/G/P/C	Source	Destination
x	Power Ground	G	RESS	Battery Controller
x	Battery Sensor Module Fault Flag	I	RESS	Battery Controller
x	POS Battery Main Contactor	O	Battery Controller	RESS
x	NEG Battery Main Contactor	O	Battery Controller	RESS
x	Battery Pre-Charge Contactor	O	Battery Controller	RESS
x	Control Pilot	I	Charging Inlet	Battery Controller
x	Proximity	I	Charging Inlet	Battery Controller
x	Coupler Temp Sensor (Signal)	O	Battery Controller	Charging Inlet
x	Coupler Temp Sensor (Return)	I	Charging Inlet	Battery Controller
x	Locking Actuator Drive	O	Battery Controller	Charging Inlet
x	Locking Actuator Position Feedback	I	Charging Inlet	Battery Controller
x	Charge Port Door Position Feedback	I	Charging Inlet	Battery Controller
x	Potentiometer (Ground)	G	Charging Inlet	Battery Controller
x	Potentiometer (Signal)	I	Charging Inlet	Battery Controller
x	Potentiometer (Feedback)	I	Charging Inlet	Battery Controller
x	Charge Receptacle Position	I	Charging Inlet	Battery Controller
x	Pump (Enable)	O	Battery Controller	PUMP
x	Pump (Control)	O	Battery Controller	PUMP
x	Coolant Temp (Signal)	I	PUMP	Battery Controller
x	Coolant Temp (Return)	G	PUMP	Battery Controller
x	Coolant Temp (Feedback)	I	PUMP	Battery Controller

Figure 13: Control Signals and Interface Definition Document

			Element Operating States										
Item Number	800V DCFC (SSW)	Function(s) (Responsibilities) NEW COLUMN	EVSE and Vehicle Connection	Coupler Locking Actuator	DC Charge Temperature	DC Charge Temperature #2	Control Pilot	Proximity	Locking Actuator Position Sensor	Impact of Element Fault (Impact prior to any remedial or mitigation actions)	Immediate Resulting State (State of the system prior to any remedial or mitigation actions)	Diagnostic Method(s)	Mitigation Action(s)	System State After Mitigation
	Normal Operation		1	1	1	1	1	1	1	NORMAL OPERATION		NONE	NONE	NONE
1	EVSE and Vehicle Connection	*High Voltage connection between DC Charge Station and Vehicle. Allowing energy transfer*	0	1	1	1	0	1	1	Cannot charge vehicle. Loss of EVSE Connection	Stop Charge	Battery controller detects control pilot	Open HV Contactor immediately	Stop charge
2	Coupler Locking Actuator	*Charging Lock Actuator*	1	0	1	1	1	1	1	Loss of protection. Locking actuator prevents the ability to remove coupler	- Don't engage charging - If charging, no change	Locking actuator position sensor	Stop Charging, then open contactors	Stop charge

Figure 14: Example Fault Analysis of Charge Inlet Functions



(a) Quad RESS Sensor Locations (b) Junction Box Sensor Locations

Figure 15: Sensor Locations for (a) Quad RESS and (b) Junction Box

Embedded Controller Architecture

The embedded controller architecture was primarily defined by the vehicle, which had previously been converted to AWD electric propulsion with independent front/rear propulsion systems controlled by a single driver interface. Although the vehicle originally only implemented AC charge, input/output signals and functions necessary for implementing DC fast charge were available in the controller hardware and software, so no modification to controller hardware was required. However, additional communication links were required in order to implement the interfaces to the new battery subpacks. Figure 16 shows the relevant section of the communication bus network of the vehicle after modification.

Subsystem Requirement Definition

Key subsystem system requirements for the final selected RESS/Junction Box/Solid-state Switch, Charge Inlet, and Control System subsystem concepts are shown in Table 9.

Table 9: Summary of Subsystem Requirements

RESS and Junction Box Requirements Summary

Requirement	Value
Packaging	Volt pack sections in straight line – arranged flat 4X1
Energy	72 kWhr (Total)
Capacity, charge mode	104 AH (charge)
Operating Modes	Propulsion (400V), Charge (800V). Controllable via service mode to allow discharge via external load (400V)
Ambient temp	-40 C to 80 C
Dust and Water Protection	IP6K8/9K
Liquid Cooling	Required, 10 L/min, 25C
Electrical Architecture	Global A

Solid-state Switch Power Module Requirements Summary

Requirement	Value
Packaging	Within RESS/Junction Box assembly
Ambient Temp	-40C to 80C
Liquid Cooling	Baseplate < 80C
Voltage, Series (Parallel)	418V - 803V (259V - 401V)
Charge Current, Series	500A Continuous
Discharge Current, Parallel	100A Continuous, 500A 15 Sec
Maximum Voltage Drop	1V @ 500A
Interface	Low Voltage High Side Drive
Switching Events	> 1M

Charge Inlet Requirements Summary

Requirement	Value
Type	Type 1 combo AC and DC
Ambient temp	-40C to 80C

Control Module Requirements Summary

Requirement	Value
Packaging	Mount to RESS, in Vehicle Interior
Normal Operating Voltage Range	9.0V to 16.0V

Liquid cooling	Required, 10 L/min, 40C
DC Voltage	259 to 803V
Peak DC current	500A for 600 sec
Intermediate DC current	265A for 1062 sec
Continuous DC current	200A for 2250 sec
AC power/current	11kW, 48Arms
Fusing	AC –Yes, DC - No

Ambient temp	-40 C to 80 C
Dust and Water Protection	IP5K2
Electrical Architecture	Global A
I/O Pin Count	68

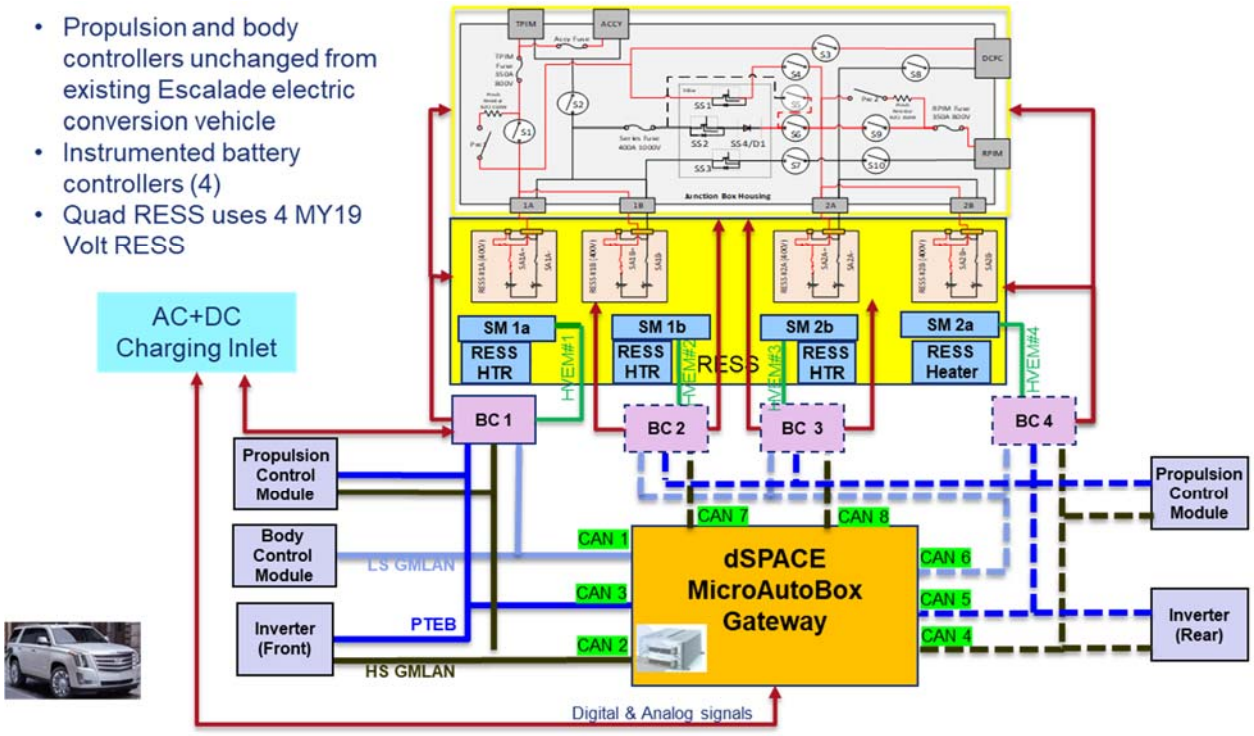


Figure 16: Vehicle CAN Bus Network after Modification for Quad RESS

System Optimization and Initial Performance Prediction

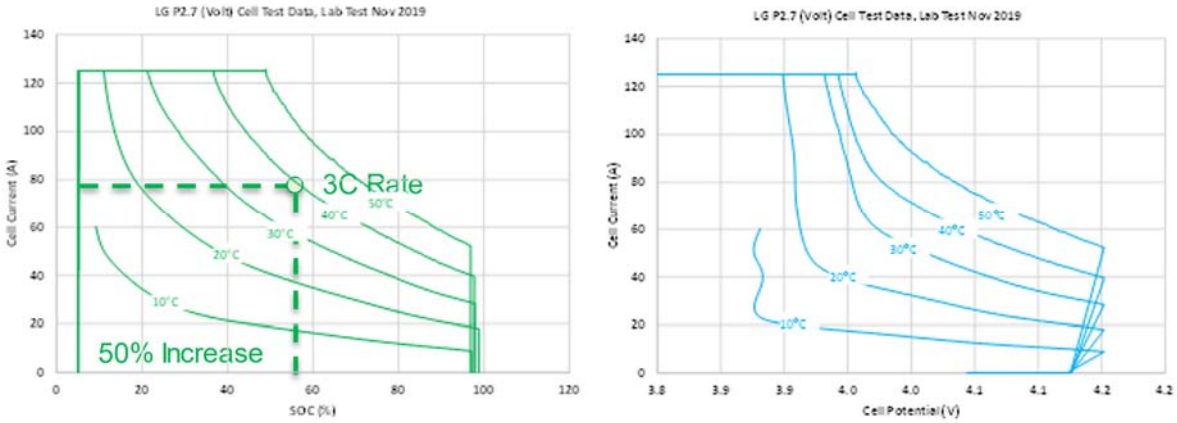
Following completion of system trade studies and selection of design concepts, further characterization testing was conducted on the battery cells to better understand electrochemical constraints and support construction of a model that could be used for predicting and optimizing the charging performance of the RESS.

Cell Characterization to Define Electrochemical Limits

Li plating occurs in Li-Ion cells when charge rate exceeds level allowing all Li-Ions to be intercalated to the carbon anode. If plating occurs, the cell can be damaged, and the onset of lithium plating depends on temperature and the specific cell design. The system charging model uses a map of cell current and voltage limits vs. temperature to define electrochemical operating limits to avoid Li plating during charging. The selected cell was characterized using a proprietary method developed by GM to establish plating voltage and current limits for different temperatures. This data was used to refine the charge control calibration tables in the model and in the embedded control software.

Figure 17 shows how the operating limits of the cell, as established by the characterization test, vary with temperature and state-of-charge. In general, allowable charging current decreases at lower temperature and higher states of charge. Key findings of the test were:

- Charge acceptance of the cells improved significantly in mid SOC band between 25C to 50C. In order to optimize charge performance, cell temperature should increase to at least 40C during the initial high current portion of the charging. A target band of 40C to 50C cell temperature was established for the XFC system to maximize charge performance and meet target of 50% SOC increase at >= 3C rate.
- Starting temperatures below 25C significantly limited charge rate as state of charge increased. In the event of cold ambient conditions and/or low initial battery temperature, the system could use the pack heating function included in the 4 subpacks to increase the cell temperature during the initial part of the charging to increase charge acceptance of the battery.



(a) Cell Current vs. SOC, T (b) Cell Current vs. Cell Potential, T

Figure 17: Cell Test Data – (a) Current vs. SOC and Temp, (b) Allowable Current Vs. Cell Potential

System Modeling and Optimization Studies

A combined thermal/electrical Saber model was developed leveraging previous work on Volt packs and cells for the purpose of predicting and optimizing the charging performance of the RESS. The model included the following pieces:

- Electrical models of the charge inlet, high voltage distribution, electrical loads, and battery pack cells.
- 1D thermal models of the Volt pack cells and sections, charge inlet, battery heaters, and battery cooling system
- Control strategy to control requested charge power and thermal system operation based on cell measurement and temperature feedback

The model was initially developed and run with generic control parameters to check correctness and functionality of the model. Once cell characterization data was available from lab tests, this data was added to the model to accurately represent the intended control strategy. An optimization study was performed to identify the effect of remaining design variables and control parameters on charge time.

Single vs. Dual Battery Cooling Study

As described earlier, the accessory power mechanization and thermal system chosen for the mainstream concept supported a maximum of 2 compressors for cooling the battery pack, with an option to delete one of the compressors if not needed. In order to understand if a single compressor was sufficient to achieve the targeted charging performance, a simulation of charge starting at 5% SOC and 25C initial temperature was run comparing single vs. dual compressor thermal systems as shown in Figure 18.

When comparing the single refrigerated cooling system with 3 LPM per Volt pack to a dual refrigerated cooling system with 6 LPM per Volt pack, the study showed that a single RESS cooling loop with 3 LPM per pack provides adequate cooling to the pack to meet the project targets. Although earlier in the project it was anticipated that a 2nd refrigerated cooling loop would provide benefits to DC fast charge time, this result showed minimal benefit, since the system charges at high rate for only a short time during which most of the heat goes into warming the cells. As the pack SOC increases, the cell current becomes limited due to electrochemical constraints, reducing heat loss to a value within the capability of the single thermal system. The dual cooling system reduced peak cell temperature by only 1 degree C as compared to the single system, and had negligible impact on charging rate. This was consistent with results of the electrochemical testing which had shown that cell heating during the high current phase of charging reduced charging time as long as cell temperature did not exceed the upper limit. Based on results of this study, the single compressor system was implemented.

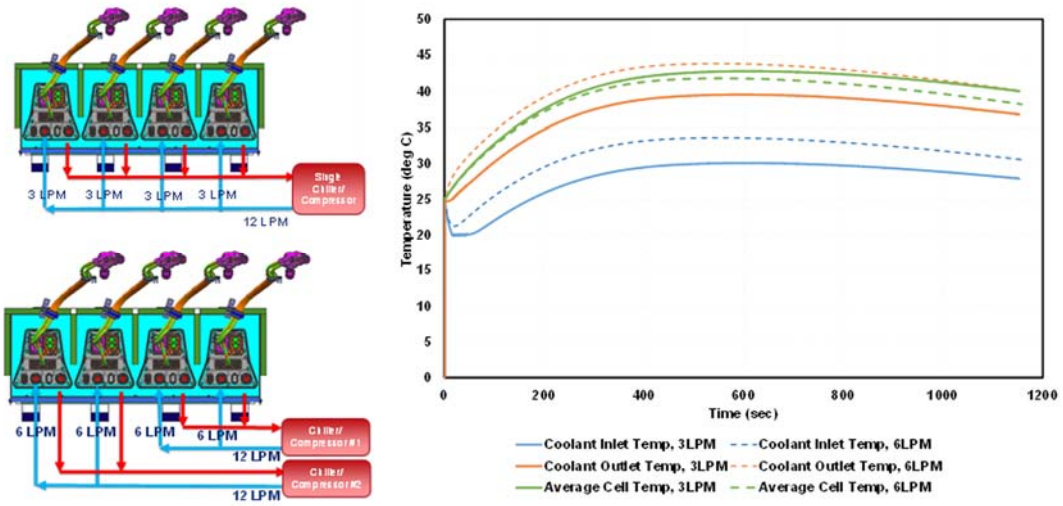


Figure 18: Single vs. Dual Compressor Study Configurations, Temperature vs. Time During Charge

Charge Inlet Cooling Study

Simulations were run to compare alternatives for cooling the charge inlet. The study showed that the charge inlet pins could be maintained below the 75C target for the expected current profile. Example results from the simulations showing temperatures and charger power are shown in Figure 19, which shows temperatures predicted by the simulation for 2 cases: 25C and 32C initial temperatures. The result shows the inlet pin temperature peaks well below the limit of 75C.

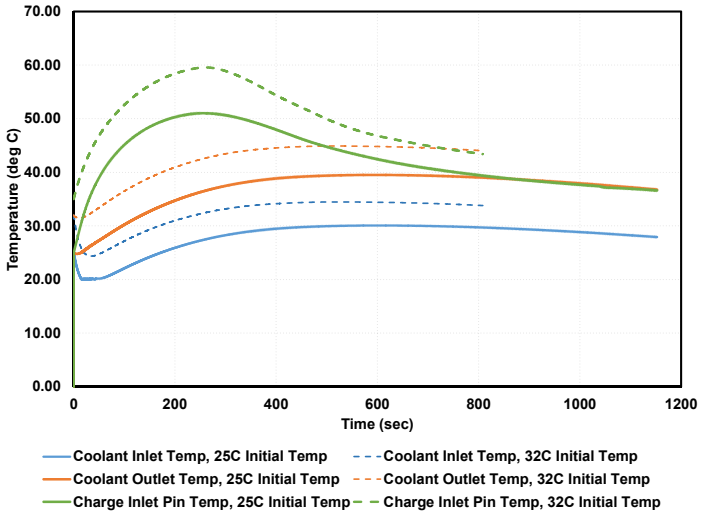


Figure 19: Charge Inlet Pin Temp During Charging, 25C vs. 32C Initial Temperature

Charge Parameter Optimization Study

A design-of-experiments study was run to evaluate the effect of maximum allowed charger current, initial cell temperature, and initial SOC on charge performance and charge inlet pin temperature. The control system was designed to limit charging current if needed to keep the charge inlet pin temperature below the maximum limit of 75C. Study parameters were defined as listed in Table 10.

Table 10: Charge Parameter Optimization Study Design-of-Experiments

Inputs					Outputs						
Case #	Initial Cell T, deg C	Initial SOC	Peak Current, A	Flow per Pack	Charge Time, Min	Energy Gained in kWh			Max Cell Temp (degC)	Max Pin Temp (degC)	End SOC%
						5 Mins	10 Mins	20 Mins			
1	25	5%	500	3	19.2	26.8	46.0	70.3	42.8	51.0	89.0 %
2	25	5%	350	3	22.8	21.3	40.3	64.7	39.4	45.8	91.5 %
3	25	5%	400	3	20.4	24.4	43.8	68.2	41.3	49.0	89.0 %
4	25	5%	450	3	20.4	26.5	45.7	69.8	42.6	50.8	91.0 %

18	**45**	**30%**	500	3	14.4	24.5	40.3	N/A	48.9	53.3	93.1 %
19	**32**	5%	**400**	3	19.2	24.2	45.3	N/A	45.8	53.1	91.9 %
20	**32**	5%	500	3	13.2	29.7	49.9	N/A	48.6	59.6	80.0 %

Conclusions from the study were as follows:

- Initial starting temperature should be about 32C for best charging performance with 400 to 500A current
- Charge performance was expected to meet the target with 25C initial temperature
- Charge inlet thermal performance was adequate to cool the pins with the expected charge current profile and cooling concept, and the charge inlet pins could be maintained well below the 75C target for the full range of initial cell temperature and current limits studied.
- Initial SOC should be as low as possible to provide extended charging at high current. At higher states of charge current will be limited due to electrochemical limits, even if the battery is preheated.

Initial Performance Prediction

Results of the optimization study were used to predict performance of the system. Figure 20 shows the charger power vs. time for 400A and 500A cases. At 400A, the system charge power peaks at about 300kW, and at 500A it is capable of 360 kW for several minutes. Figures 21 and 22 show the charger current, average cell temperature, and state of charge vs. time for 400A and 500A cases, respectively.

In summary, the system is expected to meet the project performance targets. The projected performance against key metrics is given in Table 11 and compared to earlier estimates based on initial cell test data only.

- Comparing 32C vs. 25C initial temperature, the initial cell temperature of 32C was optimal to enable the peak cell temperature to reach the upper end of the 40C to 50C target and maximize the charge power, improving energy delivered in 10 minutes by 3%.
- Comparing 500A to 400A current limit, increasing the allowed current to 500A improved energy delivered in 10 minutes by 4 to 9% depending on the initial temperature.
- A key finding from the study was that the peak charging power was expected to be limited by electrochemical rather than thermal limits of the system, even with a current limit of 500A. This is due in part to the relatively short time the system needs to spend at high current to deliver significant energy when charging at or above a 3C rate.
- Final results of the simulation show that the system charge performance is expected to achieve 53% increase in SOC at a rate ≥3C, exceeding the project target of 50%.

Table 11: Initial Performance Projection

Requirement	Target	Initial Estimate -Cell Data	Refined Projection - Saber Model
% SOC increase at 3C rate	≥50%	60%	53%
Energy delivered in 10 minutes	≥36.8 kWhr	44 kWhr	41 kWhr
RESS Energy	≥60 kWhr	72 kWhr	72 kWhr
Charge Power, Peak (>30 sec)	≥320 kW	350 kW	360 kW

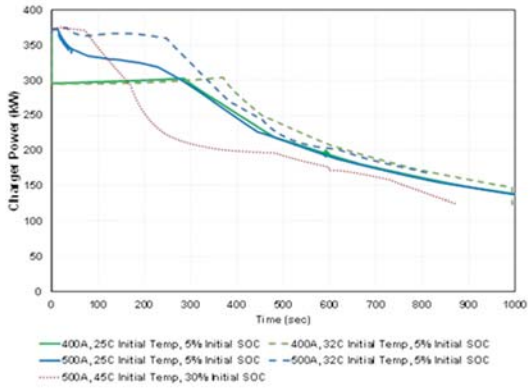
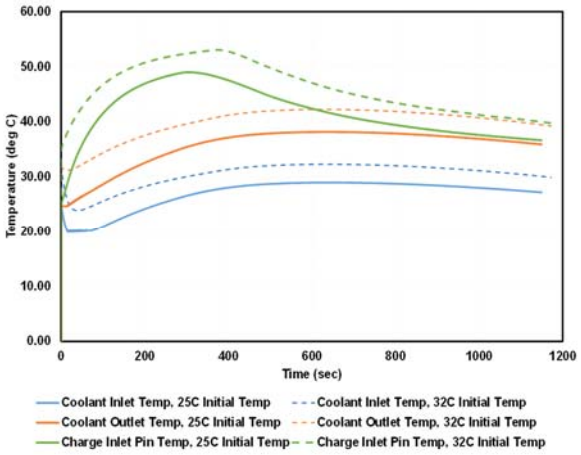
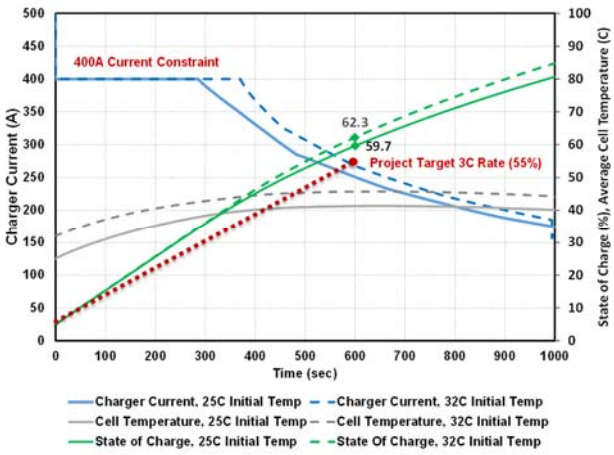


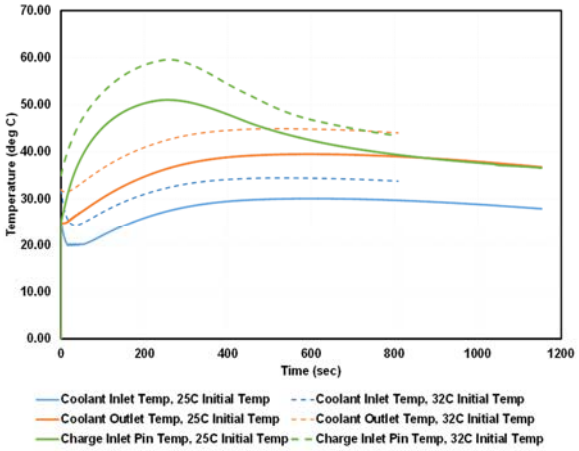
Figure 20: Charger Power vs. Time



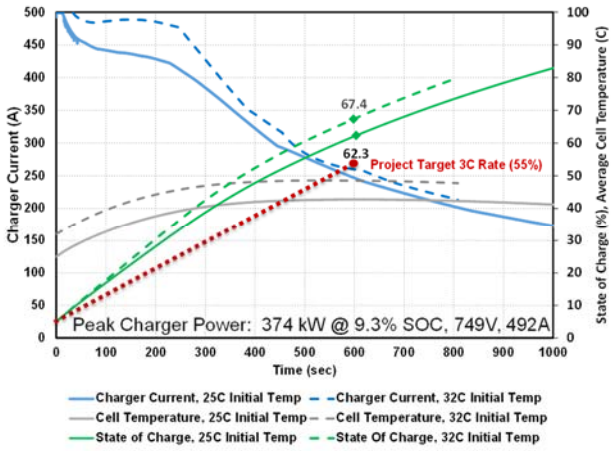
(a) Coolant and Pin Temperature vs. Time vs. Time



(b) Charge Current, Cell Temperature, and SOC vs. Time



(a) Coolant and Pin Temperature vs. Time vs. Time



(b) Charge Current, Cell Temperature, and SOC

Component Design, Build, and Functional Test

The charging and energy storage components that were needed for retrofit of the vehicle are shown in Table 12. After components were sufficiently defined as a result of trade studies, work began to order the components from suppliers and/or order parts as needed to build parts of the system in house.

Table 12: Source of Component and Subcomponents

Component	Source of Component and/or Key Subcomponents
Charge Inlet	Prototype part from supplier, custom HV cable length
RESS	4 MY 2019 Volt Packs procured internally from production build facility Re-orient modules from T to line configuration, mount in quad pack enclosure
High Voltage Junction Box	Initial design of Battery Disconnect Unit - Utilized existing prototype parts from supplier, substituted contactors with increased rating. Final design of Battery Disconnect Unit – Assembled in-house from commercially available parts Solid-state Switch Assembly – Assembled in-house from internally developed power modules and other commercially available parts
Battery controllers	Use instrumented version of existing production controllers, re-use 2 from donor vehicle with additional 6 available from previous projects within GM
Prototype Controllers	Reuse 1 from donor vehicle with additional 1 available from previous projects within GM

Mechanical and electrical design – RESS

Electrical components for the RESS utilized the existing production parts. Some changes were made to interconnecting cables between the modules to facilitate repackaging. The internal component designs were reviewed as needed to ensure adequate margin to meet the required withstand voltage when used in series configuration, and some unneeded components were removed.

The mechanical design for the RESS is shown in Figure 23. Figure 24 shows how the modules from the original t-shaped packs were mounted into the new pack. Design mass of the quad RESS was estimated at 1894 lbs.

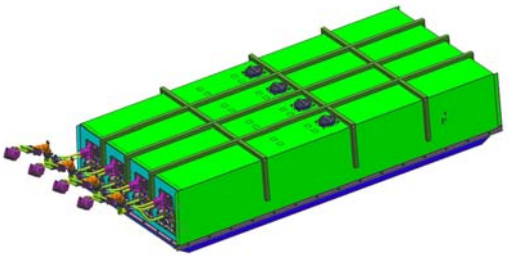


Figure 23: Quad RESS Mechanical Design

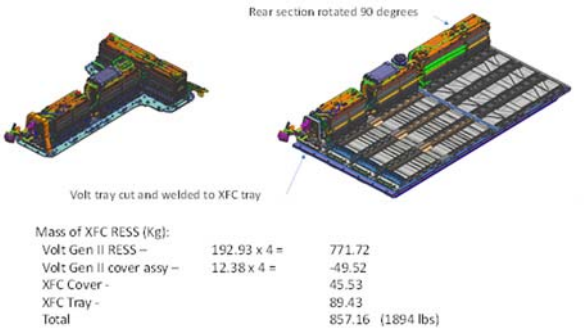


Figure 24: Module Reorientation, Mass Estimate

Mechanical and electrical design – XFC BDU (Junction Box) and High Voltage Hardware

Initial Design Concept

The initial mechanical design concept for the junction box integrated several previously developed parts as assemblies within the junction box enclosure. Battery disconnect switching hardware was based on an existing liquid cooled battery disconnect design, with upgraded contactors to meet increased voltage and current requirements. A solid-state switch assembly consisting of power modules mounted to a commercially available cold plate was packaged between the two disconnect units. Connector locations were established to facilitate packaging and cable routing within the retrofit vehicle. High voltage connections between parts and connectors mounted to the sides of the box were made via lug terminated cables.

Six design options using small, medium, and large coldplates arranged in series and parallel were studied to ensure adequate cooling to the solid-state switch modules while meeting the 10 liter/min flow rate and 30 kPa pressure drop requirements of the cooling system. The selected option utilizing two medium-sized coldplates is shown in Figure 25. This option had the advantage of matching the specified flow rate through the coldplate while minimizing the temperature rise in the coolant from inlet to outlet, and from the coolant to the switch module thermal interface. To avoid exceeding the thermal capacity of the coldplates, the switches are placed such that only one switch on the coldplate is active in a given mode.

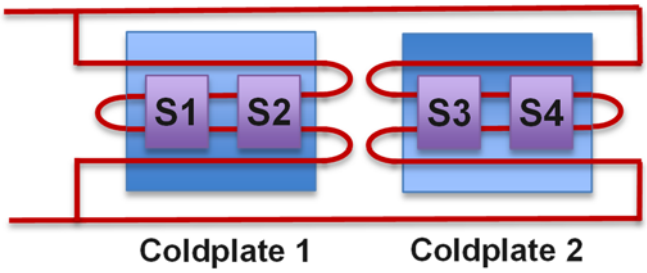
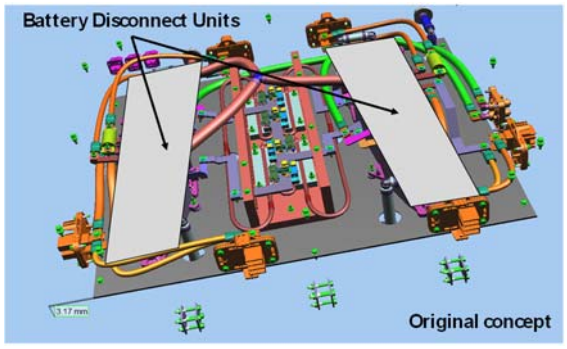


Figure 25: Selected Solid-state Switch Cooling Option



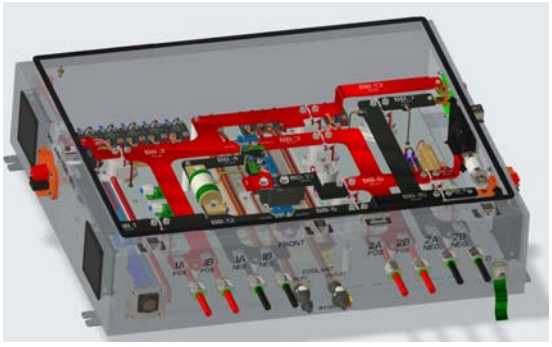


Figure 26: Initial Junction Box Design Concept

Figure 27: Final Junction Box Design Concept

As a result of issues procuring the upgraded contactors from the supplier, the original design concept using carryover battery disconnect hardware was eventually modified to use commercially available fuses and contactors. While the contactors include an integral PWM economizer circuit to minimize driver current during the on state, the higher peak coil current during pull-in exceeded the capability of the controller output driver circuit, requiring additional low voltage solid-state relays packaged in the junction box to actuate the contactors. Due to the higher number of interconnections, custom-fabricated busbars were used in place of cables for connecting the parts. In the new design, a busbar support structure around the solid-state switch assembly was eliminated; however, the rest of the solid-state switch assembly was carried over unchanged. The four RESS cable interfaces were moved to the front of the box and redesigned to use bolted ring terminal connections to the busbars, eliminating the need for RESS connectors. The busbars and mechanical contactors were air cooled, simplifying the liquid cooling circuit to include only the solid-state switch coldplates.

RESS and Junction Box Build and Functional Test

The work of fabricating the RESS enclosure and modification of the vehicle rear compartment were performed in the same vehicle garage facility to allow close coordination and test fitting of the RESS structure before installing live battery components. After fabrication, the RESS tray and cover were transferred to a high voltage laboratory for remaining work which included installation of the cells, wiring, cooling circuit plumbing, and functional test. Functional test was performed using an automated power supply and test system to discharge and charge each of the packs to confirm capacity, cell voltage balance, and function of all sensors and actuators. Figure 28 shows stages of RESS construction, including confirmation of fit with partially built tray installed in the rear of the vehicle, cover fabrication, module installation, completed RESS after functional testing, and results of functional test display with cell voltage balance.

Due to the complexity of the junction box after redesign, fabrication and assembly was performed in a specialized facility for assembly and test of high voltage electrical components. To ensure conformance to specification, each of the power modules used in the design was tested in a characterization fixture before mounting to the coldplate and installation in the junction box. Figure 29 shows the junction box during assembly, after installation of all components, busbars, and wiring. Following assembly, a breakout box with test harness was used to manually verify the function of the voltage and temperature sense channels and confirm function of the mechanical contactors and solid-state switches. After completion of the build the junction box was instrumented with thermocouples at the locations shown in Figure 30 in preparation for thermal testing.

Figure 28: Stages of Quad RESS Build

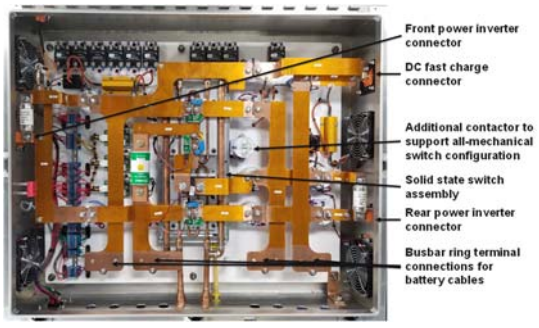


Figure 29: Junction Box After Installation of Components, Busbars, and Wiring

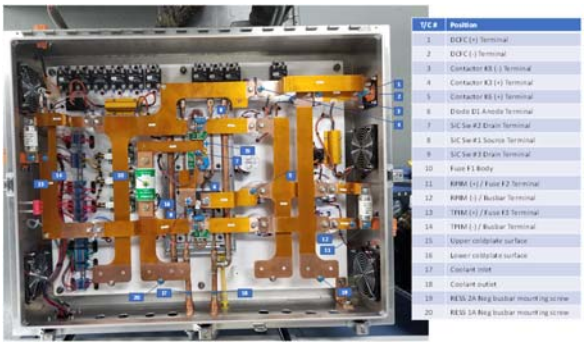


Figure 30: Thermocouple Locations for High Current Testing

Component High Voltage/Current Characterization Testing

Instrumented Thermal Testing with Current Profile

In order to confirm the thermal capacity of the design, the quad battery pack and high voltage junction box were tested to ensure that the temperature of key components remained within limits.

Thermal Testing of Quad Pack

After completion of functional test, the quad battery pack was tested to characterize the thermal response to the expected charging current profile. Each of the 4 battery subpacks was tested individual to verify temperature rise was within thermal limits after occurrence of the current profile based on the fast charging event. Since the test is primarily intended to evaluate joule heating induced temperature rise in cables, busbars, and contactors (not heat generated internally in the cells), a discharge current vs. time profile was used with current equal in magnitude to the charging current profile as determined from simulation with 500A total current and plotted in Figure 32. For this testing, each of the subpacks was instrumented as follows:

- Cell temperatures and all cell group voltages were monitored via CAN bus outputs of the battery sensing electronics
- Thermocouples were installed on manual service disconnect (contains fuse), negative and positive cables between subpack battery disconnect units and cell modules, and negative and positive main contactors. For packs 1 and 2 the thermocouple was installed on the manual service disconnect, for 3 and 4 it was moved to the fuse.
- A thermal camera was used to observe the manual service disconnect cable, positive main contactor, and rear of pack area

The system was operated with liquid cooling, 25C coolant temperature and was stabilized before the test. The RESS was operated without the cover to facilitate measurement with the thermal camera. CAN and analog data was collected in a single file via a data acquisition system. A programmable DC power supply was used to control RESS current to the desired profile.

Key findings from the test were as follows (refer to Figures 31 and 32)

- Measured temperatures within the pack disconnect units, cables, and fuses were within expected limits, consequently fast charging rate is not expected to be limited by heating in RESS power distribution components.
- In the lab test setup, contactors were controlled via an automated test controller that did not include an economizer function (reduction of coil voltage after closure to reduce heating). Contactor temperatures continued to rise moderately after current tapering rather than leveling off or falling as expected, and it was found that this was due to heat generation in the contactor coil. When the system is integrated with the intended vehicle controllers currently in bench verification testing, the system will use an economizer function to reduce heat generation while the contactors are closed.
- After a rest time of 15-20 minutes, RESS component and cell temperatures were found to have cooled substantially and approached pre-test values.

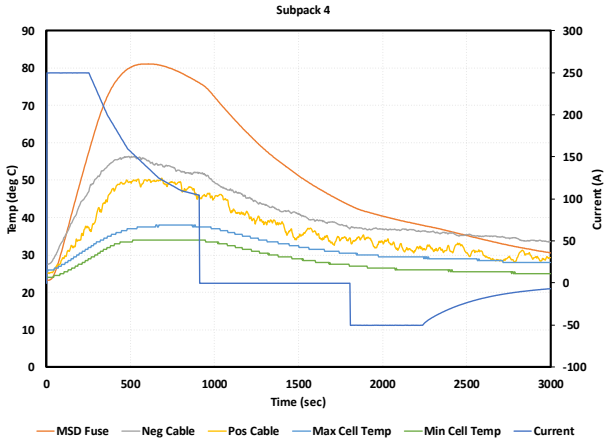


Figure 31 – Subpack 4 component cool-down after end of high current event

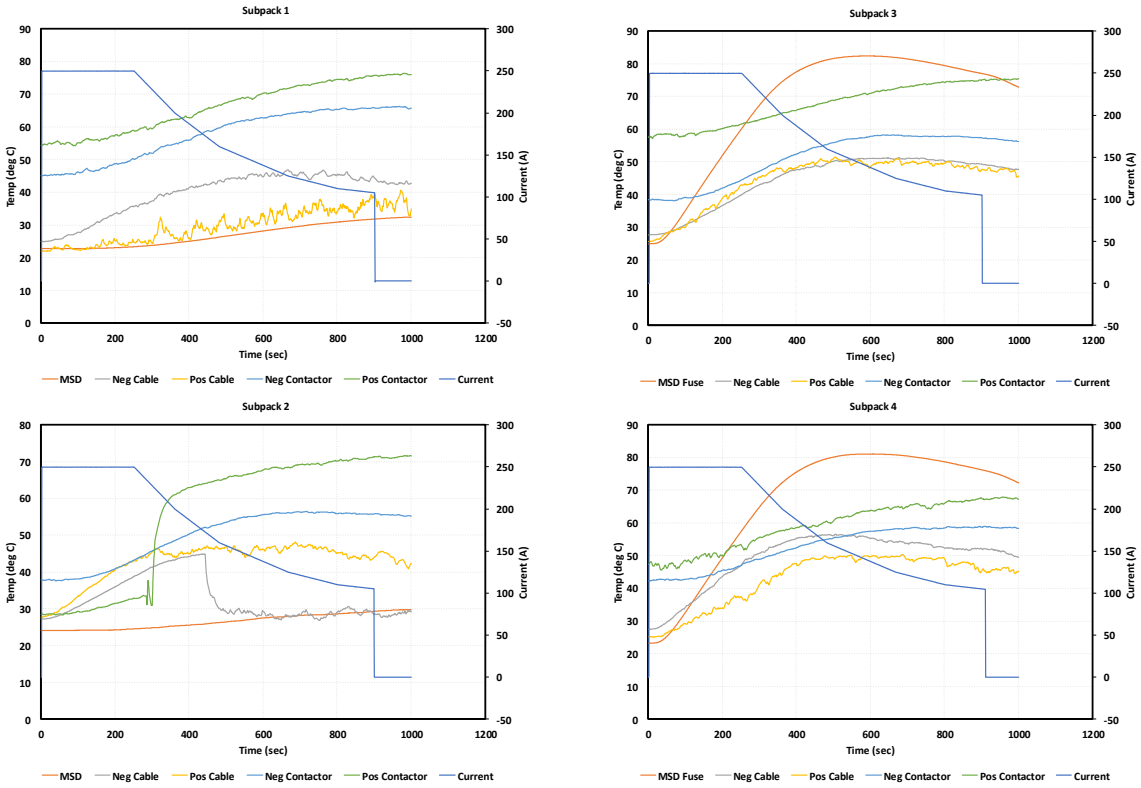


Figure 32 – Temperature rise in thermocoupled RESS components during current profile

Thermal Testing of Junction Box

The following test setup and instrumentation was used for thermal characterization of the junction box:

- A high current controllable DC power supply (Amrel SP10-2700) was used to supply current to the junction box charge inlet connector or battery busbar connection points.
- Charge current was supplied through the charge inlet cable and mating connector representative of that used in the vehicle
- Junction box internal points (20 locations) including connector attachment to busbars, liquid cooling system, mechanical switch terminals, and solid-state switch terminals, were instrumented with thermocouples connected to a Labview instrumentation system as shown in Figure 33 to record temperature rise during the current profiles. This system also recorded internal thermistor and voltage sensor outputs.
- A script was developed to control the power supply and data acquisition system. The system was tested in charge, discharge, and propulsion modes, with the closed switches manually activated via breakout boxes and powered by a 12V/10A power supply.
- The junction box was installed in a thermal chamber for test, as shown in Figure 34. Junction box liquid cooling system was connected to a Julabo 5kW chiller with 7LPM flow and 25C inlet temperature.
- A total of 5 tests were performed, including charging mode, front and rear propulsion modes, and 2 discharge modes covering both directions of current flow possible through the solid-state switches in the circuit.

Key findings from the testing were as follows (refer to Figures 35, 36, and 37):

- The liquid cooling system primarily cools power semiconductor devices, with other busbars, fuses, and connector terminals being primarily cooled by air circulation. Power removed by the liquid cooling system was calculated from coolant flow rate and measured temperature rise between outlet and inlet, and highest power was found to be 333W, occurring during the 500A portion of the DC fast charge test.

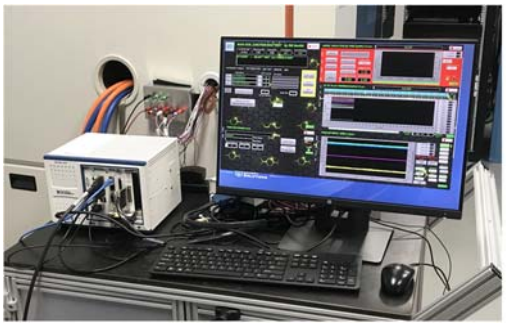


Figure 33: Data Acquisition System

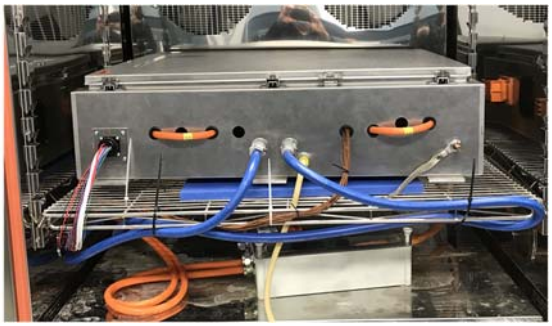


Figure 34: Junction Box in Test Chamber

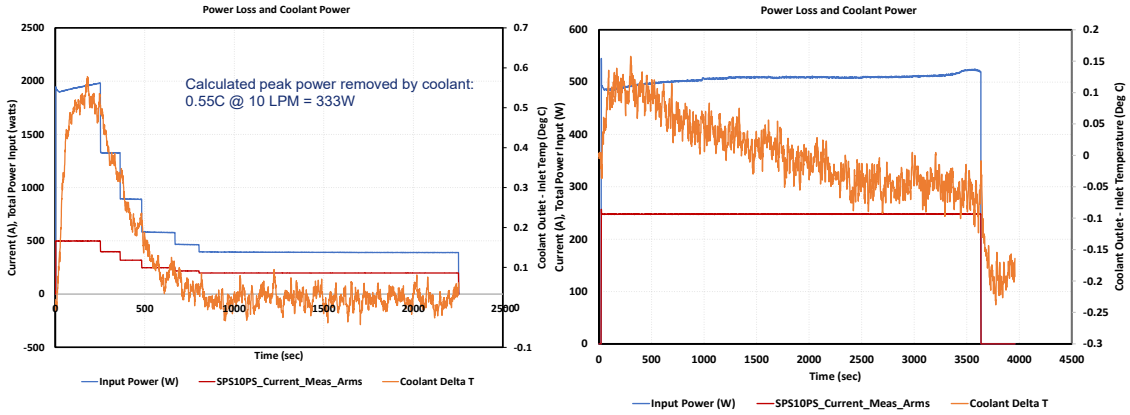


Figure 35: Charging (left) and discharging (right) current and coolant temperature

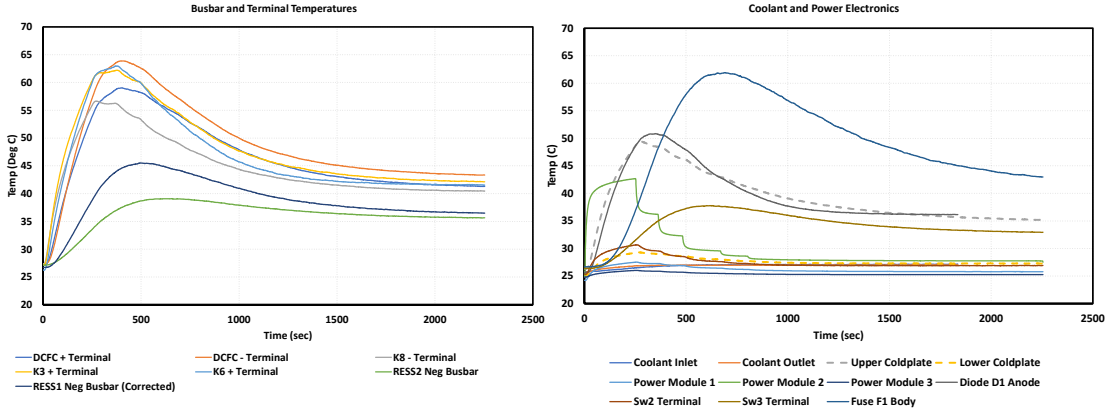


Figure 36: Charging mode temperatures (left-busbars, right-power electronics)

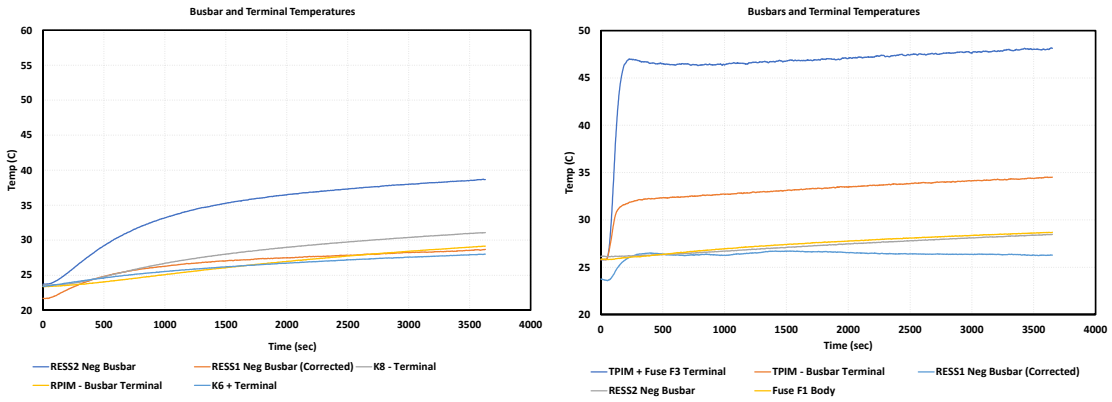


Figure 37: Discharging mode (left) and propulsion mode (right) busbar temperatures

- Liquid cooling power during the tapering portion of the fast charge test, as well as the discharge test, was much lower on the order of 50W.
- Measured temperatures were within expected limits, consequently fast charging rate is not expected to be limited by heating in the junction box components. As expected, charging mode has the highest thermal load and results in the highest peak temperatures. Temperatures in the discharge and propulsion modes resulted in lower temperatures due to lower peak and average currents.
- After reduction of current, temperatures approach final steady state values and stabilize within about 20 minutes.

Withstand Voltage Testing of Junction Box

To ensure voltage withstand capability, the junction box was tested per the specifications in Table 13. Figure 38 shows the test setup. To avoid damaging the voltage sensing circuitry which included high value resistances between busbars and chassis ground, the box was first tested at condition 1 with sense leads in place and condition 2 with sense leads grounded to chassis. In condition 1, the measured leakage current matched the expected leakage current through the sensing resistances, and in condition 2 the leakage current was below the measurement capability of the test equipment.

Table 13: Withstand Voltage Test

Parameter	Condition 1 Test	Condition 2 Test
HV Sense Leads (6 leads)	Connected to busbars	Disconnected and grounded to chassis
Duration	60 sec	60 sec
Withstand Voltage	1000 VDC	2600 VDC
Maximum Leakage Current allowed:	400 uA	52 uA
Maximum Leakage Current observed during test:	190 uA	<10 uA

Figure 38: Withstand Voltage Test Setup

Development of Plant Model to Support Control HIL Bench and Software Development

Early in the project the decision was made to implement a model of the battery pack, junction box, DC charger and charge inlet, and other components on the high voltage bus to facilitate testing of control software algorithms and hardware. This model was implemented in Matlab/Simulink, was separate from the Saber model used for early performance prediction and system optimization. Some of the features of the model are shown in Figure 39. Two configurations of the model were developed to support system and controls use cases and are compared in Table 14. The Model-in-Loop (MIL) configuration was used during system design phase for analysis of parallel contactor closure battery inrush and for other detailed analysis of contactor sequencing later in the program, while the Hardware-in-Loop (HIL) model was integrated with existing models of other vehicle controllers and used throughout the program to simulate vehicle or system operating conditions for software and controls development and system testing.

Table 14: Model-in-Loop and Hardware-in-Loop Configurations of System Plant Model

Configuration	Execution Rate	Host Platform	Control System	Charge System Plant Model Fidelity	Use Case
Model-in-the-loop (MIL)	Continuous time step, non real-time	Windows PC, Matlab/ Simulink	Simplified behavioral model	Detailed circuit models, Simscape	System requirements and design, detailed analysis of short-term events
Hardware-in-the-loop (HIL)	Discrete time step, real-time	dSpace prototype controller	Actual vehicle software and controllers	Simplified circuits with lumped loss models, Simscape	Software development, software and system tests, full charge simulation

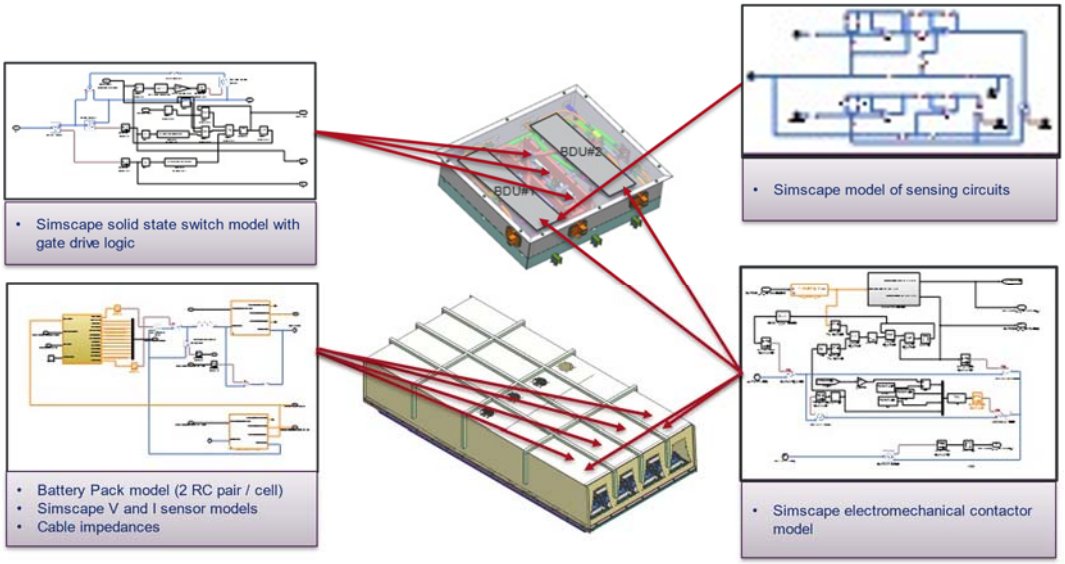


Figure 39: Details of RESS and Junction Box Plant Model Implemented on HIL Bench

Plant Model Verification

During development, parameters for the battery pack and junction box electrical and thermal models were updated based on test data from the cell tests, quad battery pack thermal characterization, and junction box thermal characterization tests. Figure 40 shows cell temperature predicted by the plant model with initial and updated parameters compared with hardware measured data. Figure 41 shows the overall voltage drop in the junction box model broken down into MOSFET, Diode, and remaining circuit resistance, compared with total voltage drop measured during the characterization test.

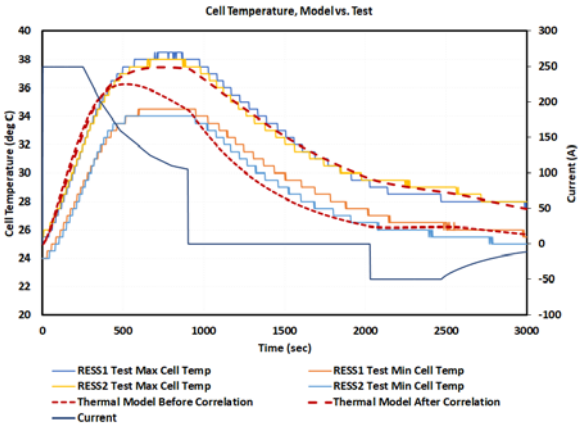


Figure 40: Cell Temperature, Model vs. Test

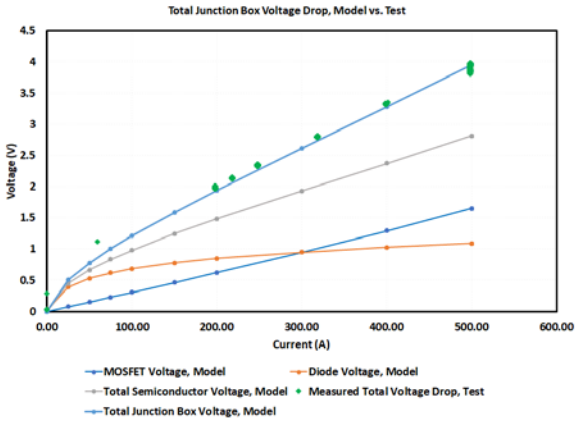


Figure 41: Voltage Drop, Model vs. Test

Integration Testing of Components with Control System

Bench verification testing was completed in two phases, both utilizing the HIL plant model.

- Phase 1 of the testing confirmed the communication and interfaces utilizing a single battery controller.
- Phase 2 of the testing confirmed the communication and interfaces for the full system setup consisting of prototyping gateway controller, 1 primary and 3 secondary battery controllers

After verification of the bench test environment, the following functional testing of DC fast charge features was performed:

- Test of the 3 modes of operation, including series charging, parallel discharging, and independent propulsion modes. After completion, the HIL plant model was revised to incorporate changes to the HV junction box circuit associated with redesign. The system was then regression tested with the revised plant model representing the final design.
- System integration testing of controller system with the DC charge inlet including testing of sensor and actuator interfaces (temperature sensing, locking actuator and position feedback, proximity and control pilot signals) and control functions.
- After completion of the junction box build and component test, contactor sequencing and diagnostics for the 3 modes of operation was tested to confirm functionality with the hardware. Figure 42 shows the final configuration of the bench test environment including HIL model running on second MicroAutobox controller. This configuration had the flexibility to use either low voltage batteries and controllable power supply in place of actual cells and charger, which was used to confirm the contactor functionality and diagnostics, or with the system voltage and current based on HIL model, for testing of charge and discharge modes with representative batteries.
- Integration testing of the control system with the hardware junction box identified an interaction between the series switching diode and the contactor closure diagnostics. A hardware change for resolution of the issue was identified, tested and implemented.

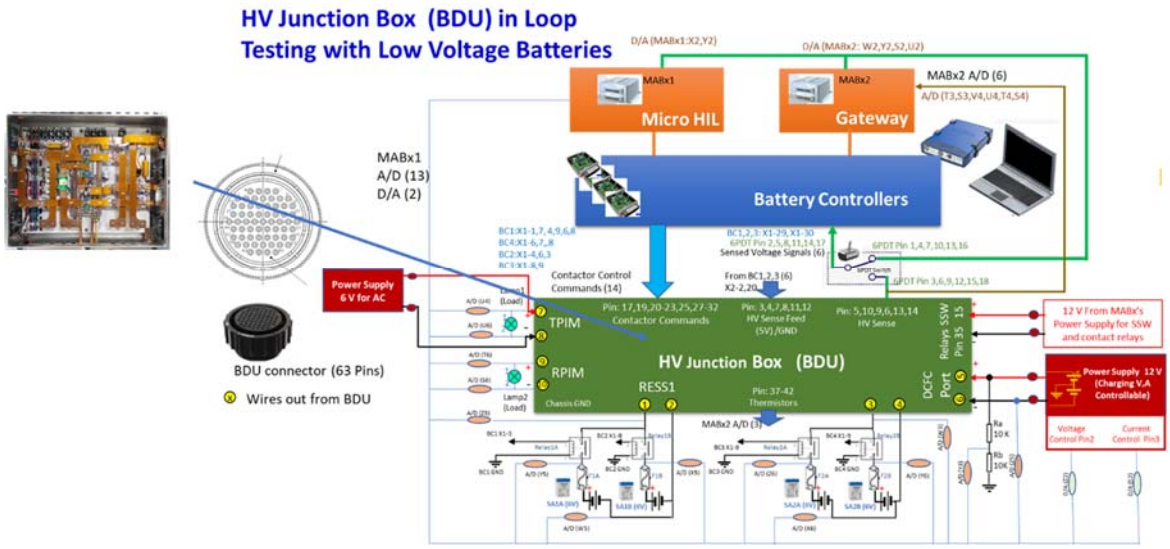


Figure 42: HIL Bench Test Environment for Controller Integration with Junction Box

Vehicle Build and Retrofit

For the retrofit vehicle, the project obtained a MY 2017 Escalade SUV which had previously been converted to electric all-wheel-drive propulsion as part of another project. The existing and new components associated with the DC charging retrofit are shown in Figure 43. Each axle was driven by a drive unit (denoted DU-F, DU-R) and power inverter module (TPIM-F, TPIM-R). Before beginning the retrofit, the vehicle had 2 sets of propulsion battery packs (RESS1 and RESS4) and controllers mounted in the rear compartment of the vehicle to power the front and rear propulsion systems. These battery packs were replaced with the newly developed quad battery pack (RESS 1-4), 4 controllers, and junction box , as shown in the diagram. Existing accessory components were mounted underhood in the front of the vehicle and included the accessory power (APM), cabin or coolant heating, and air conditioning compressor, which were powered via an existing high voltage distribution box. The existing vehicle contained two AC charge systems including on-board chargers (AC Charge-Fand R), AC charge inlets (AC-INLET-F and R), and status indicator display. Retrofit to add DC charge capability added new DC/AC Inlet with DC pins connected to new junction box and AC pins connected to existing front charger, along with additional charge port door switch (CP Dr Sw) and power line communication module. Rear AC charge system remained in the vehicle but was no longer needed.

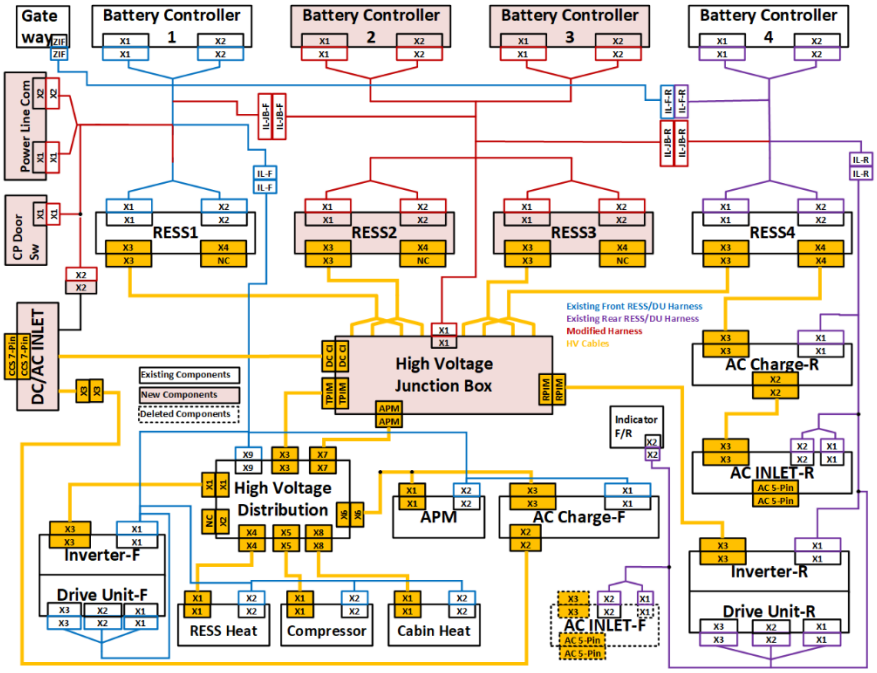


Figure 43: High and Low Voltage Wiring Showing New Components For DC Fast Charge Retrofit

Figure 44: Support Structure for RESS in Place of Rear Seat

Figure 45: Completed Quad RESS In Vehicle, With Junction Box Mockup

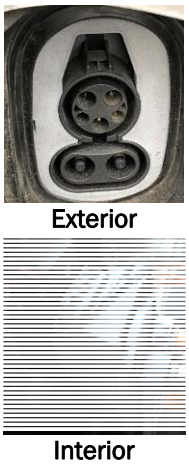


Figure 46: Charge Inlet Installed

As mentioned previously, the modification of the vehicle rear compartment to accept the new components was performed concurrently in the same vehicle garage facility as the build of the battery pack structure to allow close coordination and test fitting of the RESS structure before installing live battery components. Installation of the quad battery pack required removal of the rear seat and fabrication of additional support structure and mounting rails to support the pack and secure it to the vehicle frame. Work performed in this facility also included removal of unneeded components, installation of the new liquid cooled charge inlet, and installation of a new coolant bottle and coolant hoses to interface to the existing vehicle thermal system. Figure 44 shows the vehicle modification, including added battery pack support structure; Figure 45 shows the RESS installed in the vehicle with mockup of the junction box in mounting position; and Figure 46 shows interior and exterior views of the CCS DC charge inlet installed on the right side of the vehicle behind the rear passenger door.

Due to the prototype controls and components used, the retrofit vehicle had been developed with limited drive capability and was never planned to be driven on public roads. This made logistics of charger testing much

more difficult due to limited ability drive the vehicle to condition the battery state-of-charge for fast charge testing, unless the test site had a suitable load bank for discharging. Due to delays in the high voltage junction box availability due to required redesign, the completion of vehicle retrofit was delayed significantly and was ultimately not completed due to use of alternate 800V vehicles for testing and demonstration with the charger, and use of the HIL bench for demonstration and measurement of system charge time and C rate.

Support of NextEnergy and ACM Site Testing and Final Demonstration

Due to delays in development of the Escalade vehicle and ability to condition the vehicle for charging tests without requiring a discharging load, GM worked with Delta Electronics to provide alternate 800V development vehicles for charger and vehicle interoperability testing at the NextEnergy and ACM sites, as shown in Figure 47.

Figure 48 shows a comparison of the charge current profile from the alternate 800V vehicle test compared to the capability of the Quad RESS system. Data from a test result at ACM overlayed on Quad RESS charge current profile generated from a HIL bench test, showing that the use of the 800V development vehicles for testing allowed testing the charger at significantly higher average current over a 10 minute period, even though the vehicle was being charged at a lower average C rate due to higher capacity battery pack.

(a) NextEnergy Site (b) American Center for Mobility Site

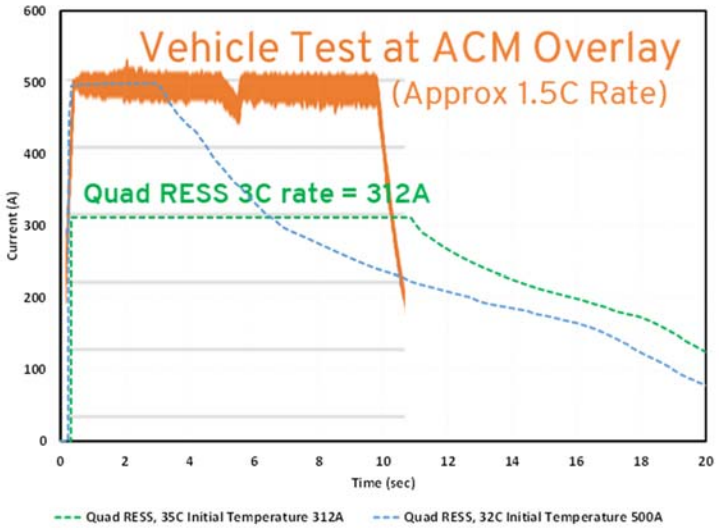


Figure 48: Comparison of Current Profiles From Quad Ress HIL Bench vs. ACM Test

Virtual Demonstration of 3C Charge Rate

Due to logistical issues transporting the vehicle to the Next Energy site, system testing to characterize charge rate as a function of initial temperature and current limit was performed using the HIL bench.

HIL Bench Setup For Demonstration

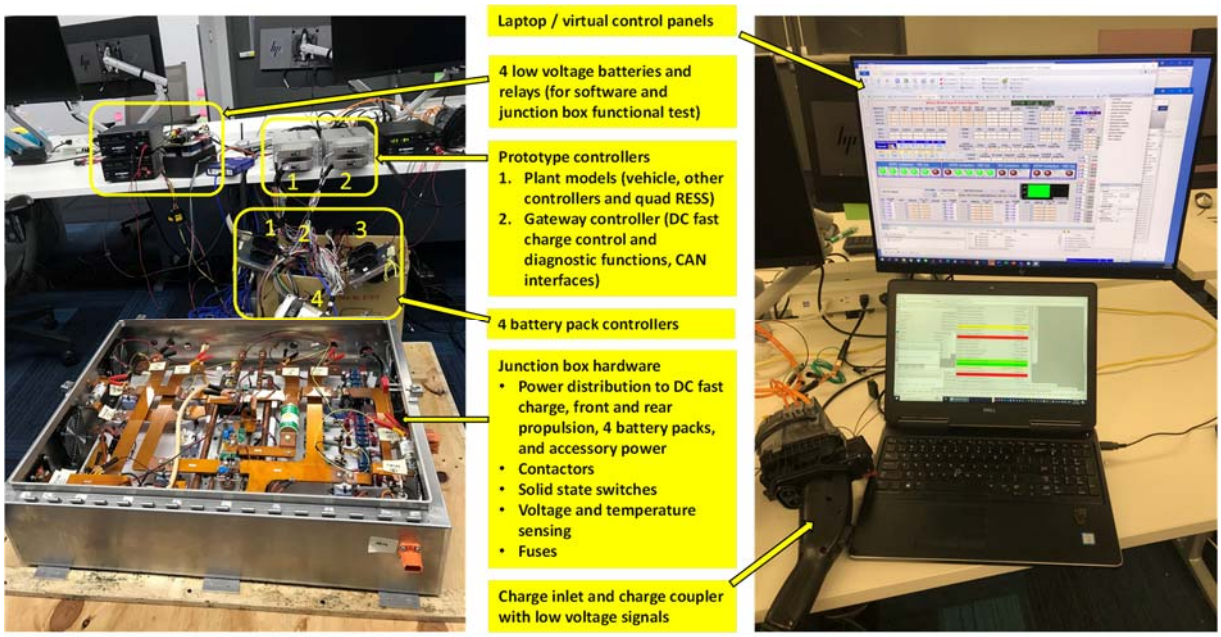


Figure 49: HIL Bench Setup for Charging Test with Charge Inlet, Battery Pack Controllers, and Junction Box Hardware

Figure 49 shows the setup of the HIL bench, which was used to measure the system C rate under various charging conditions.

(a) A laptop computer with multiple virtual control panels capability of displaying system and software inputs, internal states, calibration parameters, and outputs

(b) A low voltage battery and relay assembly which provided the capability for emulating the 4 high voltage packs, used for software and junction box functional testing. This part of the system was not used for the characterization testing, which instead utilized high fidelity electrical and thermal models implemented in the HIL prototype controller.

(c) A first prototype controller implementing the following real-time plant models: RESS, contactors, and solid-state switches; off board DC charger, including communication interface and messages; front and rear power inverter modules; battery, traction drive, and vehicle cabin heating and cooling systems; brake, power steering, vehicle body, and driver shift/pedal interface controller interfaces. This controller is utilized only on the system HIL bench, and provides a virtual, real time model of the components of the system which are either part of the vehicle system, or require high voltage/high power for operation.

(d) A second prototype controller implementing the following real-time embedded software control functions: Control and coordination of DC fast charging for the 4 battery packs; contactor and solid-state switch control and diagnostics; and CAN gateway functions needed to map the original and added data messaging onto the CAN bus network implemented in the vehicle. This controller is utilized in both the system HIL bench and vehicle configurations.

(e) A total of four battery pack controllers, one for each of the four battery subpacks. These controllers implement battery-specific control functions, such as setting charge and discharge control limits, monitoring cell voltage, current and temperature, SOC determination, and diagnostics.

(f) Junction box physical hardware, which incorporates the following functions: DC bus power distribution to DC fast charge, front and rear propulsion, 4 battery packs, and accessory components; DC bus contactors and solid-state switches; voltage and temperature sensors; and protective fuses.

(g) Vehicle charge inlet physical hardware containing the following interfaces: AC and DC pin temperature sensors; coupler proximity and control pilot signals; coupler lock actuator and position feedback.

(h) Charge coupler implementing the charger side interfaces of the coupler proximity and control pilot signals.

To initiate a charging test, the model is first manually initialized to the desired starting values for cell states of charge and temperatures via the control panel. Also, a parameter is adjusted to set the maximum available charging current to 312, 400, or 500 amps per the test case. Next, the charge coupler is inserted into the charge inlet, which initiates charging communication and contactor closure sequence to switch the packs into series configuration and connect to the off-board charger. In the HIL configuration, the contactor coils are controlled by the controller output drivers, and the contactors physically open and close based on software commands to realize the desired DC bus states. However, the cell, pack, and DC bus sensed voltages and currents are produced by the high voltage system plant model. Charging begins after the system completes the initiation sequence.

Demonstration of Charging Rate

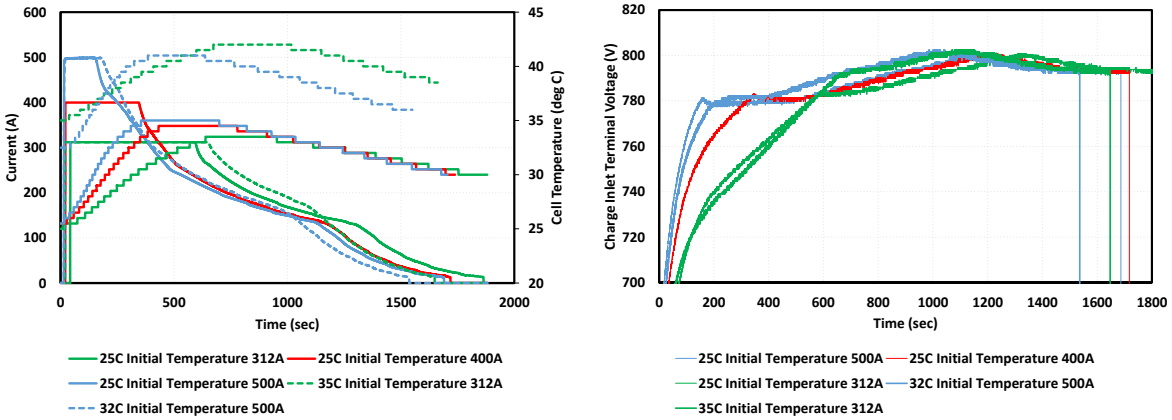
A total of 5 test cases were run on the HIL bench to evaluate the effect of maximum available current and initial cell temperature on charging time and C rate. Test cases and results are shown in Table 15. Figure 50 shows cell temperature, current, and charge inlet voltage plotted vs. time, and Figure 51 shows current, average C rate, and elapsed time from 10% SOC plotted vs. SOC for each of the 5 cases. Note that based on the single 400V accessory power system of the vehicle, power for the thermal/accessory system is drawn from only one of the two series-connected battery packs, so the state of charge between two strings diverges up to about 5% during the series charging and is equalized during subsequent parallel-mode operation. The SOC and C rate plotted is the higher of the two battery packs. From the figures it can be seen that:

1. Cases 2, 3, 4, and 5 achieve an average of ≥3C rate when charged from 10% to 60% SOC, resulting in a 50% increase in SOC in ≤10 minutes.
2. Increasing available current increases the charging rate at the beginning of the charge, but at higher states of charge the charging rate is reduced below the available current and determined primarily by cell temperature.
3. In cases 2, 3, and 5, the charging rate has dropped below 3C by the time the SOC has reached 60%. However, in case 4 due to the higher initial cell temperature, the system maintains a 3C rate for the full 10 minutes until 60% SOC.
4. Due to the large thermal mass of the pack, none of the runs reach the maximum allowed cell temperature of 50C. If this were to occur, the current would be reduced to prevent further increase in cell temperature.

Table 15: Effect of Maximum Available Current and Initial Cell Temperature

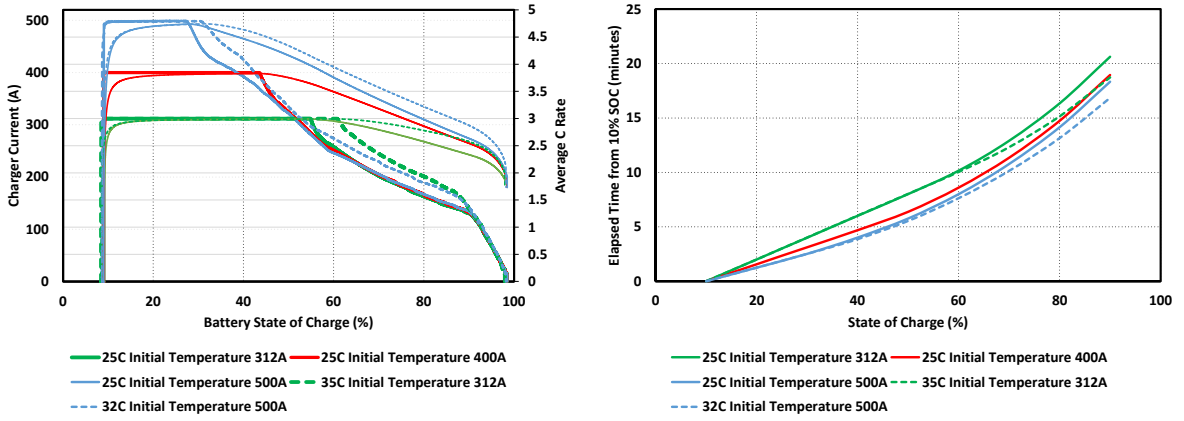
Experiment Conditions				Experiment Results					
Case	Current Limit (A)	Cell Temp at Start of	Desired SOC at start of	SOC at start of Test (%)	Peak Cell Temp	Average Current, 10-60%	Average C Rate, 10-60% SOC	C Rate at 60% SOC	Time 10% to 60% SOC (minutes)

		Test (deg C)	Test (%)		(deg C)	SOC (A)			
1	312	25	<9.5%	9.0	33.5	308	2.96	2.48	10.2
2	400	25	<9.5%	9.0	34.5	364	3.50	2.41	8.6
3	500	25	<9.5%	9.0	35.0	390	3.75	2.36	8.0
4	312	35	<9.5%	8.4	42.0	312	3.00	3.00	10.0
5	500	32	<9.5%	8.6	41.0	410	3.94	2.63	7.6



(a) Current and Temperature vs. Time (b) Charge Inlet Voltage vs. Time

Figure 50: HIL Bench Test Results: (a) Current and Temperature (b) Charge Inlet Voltage



(a) Current and Average C Rate (b) Time to Charge Starting at 10% SOC

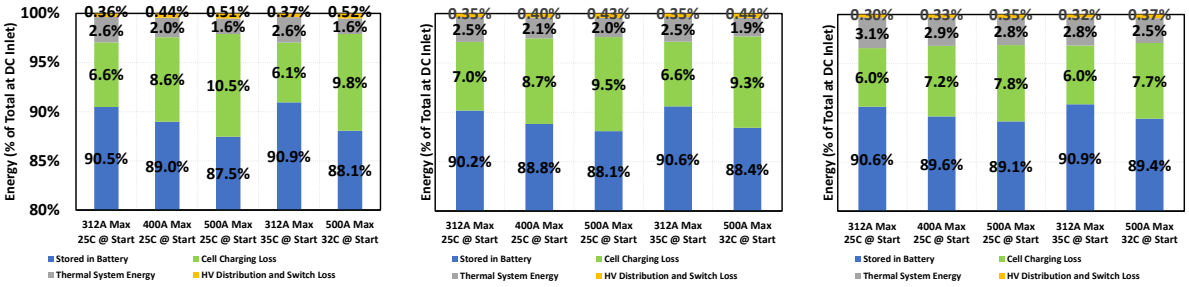
Figure 51: HIL Bench Test Results: (a) Current, Average C Rate vs. SOC (b) Time to Charge

Charging Efficiency

To calculate the charging efficiency for each of the 5 cases, the charging loss energy in the battery and solid-state switches were calculated by integrating the battery and high voltage junction box losses, which are

outputs of the model. Results are plotted in Figure 52, with the blue bars representing the portion of energy stored in the battery which can be taken as the efficiency of the on-vehicle charging process.

- Increased current negatively affects charging efficiency. As current increases from 312A to 500A, the charging efficiency decreases by 3% when charging from 10 to 30% SOC. Most of this loss is in the cells, as the HV distribution and switch loss increases from 0.36% to 0.51% which is a small part of the total charging energy.
- Higher starting temperature in the range studied positively affects charging efficiency by reducing cell losses. This is expected as cell resistance decreases with temperature in the operating range of the system.



(a) 10% to 30% SOC (b) 10% to 60% SOC (c) 10% to 90% SOC

Figure 52: Energy Breakdown for 5 cases (a) 20% SOC added (b) 50% SOC added (c) 80% SOC added

Effect of Battery Cooling on Charge Time

The significant portion of energy used for battery cooling in the previous test raised the question of whether the system would be capable of charging under the tested conditions without requiring liquid cooling of the battery pack. To understand this, experiments were run to charge the system for the 312A and 500A cases with the liquid cooling system disabled. Figure 53 shows the charging current and cell temperature for these results compared to the previous results with 25C initial temperature, and Figure 54 shows the breakdown of charging losses and efficiency. Table 16 shows the effect of cooling availability on charging time, average current, and peak cell temperature. These results showed that the cell temperatures remained within the 50C limit without cooling and that the system charged faster without the liquid cooling of the cells, due to the benefit of better charge acceptance at the higher temperatures. Charging efficiency was also better under this condition, due to the elimination of compressor accessory load.

Table 16: Effect of Cooling Availability

Experiment Conditions					Experiment Results						
Case	Current Limit (A)	Cell Temp at Start of Test (deg C)	Cell Liquid Cooling	SOC at start of Test (%)	SOC at start of Test (%)	Peak Cell Temp (deg C)	Average Current, 10-60% SOC (A)	Average C Rate, 10-60% SOC	C Rate at 60% SOC	Time 10% to 60% SOC (minutes)	Time 10% to 90% SOC (minutes)
1	312	25	Off	<9.5%	5.0	40.0	307	2.95	2.47	10.2	20.2
2	500	25	Off	<9.5%	4.0	44.0	391	3.76	2.52	8.0	17.2
3	312	35	25C	<9.5%	9.0	33.5	308	2.96	2.48	10.2	20.6
4	500	32	25C	<9.5%	9.0	35.0	359	3.45	2.18	8.7	20.8

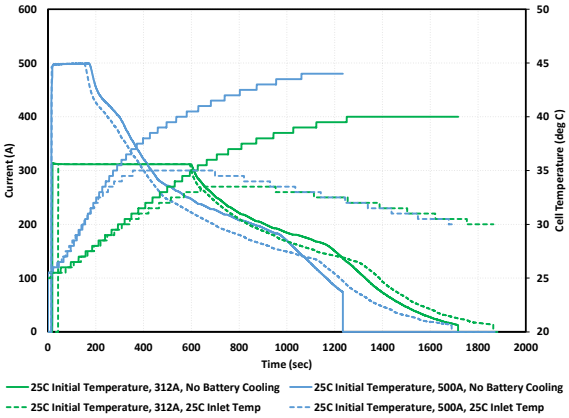


Figure 53: HIL Bench Test Result, Current and Cell Temperature vs. Time

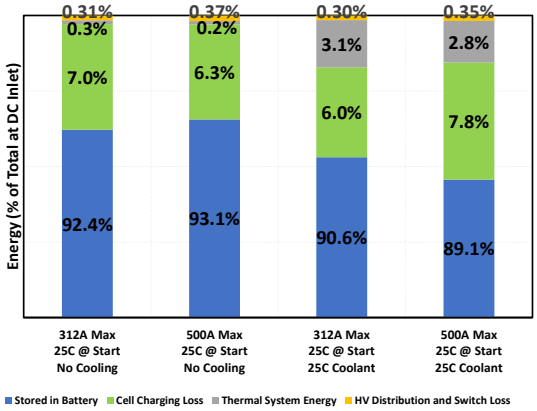


Figure 54: Energy Breakdown, 10% to 90% SOC

Conclusions

- Design for reduced electric vehicle recharge time requires increased battery charging C-rate, thereby increasing the power-to-energy ratio of the energy storage system requirements. Consequently, battery pack technology designed for extended-range EV application proved capable of meeting the project targets. As compared to an example electric vehicle pack, the project battery pack traded off energy for power, with about 28% less Whr/kg but three times the W/kg.
- A complete battery pack composed of 4 independent subpacks was built during the project, along with a junction box housing liquid cooled silicon carbide power modules for series-parallel reconfiguration and other mechanical contactors and sensors for power distribution. Both components were tested in the lab and characterized based on a 500A maximum charging current profile, and were found to be capable of meeting the project goal of 50% SOC increase at 3C charge rate
- Virtual demonstration of the system in HIL environment with the battery and charging control system showed the system could meet the charge rate goal when charged at a constant 3C rate of 312A for 10 minutes and exceed the goal when higher current up to 500A was available from the charger, charging at an average rate of 3.9C for 10 minutes.
- Use of silicon carbide switches in a series-parallel reconfigurable battery pack had a slight negative effect on DC fast charge efficiency, reducing efficiency by up to 0.5% at high currents as compared with mechanical switches.
- As a result of achieving the requirement for fast recharge time, demand for power is increased for short durations but reduced for long durations as compared with longer recharge events that are limited by battery C rate or available charger power. The shorter duration charge event enables system design tradeoffs to rely on short term as opposed to continuous means for mitigating the heat generated by the charging event, i.e. relying on component thermal mass rather than cooling strategies. The RESS designed for the project did not require active liquid cooling to achieve the required charging rates, due to the short duration of the charging current and large thermal mass of the RESS.

Inventions

- One ROI has been submitted resulting in an application for patent being filed
    1. P104087– Electric Vehicle Recharge Control

Test Results from American Center for Mobility

The American Center for Mobility (ACM) site is a collaboration between Delta, DTE Energy and ACM. This site draws directly from Medium Voltage 13.8 kV, which was already available on this site. ACM also provides a step to "Real-World" usage in a semi-controlled environment, as many ACM customers are running tests with Electric Vehicles where a Fast Charge will help them get back to testing quickly.

This site constructed under the direction from DTE Energy, most closely mimics the process for fielding one of these EV chargers. Shown in the image below are the Electricians tasked with building the grounding structure and the concrete pads where the system will mount.

Constuction of the EV Extreme Fast Charge site at American Center for Mobilty

The completed test site at ACM, from Left to Right in front of the brick building, is the Medium Voltage switch (green) the SST, and the Power Cabinet. To the Right with the two yellow bollards is the Dispenser.

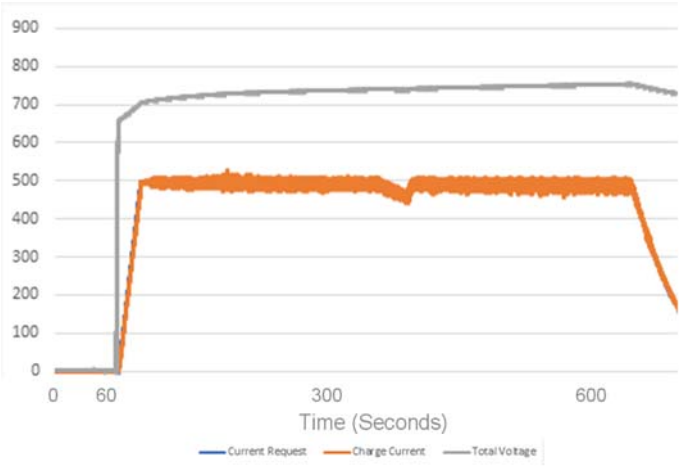
Due to supply chain issues and lead-time, exceeding our program needs a manual switch was used in place of the pad mounted recloser, which had been originally planned. Normally the SST is design to have full control of the switch between the Medium Voltage source and the AC Input. When manually commanded the SST will precharge its circuits from the 120V supply before commanding the Medium Voltage switch to close. This prevents a large inrush current and possible damage. Given our manual switch, a handshake needed to be devised that The SST could inform a licensed electrician in his Personal Protection Equipment

Image Left Electrician in Cat 4 PPE, Image Right the Green Light informing the electrician they can close the switch.

The electrician would reset the switch and ready his Hot Stick. The SST would then be commanded to start. Precharge takes around 40 seconds, the SST will illuminate the Green Light shown above when it is safe for the electrician to close the medium voltage switch.

The ACM system has charged Chevy Bolts, GMC eHummers, Ford F150 Lightning Pick-ups and Cadillac Lyrics. The GMC eHummer was the only vehicle available that would charge at 800V. These vehicles have their traction battery split in two. During driving modes the battery halves run in parallel, but for DC fast charge with an EVSE that is capable the eHummer with configure its battery halves in series to charge faster.

The e-Hummer shown above uncovered unique issues, as loads inside the e-Hummer are shifted back and forth between the two battery halves to keep them balanced. During this shift, voltages readings swing making it appear as a ground fault to the dispenser. Software was updated to include this learning.



The e-Hummer allowed full 500 Amp charging for about 9 minutes, at an average of 725V resulting in about 55 kWhr being pumped into the battery before the system begins to limit current.

We also charged the Ford F150 Lightning, this vehicle charges at 400V

The Project concluded with a Demonstration where many from around, industry, and government came together to witness the Fast Charge system

Conclusions

There are many learnings from this program that can be applied to bring these DC fast charge stations to the market.

1. In today's supply-chain, the procurement of a medium voltage step down transformer is much longer than it was before. The SST system eliminates this item.
2. In this design and other Fast Charge stations, the high voltage terminal that connect to the stiff feed wires from underground conduit should be located as high as possible in the cabinet to account for bending radius.
3. Electricians around the world use different terminal designs on their High Voltage wires. These terminals should provide sufficient material that the installer can customize it as needed.
4. The diagnostics originally designed in the system are set on a hair trigger to prevent damage to the prototypes, for field applications, some of these diagnostics are set too tight.
5. In this system, the power cabinet uses carryover production converters, which are very power dense and require liquid cooling with a chiller. A production program would be best to redesign this to be air-cooled.
6. There some parts, which would need redesign to facilitate service, for example, the chiller that cools the charge handle of the ACM Dispenser is very difficult to fill and would be nearly impossible to swap-out.
7. The System at ACM will be maintained for at least the next year, we should gain a better understanding of the reliability of this type of system in that time.
8. The System at NextEnergy will be relocated to the Delta Office in Plymouth MI and provide a test bed for future developments.
9. A 500-amp charge may heat the battery too fast. A lesser charge current may charge the vehicle better; this is controlled by the vehicle developers.
10. The Optimum size for a vehicle's battery is determined by the vehicle size and desired range, The Delta Fast Charge system presented here can run continuously to charge at up to 500 amps for as long as the vehicle needs.
11. Next Steps would include, cost reduction, design for installation, design for service, and other DCFC features that were designed in the market during this program.

Key Publications

Charles Zhu, "180-Mile Charge in 10 Minutes: Utilizing Solid-State-Transformer Technology for Micro-Grid-Capable Extreme Fast Chargers," presentation in SAE Hybrid and Electric Vehicle Technologies Symposium, February 2019, Anaheim Garden Grove, CA.

C. Zhao, Y. -H. Hsieh, F. C. Lee and Q. Li, "Design and Analysis of a High-frequency CLLC Resonant Converter with Medium Voltage insulation for Solid-State-Transformer," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 2021, pp. 1638-1642, doi: 10.1109/APEC42165.2021.9487101.

Z. Li, Y. -H. Hsieh, Q. Li, F. C. Lee and C. Zhao, "Evaluation of Double-Line-Frequency Power Flow in Solid-State Transformers," 2021 IEEE Fourth International Conference on DC Microgrids (ICDCM), 2021, pp. 1-7, doi: 10.1109/ICDCM50975.2021.9504649.

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Journal Paper "Design and Analysis of High-frequency CLLC Resonant Converter Design with Medium Voltage Insulation Capability for Solid-State-Transformer"

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