A PWM Strategy for Cascaded H-bridges to Reduce the Loss Caused by Parasitic Capacitances of Medium Voltage Dual Active Bridge Transformers

Haiguo Li
Min H. Kao Department of Electrical Engineering and Computer Science the University of Tennessee, Knoxville
Knoxville, TN, USA
hli96@vols.utk.edu

Zihan Gao
Min H. Kao Department of Electrical Engineering and Computer Science the University of Tennessee, Knoxville
Knoxville, TN, USA
zgao15@vols.utk.edu

Fred Wang
Min H. Kao Department of Electrical Engineering and Computer Science the University of Tennessee, Knoxville
Knoxville, TN, USA
Oak Ridge National Laboratory
Oak Ridge, TN, USA
fred.wang@utk.edu

Abstract— **In this paper, to reduce the power loss caused by the parasitic capacitances of medium voltage medium frequency transformers in a two-stage dc/ac converter, including a dual active bridge (DAB)-based dc/dc stage and a cascaded H-bridge (CHB)-based dc/ac stage, a PWM strategy is proposed for the dc/ac stage. For each H-bridge, by shifting the high switching frequency to one half-bridge and having the other half-bridge switching at the fundamental frequency of the ac voltage, equivalent frequencies of transformer terminal-to-ground voltages are reduced. As a result, the frequencies of charging and discharging current to the parasitic capacitance are reduced, and therefore the loss caused by the parasitic capacitances is reduced. Compared to the conventional phase-shift PWM, the proposed PWM strategy can reduce the parasitic capacitance loss by about 75%. Experimental test results of one phase in the 13.8 kV/ 100 kW converter prototype are provided to validate the approach.**

Keywords—cascaded H-bridge, dual active bridge, losses, parasitic capacitances, PWM

I. INTRODUCTION

In many grid applications, such as PV, solid-state transformers, microgrids, and power conditioning system (PCS) converters, medium frequency (MF) magnetic transformers are used to achieve galvanic isolation and voltage conversion [1-3]. These transformers are not ideal and can have many parasitics, such as parasitic capacitances between windings, winding turns, and windings to the ground [4-6]. These parasitic capacitances impact the performances of the transformer and the whole converter.

It is well known that parasitic capacitances of the MF transformer introduce common-mode (CM) paths and thus CM currents, which aggravates the electromagnetic interference (EMI) of the converters [7-11]. Methods have been proposed to mitigate the CM current by adding a shielding layer [7], changing the topology to minimize the MF CM voltage [8] or the equivalent CM impedance [9], or modifying the modulation strategy in some special topologies to reduce the CM voltage so that the CM current can be reduced [10], etc. Besides the CM current, the parasitic capacitances of the MF transformers also lead to power loss. The parasitic capacitance-related loss has been discussed in the LV devices and converters [12, 13]. However, it is rarely discussed in the MF transformer. Besides, in the medium voltage (MV) applications, the losses caused by these parasitic capacitances are much larger with comparable capacitance and switching frequencies than those in LV applications because of the higher voltage.

The loss mechanism of some device-related parasitic capacitances is discussed in the literature. The device's transient switching current is increased to charge/discharge the parasitic capacitance, which increases the switching losses [12-14]. Losses are induced by parasitic capacitances with high-frequency voltage variation, including the parasitic capacitance introduced by the heat sink, the load [15], the device power module package [12], and PCB layout [13], etc. Also, the loss caused by the parasitic capacitance is linearly proportional to the capacitance, equivalent switching frequency, and the square of the voltage applied to the capacitance [13, 14]. The loss caused by MF transformer parasitic capacitance has a similar mechanism.

In this paper, a PWM modulation strategy is proposed for the cascaded H-bridge (CHB)-based dc/ac stage to reduce the losses induced by the dual active bridge (DAB) transformers in the dc/dc stage. The proposed PWM modulation reduces the equivalent frequency of the transformer winding voltages to reduce the losses induced by the parasitic capacitance between the winding and the ground.

The rest of this paper is organized as follows. The system configuration, transformer parasitic capacitances, and the conventional phase-shift PWM (PS-PWM) strategy for the CHB are introduced first in Section II. Then, the proposed PWM strategy is discussed in Section III, considering the modulation, device loss, parasitic capacitance loss, and voltage harmonics. In Section IV, the experimental results are provided to validate the proposed PWM strategy. Finally, Section V concludes this paper.

II. THE SYSTEM CONFIGURATION, TRANSFORMER PARASITIC CAPACITANCES, AND THE CONVENTIONAL PS-PWM

A. The Converter Topology

As shown in Fig. 1, the 13.8 kV/ 100 kW dc/ac converter is used to connect an 850 V LV dc grid and a 13.8 kV (line-to-line) MV ac grid. The converter consists of two stages, including a DAB-based dc/dc stage and a CHB-based dc/ac stage. The dc/dc stage is used to realize galvanic isolation and boost the 850 V dc to 6.7 kV dc. The dc/ac stage is a three-phase four-wire configuration, converting the MV dc to MV

ac, and the neutral point is grounded. 1.7 kV SiC MOSFETs are utilized on the LV side, and 10 kV SiC MOSFETs are used on the MV side. The switching frequency of the DAB converter and the CHB converter is 10 kHz and 3 kHz, respectively, considering the efficiency requirement.

Parasitic capacitances of the DAB transformers are also shown in Fig.1. Since the MV winding is shielded and the shielding layer is connected to the core and then grounded, the parasitic capacitance between the LV winding and the MV winding is decoupled by the ground. The LV-side capacitances are neglected because of the low voltage, and the MV-side parasitic capacitances, which are marked in red, are the focus of this paper. Since the three phases are identical, the following analysis only focuses on one phase.

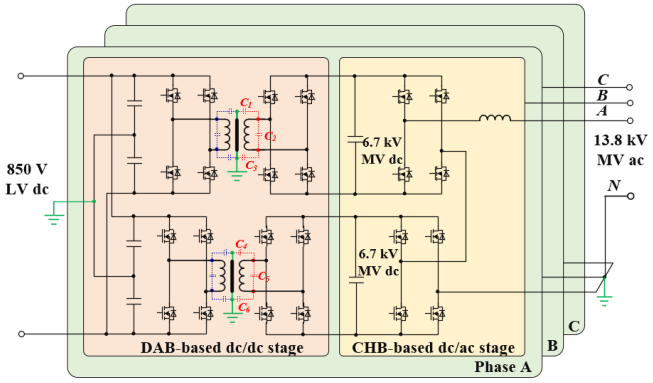


Fig. 1. Converter topology and the transformer parasitic capacitances.

The simplified circuit of phase A, only considering the MV-side parasitic capacitances, is shown in Fig. 2. The parasitic capacitances between the transformer winding terminals are C_2 and C_5, respectively, and the parasitic capacitances between the winding and the ground in the two transformers are C_1, C_3, C_4, and C_6, respectively. Since the neutral point is grounded, the dc-link terminal-to-ground voltage changes with the switching of the dc/ac stage. The half bridges in the dc/ac stage and their switching states are denoted as S_k (k=1, 2, 3, 4), and

$$S_k = \begin{cases} 1, & when\ the\ upper\ device\ is\ on \\ 0, & when\ the\ lower\ device\ is\ on \end{cases} \quad (1)$$

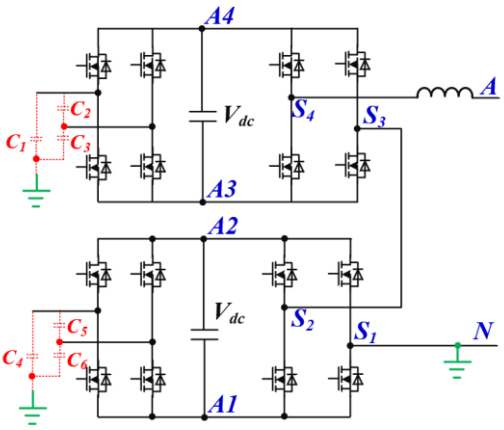


Fig. 2. The equivalent circuit of the MV stage including the MV-side transformer parasitic capacitances.

The dc-link terminals are represented as *A1*, *A2*, *A3*, and *A4*, respectively, and their voltages, to the ground, can be expressed as

$$\begin{cases} v_{A1} = -S_1 V_{dc} \\ v_{A2} = (1 - S_1) V_{dc} \\ v_{A3} = (S_2 - S_1 - S_3) V_{dc} \\ v_{A4} = (1 + S_2 - S_1 - S_3) V_{dc} \end{cases} \quad (2)$$

B. Parasitic Capacitance Loss

The equivalent circuit of the parasitic capacitance's charging and discharging loop is shown in Fig. 3. The voltage change, from V_1 to V_2, is caused by the switching of the devices, and R_s and L_s represent the overall resistance and inductance in the loop. Due to the existence of the L_s, resonance could occur. However, since L_s is mostly the stray inductance and is small, the resonant frequency is higher than the converter switching frequency, and thus the resonance will be quickly damped before the end of the switching period. Therefore, the voltage on the parasitic capacitance also changes from V_1 to V_2 during the switching period. In this period, the energy provided by the voltage source, E_s, which is the dc-link capacitor of the converter (considered to be a constant voltage), is:

$$E_s = V_2 \int_0^t i_c \, dt \quad (3)$$

and the current integration equals to the total charge into the capacitance, i.e.,

$$E_s = V_2 \int_0^t i_c \, dt = V_2 C (V_2 - V_1) \quad (4)$$

where i_c is the charging/discharging current and C is the parasitic capacitance.

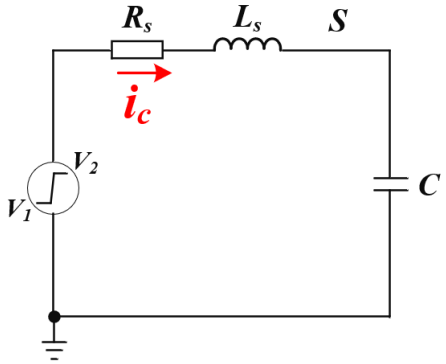


Fig. 3. Equivalent circuit of the parasitic capacitance loop.

The capacitance's energy change is

$$E_c = \frac{1}{2} C V_2^2 - \frac{1}{2} C V_1^2 \quad (5)$$

Then, the total energy loss in the circuit equals to the energy provided by the voltage source subtracted by the energy stored in the capacitance, which can be calculated as

$$E_{loss} = |E_s - E_c| = \frac{1}{2} C (V_2 - V_1)^2 = \frac{1}{2} C \Delta V^2 \quad (6)$$

where ΔV is the voltage change step, and it equals to V_2-V_1. Since in each switching cycle, the voltage changes from V_1 to V_2 and then from V_2 back to V_1, the power loss introduced by the parasitic capacitance charging and discharging is

$$P_{loss} = 2 \frac{E_{loss}}{T_s} = 2 E_{loss} f_s = C \Delta V^2 f_s \quad (7)$$

where T_s is the equivalent switching period; f_s is the equivalent frequency of the voltage applied on the parasitic capacitance. From (7), the power loss in the parasitic capacitance loop is related to the parasitic capacitance, the voltage change applied to the capacitance, and the equivalent voltage frequency. Reducing the capacitance and voltage change can reduce the loss, but both require hardware

changes and have design constrains. Changing the equivalent voltage frequency is another approach to reduce the loss without changing the hardware.

C. Parasitic Loss with the Conventional PS-PWM for the CHB-based dc/ac stage

PS-PWM is commonly used for CHB-based dc/ac converter, and the modulation scheme is shown in Fig. 4. Four high-frequency carrier waveforms, v_{cr1}, v_{cr3}, v_{cr2}, v_{cr4}, with a phase shift of 90 degrees in sequence, are used to generate the switching states for S_1, S_3, S_2, and S_4, respectively, as introduced in [16]. For sinusoidal voltage output, the voltage reference, v_{ref}, is

$$V_{ref} = 0.5 + 0.5\sin(\omega t) \tag{8}$$

With the same frequency, f_s, for each carrier waveform, the total output voltage, v_{out}, has an equivalent switching frequency of $4f_s$. Based on (2), the dc-link terminal voltages, v_{A1}, v_{A2}, v_{A3}, and v_{A4}, have an equivalent frequency of f_s, f_s, $3f_s$, and $3f_s$, respectively. As a result, each switching action in the dc/ac stage charges/discharges the parasitic capacitance of C_1, C_3, C_4, and C_6, and losses are induced. Since the voltage on C_2 and C_5 are determined by the switching state of the DAB converter, the switching action of the dc/ac stage does not change the voltage on C_2 and C_5.

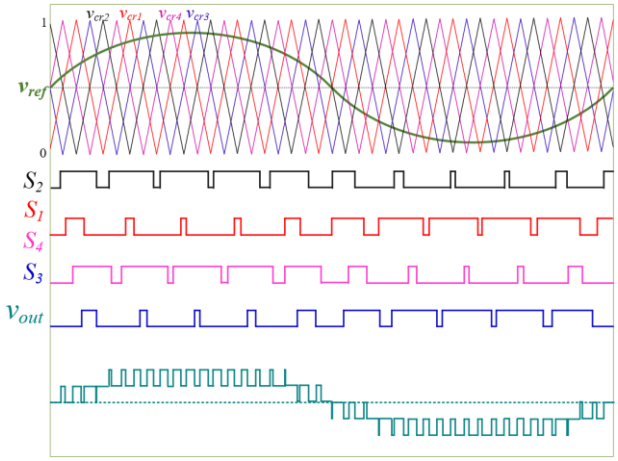


Fig. 4. The PS-PWM for CHB-based dc/ac converter.

Based on Fig. 2, (2), and (7), the possible voltage applied on dc-link terminals, corresponding to different switching states, are shown in Table I. The voltage change step of each dc-link terminal is V_{dc}.

TABLE I: POSSIBLE DC-LINK TERMINAL VOLTAGES.

Dc-link terminal	Possible voltage
A1	$-V_{dc}$, 0
A2	0, V_{dc}
A3	$-2V_{dc}$, $-V_{dc}$, 0, V_{dc}
A4	$-V_{dc}$, 0, V_{dc}, $2V_{dc}$

Then, the total DAB transformer parasitic capacitance loss caused by the switching and grounding loop of the CHB converter is

$$P_{TX1} = C_4 {V_{dc}}^2 f_s + C_6 {V_{dc}}^2 f_s + 3C_1 {V_{dc}}^2 f_s + 3C_3 {V_{dc}}^2 f_s \tag{9}$$

Assuming the DAB transformer parasitic capacitances are the same, i.e., $C_1 = C_3 = C_4 = C_6 = C_p$, which could be achieved when the winding structure of the transformer is symmetric, then (8) becomes

$$P_{TX1} = 8C_p {V_{dc}}^2 f_s \tag{10}$$

III. THE PROPOSED PWM STRATEGY

A. The Proposed PWM Strategy

From (2) and Fig.2, the equivalent switching frequencies of the dc-link terminals of *A1* and *A2* are only related to S_1, and the equivalent switching frequencies of the dc-link terminals of *A3* and *A4* are related to S_1, S_2, and S_3. Also, with PS-PWM, the equivalent frequency of the output voltage of each H bridge is doubled by switching the two half bridges at the same frequency. This can be also achieved by letting one half-bridge switch at the doubled switching frequency and the other half-bridge only switches at the fundamental frequency. Therefore, with a low switching frequency on S_1 and S_3 and doubled switching frequency on S_2 and S_4, the equivalent frequency of the output voltage of each H-bridge does not change, but the overall equivalent switching frequency of the dc-link terminals is reduced. Based on this, a PWM strategy shown in Fig. 5 is proposed.

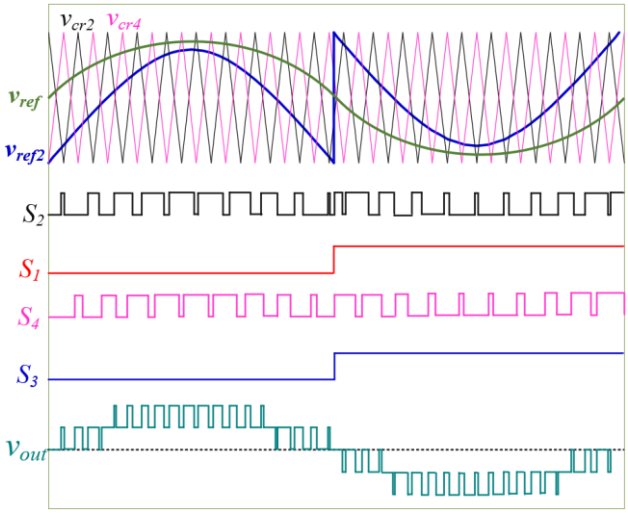


Fig. 5. The proposed PWM modulation strategy.

Different from the PS-PWM, the proposed PWM strategy only has two high-frequency carrier waveforms, v_{cr2} and v_{cr4}, with a phase shift angle of 180 degrees, and they are used to generate the switching states of S_2 and S_4, respectively. The voltage reference is changed from (8) to

$$V_{ref2} = \begin{cases} \sin(\omega t) & when\ 0 < \omega t < \pi \\ 1 + \sin(\omega t) & when\ \pi < \omega t < 2\pi \end{cases} \tag{11}$$

In this modulation, S_1 and S_3 are 0 when the voltage reference, v_{ref}, is positive, and are 1 when v_{ref} is negative. To keep the equivalent switching frequency of the ac side output voltage constant, the frequencies of S_2 and S_4 need to be doubled. Then, the frequencies of S_2 and S_4 are $2f_s$, and the frequencies of S_1 and S_3 are the same as the fundamental frequency of the ac voltage, f_0. As a result, the equivalent switching frequency of the dc-link terminals of *A1*, *A2*, *A3*, and *A4* are f_0, f_0, f_s+2f_0, and f_s+2f_0, respectively. Therefore, the loss due to the parasitic capacitances of DAB transformers and the switching of CHB converter is

$$P_{TX2} = C_p {V_{dc}}^2 (6f_0 + 2f_s) \tag{12}$$

f_0 can be neglected since it is much smaller than f_s, which means the proposed PWM strategy can reduce the parasitic capacitance loss of the DAB transformer caused by the switching of the CHB converter by about 75%, comparing (12) and (10).

B. Loss Estimation

The proposed PWM strategy changes the device loss distribution. Assume the device junction temperature is designed to be the same as that with PS-PWM. With the same gate drive, the conduction loss of each device does not change since the device conduction time within one fundamental cycle does not change. However, the switching loss changes. The devices switching at the ac voltage fundamental frequency will have much less loss than those with a high switching frequency.

The device loss estimation is conducted based on DPT data of the 10 kV SiC MOSFET. As shown in Table II, with the conventional PS-PWM and 3 kHz switching frequency, all devices have the same loss, 24 W. With the proposed PWM strategy, the devices with low switching frequency only have a 5 W loss, and the devices with high switching frequencies have 44 W loss. The total device loss of the dc/ac stage only changes from 192 W to 196 W. Therefore, the proposed PWM strategy does not increase the total device loss.

The transformer winding capacitances are measured to be $C_1 = C_3 = C_4 = C_6 = 108$ pF with Keysight impedance analyzer *E4990A*. The power loss induced by the DAB transformer parasitic capacitance can be estimated based on the capacitance, voltage, and the equivalent voltage frequency with (7). As shown in Table III, because of the higher equivalent frequency of the high-side H bridge, losses caused by C_1 and C_3 are higher than those caused by C_4 and C_6. With the conventional PS-PWM strategy, the total parasitic capacitance loss is around 116 W, and the loss is reduced to 30.8 W with the proposed PWM strategy.

TABLE II: DEVICE LOSS ESTIMATION.

Device	PS-PWM	Proposed PWM
In half-bridge S_1	24 W	5 W
In half-bridge S_2	24 W	44 W
In half-bridge S_3	24 W	5 W
In half-bridge S_4	24 W	44 W
Total	192 W	196 W

TABLE III: TRANSFORMER PARASITIC CAPACITANCE LOSS ESTIMATION.

Parasitic capacitance	Equivalent voltage frequency		Parasitic Loss	
	PS-PWM	Proposed PWM	PS-PWM	Proposed PWM
C_1	9 kHz	3.12 kHz	43.6 W	15.1 W
C_3	9 kHz	3.12 kHz	43.6 W	15.1 W
C_4	3 kHz	60 Hz	14.5 W	0.3 W
C_6	3 kHz	60 Hz	14.5 W	0.3 W
Total loss			116 W	30.8 W

C. Voltage Harmonics

Although the PWM strategy is changed, the output voltage waveforms of the PS-PWM and the proposed PWM are the same, as shown in Fig. 6. Even considering dead time and switching delay, which should also be the same, the output voltage waveforms are the same. Therefore, the voltage harmonics and the current harmonics, when with the same impedance, also stay the same.

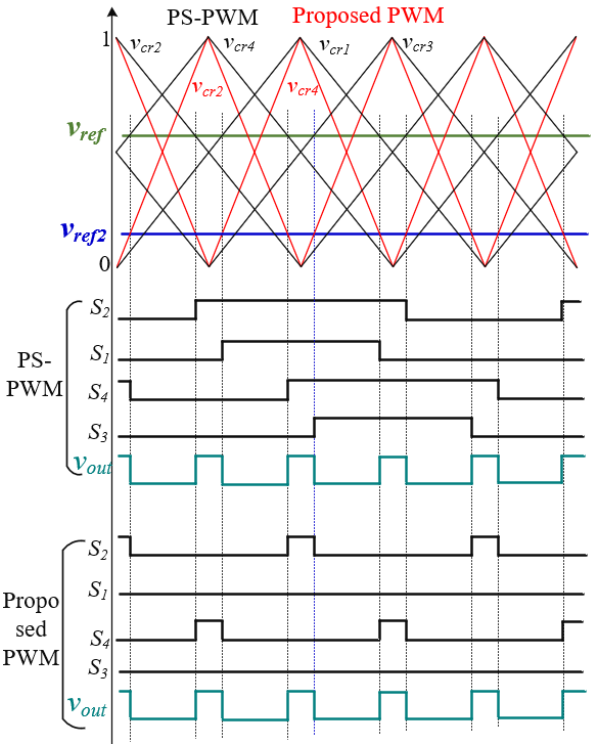


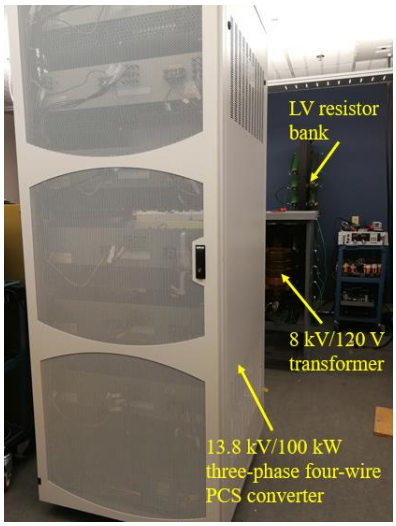
Fig. 6. Comparison of the modulation and output voltage waveform at a certain duty cycle

IV. EXPERIMENTAL TEST

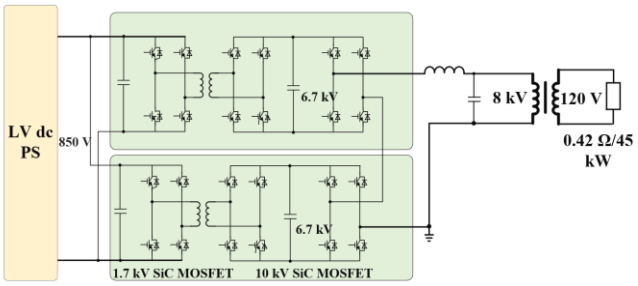
To verify the analysis, experimental tests are conducted with the three-phase four-wire 13.8 kV/100 kW converter prototype with the same configuration discussed in Section II. The converter hardware picture is shown in Fig. 7(a). Since it is difficult to only measure the power loss caused by the DAB transformer parasitic capacitance, the whole converter loss is measured. Only a single-phase test is conducted with the setup scheme shown in Fig. 7(b) since the three phases are identical. The converter input power and output power are measured with power analyzer WT3000E at the LV dc side and the MV ac side, respectively. The LV dc voltage is directly sampled by the power analyzer, and the current is measured with an external current sensor (LEM IT 400-S) because of the high current rating and easy connection. Due to the high voltage, the MV ac voltage is measured by the power analyzer through a resistor divider. The resistor divider ratio is calculated based on the resistance measurement with Tektronix Keithley 2100 digit multimeter, considering the input impedance of the power analyzer. Because of the high voltage and insulation requirement, the MV ac current is measured with an external current sensor (LEM IT 60-S) with a high insulation wire going through it.

The converter total loss with the conventional PS-PWM and the proposed PWM are measured separately, both under different output power levels. As shown in Fig. 8, with the

proposed PWM strategy, the converter total loss is reduced in the entire output power range. As discussed in Section II, the loss induced by the parasitic capacitance is only related to the voltage, equivalent switching frequency, and capacitance. For different output power levels, the loss reduction is almost constant, about 90 W, considering the measurement accuracy, and this matches the theoretical calculation shown in Table III.



(a)



(b)

Fig. 7. Test setup (a) hardware and (b) scheme.

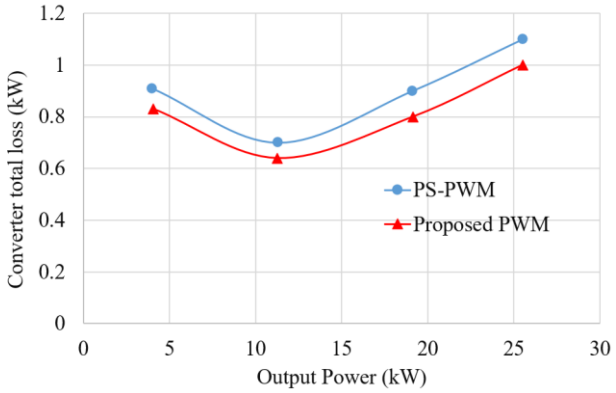


Fig. 8. Converter total loss comparison.

V. Conclusions

This paper has discussed the power loss induced by the parasitic capacitance of the MV DAB transformers in a two-stage 850 V dc to 13.8 kV ac converter. The loss is caused by the charging and discharging of the parasitic capacitance through the grounding loop of the DAB transformer and the dc/ac stage of the converter. The parasitic capacitance loss is linearly proportional to the equivalent voltage frequency, parasitic capacitance value, and the square of the voltage step in the dc/ac stage. A new PWM strategy is proposed to reduce parasitic capacitance loss while keeping the total device loss and voltage harmonics the same. The equivalent voltage frequency of the MV dc-links is reduced by shifting the high switching frequency to one half-bridge in each H-bridge, and thus the equivalent voltage frequency on the DAB transformer's parasitic capacitance is reduced. Compared to the conventional PS-PWM, the proposed PWM strategy can reduce the loss induced by the DAB parasitic capacitance theoretically by 75% considering the same capacitance and voltage step. Experimental tests are conducted with one phase in the 13.8 kV/ 100 kW converter prototype. Compared to the PS-PWM, the total converter loss with the proposed PWM strategy is reduced by about 90 W which is 0.27% of the converter efficiency, and ~10% of the converter total loss at light load and ~7% at heavy load. Since the other losses, including the losses in the DAB stage, the total device loss in the dc/ac stage, as well as the filter inductor loss stay the same, the measured loss reduction is the parasitic capacitance loss reduction of the DAB transformers, which matches the theoretical calculation.

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