

AUTOMATED MANAGEMENT OF LIBERA SPARK MODULE IOCs IN SPEAR3*

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Abstract

We are actively upgrading BPM processors in the SPEAR3 accelerator complex as several of the existing systems are reaching end-of-life. To consolidate the resources required for development and maintenance we have evaluated and installed several processors from the Libera SPARK hardware series. We found that two common deployment methods typically used with these modules, micro-SD card and network boot, are either hard to maintain or lack flexibility. Instead we have developed an automated method based on a network boot scheme where an external EPICS soft IOC manages the assignment of specific SPARK modules to physical BPMs in the accelerator. Each module queries the soft IOC at boot time to determine which BPM it is assigned to and then starts its IOC with the appropriate BPM prefix for the PV names. This deployment method allows for quick, seamless swapping of SPARK modules by machine operators or physicists. It addition, it allows us to bring additional modules online for testing, or to move modules to different locations with a different PV prefix for the new location. This method is applicable to other EPICS-enabled devices where the device hardware also hosts an IOC.

INTRODUCTION

SPEAR3 is a 3 GeV, 500 mA, 3rd generation synchrotron light source, commissioned in 2004 [1]. It operates with beam current distributed in four bunch trains and a single isolated timing bunch for pump-probe experiments. Top-up occurs at 5-minute intervals. Each top-up event requires about 50 single-bunch charge pulses into targeted SPEAR3 buckets at a 10 Hz rate. The SPEAR3 storage ring contains 18 lattice cells each with 6 button-style Beam Position Monitors (BPMs). Three BPMs per cell are connected to Bergoz processors for fast orbit control and beam inter-lock purposes. Several more BPMs are connected to the Echotek processors [2] to provide Turn-by-Turn (TbT) orbit information at discrete locations. The Echotek processors were developed in-house and produced commercially when SPEAR3 was commissioned; they are used for accelerator physics programs and not for operations. The Echotek have reached their end of life and we have evaluated commercial alternatives for replacement. A Libera Brilliance+ was first tested in SPEAR3 in 2017 [3]. Since TbT studies for accelerator physics programs do not require the long-term stability capability of the Brilliance+, and additionally the fast or-

bit feedback is implemented in the Bergoz BPM system, a SPARK-ERXR processor [4] was purchased and installed for accelerator physics applications. Additionally we are in the process of installing and testing Beam Loss Monitors (BLMs) for Libera that have the same base hardware and software infrastructure as the SPARKs.

The SPEAR3 injector was commissioned in 1990 [5], and includes the 120 MeV linac injector with a thermionic RF gun [6], the booster synchrotron [7] and the Transport Lines. The entire injector, including the Transport Lines, is equipped with stripline-style BPMs. The original booster synchrotron BPM electronics used a commercial multiplexer to switch between several BPM signals into an in-house built analog BPM processor [8]. In the Linac-To-Booster (LTB) and Booster-To-SPEAR (BTS) Transport Lines 1990's-era Bergoz BPM processors have provided reliable shot-by-shot single-pass data at 10 Hz with limited resolution [8]. As an upgrade to the original Transport Line BPM processors, two smaller-diameter stripline BPMs connected to two SLAC-built uTCA-based BPM processors replaced the last two BPMs at the end of the BTS in 2015 (BTS BPMs 8 and 9). This system has proven hard to maintain and we have evaluated single-pass SPARK-EL processors as a replacement. The units were tested in the BTS and LTB Transport Lines demonstrating comparable position resolution to the uTCA processors at the small-diameter striplines, as well as substantially improved resolution at the large-diameter striplines.

Since these BPM processors, as well as the BLMs, have the same base hardware and software, we wanted a unified architecture of deploying and managing these modules. We aim for an architecture that allows for easy swaps in the event of a module failure, but additionally gives us the flexibility to bring modules online for testing or to relocate modules and change the EPICS Process Variable (PV) prefix they publish appropriately. All these requirements come down to having the ability to dynamically change the EPICS PV prefixes. We perform this through an external EPICS soft Input/Output Controller (IOC) that manages the information for the prefixes and settings. Each module runs a shell script that acquires all this information and starts its IOC with the appropriate prefix and settings. This work is organized as follows: we begin by explaining our considerations for choosing this deployment architecture and then give a high-level description of our solution. Subsequently we describe the infrastructure that is needed to implement this architecture and the details of how a module boots and acquires its PV prefixes. Finally, in the appendix we show certain important code snippets.

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SPEAR3 operates with a very small accelerator team; typically only one person is an expert on any given system, with a second person having some knowledge about it. As a result in deploying new electronics systems we are aiming for architectures that if a module fails, an operator can swap the failed module with a spare with only minimal guidance.

Using the uSD card involves hard-coding the PV prefixes and settings in the card. Note that the uSD card can itself become corrupted. Therefore for each physical BPM we need to maintain two uSD cards. The cards themselves are small and labeling them is very hard, thus making management difficult. In addition, it is time consuming to upgrade the firmware in the event of a software update from Libera; we would need to update all the uSD cards including the spares. Alternatively we could have one uSD card template where someone would have to clone during a module swap and change the settings. Most operators, however, do not have the skills to perform this task. Additionally in the BTS the different BPMs are physically different and need different configuration, thus increasing the chances of an error during a module swap.

SOLUTION OVERVIEW

TUPP12

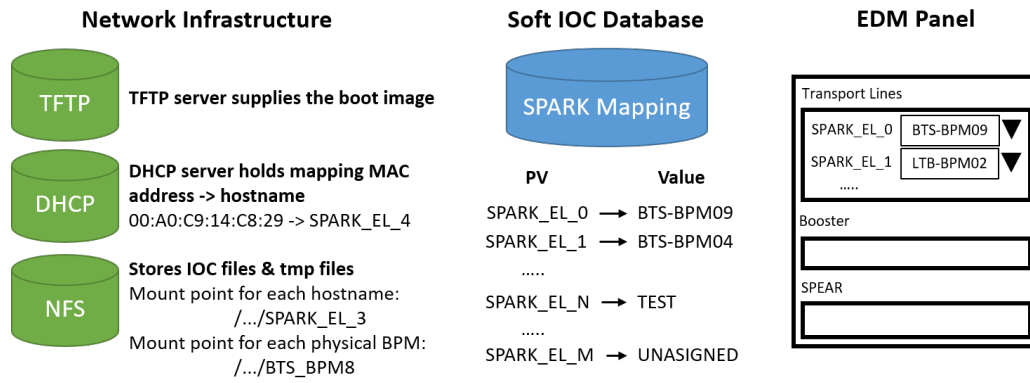


Figure 1: Overview of the Infrastructure needed to perform Network Boot with a Hostname/PV prefix Soft IOC database.

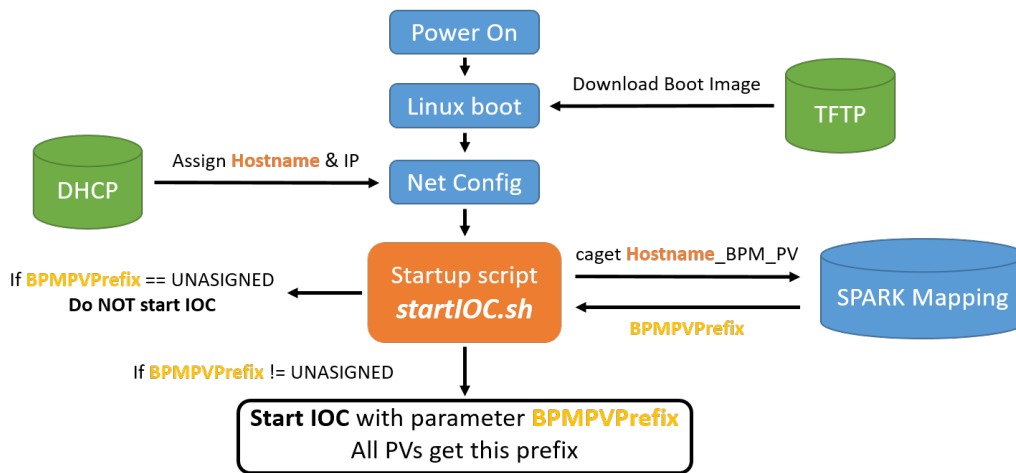


Figure 2: Simplified boot sequence of a SPARK module.

BPM number within the Transport Line, i.e. BPM08. In our implementation these two PVs for module with host-name \$UNITNAME are SPARKMgr:\$UNITNAME:BPM:TL and SPARKMgr:\$UNITNAME:BPM:BPM. The options for SPARKMgr:\$UNITNAME:BPM:TL are LTB, BTS, TEST, and UNASSIGNED, while for SPARKMgr:\$UNITNAME:BPM:BPM the options are BPM01 through BPM09. At boot time a script in the module will query these two PVs and determine the BPM prefix, i.e. SPARK-BTS-BTS08. We further use this soft IOC to hold the settings for each BPM, such as gains and offsets. We do this with another set of PVs per BPM, i.e. SPARKMgr:SPARK-BTS-BTS08:Kx.

Finally a set of EDM panels are needed as an interface to this system. One EDM panel shows the list of SPARK modules and for each module the assignment of Transport Line and BPM number within that Transport Line, and similarly for the Booster and SPEAR3. Another EDM panel holds the settings for each physical BPM.

MODULE BOOT SEQUENCE

Figure 2 illustrates the boot sequence of each SPARK module. When the unit powers on it announces itself to the

network and TFTP supplies the linux Boot Image. Then linux starts running and it gets from DCHP the hostname and IP based on its MAC address.

Eventually the startIOC.sh scripts executes. We have modified this script from what was supplied from Libera to perform the following steps:

1. Query PVs on the soft IOC based on its hostname and calculate the PV prefix for the module's IOC.
2. Perform a series of checks that this PV prefix is valid in the accelerator, and additionally that there is no other IOC on the network running with it. This PV prefix is written in a temporary file read by the st.cmd.
3. Query PVs on the soft IOC based on the PV prefix to obtain the settings for the physical BPM, i.e. gains and offsets. These settings are written in another temporary file as EPICS dbpf commands read by the st.cmd after the iocInit().
4. Start the IOC with procServ and a modified st.cmd to read the PV prefix and settings.

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