Submit to	Department of Energy, Office of Energy Efficiency and Renewable Energy
Nature of Report	Final Technical Report
Project Name	SiC Based Modular Transformer-less MW-Scale Power Conditioning System and Control for Flexible CHP System
Award Number	DE-EE0008410
Award Type	Cooperative Agreement
Recipient Organization	University of Tennessee
Principal Investigator	Fei (Fred) Wang, Professor, fred.wang@utk.edu, (865)974-2146
Team Members	Chattanooga Electric Power Board North Carolina State University General Electric Oak Ridge National Laboratory
Business Contact	Allyson Graves Office of Sponsored Programs Office of Research & Engagement The University of Tennessee, Knoxville 1534 White Avenue, Knoxville, TN 37996-1529 Phone: 865-974-3466 Email: osp@utk.edu
DUNS Number	00-338-7891
Reporting Period	Start: 10/1/2018, End: 12/30/2022
Report Date	03/30/2023

ACKNOWLEDGEMENT

This material is based upon work supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under the Advanced Manufacturing Program Award Number DE-EE0008410."

CONTENTS

EXECUTIVE SUMMARY

This project aims at developing a SiC-based, modular, transformer-less (60-Hz-transformers-free), MW-scale, four-wire DC/AC power conditioning system (PCS) converter, and a corresponding control system for flexible-CHP (F-CHP) systems. With the help of an F-CHP controller and power electronics converters, different CHP sources, renewable sources, and batteries can be assembled to the DC grid, which is then connected to the medium voltage (MV) AC grid through the PCS converter. To meet grid support and performance requirements, the F-CHP controller design and PCS converter design follow IEEE 1547 and IEEE 2030.7 standards. Five main tasks, including PCS converter design, F-CHP controller development, PCS converter prototype building and testing, F-CHP controller testing, and PCS paralleling, have been carried out. In this project, the F-CHP controller testing has been completed in simulation, HIL and HTB, and the PCS converter prototypes have been successfully built and tested.

Different CHP sources, including microturbine, fuel cell, and 60Hz energy source, could be supported by this system. It can also integrate renewable resources and energy storage systems. The PCS converter and the F-CHP central controller play significant roles in this system, supporting both the F-CHP system and the MV AC grid.

The MV PCS converter prototype has been built and tested under the full rating of 13.8 kV and 100 kVA. The line-to-line voltage is around 13.8 kV, and the total power output is 100 kVA. The PCS efficiency of 98.4%, voltage control bandwidth of 300 Hz, and current control bandwidth of 1.1 kHz have been tested. The insulation capability of inductors, transformers, and power stages have all been tested. The converter performances on grid functions, such as voltage ride-through, frequency-ride-through, protection, etc. have also been tested.

The F-CHP central controller has been first tested in HIL. Several CompactRIOs have been used as the central controller and local controllers, and an OPAL-RT has been used as the simulator. All functions, including black start, grid-connected operation, islanded operation, reconnection, grid fault and islanding, and internal component fault handling have been tested in HIL. Then, the F-CHP central controller has been tested in hardware testbed (HTB), in different operation conditions, including system startup, grid-connected operation, islanded mode operation, planned and unplanned islanding, reconnection, and grid faults.

1. INTRODUCTION

1.1 BACKGROUND

Combined heat and power (CHP) systems can provide both electricity and heat for clients [1, 2]. CHP systems have mostly saturated the large industrial facility market, where economies of scale and the required presence of technical staff make the deployment of large systems—greater than 20 megawatt (MW) electrical capacity—cost effective and practical [1]. There remains, however, substantial room for growth of smaller CHP systems suited for small and mid-size manufacturing facilities [1].

However, in order for CHP systems to seamlessly integrate with the grid and provide more advanced grid services, further technical development is needed. In particular, the development of advanced power electronics and controls for flexible CHP systems is needed to meet grid interface standards, have the ability to respond to rapidly changing grid conditions, and achieve high resiliency and low cost [1]. Renewable sources, e.g. PV and wind etc., can also be combined with the CHP system, to achieve further economical operation and dispatch capability [3].

This project aims to address this challenge by developing a MW-scale modular silicon carbide (SiC)-based power conditioning system (PCS) and a corresponding control system for flexible CHP applications. The PCS is capable of grid support functions, such as low/high frequency and voltage ride through, as well as dealing with other abnormal grid conditions, including unbalance, faults, and overvoltage. The transformer-less (i.e., no 60 Hz transformers) PCS utilizes a four-wire system to support both three- and single-phase loads. It takes advantage of fast-switching SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) to enable additional system-level functions like harmonic filtering and stability enhancement, as well as feature a lighter and more compact modular design. The technology developed enables automatic control of the CHP grid support functions.

1.2 OBJECTIVE AND MAIN TASKS

The objective of this research is to develop a SiC-based, modular, 60-Hz transformer-less, MW-scale, four-wire DC/AC power conditioning system (PCS) converter and corresponding control system for the flexible-CHP (F-CHP systems). The conceptual diagram of the F-CHP system is shown in Fig. 1-1. The targets of the proposed PCS and F-CHP controller are listed in Table 1-1.

There are two main tasks in the project:

- Develop and test the MV PCS converter, based on 10 kV SiC MOSFETs. The PCS for F-CHP should be 1) capable to integrate with all types of CHP sources, 2) modular and 60-Hz transformer free for resiliency, scalability to MW level and low cost; 3) can deal with unbalanced loads and abnormal grid-conditions and provide extra system benefits (power quality and stability enhancements) utilizing SiC fast switching capability; 4) meet IEEE Std. 1547 and 2030.7 with the PCS controller.
- Develop the F-CHP central controller. The controller should achieve: 1) can integrate with different CHP sources including 60-Hz sources and functions together or independent of the PCS; 2) can meeting IEEE DER and microgrid standards, be easily integrated with existing distribution grid controller, and provide grid-support functions; 3) enable automatic transfer between various operation modes including a dynamic microgrid boundary to maximize utilization of resources and better resiliency/reliability; 4) based on general-purpose controller hardware and easy to deploy for reduced cost.

In order to achieve the goals, there are three critical success factors including: 1) PCS converter design with low cost which meets grid requirements and provides sufficient grid support functions; 2) flexible and low-cost F-CHP controller development; and 3) validation testing.

Table 1-1. Targets of proposed PCS and F-CHP Controller

Voltage level	LVDC (800 V to 1 kV), MVAC (13.8 kV)	Voltage and current control bandwidth	300 Hz and 1 kHz (enhanced grid support functions, e.g., harmonic filtering, stabilizer)
Full load efficiency	98%		
Power rating	2 units PCS (3-phase 100 kW for each)		
Grid requirements and control targets		1) conform with IEEE 1547 and IEEE 2030 for grid interface control; 2) grid support functions including var support, low voltage ride through (LVRT), protection, stability, and harmonic filtering; 3) multiple operation modes including grid connected, islanded and stand-by; 4) unbalanced load (max 33%) and fault;	

	5) uninterrupted power for facility loads; 6) ±5% LVDC voltage variation

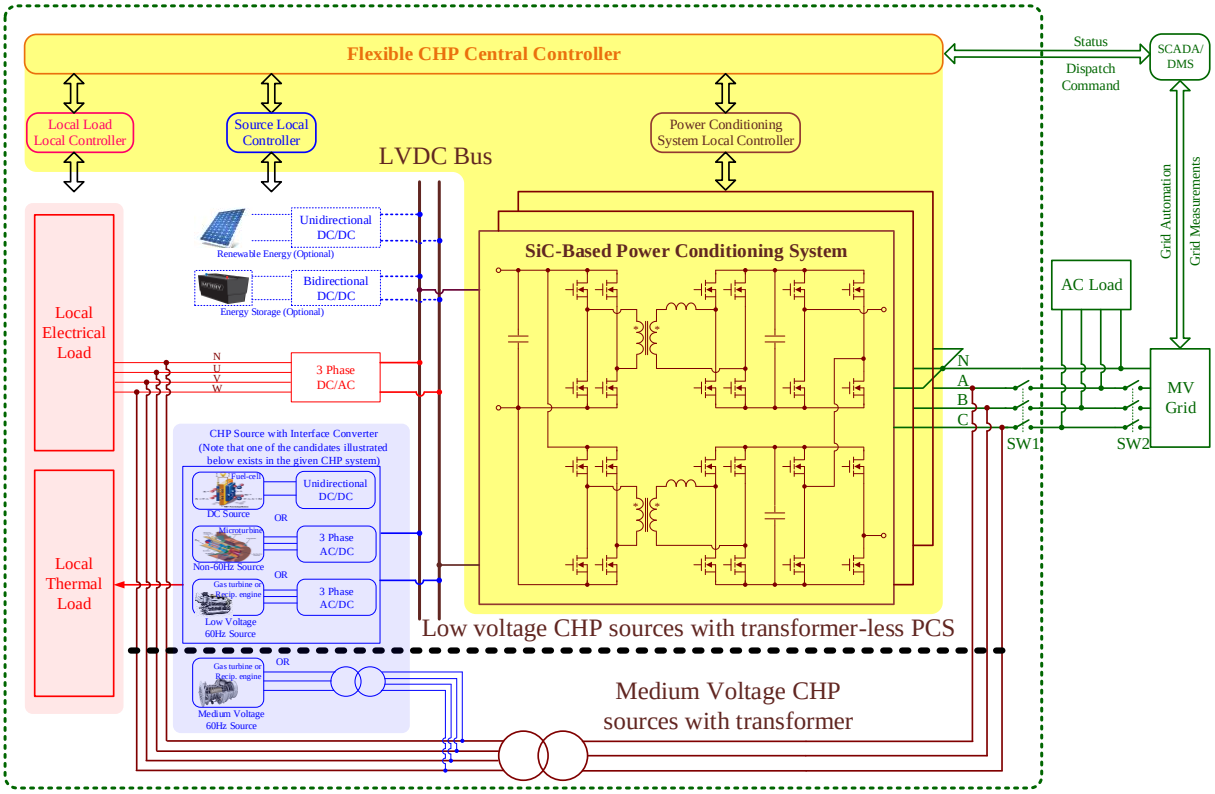


Fig. 1-1. Conceptual F-CHP System (PCS and Controller highlighted with yellow background)

1.3 TECHNICAL APPROACHES

To achieve the above targets, three key technology development tasks are planned as shown in Fig. 1-2, including: 1) PCS converter development; 2) F-CHP Controller development; and 3) Scalable PCS converter development. The approach to addressing these key technologies and their feasibility based on our previous work are highlighted as follows.

1.3.1 PCS converter development

First, the grid requirements of a PCS converter for F-CHP have been identified. These requirements include, but are not limited to LVDC power quality for the local electrical loads in the CHP site, and MVAC grid side active/reactive power support, low voltage/frequency ride-through, islanded mode operation, seamless mode transition, black start support, protection, unbalanced load, fault isolation, stability, and harmonic filtering. The F-CHP PCS converter has been designed considering grid requirements for both LVDC and MVAC sides. The converter accommodates unbalanced loads in a four-wire AC system. The grounding, topologies and modulation methods considering common mode voltage reduction in the transformer-less system are also considered in the design. The grid function requirements on passive selection, device current rating, insulation, etc., have been determined.

The grid functions of the PCS converter can be first validated with UTK's low voltage HTB, including voltage/current bandwidth, LVRT, unbalanced load, and grid fault. A MV test platform has been built to validate these grid functions at the rated voltage and power rating. A grid emulator

converter has also been implemented by a low voltage converter with a step-up transformer. The grid voltage and frequency, faults, and unbalanced load can be easily emulated by controlling the converter.

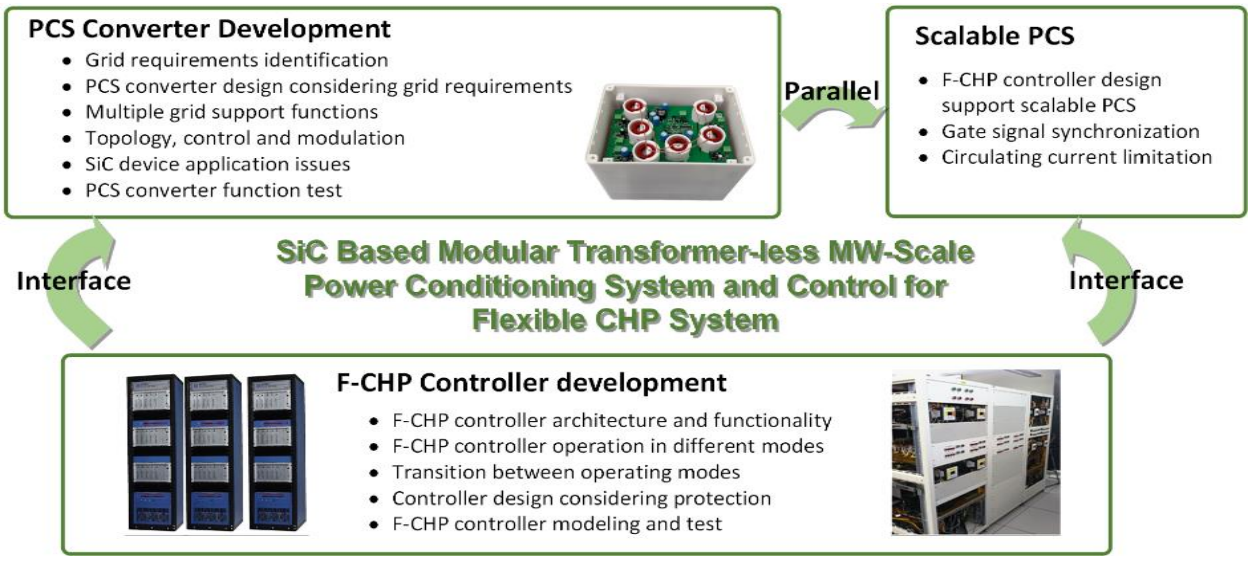


Fig. 1-2. Key technology summary

1.3.2 F-CHP Controller development

The proposed F-CHP Controller is comprised of two layers, including a CC, and LCs for the sources, local loads, and the PCS. The CC communicates with the distribution grid SCADA, and achieves system-level control and energy management functions. Meanwhile, it communicates and supervises each LC to ensure stable operation in both grid-connected and islanded modes. The PCS LC determines the operating modes of the PCS according to the operating state of the F-CHP system: (1) the PCS may provide stable voltage reference during islanded operation; or (2) output active and reactive power during grid-connected operation. The Source LC coordinates the CHP and all other renewable energy sources or energy storage to serve the local loads. Also, the Local Load LC may shed or restore the loads for economic purposes such as peak shaving and demand response. Note that the proposed controller is independent of the PCS and can work with existing CHP. The basic F-CHP operational principle has been achieved in both islanded and grid-connected operation modes. The transitions between different modes have also been studied.

This project utilizes the National Instruments (NI) development and multi-function LabVIEW software. They are also used by UTK for developing microgrid controllers, and in the HTB which is used to validate the developed F-CHP system and controller. Three steps have been taken to test the proposed F-CHP controller: (1) Computer based simulation test; (2) Controller hardware in the loop (HIL) test; and (3) HTB with actual scaled down PCS test.

1.3.3 Scalable PCS converter development

It is more reliable and economical to scale modular PCS converters, to achieve the needed power for a given F-CHP. Consequently, it is necessary to parallel multiple PCS. The paralleled PCS converters can be controlled by one PCS LC. Therefore, the PCS LC should be designed with capability for multiple paralleled PCS converters. There are two main challenges for converter paralleling: (1) circulating current ripple at the switching frequency, and (2) circulating current at fundamental frequency. It has been proven that the switching frequency ripple can be filtered by the PCS DC/AC inductors, while the fundamental frequency circulating current can be suppressed

by the PCS controller in the paralleling mode. Several structures of paralleling modular F-CHP PCS and corresponding protection issues have also been discussed.

1.4 ORGANIZATION OF THE REPORT

The rest of the report is organized as follows:

Chapter 2: "F-CHP PCS Design" discusses the hardware and controller design and tests with medium voltage SiC devices and transformer-less configurations as well as grid requirement.

Chapter 3: "F-CHP Controller Design" presents the requirement, design and tests of the central controller and local controllers in the F-CHP system.

Chapter 4: "Scalable PCS Development" provides a detailed discussion on different scenarios of PCS paralleling, PCS control strategy and corresponding test validation.

Chapter 5: "Summary" provides a concise summary of the completed work in this project.

2. F-CHP PCS DESIGN

To develop the SiC-based, modular, transformer-less (i.e., no 60 Hz transformers), MW-scale, four-wire DC/AC PCS, the converter ratings should be first identified, considering grid requirements. Then, the converter at MW-level has been designed. After the MW-level converter has been successfully designed, the two 100-kW PCS units have been implemented and tested up to the full rating on the LVDC (800 to 1000 V) and MVAC (13.8 kV), with grid transients.

2.1 GRID IMPACT ON CONVERTER DESIGN

To figure out the grid impact on the PCS converter design, the specification is listed below in Section 2.1.1. Then, with the specifications, the converter baseline design and grid requirement impact can be studied. The final conclusion has been drawn in 2.1.2 with the final design of the MW-level converter considering grid standard requirements. The technical approach of studying the grid impact is shown in Fig. 2-1.

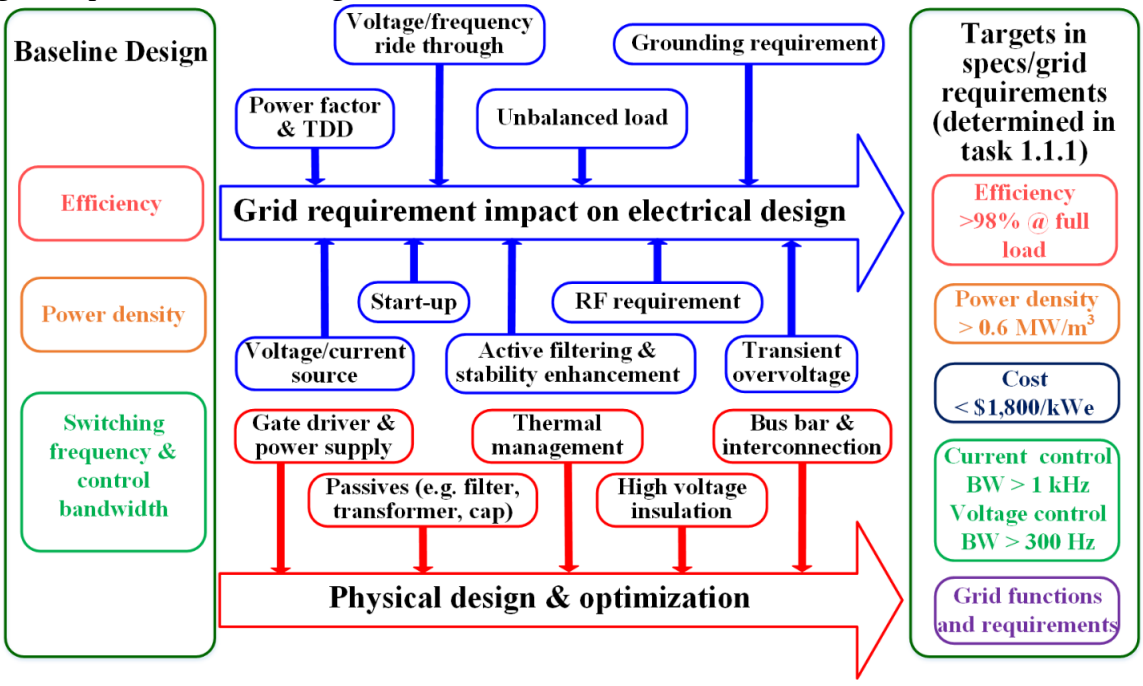


Fig. 2-1. Technical approach of PCS converter design considering grid requirements

2.1.1 PCS specification and baseline design

2.1.1.1 PCS specification

To begin with, the specifications and grid requirements of the CHP PCS converter, including power rating and voltage rating and requirement for grid application (4-wire system, unbalance load support, grounding system, PCS module protection, low voltage ride-through and fault, transient overvoltage etc.), as given in Table 2-1. It should be noted that LVDC bus voltage (i.e., 850 V) is determined to support fuel cells, 480V microturbine and 60Hz CHP source, and 480V 4-wire local grid.

Table 2-1. Specifications and grid requirements of PCS converter

Parameter	Value
Power rating	1 to 20 MW
MVAC voltage rating	13.8 kV (-12% ~ 10%)
LVDC voltage rating	850 V (-5% ~ 5%)
Power factor	Four-quadrant operation
TDD in MVAC	5% (IEEE Std 1547)
Efficiency	98%
Ambient temperature	-25ºC ~ 55ºC
Cooling	Forced air (liquid if necessary for HF transformer)
Power density	> 0.6 MW/m^3
Cost	<$1,800/kilowatt rated electrical power
Reliability	MTBF > 10 years
Fault	1) AC side fault including three-phase and single-phase grounding, and phase-to-phase short 2) Overvoltage and overcurrent fault in LVDC bus
Grounding	1)Chassis grounded 2)Midpoint of LVDC grounded 3)MVAC side: Neutral is grounded in grid-connected and islanded modes; No impact on temporary over voltage/current level under ground faults for existing grid; No impact (or minor change) on ground fault protection for existing grid.
MVAC side functions	1)Low/high voltage ride through follow IEEE Std 1547 2)Low/high frequency ride through follow IEEE Std 1547 3)Active power for frequency support, reactive power/power factor for voltage support 4)Current source operation for grid-connected mode, voltage source operation for islanded mode 5)Voltage ride through in islanded mode 6)Active power filtering 7)Stability enhancement 8)Seamless mode transition between islanded/grid-connected mode 9)Start up both from LVDC and MVAC sides 10)Ground fault isolation between MVAC and local load side
LVDC side functions	±5% LVDC voltage variation
Unbalance load support	33% unbalance load support for AC grid side, <4% voltage variation, 120 +/- 2.8˚
RF requirement	47 CFR 1.1307 (FCC standard)
EMC requirement	1) No requirement in MVAC 2) FCC 15 CLASS B in LVDC
Control bandwidth	voltage control bandwidth > 300 Hz, current control bandwidth > 1 kHz
PCS protection (external)	Over-voltage protection, over-current protection, under-voltage, ground fault
Transient overvoltage	Lightning and switching overvoltage

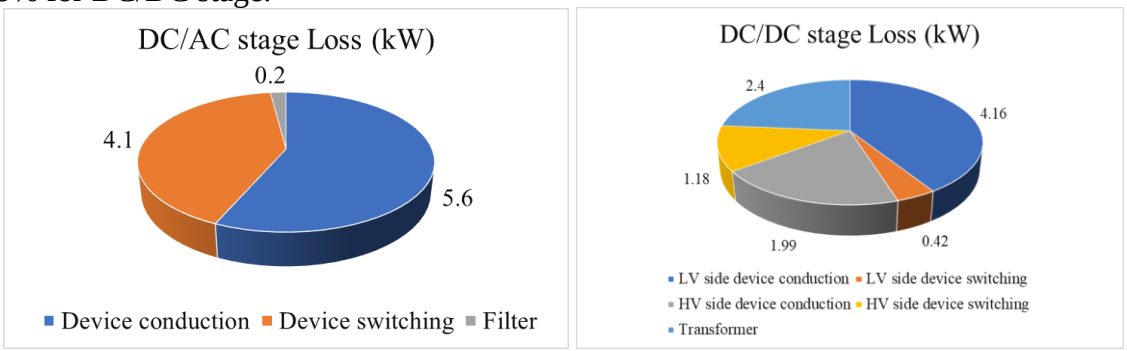
2.1.1.2 Baseline design of the MW-level PCS

The baseline design of the MW-level PCS hardware is shown in Table 2-2 below.

Table 2-2. Baseline design of the PCS

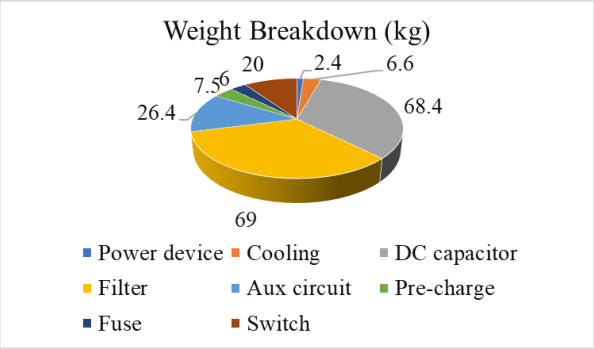
DC/AC stage (CHB based)		DC/DC stage (DAB based)	
Parameter	**Value**	**Parameter**	**Value**
Power rating	1 MW	**Power rating**	167 kW each/1 MW total
AC voltage rating	13.8 kV	**DC voltage (LV)**	850 V
Topology	5-level Cascade H-bridge (2 SMs in each phase)	**DC voltage (HV)**	6.6 kV
		Topology	Dual active bridge
DC voltage/current ripple of H-bridge	Voltage rating: 6.3 kV, current ripple: 27 A	**Transformer**	Ratio: 7.76:1, Magnetizing: 5 mH, leakage inductance: 36 uH, current rating: 230 Arms (LV), 38.9 Arms (HV)
DC capacitor	114 μF		
Max AC current	72 A	**DC link capacitor**	27 mF
Power factor	-1.0 ~ 1.0	**Switching frequency**	10 kHz
Switching frequency	10 kHz	**Power device**	LV: > 1.7 kV/251 A MOSFET
Power device	> 10 kV/72 A MOSFET		HV: > 10 kV/32 A MOSFET
Filter	6.7 mH (1.3%) / 72 Apeak	**DC bias limitation**	DC control + air gap transformer
Modulation	Phase shift PWM	**Modulation**	Single phase shift

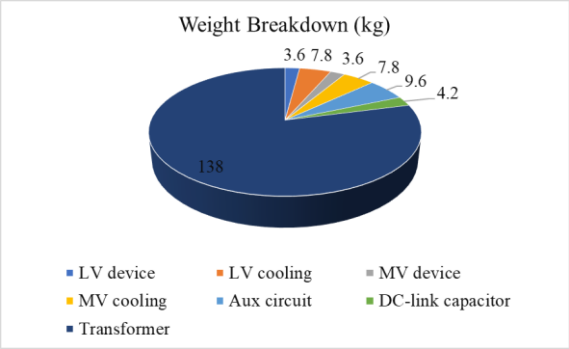
Fig. 2-2 to Fig. 2-4 shows the baseline design results of the PCS converter including DC/AC and DC/DC stages. The overall weight is 380.9 kg consisting of 174.6 kg for DC/DC stage and 206.3 kg for DC/AC stage. The overall size is 0.383 m3 consisting of 0.147 m3 for DC/DC stage and 0.236 m3 for DC/AC stage. The overall efficiency is 98% while 99.01% for DC/AC stage and 98.99% for DC/DC stage.



(a) (b)

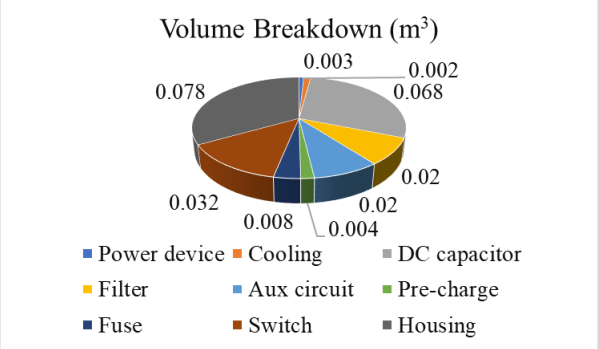
Fig. 2-2. Power loss of PCS: (a) DC/AC, (b) DC/DC

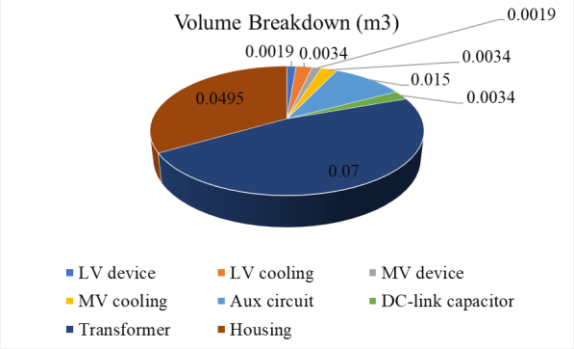




(a) (b)

Fig. 2-3. PCS weight breakdown: (a) DC/AC, (b) DC/DC





(a) (b)

Fig. 2-4. Volume breakdown of PCS: (a) DC/AC, (b) DC/DC

As estimated, the total specific power is 2.62 kW/kg, and the power density is 2.6 MW/m3.

2.1.2 Design with grid requirements

2.1.2.1 Grid impact study

Based on the baseline design, evaluations can be performed considering several grid conditions, stated in Table 2-1 and in IEEE standards. The studied grid impact on DC/AC PCS is shown in Table 2-3. The DC/DC stage impact of system requirements are shown in Table 2-4.

Table 2-3. Grid requirement impact on PCS

Grid Functions	Impact on PCS design (Compared to baseline)
Voltage/current mode operation	Control: control algorithm for both voltage and current mode Hardware: no impact
Start-up	Control: control program for start-up Hardware: pre-charge circuit in AC side
Low and high voltage ride through	Control: Current overshoot limitation; Proper voltage controller parameters; Hardware: DC link voltages increase from 6.3kV to 6.67kV; Capacitor voltage should increase too
Grid faults	Control: Need to cease to energize or trip when the healthy phases have higher voltages than 1.2pu, HV protection of DC link. Hardware: No impact
Unbalance load support	Control: unbalance mitigation control scheme Hardware: four-wire system

Frequency ride through	Control: Current overshoot limitation(same as LVRT) [4, 5]; Frequency adaptive controller; Hardware: Larger HV DC-link capacitance due to higher HV DC-link voltage ripple during LFRT;
Transient overvoltage	Control: No impact Hardware: 10.2kV Arrester for lightning and switching overvoltage; insulation meets BIL requirement [6]
LVDC voltage quality	Control: Proper control bandwidth of PCS LVDC control Hardware: Larger LVDC capacitor to maintain LVDC voltage under source/load change

Table 2-4. DC/DC design considering system requirements

Grid Functions	Impact on PCS design (Compared to baseline)
Basic control scheme	Control: Voltage/Power control modes and mode transition control needed Hardware: No impact
DC bias current	Control: Intermediate phase shift loading, PWM duty cycle control Hardware: Transformer magnetizing inductance need to be reduced
Second order DC link fluctuation	Control: PIR controller and second order harmonic suppression needed Hardware: No impact
Short/Open circuit operation	Control: PWM blocking for SC protection; Forced LVDC control mode during LVDC overvoltage Hardware: LV side Voltage sensing needed
System paralleling/output balance	Control: Dual PI loop for LV Mode, MV balance for CHB needed Hardware: Current Sensing in MV
Lightning impulse	Control: No impact Hardware: 95 kV BIL for MV winding
LVDC bus transient	Control: No impact Hardware: enlarged LVDC capacitor bank

2.1.2.2 PCS design with grid requirements

With the grid impact considerations, the PCS design has been modified to comply with the grid requirements. The design summary of DC/AC is shown in Table 2-5. Other than the grid functions, the lightning arresters, pre-charge circuits and protection sensors, fuses and switches are also selected.

Table 2-5. PCS DC/AC power stage design summary

Components	Baseline	Considering grid requirements
Device	Efficiency: 99%; 10 kV / 60 A SiC MOSFET; Junction temperature under normal operation: 150 ºC; Size: 2.34 L; weight: 2.4 kg;	Efficiency: 99%; 10 kV / 60 A SiC MOSFET; Junction temperature under normal operation: 125 ºC; Size: 2.34 L; weight: 2.4 kg;

Cooling	Water cooling; Inlet coolant temperature: ≤76 ºC; Flow rate: 1 pgm; Cold plate size: 3.34 L; weight: 6.6 kg;	Water cooling; Inlet coolant temperature: ≤51 ºC; Flow rate: 1 pgm; Cold plate size: 3.34 L; weight: 6.6 kg;
DC-link Capacitor	DC-link voltage: 6.3 kV (±5%); DC-link capacitance: 114 μF; Capacitor: TDK B25620B1447K983(4 in series); Size: 68.5 L; weight: 68.4 kg;	Considering HVRT and LFRT: DC-link voltage: 6.67 kV (±5%); DC-link capacitance: 106 μF; Capacitor: TDK B25620B1447K983(4 in series); Size: 68.5 L; weight: 68.4 kg;
Inductor	Inductance: 4.4 mH; Current: 44 Arms / 63 Apk; Size: 20.1 L; weight: 69 kg;	Considering LVRT, fault, lightning, and switching transient overcurrent: Inductance: 4.4 mH; Current: 44 Arms / 200 Apk; Size: 39 L, weight: 170 kg;
Arrester	none	Considering lightning and switching: SIEMENS 3EK7 120 - 3AC4; Size: 9.1 L; weight: 5.6 kg;
Pre-charge circuit	Resistor: TAP600K10KE; relay: RL 38-h; Size: 4.1 L; weight: 7.5 kg;	
Sensors and sampling	MVDC-link voltage sensor, AC voltage sensor, AC current sensor	
Fuse	Littelfuse 15NLE50E; Size: 8.3 L; weight: 6 kg	
Switch	ABB VSC12; Size: 32 L; weight: 20 kg;	

Similarly, the design of DC/DC power stage and transformer are also modified, as shown in Table 2-6 and 2-7.

Table 2-6. DC/DC transformer design summary

	Grid impact design	Baseline design	Change
Insulation	8.5 mm for 95 kV BIL	2.76 mm for 13.8 kV	Lightening requirement
Core	VAC W160, 6 parallel 2.52*6=15.12 kg	VAC W159, 8 parallel 1.57*8=12.56 kg	Larger core with less parallel due to increased winding area requirement
Flux density	0.655 T, 237.4 W	0.7415 T, 208.9 W	Reduced because increased winding area leads to a larger core, core loss increases
Gap	Magnetic gap, 0.14 mm*2	Magnetic gap, 0.11 mm*2	For dc bias detection, provide 10 A low load ZVS current
Current density	2.6 A/mm2, 171.7 W	3.2 A/mm2,183.9 W	Reduced to limit total loss with a higher core loss
Window utilization	0.277	0.354	Reduced due to higher insulation
Primary winding	7 turns, 1 layer, 3.42 kg	7 turns, 1 layer, 4.34 kg	Increase to reduce core loss
Secondary winding	56 turns, 2 layers, 4.02 kg	56 turns, 2 layers, 4.51 kg	Increase to reduce core loss Rectangle Litz wire used

Temperature rise	70 K, 0.89 kg heat sink (Aluminum)	70 K, 1.4 kg heat sink (Aluminum)	Temperature rise kept same for insulation life, and heat sink reduced due to increase surface
Efficiency	99.77%	99.76%	Optimized results
Power density	10.4 kW/dm3 7.08 kW/kg3	14.32 kW/dm3 7.28 kW/kg3	Volume density reduced 30% due to increased winding area, weight density slightly reduced
Leakage inductance	35.9 uH	35.9 uH	Meet leakage inductance requirement

Table 2-7. PCS DC/DC power stage design summary

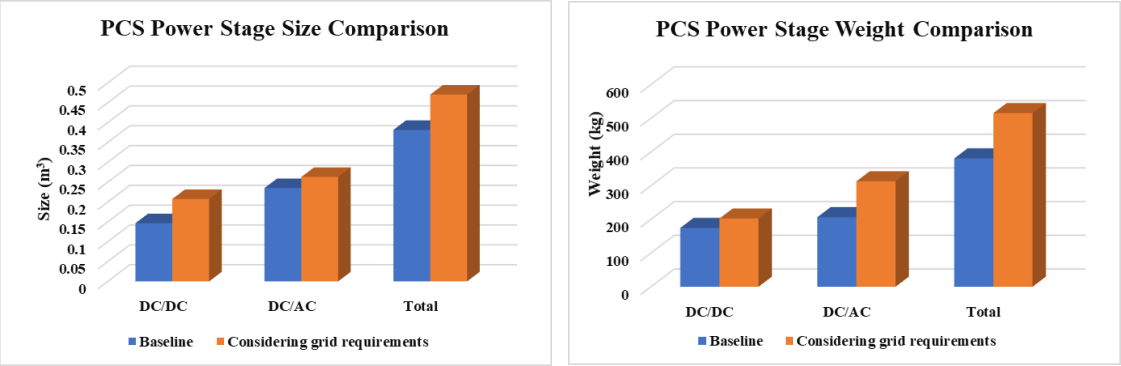
		Baseline	Considering grid requirement
Device Selection	**LV Device**	GE17042CCA3 (1.7 kV 425 A)	GE17042CCA3 (1.7 kV 425 A)
	MV Device	10 kV / 40 A SiC MOSFET	10 kV / 40 A SiC MOSFET
Cooling		Liquid cooling Size: 6.7 L, weight: 15.6 kg	Liquid cooling Size: 6.7 L, weight: 15.6 kg
MV MF Transformer Parameter	**Voltage Rating**	850 V / 6800 V	850 V / 6800 V
	Current Rating	230 A / 29 A	230 A / 29 A
	Leakage Inductance	35 µH	35 µH
	Magnetizing Inductance	1.5 mH	1.5 mH
	Insulation	13.8 kV / 60 Hz continuous	95 kV lightning
LVDC Capacitor		900 V, 138 µF Size: 3.4 L, Weight: 4.2 kg	900 V, 5.4 mF Size: 18.1 L, Weight: 28.8 kg;
Sensing		LV/MV DC Voltage LV/MV Transformer Current DC/DC Output Current	LV/MV DC Voltage LV/MV Transformer Current DC/DC Output Current

Table 2-8 summarized the PCS converter size and weight of baseline design and the design considering grid requirements, and Fig. 2-5 (a) and (b) show the size and weight comparison, respectively. The total PCS converter size and weight are increased after considering the grid requirements. The estimated specific power density would drop from 2.62 kW/kg to 1.93 kW/kg, and the estimated power density would drop from 2.6 MW/m^3 to 2.08 MW/m^3.

Table 2-8. PCS converter design comparison

	Weight (kg)		Size (m^3)		Comment
	Baseline	Grid	Baseline	Grid	
DC/AC stage	206.3	314	0.236	0.271	Most of weight and size increase due to: ➢ Filter inductor because of increasing insulation and overcurrent condition; ➢ Transient overvoltage limitation device (e.g., arrester);

DC/DC stage	174.6	203.1	0.147	0.209	Most of weight and size increase due to: ➢ Transformer because of increasing insulation; ➢ Larger DC link capacitor considering source/load change;
Total	380.9	517.1	0.383	0.480	Specific power: 2.62 kW/kg → 1.93 kW/kg Power density: 2.6 MW/m^3 → 2.08 MW/m^3



(a) (b)

Fig. 2-5. PCS power stage (a) size and (b) weight comparison

2.2 100-KW PCS IMPLEMENTATION

After the grid requirements are discussed, the actual hardware of two 100-kW PCS is then designed and built. Tests have been completed to validate the design for the two PCS systems. The first generation of the F-CHP PCS was developed in Budget Period 2, followed by the Gen. II PCS with modifications to achieve higher insulation capability, higher efficiency and power density.

2.2.1 Design and test of Gen. I PCS

The PCS hardware design mainly consists of MV/LV power stages, MV AC inductors, DC/DC transformers, controller, and the mechanical cabinet.

2.2.1.1 MV power stage design

To limit the medium-voltage (MV) DC-link voltage variation below 5%, the DC-link capacitance is determined at 10 µF. To withstand the voltage (6.7 kV), four 2 kV / 40 µF film capacitors (TDK B25620B1406K981) are connected in series. Since the current rating is low, the PCB-based busbar is designed considering the stray inductance. Forced-air cooling is used to cool the MV SiC devices. The simulation of thermal design is shown in Fig. 2-6. The physical design of the MV power stage is depicted in Fig. 2-7.

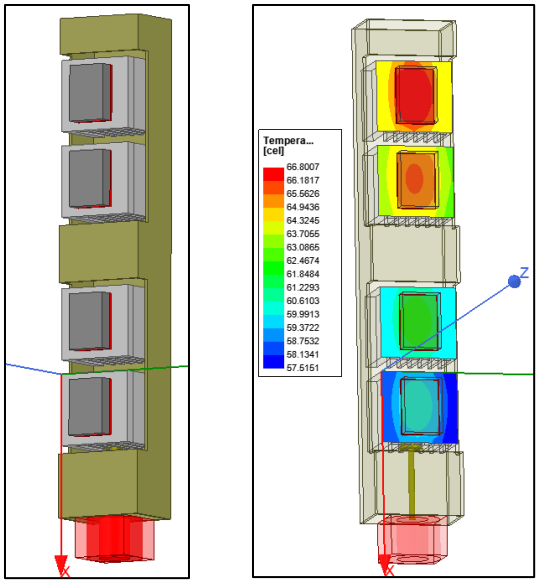
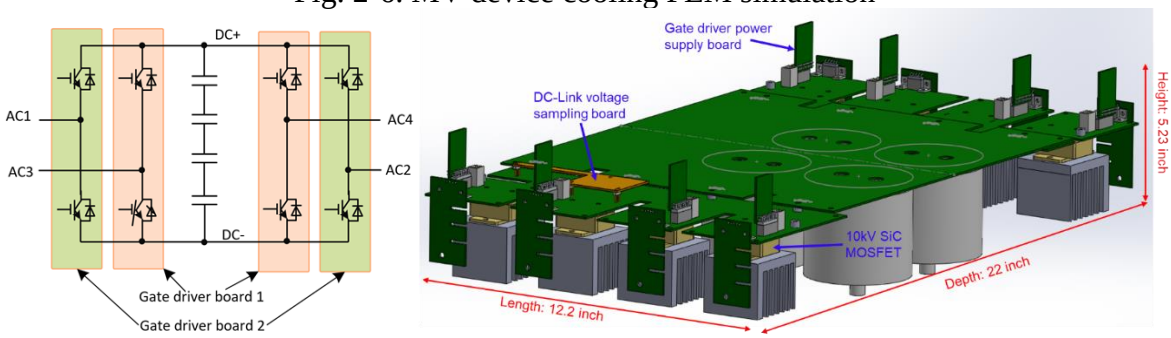


Fig. 2-6. MV device cooling FEM simulation



(a) (b)

Fig. 2-7. MV Power module: (a) schematics, (b) physical drawing

2.2.1.2 LV power stage design

With the LV DC-link capacitance determined to be 105 µF for each stage, the PCS LVDC power stage PCB has been layout, along with the LVDC voltage sensor board. The hardware design of the sensor board and the power stage is shown in Fig. 2-8. Devices of C2M0080170P from Wolfspeed are used.

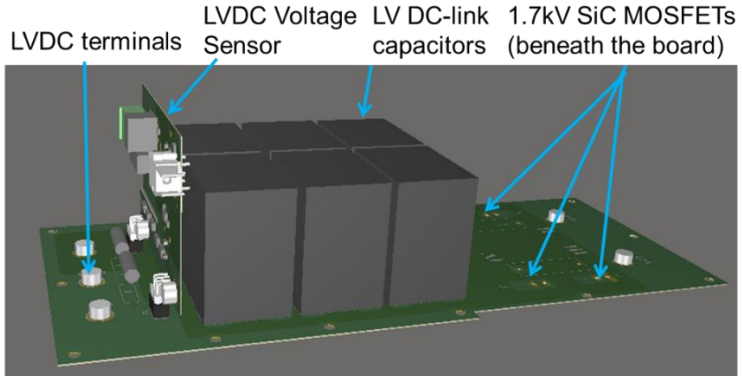


Fig. 2-8. LVDC power stage and sensor board design.

2.2.1.3 MV inductor design

The grid side filter inductance is mainly determined by the current THD requirement (<5%). In addition, the inrush current also affects the inductor design. Some grid conditions can induce inrush current flowing through the inductor, of which the LVRT and lightning are the sever two conditions. Under LVRT, the grid voltage suddenly drops, while the converter would detect the voltage drop after a short delay, and the converter controller needs at least a control cycle to respond to the grid voltage drops. Therefore, an inrush current will occur due to the delay of the converter controller. With the PWM mask function (temporarily mask the PWM output), the inrush current induced by LVRT can be limited. However, during lightning, the inrush current cannot be limited since the grid voltage is much higher than the MVDC voltage, even though the arrester can clamp the lightning surge voltage at a certain level. After considering those conditions, the inductor design requirements are summarized in Table 2-9 [7].

Table 2-9. PCS DC/AC stage inductor design requirements

Parameters		Values
Inductance:		44 mH(0.009 p.u.)
Current rating	Continuous:	4.2 Arms
	Inrush current capability:	15 A (LVRT without PWM mask) 10 A (LVRT with PWM mask) 23 A (Lightning)
Insulation:	Continuous:	13.6 kV (PWM pulse)
	Short duration:	35 kV (60 Hz, 1 minute)
	Lightning impulse:	95 kV (1.2/50 us)
Thermal	Temperature rise:	≤90 ºC

The inductor is designed with an amorphous core to reduce the core loss due to the high switching ripple, and the main design parameters are shown in Table 2-10.

Table 2-10. PCS DC/AC stage inductor design parameters

Parameters	Values
Inductance:	44 mH
Core size:	AMCC0500 (Amorphous)
Steady-state RMS current Irms:	4.2 A
Steady-state peak current Ipeak:	7 A
Maximum inrush current I_{inrush}:	23 A
Winding wire gauge:	AWG#16
Winding turns:	330
Winding wire length:	95 m
Air gap:	5.0 mm
Wire loss:	28 W
Core loss:	18 W

To meet the insulation requirements, the inductor winding is potted with silicone elastomer. To realize the potting, a 3D-printed bobbin is designed. The bobbin divides the winding into several sections to increase the insulation between turn to turn. A case is designed to contain the bobbin and the winding, and there is enough distance between the bobbin and core, between the winding and case, and between the windings on two core legs [4, 7]. The designed inductor is shown in Fig. 2-9. The inductors have past the partial discharge (PD) test and the PD inception voltage (PDIV) is up to 11 kVrms.

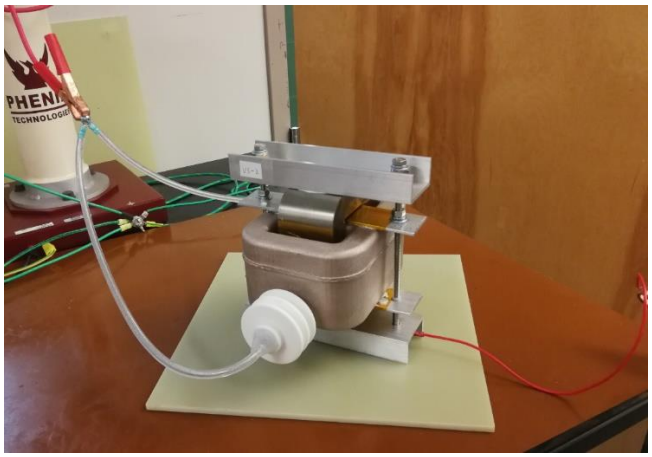


Fig. 2-9. MV inductor

2.2.1.4 MV DC/DC transformer design

The transformer design parameters are shown in Table 2-11. Similar to the MV inductor, the MV winding is encapsulated with silicone elastomer to withstand high voltage between the MV power stage and the LV power stage. Vacuum pressure potting process is implemented for every MV winding to achieve high quality of dry-type insulation.

Table 2-11. Design parameters of 6.7kV/850V natural air cooling MFT

Core	Nanocrystalline	MK Magnetics SC2062M1
	Flux density	0.728 T
	Core loss	30 W
	Magnetic gap	0.2mm * 2 for 3 A
Winding	Current density	Primary: 6.78 A/mm2 Secondary: 4.52 A/mm2
	Window utilization	0.19
	Primary winding:	33 turns, 2 layers
		Litz wire 259 turns AWG36
		Loss 22.6 W
	Secondary:	260 turns, 6 layers
		Litz wire, 50 turns AWG36
		Loss 23.1 W
Temperature rise	65 ºC (Natural Air Cool)	
Efficiency	99.544%	
Power density:	8.94 kW/cm^3	
Leakage inductance:	342 µH	

The MV DC/DC transformer assembled is shown in Fig. 2-10. The partial discharge (PD) test has been conducted for each MV winding, and the PD inception voltages are all around 8.6 kV, which satisfies the testing requirement for the PCS.

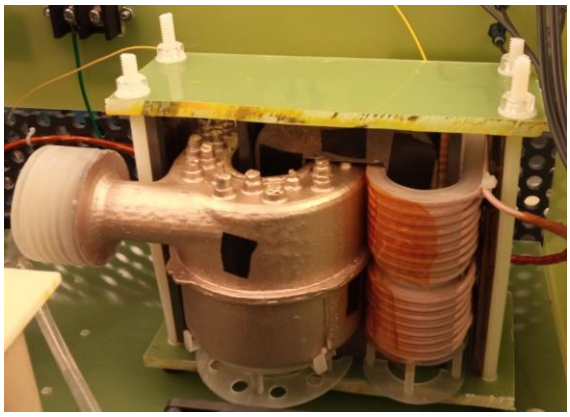


Fig. 2-10. The MV DC/DC transformer assembly.

2.2.1.5 PCS controller design

The main controller board for the PCS converter includes two pairs of FPGA and DSP. Each pair of DSP and FPGA control either DC/DC or DC/AC stage, of which the DSP is going to do the calculation for voltage and current regulators and communicate to upper-level CHP controller, and the FPGA is going to output the gate signals and interface with current and voltage sensors. The controller board uses fiber optics to do communication between controllers and the power stage as well as upper controllers. The detailed structure is shown in Fig. 2-11.

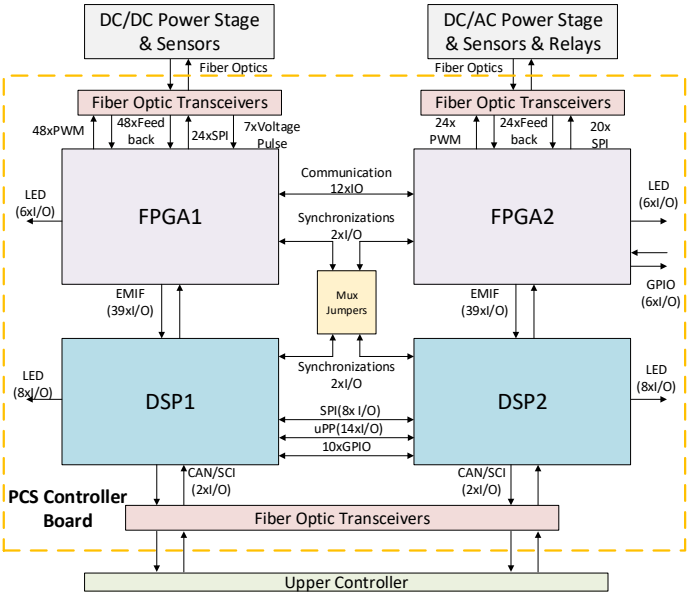
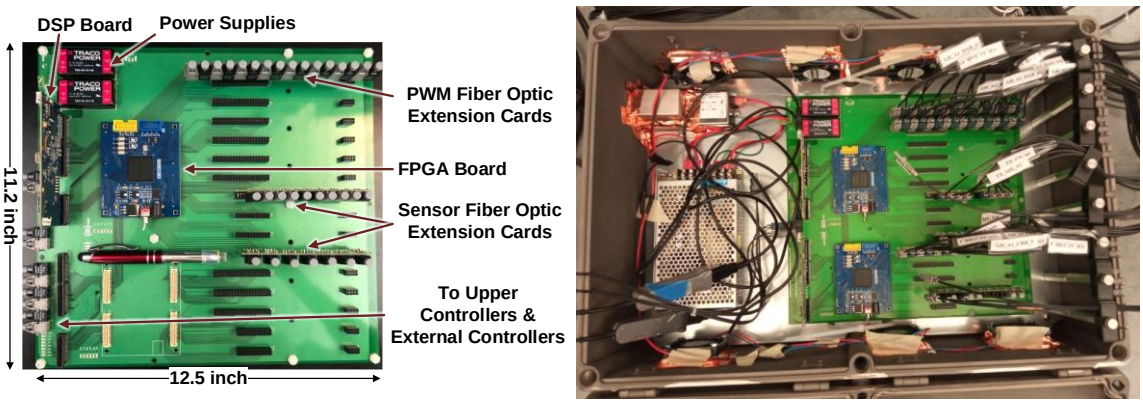


Fig. 2-11. The structure of the PCS controller board.

To facilitate the converter control, a controller box has also been designed, built, and mounted onto the PCS cabinet. The PCS controller board and cabinet are shown in Fig. 2-12.



(a) (b)

Fig. 2-12. The implementation of the (a) PCS controller board, and (b) cabinet.

2.2.1.6 PCS Mechanical design

As shown in Fig. 2-13, the MV power unit consists of a DC/DC stage and a DC/AC stage. It has an LV DC terminal, which is rated at 850V DC, and an MV AC terminal, which is rated at 4 kVrms. There are two power modules in one phase, with the LV side terminals parallel connected and the MV side terminals series connected.

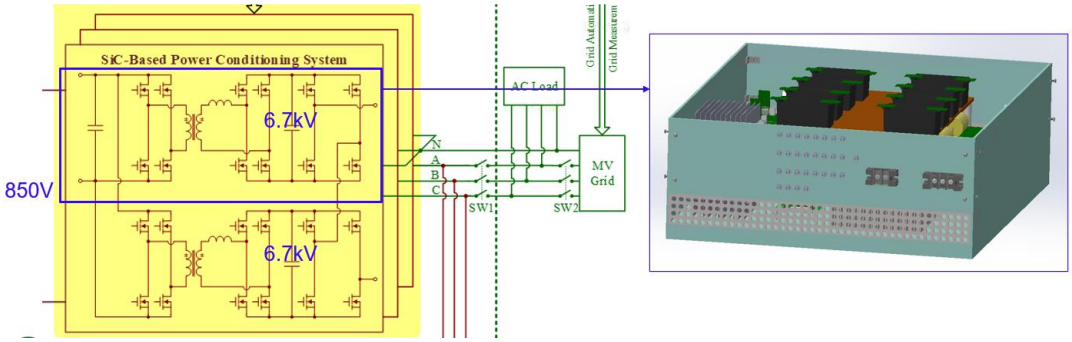
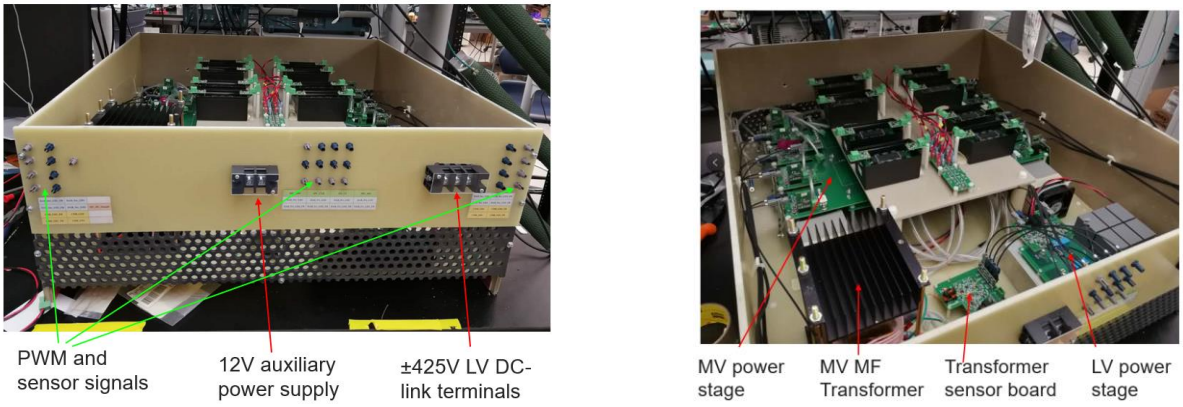


Fig. 2-13. MV power module design

After all of the subsystems are tested, the first power unit is completed with the LV power stage, MV MF transformer, transformer current sensor board, and MV power stage assembled. As shown in Fig. 2-14 (a), the fiber optic connectors, auxiliary power supply, and the LV DC terminals are led out on the front panel. The MV AC terminals can be led out through the rear panel. The inside configuration of the power module is shown in Fig. 2-14 (b).



(a) (b)

Fig. 2-14. MV power module (a) front panel and (b) top view.

The three-phase converter cabinet has also been designed. The cabinet has seven levels, and the top six levels are the three-phase power modules, with two levels for each phase. The bottom level is used to locate the AC side filter inductors, current and voltage sensors, auxiliary power supply, etc. The three single-phase converters are assembled into a three-phase 13.8 kV / 100 kW PCS converter. As shown in Fig. 2-15, all three phases are located in one cabinet, and the converter controller is attached to the side panel of the cabinet.

Fig. 2-15 Picture of the three-phase 13.8 kV/ 100 kW PCS converter

2.2.1.7 Gen I. PCS test results

After the power unit being designed and assembled, several tests have been performed to validate the design.

- **Converter efficiency measurement**

The converter efficiency test is conducted in the single-phase converter with the test setup shown in Fig. 2-16. Since the three phases are identical, the single-phase converter efficiency can represent the three-phase converter efficiency.

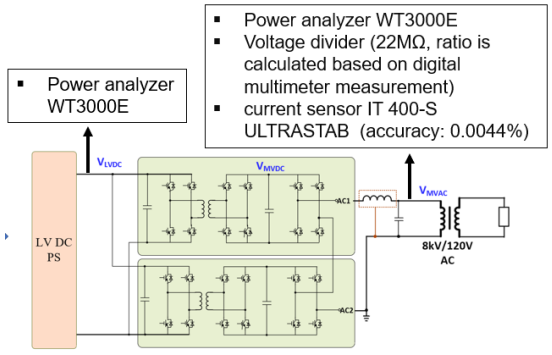


Fig. 2-16. Efficiency test setup with power analyzer at both input and output

The efficiency at the rated power output is around 96.0%, and the test waveform is shown in Fig. 2-18.

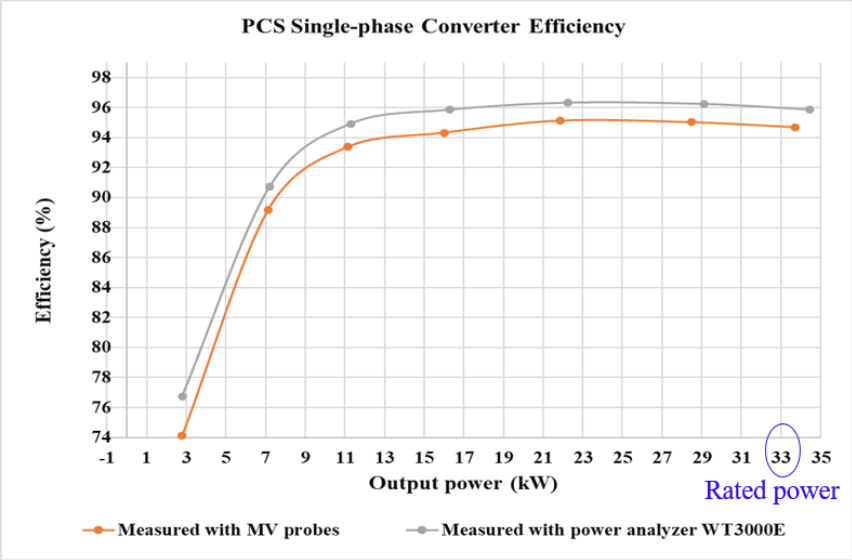


Fig. 2-17. Efficiency comparison between the power analyzer measurement and the oscilloscope measurement

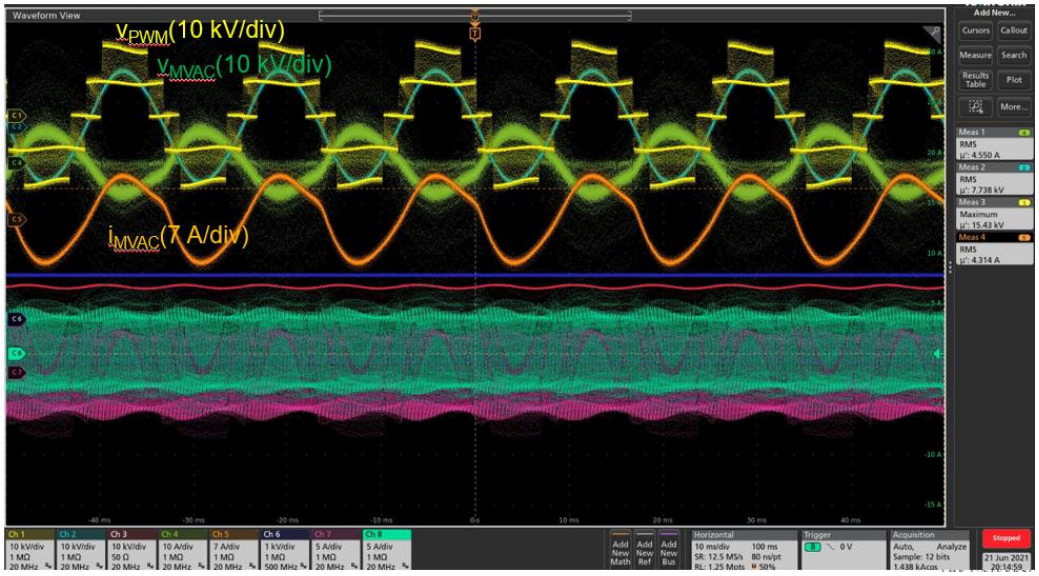
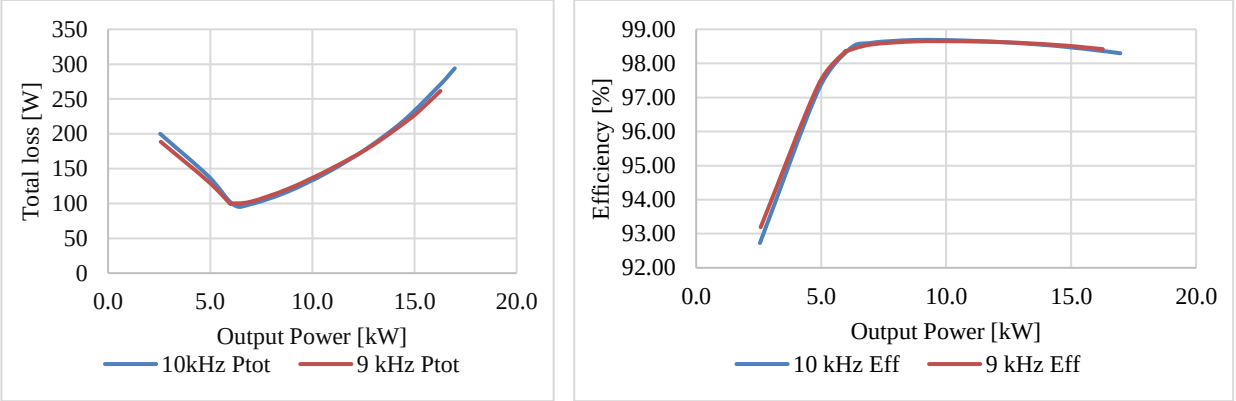


Fig. 2-18. MVAC side waveforms under the rated voltage and rated active power rating

- **Loss breakdown of the DC/DC stage**

To analyze the loss breakdown, the efficiency of the DC/DC converter has been tested individually, and the corresponding loss breakdown has been estimated. To estimate the switching and core losses, the DC/DC converter is tested at two different switching frequencies, i.e., 10 kHz (rated) and 9 kHz. As shown in Fig. 1.5, the peak efficiency of the converter is 98.7%, and the full load efficiency 98.2%. At the load below 6 kW (35% of the rated power), due to the loss of zero voltage switching (ZVS), the loss increases as the load decreases. Beyond 6 kW, full ZVS can be achieved, and the efficiency remains above 98%.



(a) (b)

Fig. 2-19. The DC/DC converter (a) power loss curve, (b) efficiency curve

However, the DC/DC converter efficiency is below the design target, which is 99%. From the loss test of one DC/DC converter, the total loss is 294 W at full load. The DC/DC stage loss breakdown is shown in Fig. 2-20. The core loss of the transformer is as expected, while the winding loss is slightly larger, as the winding has been enlarged to meet the insulation requirement. Apart from the device and transformer losses, there is 105 W extra loss which was unexpected in the design, which is highly possible to be the eddy current loss generated on the surface of the transformer core, due to the leakage flux surrounding the transformer core.

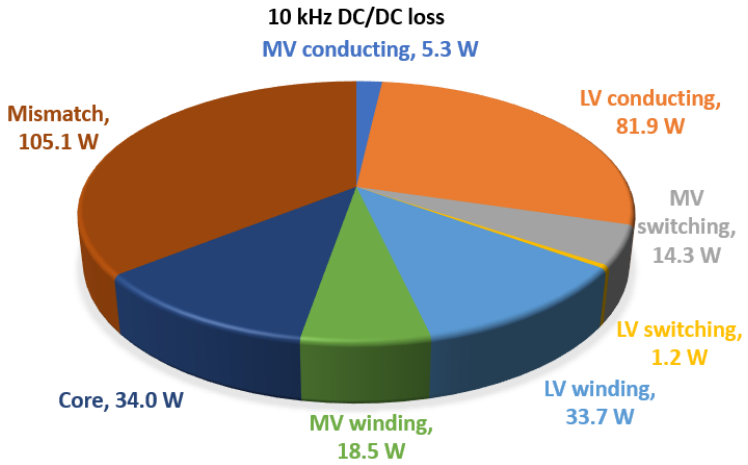


Fig. 2-20. The DC/DC converter loss breakdown

- **The MV MF transformer eddy current loss**

As mentioned above, excessive loss has been found in each unit due to the eddy current loss of the transformer core. The reason for it is that a large leakage inductance is designed to be integrated into the transformer, for power transfer and realizing of ZVS of the DC/DC. However, because of the large leakage inductance, and hence the leakage magnetic field, a higher flux density appears on the surface of the transformer core, and perpendicularly to the core laminations. Therefore, a large eddy current can be found on the surface of the transformer core, for which the laminating of the nanocrystalline core material cannot help. This has been found in some literature and verified in the transformer short-circuit test by measuring both the total loss and thermal image, as shown in Fig. 2-21.

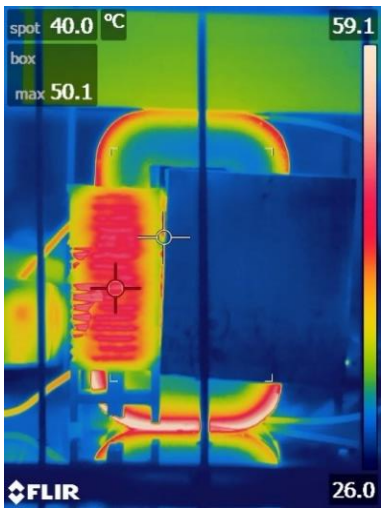


Fig. 2-21. The outer layer of the transformer core heated up due to the leakage flux [8]

- **Parasitic capacitance loss [9]**

There are many parasitic capacitances in the PCS converter, such as the transformer winding to case capacitance, the gate driver power supply primary-to-secondary capacitance, the capacitance between device heat sinks, etc. If the voltage of the capacitance is not constant, the capacitance will be charged and discharged, and during this charging and discharging process, the loss is induced. A larger capacitance, higher charging and discharging voltage, and higher charging and discharging frequency led to a large loss. The parasitic capacitance loss estimation is shown in Table 1.1, and the total parasitic loss is estimated to be 218.1 W.

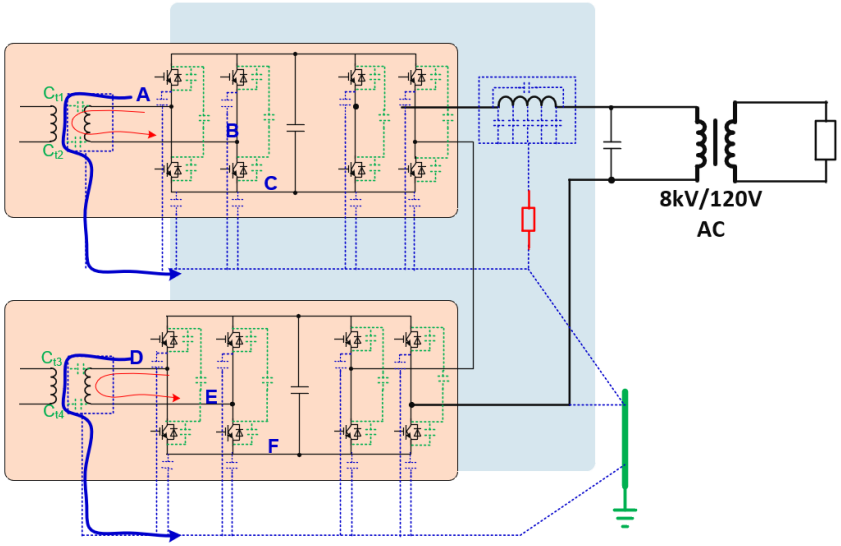


Fig. 2-22. The parasitic capacitances in the PCS converter

Table 2-12. The parasitic capacitance loss estimation.

Parasitic capacitance	Value	Frequency	Loss/phase
Between transformer winding terminals	17 pF	10 kHz	60 W
Gate drive PCB to heat sink	1.6 pF	10 kHz for the DC/DC stage	7.5 W
Heat sink to heat sink	1 pF	3 kHz for the DC/AC stage	4.6 W

Between transformer windings and the ground shielding	217 pF	3 kHz for the bottom stage 9 kHz for the top stage	117 W
Gate drive power supply primary to secondary	1.85 pF	3 kHz; 6 kHz; 12 kHz, 13 kHz, 16 kHz for different locations	15 W
Between the inductor terminals	25 pF	12 kHz	14 W
Total			218.1 W

- **Converter loss breakdown**

With the DC/DC stage loss tested and analyzed, the loss breakdown of the whole single-phase converter is analyzed, as shown in Fig. 2-23. Except for the power stage and passive losses, there are also losses caused by parasitic capacitance, of which the transformer parasitic capacitance is the biggest one. Besides, the "DAB loss mismatch" is the same as the "mismatch" in Fig. 2-20, which is caused by the eddy current induced by the leakage flux. The "other mismatch" is considered to be the device loss calculation error and the parasitic capacitance loss estimation error or some other losses that have not been identified.

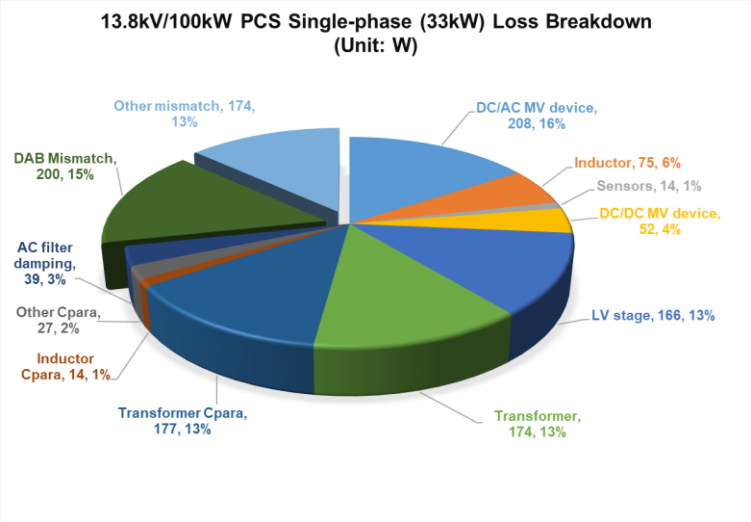


Fig. 2-23. The single-phase converter loss breakdown

The losses are divided into four categories, as shown in Fig. 2-24. The sum of the parasitics loss and the DAB mismatch, which is highly possible for the eddy current loss, is about 32% of the total loss, and all these losses are not expected in the converter design. Besides, a part of the "other mismatch" may also belong to the parasitic loss or the eddy current loss.

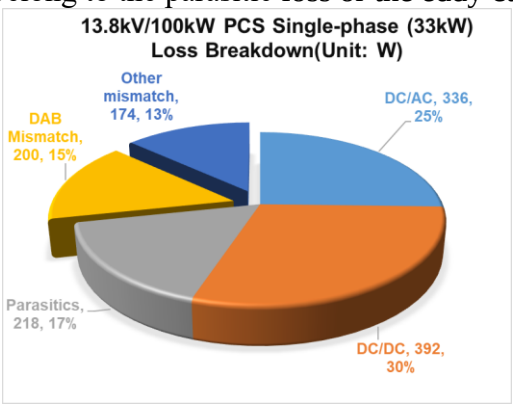
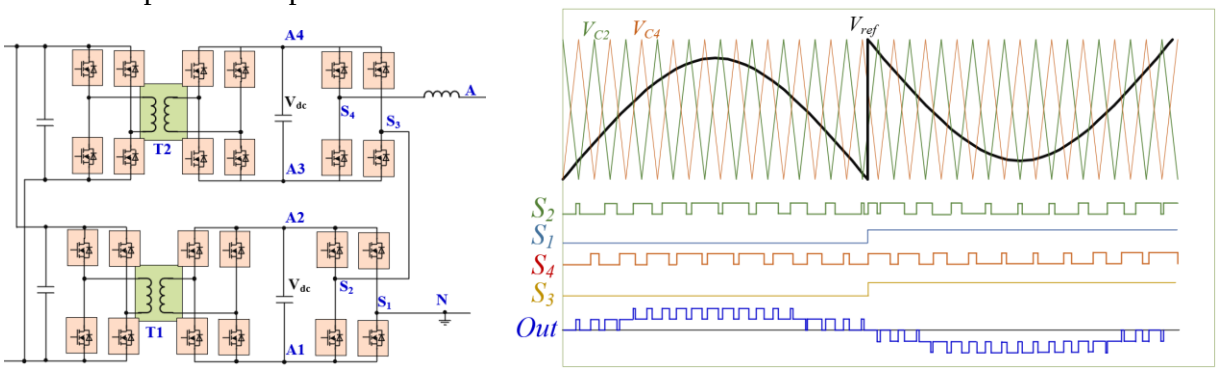


Fig. 2-24. The single-phase converter loss categories

- **Parasitic loss reduction method [9]**

Since the transformer parasitic loss dominates the total parasitic loss, reducing the transformer parasitic loss can effectively improve the converter efficiency. The charging and discharging of the transformer winding to shielding parasitic capacitance also depends on the DC/AC stage switching actions due to the grounding configuration. Therefore, a PWM modulation scheme is proposed to reduce the equivalent switching frequency of the transformer winding to the ground, which is also related to the equivalent switching frequency of the DC links. As shown in Fig. 2-25 (a), in the previous PWM modulation, all the four half bridges, i.e., S1, S2, S3, and S4, are switching at 3 kHz. As a result, the bottom DC-link has an equivalent switching frequency of 3 kHz, and the top DC-link has an equivalent switching frequency of 9 kHz.

The new PWM modulation scheme is shown in Fig. 2-25 (b), and the half-bridges of S1 and S3 switch with the fundamental frequency, i.e., 60 Hz, and the half-bridges of S2 and S4 switch with 6 kHz. With this modulation, the AC output equivalent switching frequency is still 12 kHz, so that the control bandwidth and power quality can be maintained. However, the bottom and top DC-link equivalent witching frequencies are 60 Hz, and 6.12 kHz, respectively, and the transformer parasitic capacitance loss can be reduced.



(a) (b)

Fig. 2-25. The (a) switching signal and (b) scheme of the proposed PWM modulation method

The efficiency comparison of the proposed PWM modulation with the conventional PS PWM is shown in Fig. 2-26. The efficiency improvement at light load is more obvious because the parasitic capacitance loss is related to the voltage but not related to the current. Therefore, with higher output power, the ratio of the loss reduction to the total power, which is related to the efficiency improvement, is reduced. With the proposed PWM modulation, the converter has an efficiency of 96.4% at the rated power output.

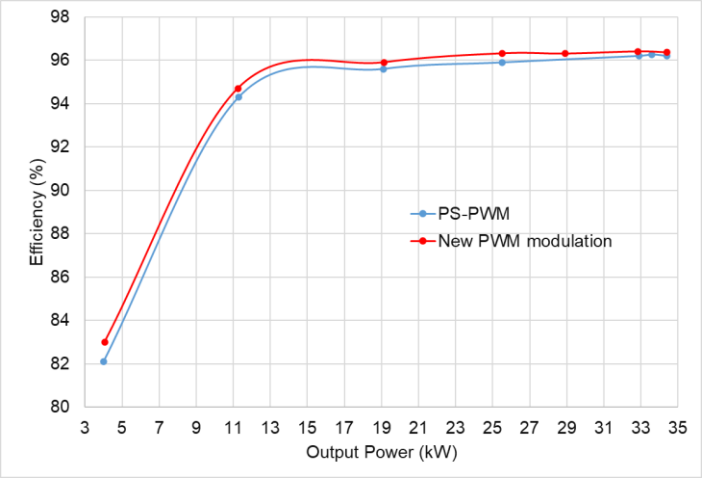


Fig. 2-26. The efficiency comparison of the proposed PWM modulation and the conventional phase-shift PWM modulation

- **Full rating test**

Because each single-phase converter has been tested at the rated active power output, the three-phase full rating test is conducted with reactive power load due to the test platform power rating limitation. As shown in Fig. 2-27, the PCS converter is supplied from the LV DC side, and three resistor and capacitor series-connected loads are connected at the MV AC side of the PCS converter.

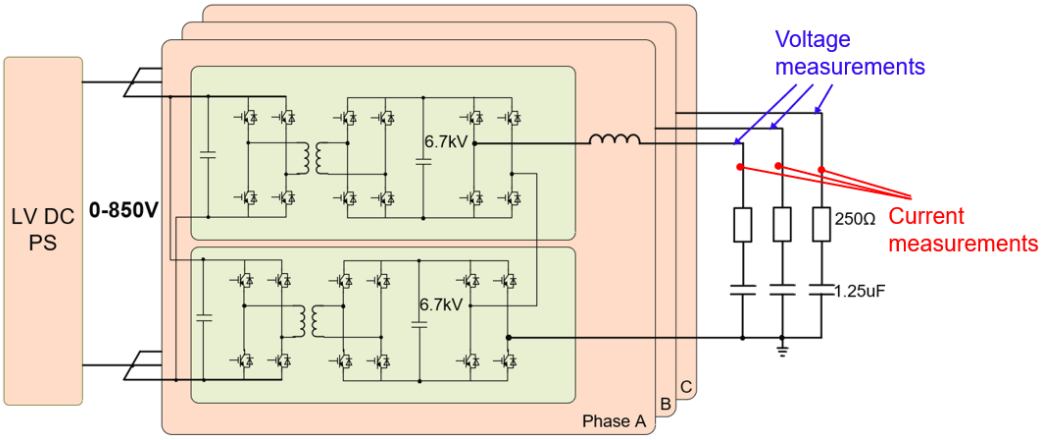


Fig. 2-27. Diagram of the three-phase PCS converter full rating test setup

The MV AC side waveforms at the rated voltage and power ratings are shown in Fig. 2-28, the line-to-line voltage is around 14.2 kV (3% higher than 13.8 kV), and the total output power is around 101 kVA.

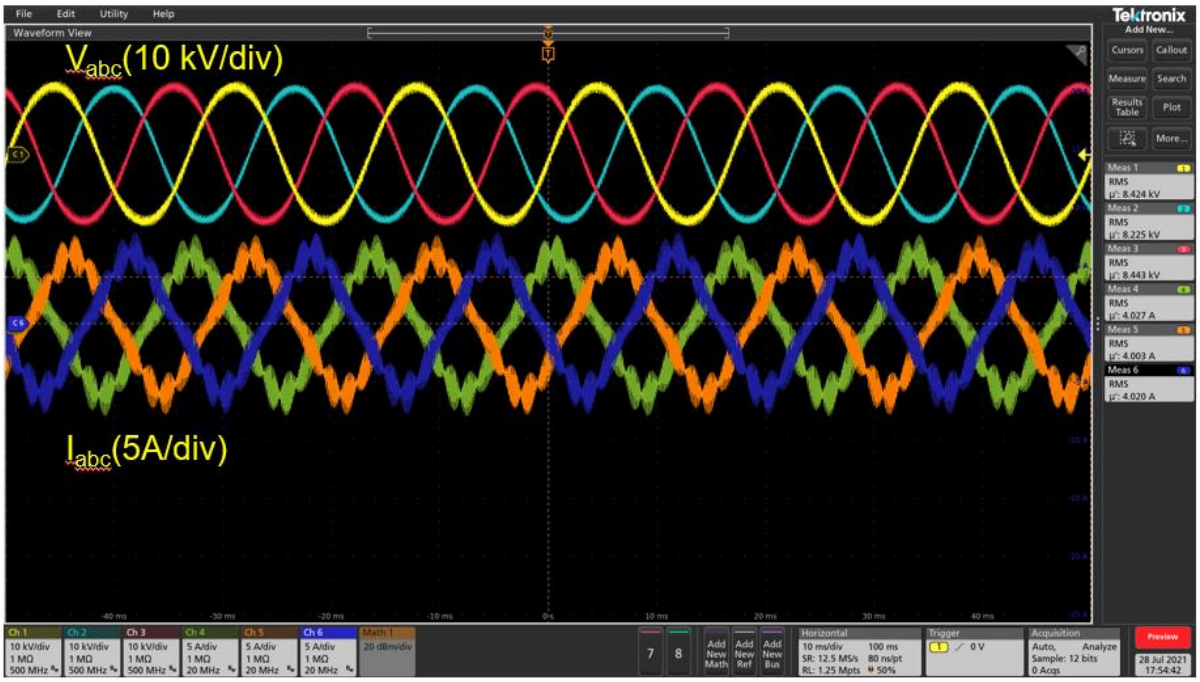


Fig. 2-28 PCS converter AC side waveforms at full voltage and power ratings

- **AC voltage power quality**

The voltage harmonic spectrum is analyzed by doing Fast Fourier Transform (FFT) to the AC voltage waveform in Fig. 2-28. As shown in Fig. 2-29, the fundamental component is around 12 kV, and the maximum harmonic is the 3rd-order, which is around 312 V (2.6%). The THD is calculated to be 2.72% by doing the math to the harmonics up to the 50th-order, according to the definition in the IEEE Std. 519 and IEEE Std. 1547-2018.

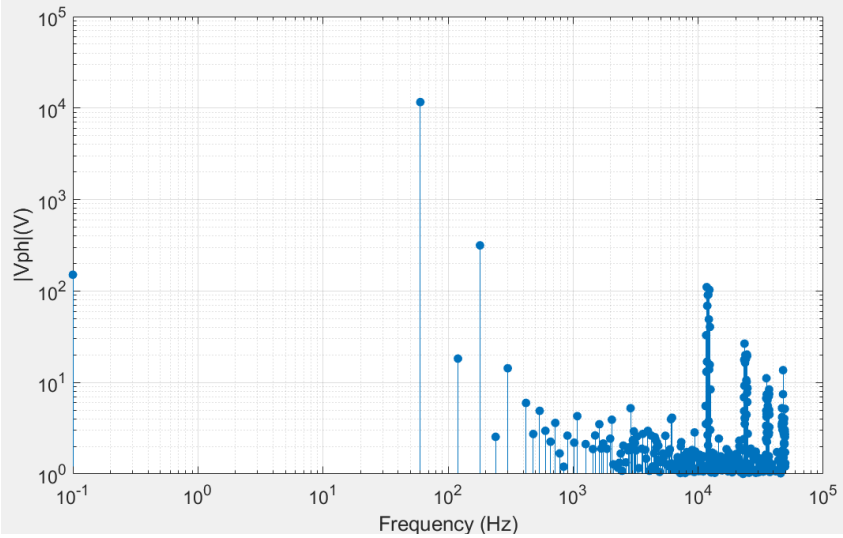
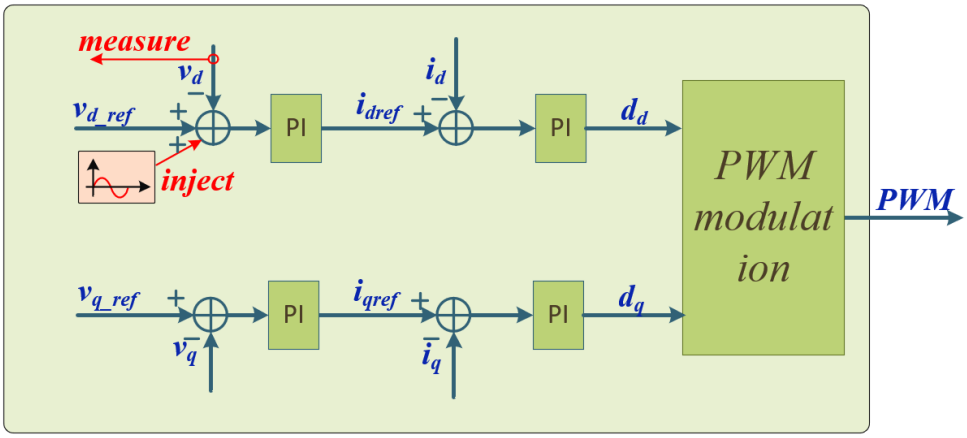


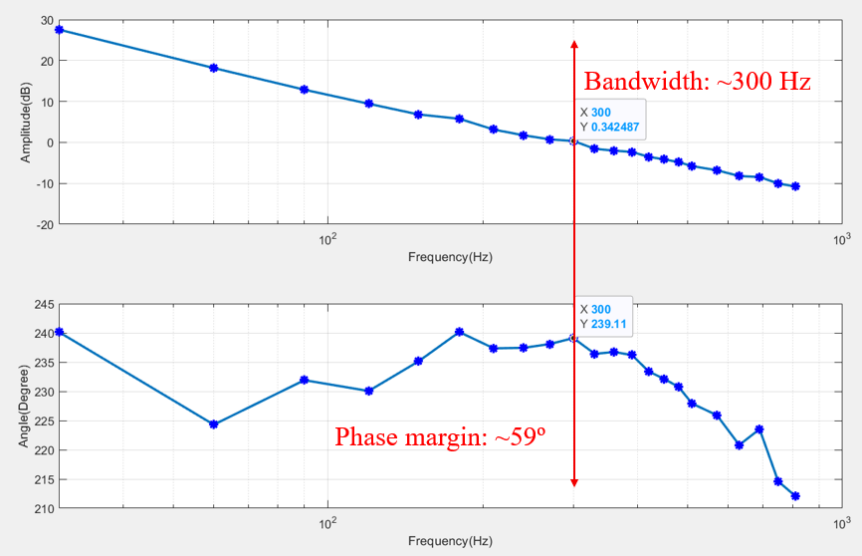
Fig. 2-29. PCS converter AC voltage harmonic spectrum

- **AC voltage control bandwidth**

The AC voltage control bandwidth is tested by injecting a single sinusoidal disturbance, with a certain frequency, to the voltage controller d-axis reference in each test, as shown in Fig. 2-30 (a). The d-axis voltage feedback is recorded. After doing FFT to the injected and feedback signal data arrays, the amplitude and angle of both the injected and feedback signals are obtained, so the open-loop transfer function gain and phase angle at the injected frequency can be calculated. After doing different frequency injections one by one, the gain and phase angle curves of the open-loop transfer function can be achieved. As shown in Fig. 2-30 (b), the AC voltage control bandwidth of the PCS converter is 300 Hz, and the phase margin is around 59º.



(a)



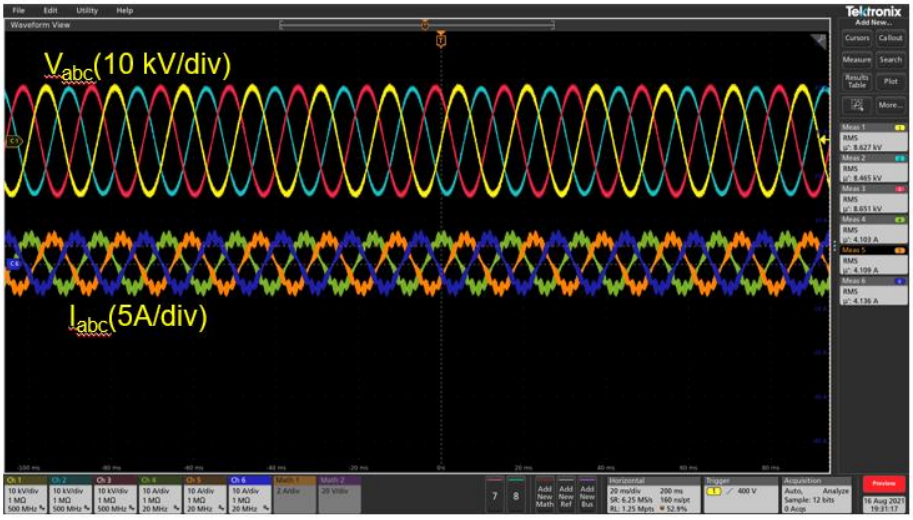
(b)

Fig. 2-30. AC voltage bandwidth test (a) scheme and (b) results

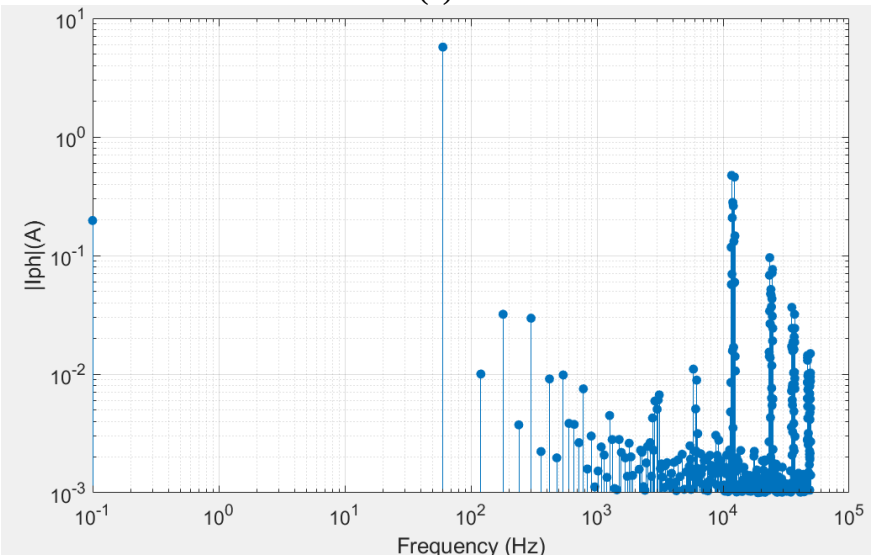
- **The AC current power quality**

The current power quality test is conducted with the same setup as shown in Fig. 2-27, but only the current control loop is used because the AC voltage and current are highly related by the passive loads. A 3rd-order current controller is used to reduce the 3rd-order harmonics, which is induced by the 2nd-order voltage on the DC-links. The AC voltage and current waveforms are

shown in Fig. 2-31 (a), and the current harmonic spectrum is shown in Fig. 2-31 (b). The current THD is calculated to be 0.81%, considering harmonics up to 50th-order, based on the IEEE Std. 519 and IEEE Std. 1547-2018. Since the current in the test is almost the rated current, the TDD and TRD of the current are same as the THD, i.e., 0.81%.



(a)

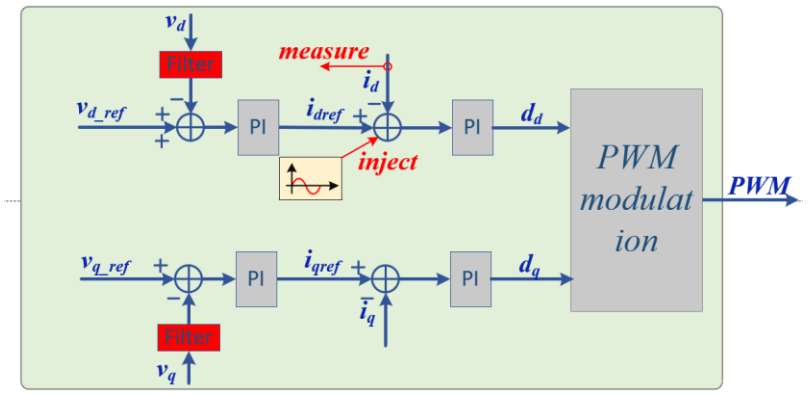


(b)

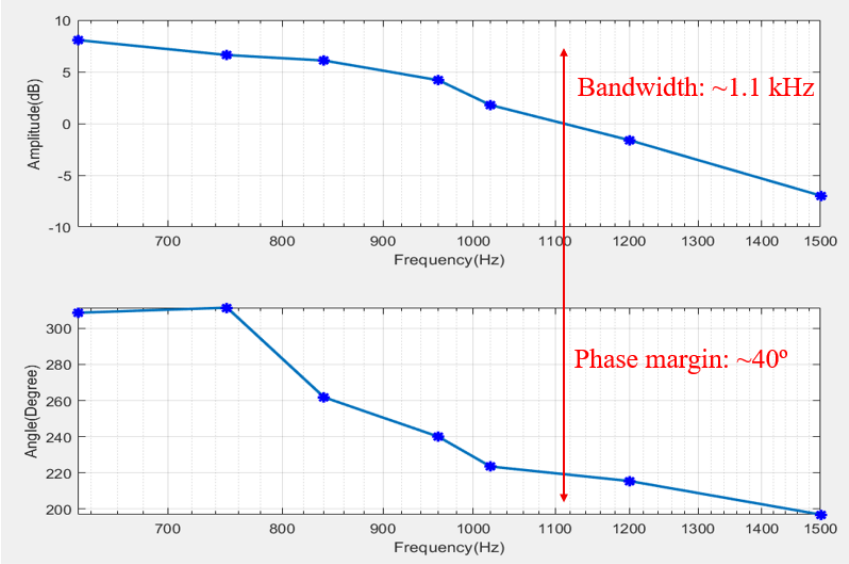
Fig. 2-31. The AC current (a) waveforms and (b) harmonic spectrum

- **The AC current control bandwidth**

A similar harmonic injection method as the AC voltage control bandwidth test is used to test the AC current control bandwidth. As shown in Fig. 2-32 (a), to decouple the relationship between the AC voltage and the AC current, a band stop filter, for the injected harmonic, is added on the voltage feedback. The AC current controller open-loop transfer function gain and phase angle curves are shown in Fig. 2-32 (b). According to the test results, the AC current control bandwidth of the PCS converter is around 1.1 kHz, and the phase margin is around 40º.



(a)



(b)

Fig. 2-32. The AC current bandwidth test (a) scheme and (b) results

- **Converter function tests and analysis**

The test setup developed is shown in Fig. 2-33, is used to test the PCS converter functions.

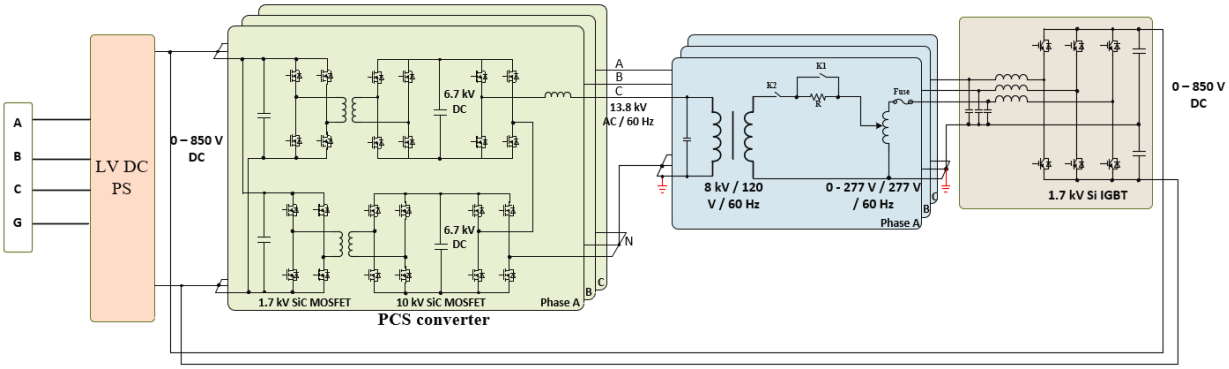
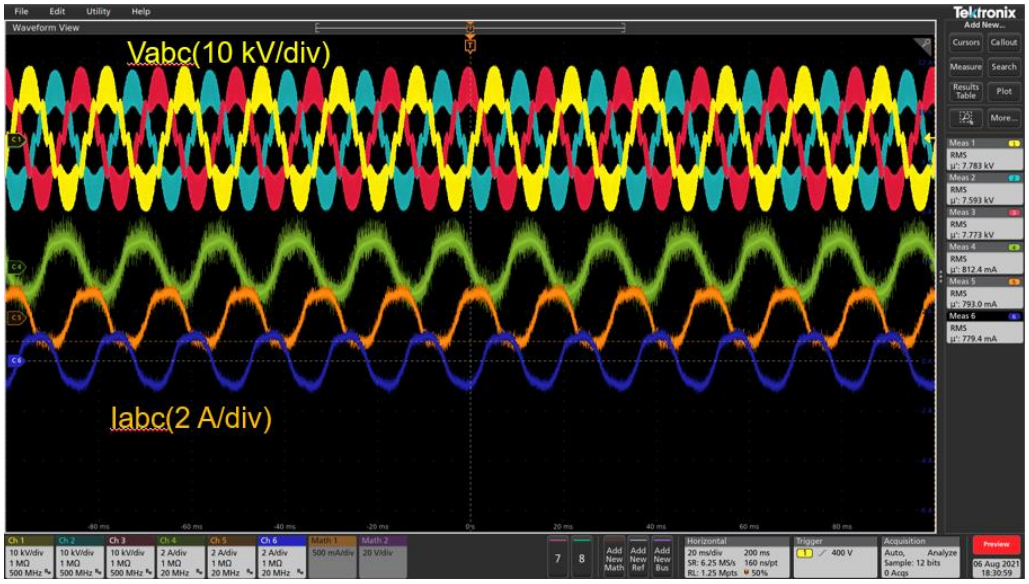


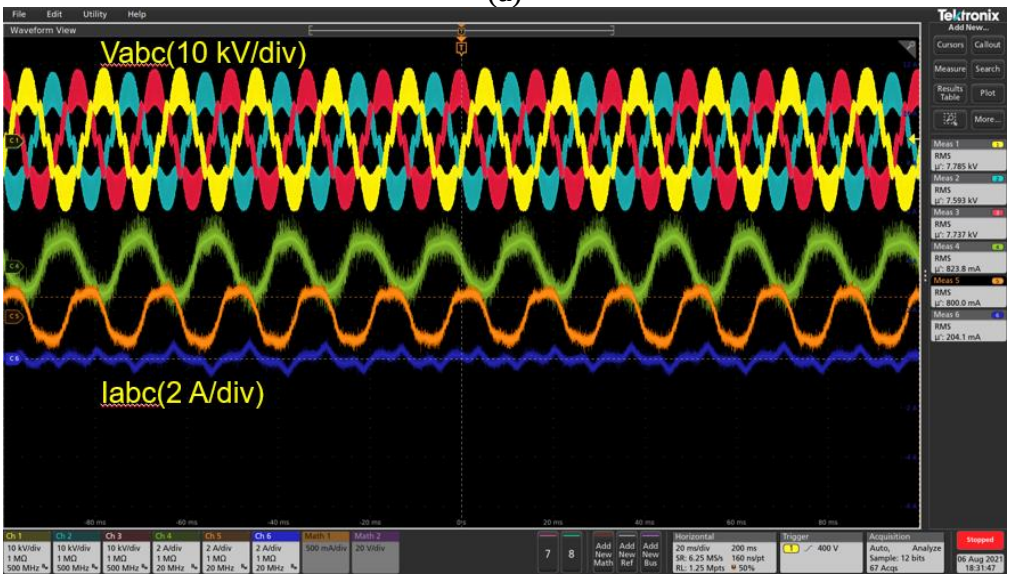
Fig. 2-33. The PCS converter function test setup [10]

Islanded mode balanced/unbalanced AC load support

In the islanded mode, the PCS converter regulates the AC voltage and frequency, and the three-phase two-level converter operates as a load emulator, emulating the balanced/unbalanced load. Fig. 2-34 (a) shows the balanced AC load support test waveforms, and the three-phase current waveforms are balanced. The unbalanced load support waveforms are shown in Fig. 2-34 (b), of which phase C has no load, and the small current of phase C is the magnetizing current of the 8 kV/ 120 V transformer.



(a)



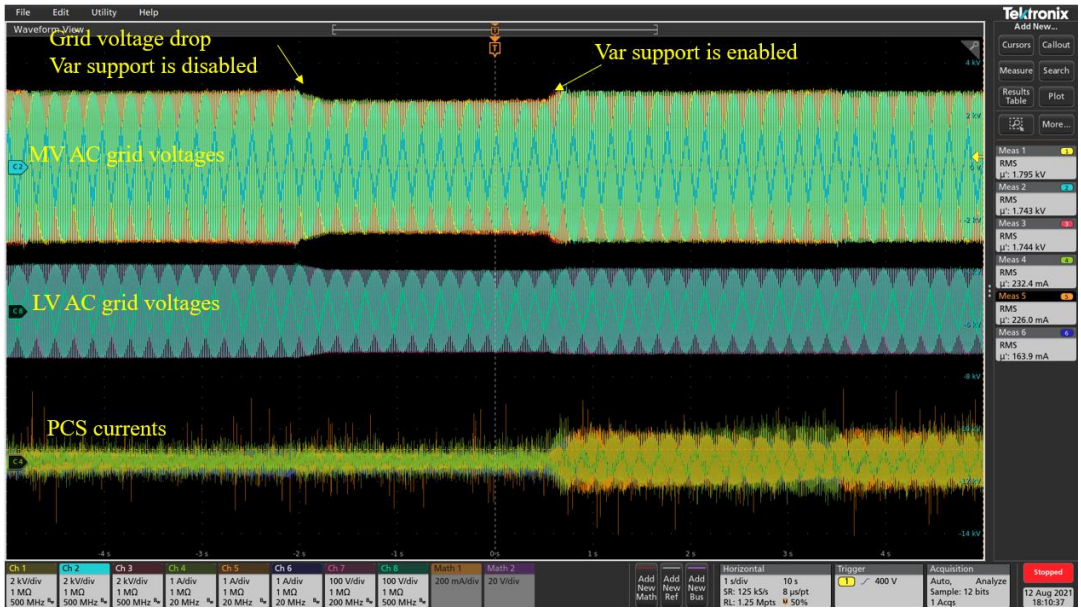
(b)

Fig. 2-34. The PCS converter (a) balanced and (b) unbalanced load support in the islanded mode operation

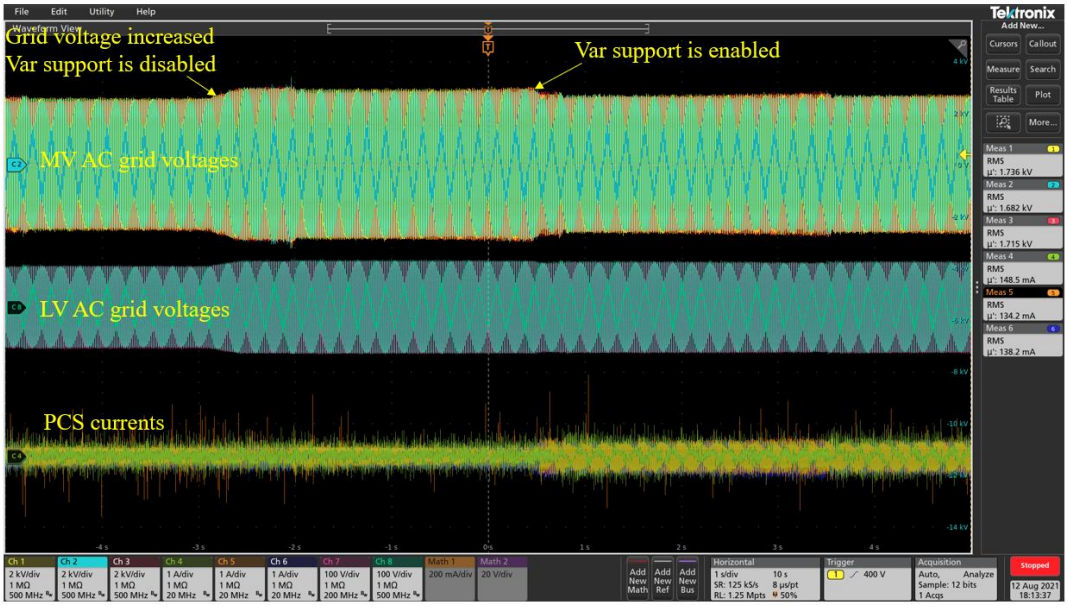
Var (reactive/voltage) support

In the grid-connected mode, the PCS converter can help to support the grid voltage through reactive power control. The test is conducted with the same setup shown in Fig. 2-33, but the three-phase two-level converter emulates the AC grid, and the PCS converter controls the active and reactive power. To show the functionality of the var support function, the var support function is

disabled at the beginning. As shown in Fig. 2-35 (a), the grid voltage first drops, since the var support function is disabled, the PCS converter current keeps constant and the grid voltage is not supported. When the var support function is enabled, the PCS converter outputs more reactive power, and the grid voltage recovers to the normal value. A similar test is conducted in the high voltage case, as shown in Fig. 2-35 (b), the PCS converter absorbs reactive power to get the grid voltage reduced to the normal value.



(a)



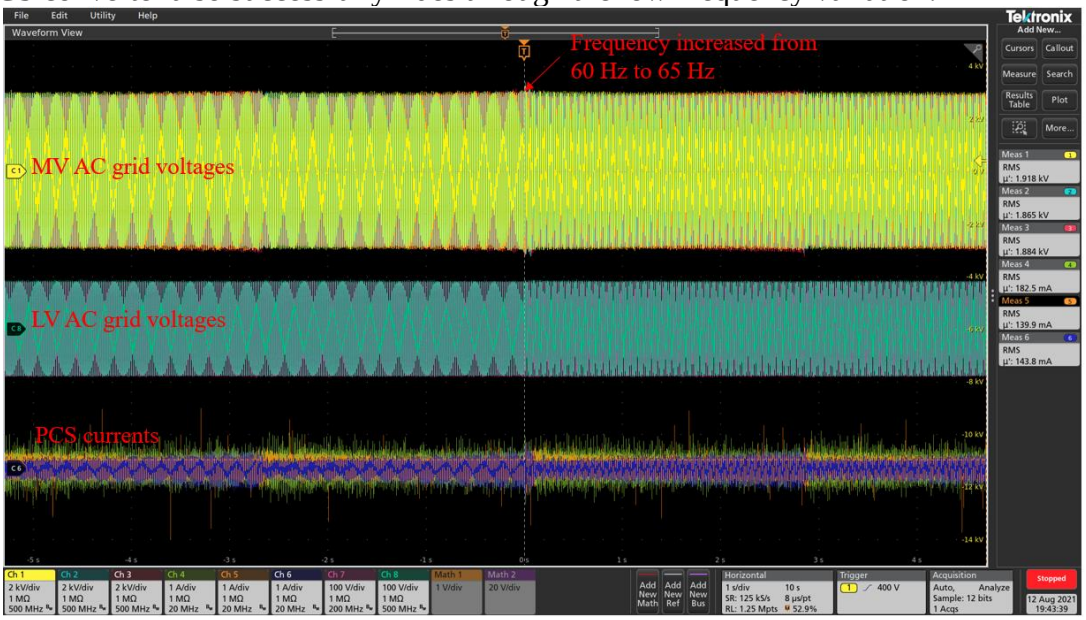
(b)

Fig. 2-35. The PCS converter var support at (a) low voltage and (b) high voltage conditions

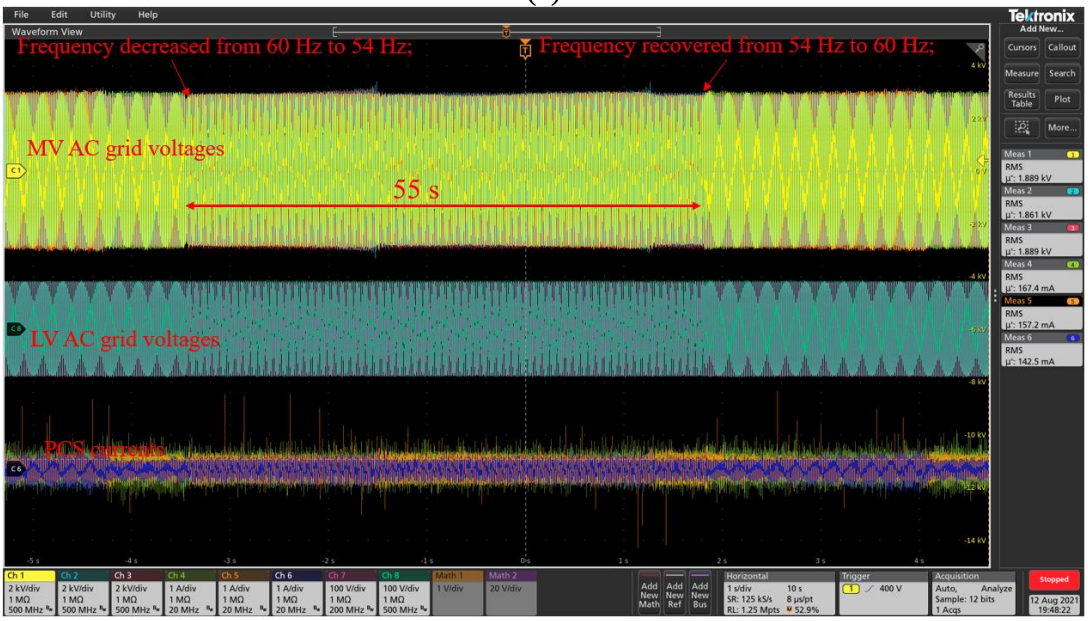
Frequency ride through and protection

In the test, the AC grid voltage frequency is varied by the grid emulator. According to IEEE Std. 1547-2018, the PCS converter needs to ride through the low-frequency range of [50 Hz, 58.8 Hz] and high-frequency range of [61.2 Hz, 66 Hz] for up to 1000 seconds.

The high-frequency ride-through (HFRT) test waveforms are shown in Fig. 2-36 (a). The grid frequency increases from 60 Hz to 65 Hz within one and a half of the fundamental cycle (24 ms), which is much faster than the required frequency variation in the IEEE Std. 1547-2018. However, the PCS converter rides through the frequency variation without any abnormal performance. The low-frequency ride-through (LFRT) test waveforms are shown in Fig. 2-36 (b), the frequency drops from 60 Hz to 54 Hz within 2 fundamental cycles (32 ms) and keeps at 54 Hz for 55 seconds. The PCS converter also successfully rides through the low-frequency variation.



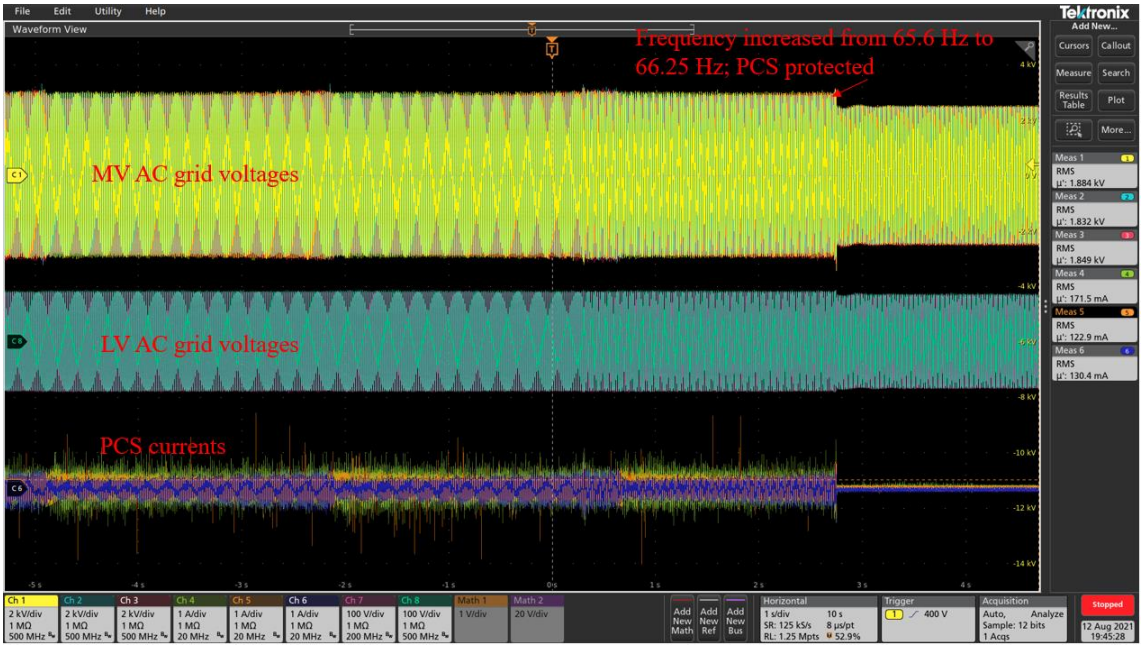
(a)



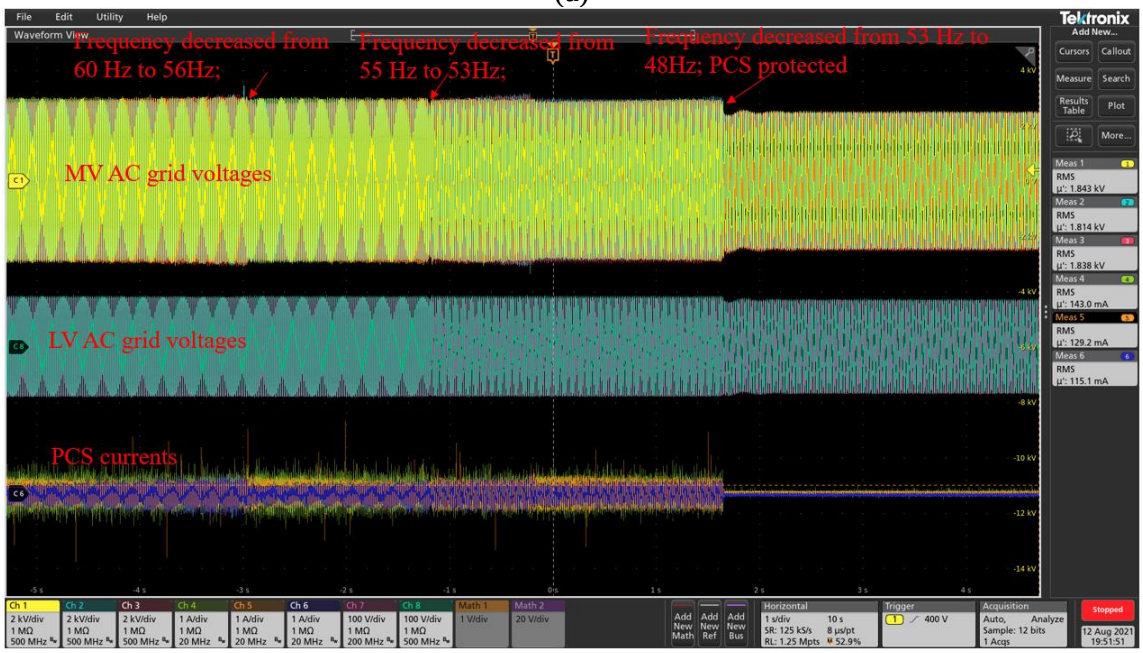
(b)

Fig. 2-36. The PCS converter (a) HFRT and (b) LFRT test waveforms.

When the frequency is higher than 66 Hz or lower than 50 Hz, the PCS converter should protect. The over frequency and under frequency protection test waveforms are shown in Fig. 2-37 (a) and (b), respectively. The PCS converter protects itself in both conditions.



(a)



(b)

Fig. 2-37. The PCS converter (a) over-frequency protection and (b) under-frequency protection test waveforms.

Voltage ride through and protection

Similar to the frequency variation test, the voltage variation is realized through the grid emulator control. Although the PCS converter is designed to ride through low voltage down to 0, for the test observation, the low voltage ride through (LVRT) is conducted down to 0.5 p.u. The under-voltage and overvoltage protection will be triggered once the voltage is lower than 0.5 p.u., or higher than 1.2 p.u., respectively. The LVRT test waveforms are shown in Fig. 1.28, the voltage drops from 1 p.u. to 0.5 p.u., and the PCS converter rides through the voltage variation with a little

overcurrent during the transients. There are some voltage harmonics and spikes, which are caused by the under damping of the AC side LC filters. This should not impact the PCS converter function test.

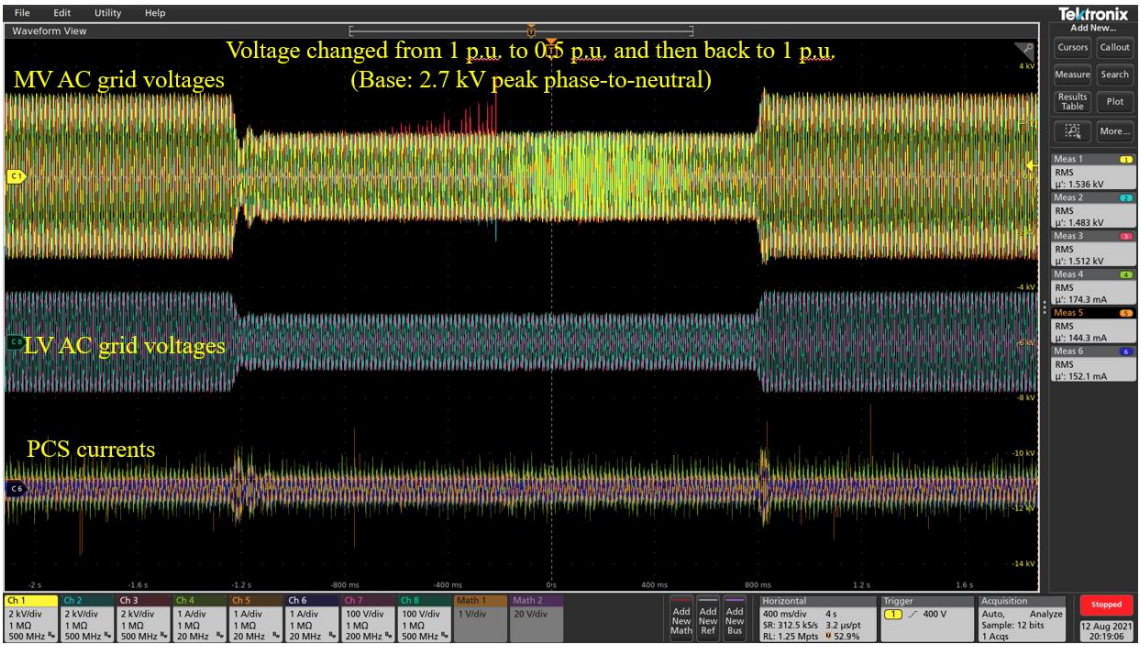
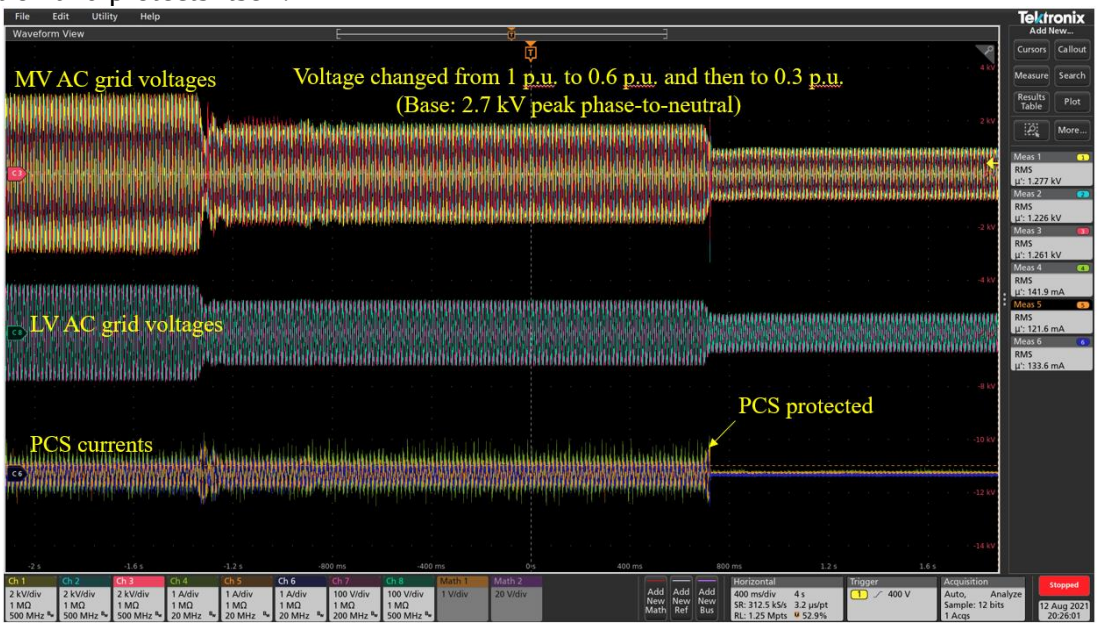
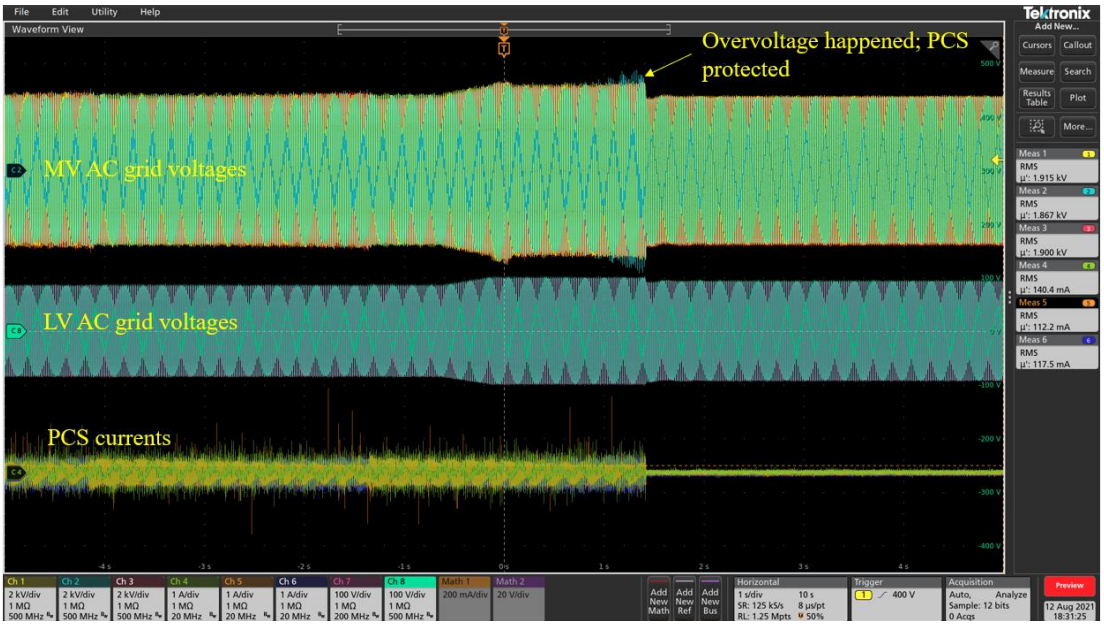


Fig. 2-38. The PCS converter LVRT test waveforms.

The under-voltage and overvoltage protection test waveforms are shown in Fig. 1.29 (a) and (b), respectively. when the voltage is lower than 0.5 p.u. or higher than 1.2 p.u., the PCS stops operation and protects itself.



(a)



(b)

Fig. 2-39. The PCS converter (a) under-voltage protection and (b) overvoltage protection test waveforms.

- **Three-phase PCS converter tests summary**

The performance and function tests of the PCS converter are summarized in Table 2-13. The design requirements of the converter voltage and power ratings, AC voltage power quality, AC current power quality, AC voltage control bandwidth, and AC current control bandwidth are all achieved. The converter efficiency achieved is 96.4%, which is lower than the design goal, i.e., 98%, and the reasons are discussed in detail above.

Besides the converter performances, the converter functions, including balanced/unbalanced load support in the islanded mode, var support, frequency ride through, LVRT, and protection are all tested with the MV PCS converter, and the requirements are all achieved.

Due to test platform limitations, some functions, such as mode transitions, AC grid faults are tested in the HTB with the small-scale PCS converter (see Chapter 3). These HTB test results can be scaled to the MV PCS converter capability since the key impact of these functions is the control strategy and the converter response speed, which is more related to the controller design and control bandwidth rather than the power loop hardware. The small-scale PCS converter has the same control algorithm and control bandwidth as the MV PCS converter, so these tests with the small-scale PCS converter can also be used to predict the MV PCS converter tests. Besides, the high-frequency stability and harmonic filtering functions are also not able to be tested in the test platform. However, based on the work from another UTK project (the Power American (PA) project), as long as the control bandwidth of the PCS converter can meet the design requirement, the high-frequency stability and harmonic filtering functions can also be achieved.

Table 2-13. Summary of the PCS converter performance and function tests.

#		Function	Status
1	Converter performance	Full voltage and power rating operation (13.8kV/100kW)	Achieved
2		Voltage THD ≤5% (Islanded mode, IEEE 519)	2.72% (achieved)

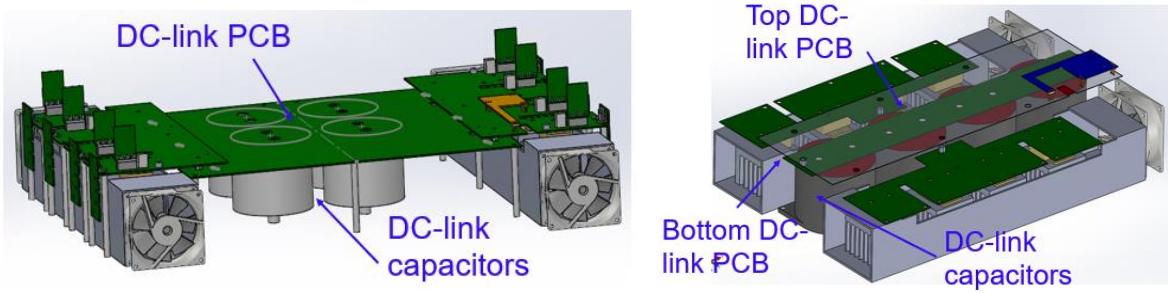
3		Current TDD ≤ 5% (grid-connected mode, IEEE 1547)	0.79% (achieved)
4		Converter efficiency ~ 98%	96.4% (achieved)
5		Voltage control bandwidth (300 Hz)	300 Hz (achieved)
6		Current control bandwidth (1 kHz)	1.1 kHz (achieved)
7	Grid requirements/functions	Var support (voltage support)	Achieved
8		Frequency Ride Through	Achieved
9		LVRT	Achieved
10		Mode transition	Achieved in the HTB test
11		Protection (Overvoltage, under-voltage, over frequency, under frequency, etc.)	Achieved
12		Unbalanced load support in the islanded mode	Achieved
13		AC grid Faults	Achieved in the HTB test
14		High-frequency stability	Leveraged from the PA project
15		Harmonic filtering	Leveraged from the PA project

2.2.2 Design and test of Gen. II PCS

Based on test results of Gen I. PCS, modifications have been made to achieve higher power efficiency and power density. The MV and LV power stages, as well as the auxiliary power supply for MV device gate drives have been redesigned to reduce volume. A new configuration of MV DC/DC transformer has also been adopted to reduce losses.

2.2.2.1 Power stage redesign

The MV power stage occupies a lot of space in the Gen. I design, and some space is wasted, as shown in Fig. 2-40(a). Therefore, in the BP3 design, a more compact design is conducted. As shown in Fig. 2-40(a), due to the creepage and clearance distance requirements on the PCB, the DC-link PCB is large and some space beneath the DC-link PCB is wasted. The large DC-link PCB in Gen. I design is separated into two smaller PCBs in Gen. II design, as shown in Fig. 2-40(b). The bottom DC-link PCB is used to connect the four DC-link capacitors in series, and the top DC-link PCB is used to connect the 10 kV devices to the DC-link. Through this design, the devices can be closer to the DC-link capacitors and the wasted space becomes less.



(a) (b)

Fig. 2.40. The figure of (a) Gen. I MV power stage, (b) Gen II. MV power stage

To improve the power density and efficiency, the LV power stage is redesigned. Since the original 1.7 kV SiC device is with high loss, another 1.7 kV SiC device from Microsemi, which is more efficient, is adopted. The heatsink is shrunk with fewer fans after utilizing more device capabilities. In the new design, the gate drive circuit has been simplified, and the size of the PCB is reduced. The assembly of the newly designed LV power stage is shown in Fig. 2-41. Compared to the LV power stage used in the Gen. I converter, the new design has a volume reduction of 30%.

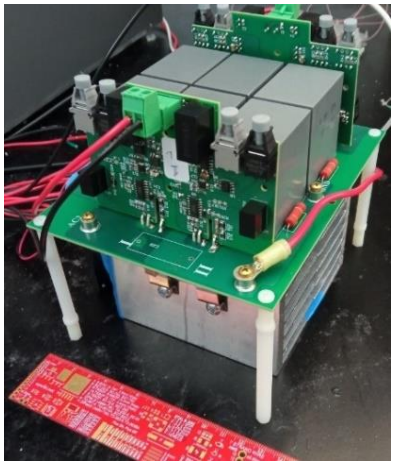


Fig. 2-41. Photograph of LV power stage

2.2.2.2 Gate drive auxiliary power supply design [11]

Based on the testing results in Gen. I PCS, the MV gate driver power supply (GDPS) design for BP3 is improved for both the volume and parasitic capacitance. As shown in Fig. 2-42, the BP3 design has a much smaller size than the Gen. I design, which is mainly achieved by using a smaller core and special creepage distance design on the side surfaces. The parasitic capacitance between the primary-side winding and the secondary-side winding of the MV isolated transformer in the GDPS is also reduced from 1.85 pF to 1.0 pF by minimizing the equivalent surface area and distance between the two windings. The parasitic capacitance reduction helps to minimize the common mode current flowing through the MV power stage to the LV control power. More detailed testing results are shown in Table 2-14, and both the Gen. I and Gen. II designs can meet the power, efficiency, and insulation requirements.

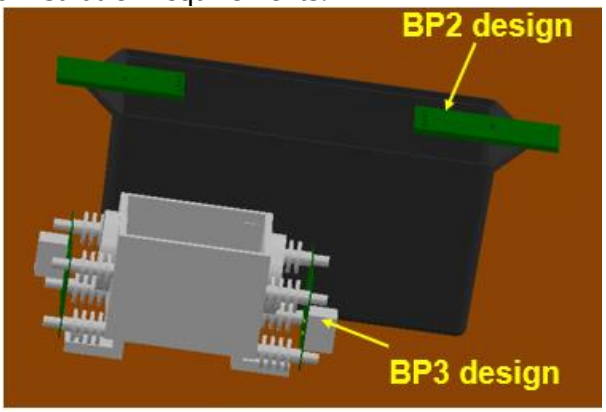


Fig. 2-42. Size comparison between Gen. I (BP2) GDPS and Gen. II (BP3) GDPS

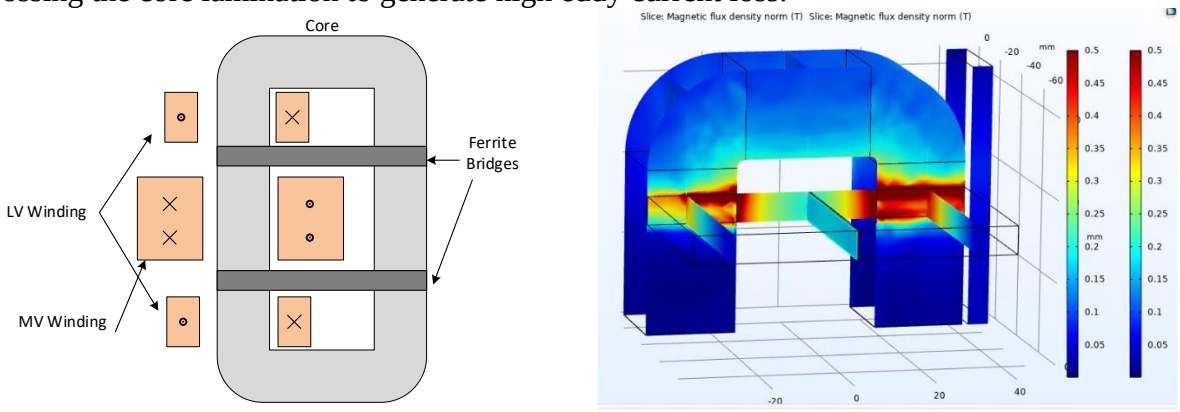
Table 2-14. Parameter comparison between BP2 GDPS and BP3 GDPS

Parameters	BP2 GDPS (Gen. I)	BP3 GDPS (Gen. II)
Power rating	> 2.4W	> 2.5 W
Efficiency	81% @ 2W output	80% @ 2W output
Dimension	139 mm × 54 mm × 62 mm	76 mm × 40 mm × 38 mm
Volume	465 cm^3	116 cm^3
Parasitic capacitance	1.85 pF	1.00 pF
PD test	15 kV	15 kV

2.2.2.3 MV DC/DC transformer redesign [8]

In Gen. I PCS, the original design employed the core type winding to increase the leakage inductance for leakage integration. However, the leakage magnetic field increased the eddy current loss in the nanocrystalline core laminations, causing excessive losses. To meet the insulation requirement, Gen. I design used conductive shielding on the whole surface of the transformer, which resulted in a high parasitic capacitance to the ground and led to high partial discharge due to high electric field concentration.

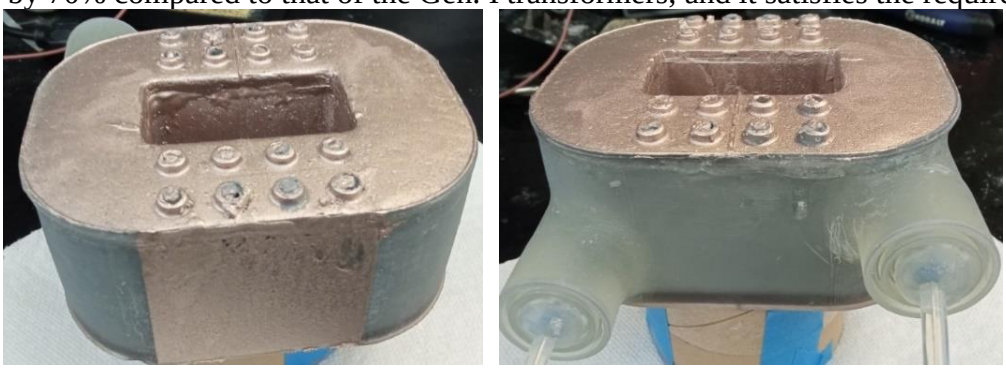
To improve the transformer efficiency, new electric and magnetic structures have been adopted in Gen. II converter. To keep a high leakage inductance, which is required by MV DC/DC converter, the stacked winding structure is selected, with ferrite bridges to bypass the leakage flux with less loss. The magnetic structure of the winding, core and ferrite bridges is shown in Fig. 2-43(a). Simulation has been conducted to verify the eddy current loss reduction. As shown in Fig. 2.-43(b), the leakage magnetic field distribution is bypassed by the ferrite bridge, instead of crossing the core lamination to generate high eddy current loss.



(a) (b)

Fig. 2-43. MV DC/DC transformer (a) magnetic structure and (b) simulation result.

To improve the insulation performance and reduce parasitic capacitance-related loss, partial shielding, instead of shielding on all the surfaces, is used for the MV winding. A partially shielded MV winding is shown in Fig. 2-44. The parasitic capacitance between the MV winding to the ground is measured to be around 90 pF, which is reduced by 60% compared to that of the Gen. I transformer winding (216 pF). The partial discharge inception voltage is around 12 kV, which is increased by 70% compared to that of the Gen. I transformers, and it satisfies the requirements.

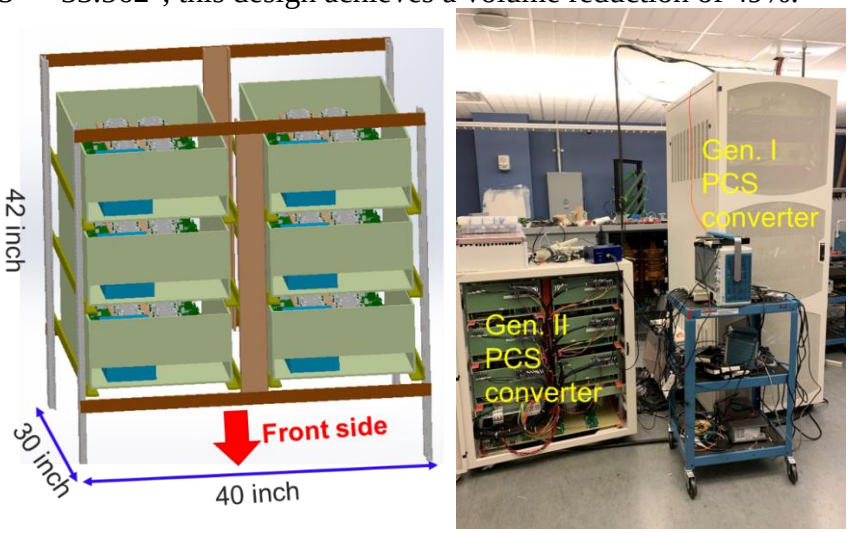


(a) (b)

Fig. 2-44. MV winding pictures of (a) rearview and (b) front view.

2.2.2.4 Gen. II PCS Mechanical Design

Mechanical design is also conducted. As shown in Fig. 2-45, the two power units in each phase are located on one level, and the three phases are vertically located on three levels. There is one more level at the bottom, which is used for the AC-side sampling boards, filter inductors, the auxiliary power supply, as well as the input and output terminals. The cabinet's exterior dimensions are 31.562" × 43.875" × 40", compared to the Gen. I cabinet, whose exterior dimensions are 36.875" × 87.625" × 33.562", this design achieves a volume reduction of 49%.



(a) (b)

Fig. 2-45. (a) The layout of the BP3 PCS converter cabinet, and (b) size comparison between Gen. I and Gen. II PCS

2.2.2.5 Gen. II PCS test results

First, the single-phase converter is tested. The waveforms of DC/DC stages in the single-phase unit are shown in Fig. 2-46.

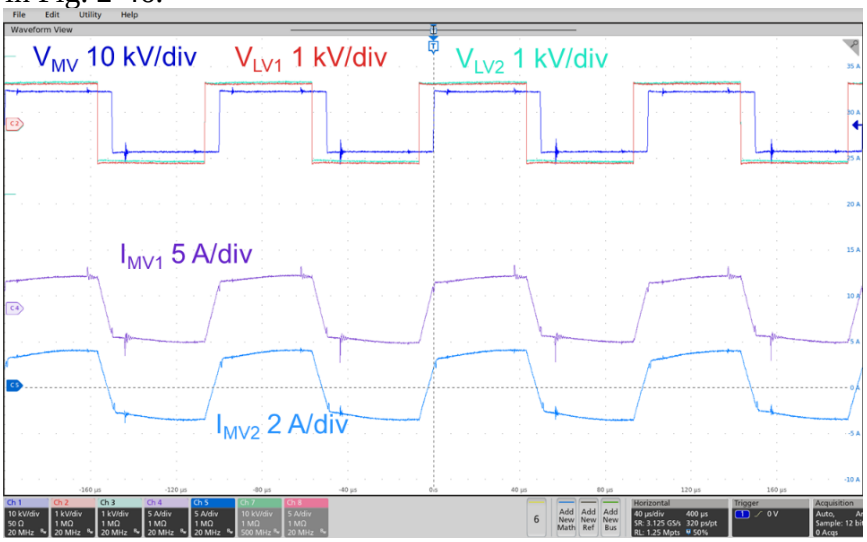


Fig. 2-46. DC/DC converter waveform in the single-phase converter

The MV AC side voltage and current waveforms are shown in Fig. 2-47. The converter efficiency is shown in Fig. 2-48. The maximum efficiency is 97.4% at the rated power output. Compared to the power unit efficiency curves, the single-phase converter has a lower efficiency,

which is caused by parasitic capacitance-related losses. Due to the cascaded connection, the voltage applied on the parasitic capacitance of the upper power unit in the single-phase converter has a higher equivalent frequency and larger voltage, which results in more losses.

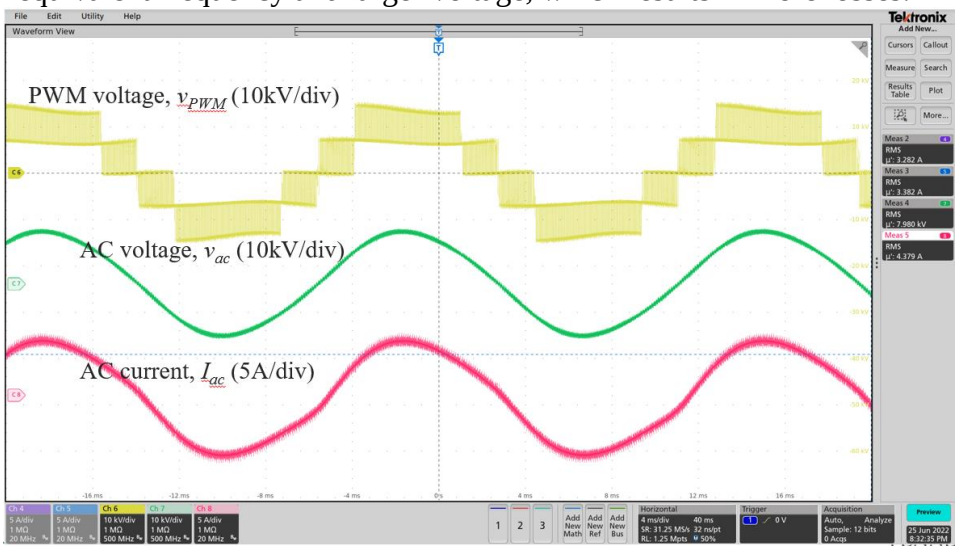


Fig. 2-47. MV AC side voltage and current waveforms of the single-phase converter

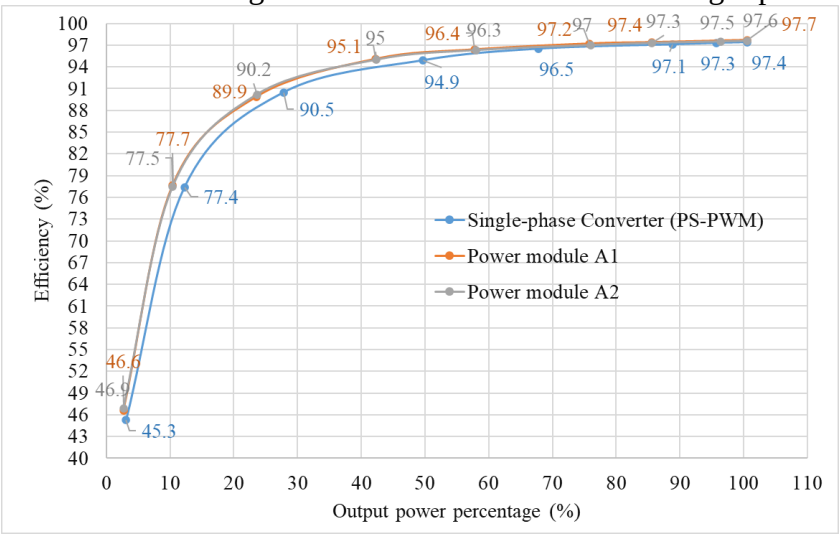


Fig. 2-48. Efficiency curve of the single-phase converter in different output power percentages

To reduce the parasitic capacitance-related losses and improve the converter efficiency, the PWM strategy introduced in Gen. I for the DC/AC stage is also adopted. With the proposed PWM, one half bridge is switched at 10 kHz, and the other one is switched at 60 Hz. The efficiency of the single-phase converter is improved from 97.4% to 98.4% at the rated power output, as shown in Fig. 2-49. Although the AC side equivalent switching frequency drops from 40 kHz to 20 kHz, it is still sufficient to meet the control bandwidth requirement.

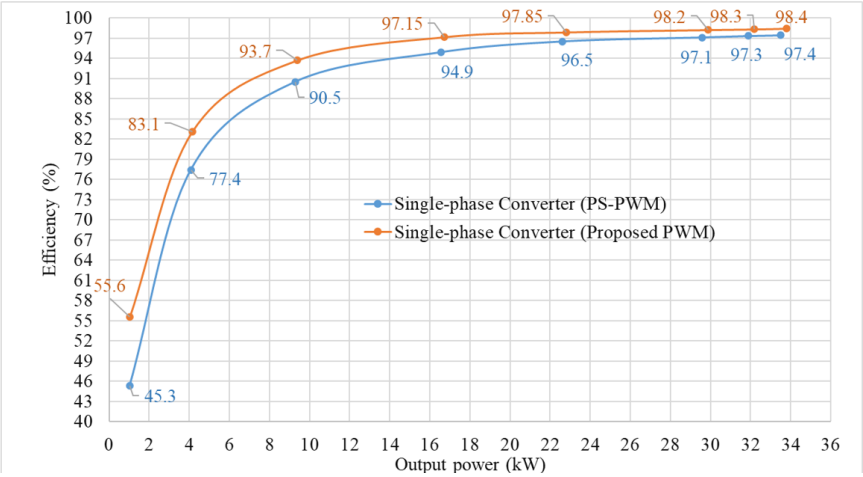


Fig. 2-49. Efficiency comparison of the single-phase converter under different PWM strategies

3. F-CHP CONTROLLER DESIGN

The F-CHP system involves multiple modes and states, and also transitions among them. The state machine and modes should be fully defined before designing the control strategies. With the defined state machines and modes, the functionality of controller can be discussed. Then, the central and local controllers are implemented in both HIL and HTB tests for validation.

3.1 F-CHP SYSTEM MODES, STATES AND FUNCTIONALITY

Fig. 3-1 shows the overall state machine of the F-CHP system. It has 5 main states – off, ready to run, grid-connected, islanded, and fault.

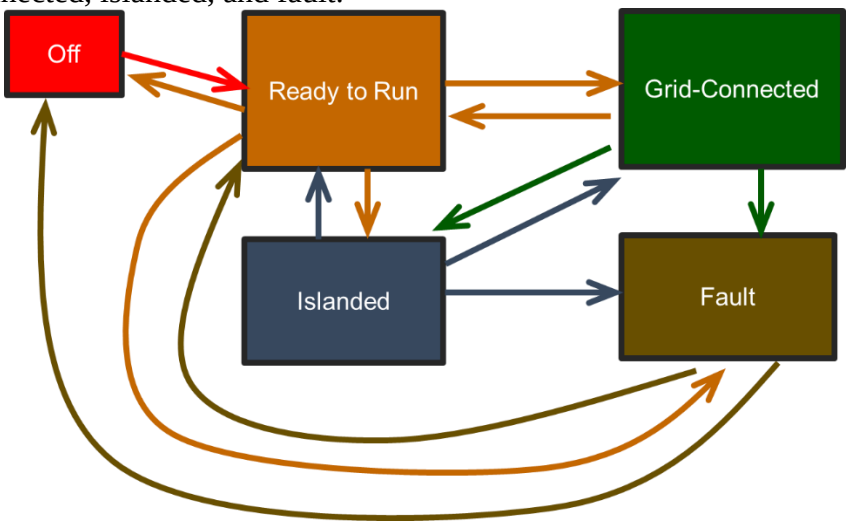


Fig. 3-1. State machine of the F-CHP system

Table 3-1 to Table 3-4 show the detailed modes in each state. In the tables, **R** indicates the component is running; **S** indicates the status of the component is stand-by, and is ready to run; **F** indicates the component is faulted, and cannot run; and **NA** indicates the component is not available in the system. Orange shaded cell indicates the component is controlling the DC link voltage, and the other component is controlling the active power output.

In each mode, when one of the components starts or stops running, the operating mode of the F-CHP system may change to a different one. The possible transitions to other modes within the state and to other states are listed.

Table 3-1. Modes in Grid connected state

Mode#	Grid	PCS	CHP	BESS	PV	Transition within GC	Transition to ISD	Transition to standby	Transition to fault
1	Yes	S/F	S/F	S/F/NA	R	3, 5, 9	1 (no change)	1, 3, 5, 7, 9, 11, 13, 15	1
2	Yes	S/F	S/F	R	S/F/NA	3, 6, 10	2 (no change)	2, 3, 6, 7, 10, 11, 14, 15	1
3	Yes	S/F	S/F	R	R	1, 2, 7, 11	3 (no change)	N/A	N/A
4	Yes	S/F	R	S/F/NA	S/F/NA	5, 6, 12	4 (no change)	4, 5, 6, 7, 12, 13, 14, 15	1
5	Yes	S/F	R	S/F/NA	R	1, 4, 7, 13	5 (no change)	N/A	N/A
6	Yes	S/F	R	R	S/F/NA	2, 4, 7, 14	6 (no change)	N/A	N/A
7	Yes	S/F	R	R	R	1, 2, 4, 15	7 (no change)	N/A	N/A
8	Yes	R	S/F	S/F/NA	S/F/NA	9, 10, 12	N/A	8, 9, 10, 11, 12, 13, 14, 15	1
9	Yes	R	S/F	S/F/NA	R	1, 8, 11, 13	9 (PCS mode change)	N/A	N/A
10	Yes	R	S/F	R	S/F/NA	2, 8, 11, 14	10 (PCS mode change)	N/A	N/A
11	Yes	R	S/F	R	R	3, 9, 10, 15	11 (PCS mode change)	N/A	N/A
12	Yes	R	R	S/F/NA	S/F/NA	4, 8, 13, 14	12 (PCS mode change)	N/A	N/A
13	Yes	R	R	S/F/NA	R	5, 9, 12, 15	13 (PCS mode change)	N/A	N/A
14	Yes	R	R	R	S/F/NA	6, 10, 12, 15	14 (PCS mode change)	N/A	N/A
15	Yes	R	R	R	R	7, 11, 13, 14	15 (PCS mode change)	N/A	N/A

Table 3-2. Modes in Islanded state

Mode#	Grid	PCS	CHP	BESS	PV	Transition within ISD	Transition (to GC)	Transition to standby	Transition to fault
1	No	S/F	S/F	S/F/NA	R	3, 5, 9	1 (no change)	17, 19, 21, 23, 25, 27, 29, 31	2, 4
2	No	S/F	S/F	R	S/F/NA	3, 6, 10	2 (no change)	18, 19, 22, 23, 26, 27, 30, 31	2, 4
3	No	S/F	S/F	R	R	1, 2, 7, 11	3 (no change)	N/A	N/A
4	No	S/F	R	S/F/NA	S/F/NA	5, 6, 12	4 (no change)	20, 21, 22, 23, 28, 29, 30, 31	2, 4
5	No	S/F	R	S/F/NA	R	1, 4, 7, 13	5 (no change)	N/A	N/A
6	No	S/F	R	R	S/F/NA	2, 4, 7, 14	6 (no change)	N/A	N/A
7	No	S/F	R	R	R	1, 2, 4, 15	7 (no change)	N/A	N/A
9	No	R	S/F	S/F/NA	R	1, 11, 13	9 (PCS mode change)	N/A	3
10	No	R	S/F	R	S/F/NA	2, 11, 14	10 (PCS mode change)	N/A	3
11	No	R	S/F	R	R	3, 9, 10, 15	11 (PCS mode change)	N/A	N/A
12	No	R	R	S/F/NA	S/F/NA	4, 13, 14	12 (PCS mode change)	N/A	3
13	No	R	R	S/F/NA	R	5, 9, 12, 15	13 (PCS mode change)	N/A	N/A
14	No	R	R	R	S/F/NA	6, 10, 12, 15	14 (PCS mode change)	N/A	N/A
15	No	R	R	R	R	7, 11, 13, 14	15 (PCS mode change)	N/A	N/A

Table 3-3. Modes in Ready to Run state

Mode#	Grid	PCS	CHP	BESS	PV	Transition within Standby	Transition to GC	Transition to fault
1	Yes	F	F	F/NA	S	3, 5, 9, 17	1	1
2	Yes	F	F	S	F/NA	3, 6, 10,18	2	1
3	Yes	F	F	S	S	1, 2, 7, 11, 19	1, 2	N/A

4	Yes	F	S	F/NA	F/NA	5, 6, 12, 20	4	1
5	Yes	F	S	F/NA	S	1, 4, 7, 13, 21	1, 4	N/A
6	Yes	F	S	S	F/NA	2, 4, 7, 14, 22	2, 4	N/A
7	Yes	F	S	S	S	1, 2, 4, 15, 23	1, 2, 4	N/A
8	Yes	S	F	F/NA	F/NA	9, 10, 12	8	1
9	Yes	S	F	F/NA	S	1, 8, 11, 13, 25	1, 8	N/A
10	Yes	S	F	S	F/NA	2, 8, 11, 14, 26	2, 8	N/A
11	Yes	S	F	S	S	3, 9, 10, 15, 27	1, 2, 8	N/A
12	Yes	S	S	F/NA	F/NA	4, 8, 13, 14, 28	4, 8	N/A
13	Yes	S	S	F/NA	S	5, 9, 12, 15, 29	1, 4, 8	N/A
14	Yes	S	S	S	F/NA	6, 10, 12, 15, 30	2, 4, 8	N/A
15	Yes	S	S	S	S	7, 11, 13, 14,31	1, 2, 4, 8	N/A
17	No	F	F	F/NA	S	1, 19, 22, 25	1	2
18	No	F	F	S	F/NA	2, 19, 23, 26	2	2
19	No	F	F	S	S	3, 17, 18, 23, 27	1, 2	N/A
20	No	F	S	F/NA	F/NA	4, 21, 22, 28	4	2
21	No	F	S	F/NA	S	5, 17, 20, 23, 29	1, 5	N/A
22	No	F	S	S	F/NA	6, 18, 20, 23, 30	2, 4	N/A
23	No	F	S	S	S	7, 17, 18, 20, 31	1, 2, 4	N/A
25	No	S	F	F/NA	S	9, 17, 27, 29	1	4
26	No	S	F	S	F/NA	10, 18, 27, 30	2	4
27	No	S	F	S	S	11, 19, 25, 26, 31	1, 2	N/A
28	No	S	S	F/NA	F/NA	12, 20, 29, 30	4	4
29	No	S	S	F/NA	S	13, 21, 25, 28, 31	1, 4	N/A
30	No	S	S	S	F/NA	14, 22, 26, 28, 31	2, 4	N/A
31	No	S	S	S	S	15, 23, 27, 29, 30	1, 2, 4	N/A

Table 3-4. Modes in Fault state

Mode#	Grid	PCS	CHP	BESS	PV	Description	Transition to Standby
1	Yes	F	F	F/NA	F/NA	All faulted (with grid)	1, 2, 4, 8
2	No	F	F	NA/F	F/NA	All faulted (without grid)	17, 18, 20, 24
3	No	R	S/F	S/F/NA	S/F/NA	No component to support LVDC	25 – 31
4	No	S	F	F/NA	F/NA	PCS cannot do anything	25, 26, 28

In addition, the controller should also allow the operation of medium voltage CHP that directly connects to the distribution network, although not the main focus of this project. In this case, there will be no PCS, BESS, and PV available. The modes in each state are shown in Table 3-5.

Table 3-5. State machine for 60 Hz medium voltage CHP that directly connect to grid

State	Grid	PCS	CHP	BESS	PV
Grid-connected	Yes	NA	R	NA	NA
Islanded	No	NA	R	NA	NA
Standby #1	Yes	NA	S	NA	NA
Standby #2	No	NA	S	NA	NA
Fault #1	Yes	NA	F	NA	NA
Fault #2	No	NA	F	NA	NA

Next, the functions that run in each state are defined in Table 3-6 to Table 3-9, showing the function is operated in which state and mode, and the inputs and outputs, respectively.

Table 3-6. Functions that run in F-CHP Central Controller

Functions	Operate in	Inputs	Outputs

State Machine	All states, all modes	• Status of each local components • Triggering event (disconnection / reconnection from operator, etc.)	• Enabling signal of each function • Current state / operating mode
Datalogging	All states, all modes	• System status and measurements	• Log files
Load Forecasting	All states except fault state	• Historic load profile • Current load measurement • Other aspects (week-day / weekend, etc.)	• Load profile in future 24h
PV Forecasting	Grid-connected and islanded states mode 1, 3, 5… 15 (PV operating)	• Historic PV profile • Current PV measurement • Other aspects (weather info: cloud coverage, temperature, etc.)	• PV profile in future 24h
Energy management	All states except fault state	• Forecasted PV/Load info • Tariff info • (CHP characteristics) • (Battery characteristics)	• Long term dispatch plan for the sources and controllable loads over next 24h according to the forecasts
Protection coordination	All states	• Status of internal components and grids	• Relay profile setting • Load shedding command • PV curtailment command
Active power control coordination	All states except fault state	• Status of internal components • Dispatch plan from energy management • Grid frequency • Output power demand	• Component to control DC link voltage • PCS output power maximum range • Source output power setpoint

Table 3-7. Functions that run in Local Load Local Controller

Functions	Operate in	Inputs	Outputs
Demand Response	Grid-connected state, mode 8-15 (PCS operating)	• Dispatch plan from energy management	• Controllable load consumption
Load shedding and restoration	Islanded state and grid-connected state mode 1-7 (PCS not operating)	• Protection coordination command	• Controllable load consumption • Other load switch

Table 3-8. Functions that run in Source Local Controller

Functions	Operate in	Inputs	Outputs
Prime mover / generation control	Grid-connected and islanded states, mode 4-7 and 12-15 (CHP operating)	• CHP output power command	• CHP prime mover command
Active power / DC link control	Grid connected and Islanded states	• Set points from Active power control coordination in MGCC • DC link voltage measurement	• Control signals of sources follow the active power setpoints

Table 3-9. Functions that run in PCS Local Controller

Functions	Operate in	Inputs	Outputs
P/Q control	Grid-connected state, mode 8-15	• P/Q command from operator • PF command from operator • Voltage setpoint from operator • Grid voltage and frequency measurements	• Control signals of PCS output active and reactive power

V/F control	Islanded state, mode 9-15	• V/F command from operator	• Control signals of PCS output voltage magnitude and frequency
Resynchronization	Islanded state, mode 9-15, by triggering resync command	• Voltage magnitude, frequency, angle difference across the PCC switch • Resync command from operator	• Output voltage magnitude, frequency offset of PCS

The control architecture of F-CHP controller is depicted below in Fig. 3-2.

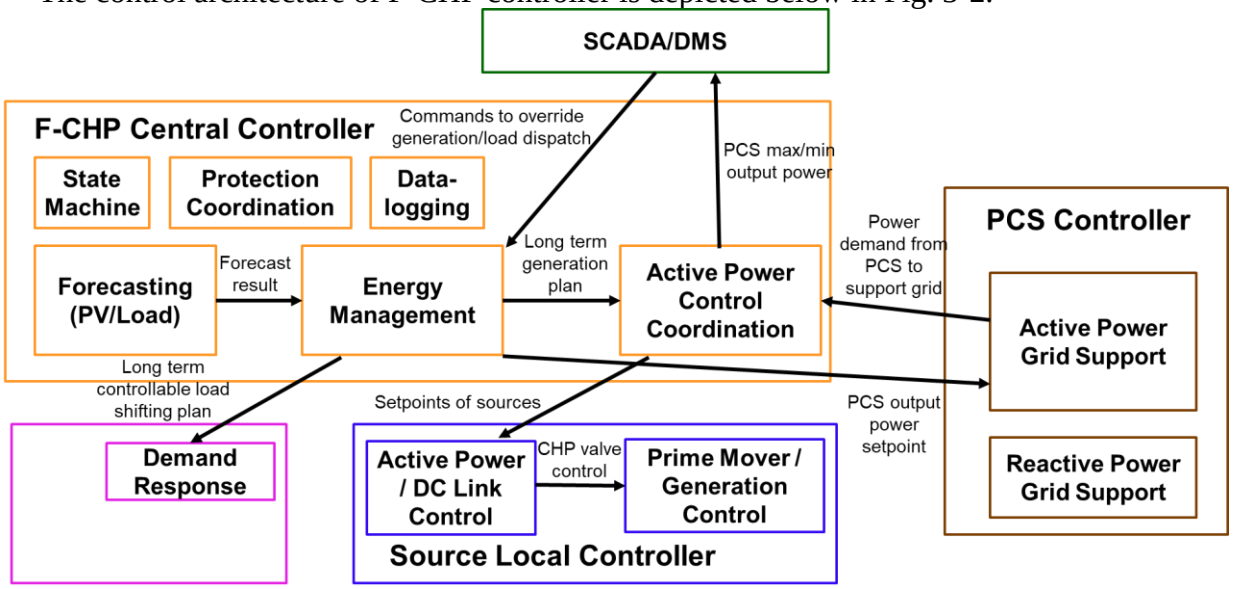


Fig. 3-2. F-CHP controller function diagram

3.2 F-CHP CONTROL ALGORITHM DEVELOPMENT

3.2.1 State Machine

The state machine function gathers the status of the components in the F-CHP system, and determines the operating condition. It has 5 main states – off, ready to run, grid-connected, islanded, and fault. Detailed modes and transitions are presented in 3.1. By determining the state, the controller can determine the functions to be enabled, and components controlling the DC-link voltage.

3.2.2 Datalogging

The datalogging function is used to record the system status for later analysis or debug. Table 3-10 shows the variables to be recorded.

Table 3-10. Datalogging variables

PCS CHP PV BESS Load	PCS CHP PV BESS Load	PCS CHP PV BESS Load	PCS CHP PV BESS Load	PCS CHP PV BESS Load
Grid voltage	CHP output electrical power	PV output power	BESS output power	Load active power
Grid frequency	CHP output thermal power	PV curtailment	BESS state of charge	Load reactive power
PCS output power	CHP speed	PV operating state	BESS operating state	Load shedding status
PCS output reactive power	CHP operating state			
PCS operating state				
DC link voltage				

3.2.3 Load Forecasting

The distribution utility usually has access to load forecasting functions in the Distribution Management System (DMS). The load forecasting function in DMS typically uses temporal and weather data to generate system load forecasts for the entire feeder or distribution system. In the F-CHP controller, the load forecasting function focuses on a small service area surrounding the CHP generator. Considering the capability of the F-CHP system to independently operate in islanded mode, the load forecasting function will use recent historical measurement data to make short-term forecasts. The Autoregressive Moving Average (ARMA) method is one of the simplest yet more reliable algorithms used for time-series data analytics. The method uses past p observations and q prediction errors to predict the next data point in the time-series. It is suitable for the prediction of stationary time-series data with periodical variations [12].

Depending on the load type (including commercial load, residential load, small and large industrial load), the loads may exhibit different characteristics on weekdays and weekends (also including holidays). Therefore, using the corresponding historical data for load forecasting on weekdays and weekends will improve forecasting accuracy. The F-CHP controller will be able to separate the historical data points into their respective data sets, and use them to generate the corresponding forecasts.

3.2.4 PV Forecasting

Similar to the load forecasting function, the PV forecasting function will also utilize historical PV generation data available to the F-CHP controller to make short-term forecasts. Research in this area shows the ARMA method to be suitable for short-term forecasting of PV generation. However, the amount of power PV output is largely affected by cloud cover. If the historical PV generation data are combined into one dataset, PV output during different cloud cover conditions will mix and detrimentally affect the forecasting accuracy. Considering the abovementioned impacts of cloud cover, the PV forecasting function will classify days by the cloud cover conditions indicated by cloud cover indices. Based on cloud cover forecasts, the PV forecasting function will use the ARMA trained by the corresponding data set to generate PV output forecasts.

3.2.5 Energy Management

The Energy Management function in the F-CHP system utilizes the load and PV forecasts generated by the Load Forecasting and PV Forecasting functions, respectively. The Energy Management function generates dispatch commands for the sources in the CHP system, as well as loads served by the CHP system. The sources in the CHP system can include the CHP generator, PV, as well as energy storage systems such as batteries. The dispatch is generated by solving optimization problems that are specific to the current operating mode and as well as the ownership of the CHP system.

Fig. 3-3 summarizes the data flow around the Energy Management function. The forecasting results are sent from the PV Forecasting and Load Forecasting functions. Other parameters required by the Energy Management function are from external inputs (for example, local data files on the controller). The dispatch setpoints are sent to the Active Power Control Coordination function for execution.

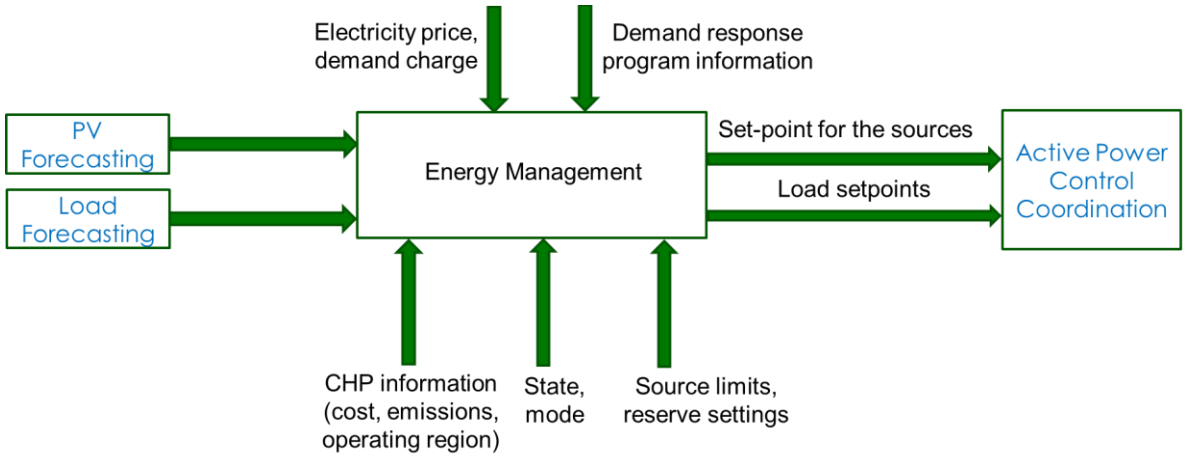


Fig. 3-3. Data flow of the Energy Management function

3.2.6 Active Power Control Coordination

After the generation plan is optimized by Energy Management function, the Active Power Control Coordination function generates the real-time set-points for the sources, loads and PCS. The Active Power / DC Link Control function in source local controller, Load Shedding and Restoration in local load local controller, and P/Q control in PCS local controller will carry out the setpoints. System operator may need to override the dispatch command provided by the Energy Management function. Active Power Control Coordination function also calculates the maximum or minimum power capability that F-CHP system has. In addition, depending on the grid frequency, the F-CHP system may help to inject or absorb additional active power to participate in the system primary frequency control. The overall data flow of this function is shown in Fig. 3-4.

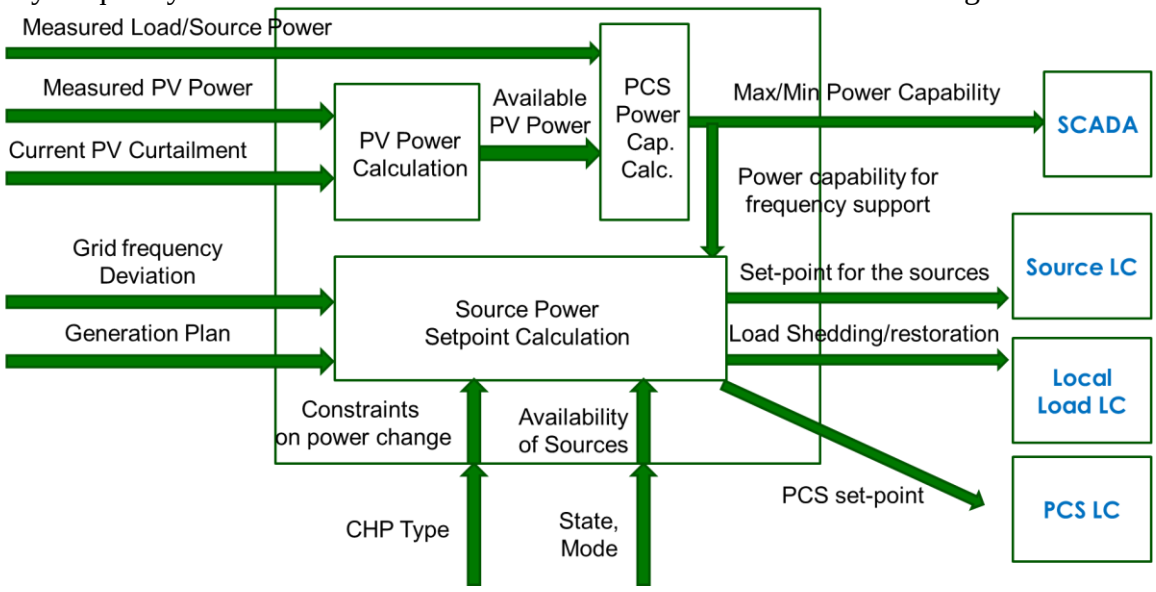


Fig. 3-4. Data flow of the Active Power Control Coordination function

3.2.7 Protection Coordination

Depending on grid-connected or islanded condition, the system response after a short circuit fault in the outside AC system is different. During grid-connected operation, the fault current is supplied by the grid, and the PCS will try to ride-through the fault. And during islanded operation, PCS supplies the fault current with reduced voltage. The protection coordination function monitors

the state of the F-CHP system, and give updates to the protection settings of the relays to ensure the safe operation of the system. In addition, during the fault ride-through or F-CHP system internal faults, DC-link voltage may rise or drop rapidly due to the power imbalance between the generation and consumption. Protection Coordination function will trigger the load shedding or PV curtailment to help maintaining system operation.

3.2.8 Active Power / DC Link Control

This function is in the source local controller. It takes the setpoints set by Active Power Control Coordination function, and sends them to the generation sources (CHP, PV, or BESS). If the generation source is controlling the DC link, a closed-loop control will be applied, as shown in Fig. 3-5.

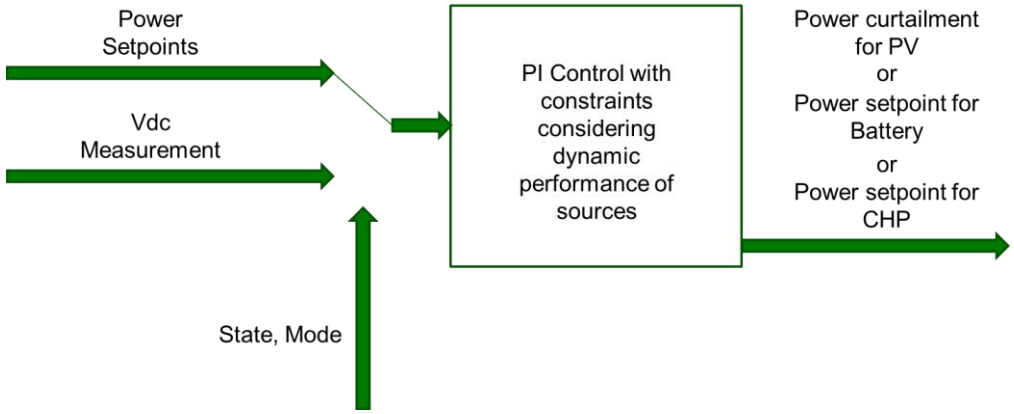


Fig. 3-5. Data flow of the Active Power / DC Link Control

3.2.9 Demand Response

This function is in local load local controllers that follows dispatch signals from the central controller. Demand response programs are ways the utilities interact with customers through Time-Of-Use (TOU) electricity pricing or load curtailment agreements. Depending on the agreement reached in the demand response program, the utility will have the ability to either directly control (curtail) the load or influence electricity consumption through setting real-time electricity prices. In the F-CHP controller, the Demand Response block is an optional function that, if a demand response agreement has been reached, controls the curtailment of the loads. The Demand Response function will follow the dispatched load setpoints given by the Active Power Control Coordination function.

3.2.10 Load Shedding and Restoration

This function is in local load controllers and will execute commands given by the central controller. The Load Shedding and Restoration function works in conjunction with Active Power Control Coordination as well as Protection Coordination functions to determine the service area of the CHP system during islanded operation. During normal islanded operation, the Active Power Control Coordination will determine the service area that is or to be energized, and send reference signals to the Load Shedding and Restoration. If the system experiences a fault, the Protection Coordination function will send tripping signals to the Load Shedding and Restoration function to trip load sections and execute reclosing functions (if applicable).

3.2.11 P/Q control

This function is in PCS local controller, enabled during grid-connected operation. It carries out the power setpoint generated by the Active Power Control Coordination function in the central controller. The output power includes economic dispatch and transient power injection for grid frequency support. For reactive power control, the PCS may output 0 var for unity power factor, or constant power factor indicated by the system operator, or actively control its terminal voltage with V/Q control.

3.2.12 V/F control

This function is in PCS local controller, enabled during islanded operation. It tries to maintain the output voltage and frequency as needed.

3.2.13 Resynchronization

This function is in PCS local controller, enabled only during transition from islanded state to grid-connected. The voltage difference between the main grid and the F-CHP island will be controlled by this function to a minimal value for reconnection.

3.3 F-CHP CONTROLLER SIMULATION

3.3.1 Simulation platform

Transient/short term model is used to validate the PCS's P/Q and V/F controls. It includes detailed CHB and DAB model, and ideal CHP and other sources and loads in the system, with very low simulation time step. The model is shown in Fig. 3-6.

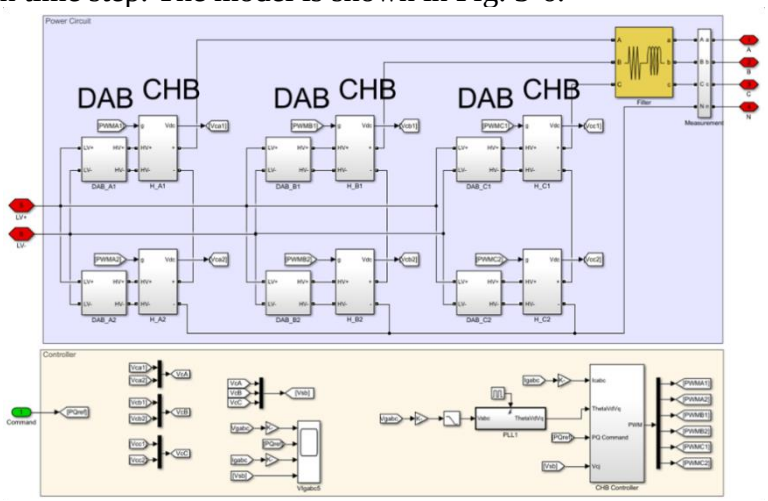


Fig. 3-6. Transient/short-term switching model of PCS

Short term model is used to validate the coordination between F-CHP system components. It includes the CHP, PV, Battery's model with constraints. And the distribution grid is derived from a prospective CHP site gathered from EPB. The model is shown in Fig. 2.2.

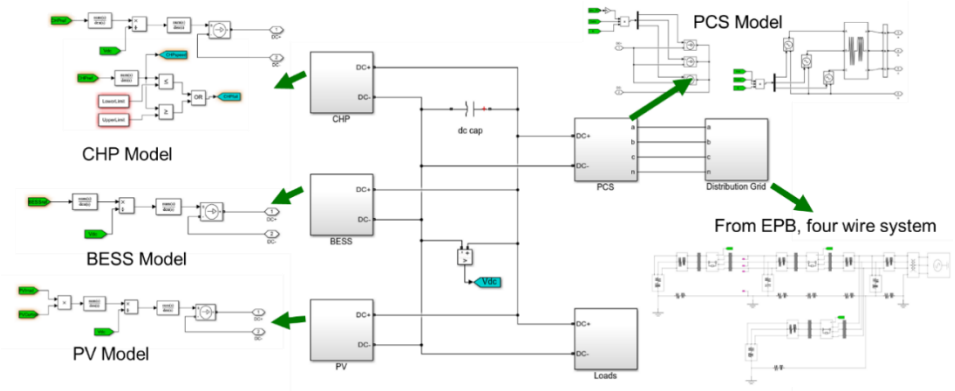


Fig. 3-7. Short term average model

Long term model is used to validate economic dispatch of F-CHP system. It is developed in the MATLAB environment. The energy management model is scripted and saved as an m-file and run by supplying it with user-input data.

3.3.2 Simulation validation

In transient/short term model, PCS closed-loop control are validated. Fig. 3-8 shows the current closed-loop control performances. The actual output current follows the references. From the step response, the control bandwidth can be estimated to be higher than 1 kHz. Fig. 3-9 shows the voltage closed-loop control performances. From the step response, the control bandwidth can be estimated to be higher than 300 Hz. Both current and voltage control bandwidths satisfy the defined controller requirement, (1000 Hz and 300 Hz respectively) Fig. 2.5 shows the frequency and voltage variation if the load changes.

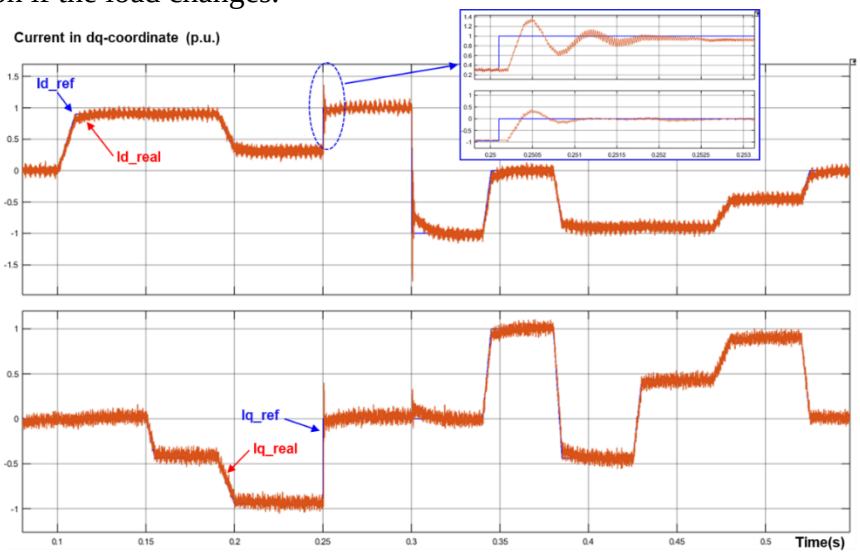


Fig. 3-8. PCS current closed-loop control simulation result

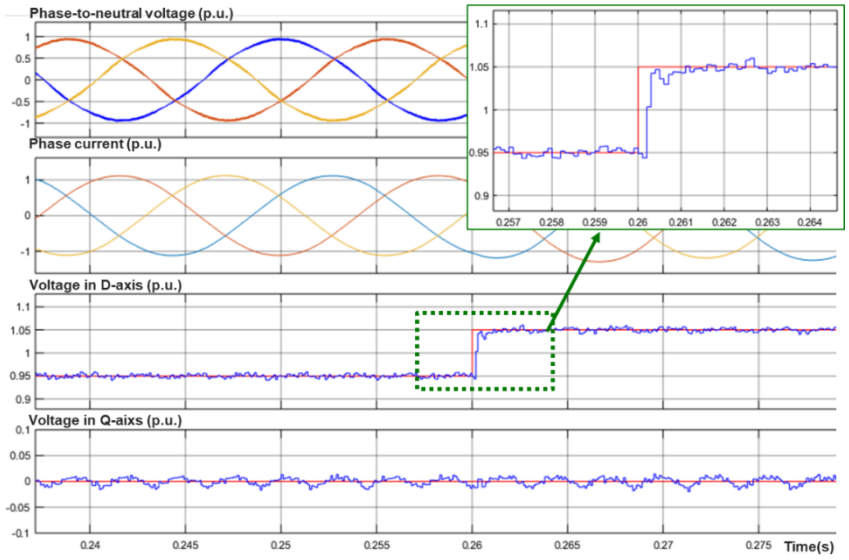


Fig. 3-9. PCS voltage closed-loop control simulation result

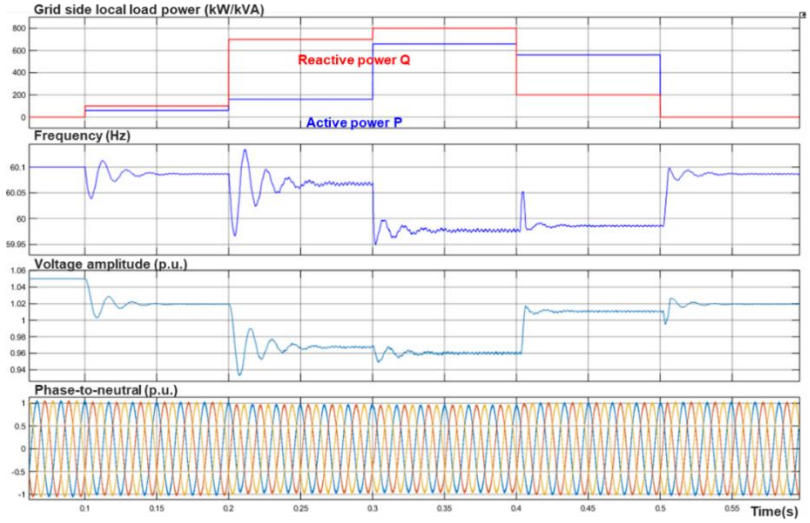


Fig. 3-10. PCS voltage closed-loop control simulation result with load variation

In short term average model, the active power coordination function in F-CHP CC and corresponding controls in local controllers are validated. Fig. 3-11 to Fig. 3-13 give some examples of the testing results. Fig. 3-11 shows the test case of PCS starting in islanded condition. Before PCS start, the PV and CHP (gas turbine) serves the critical local load through F-CHP system LVDC link. Due to the excess power, PV output is curtailed. After PCS starts, PV output power resume to be maximum, following the MPPT. CHP output power is also controlled to increase, to maintain the power balance. Control limits are applied to prevent applying too large disturbances to the CHP source.

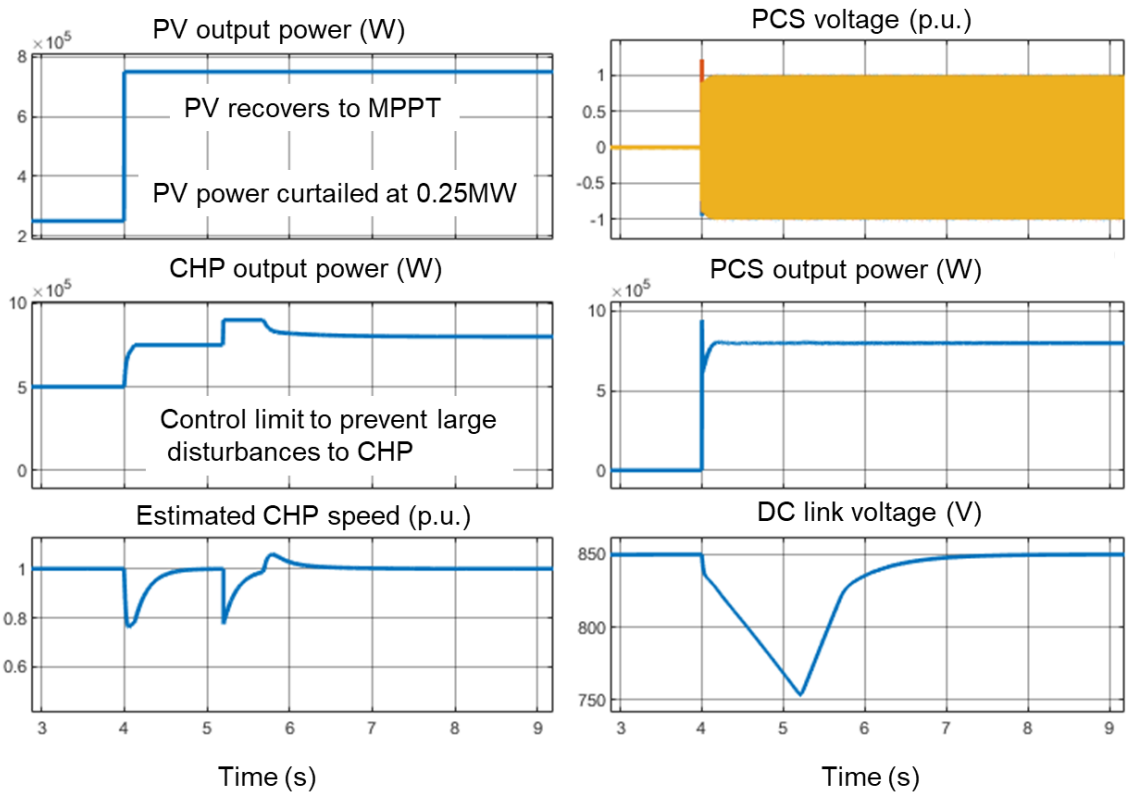


Fig. 3-11 Test case of PCS start in islanded condition

Fig. 3-12 shows the test case of internal PV fault. At 4s, PV's output power drops from 1 MW to 0 suddenly due to fault. The DC-link drops, and the fault is detected. PCS is then controlled to shut-down to reduce the total load, and help maintaining the power balance between the sources and loads. CHP (Micro-turbine) also increases its output, and continues to supply the critical load though LVDC.

Fig. 3-13 shows the test case of resynchronization. Before the event, the F-CHP system was in islanded operation. And PCS is supplying the AC loads. The main grid becomes available, and the PCS's output voltage is controlled to minimize the voltage difference across the PCC switch. Once the voltage difference is reduced, at 4.6 s, the PCC switch is closed, and the F-CHP CC notifies the PCS to transition to current closed-loop control, while maintaining the previous output power. Since the overall power balance between the sources and loads remains the same, the variation on the LVDC voltage is also small.

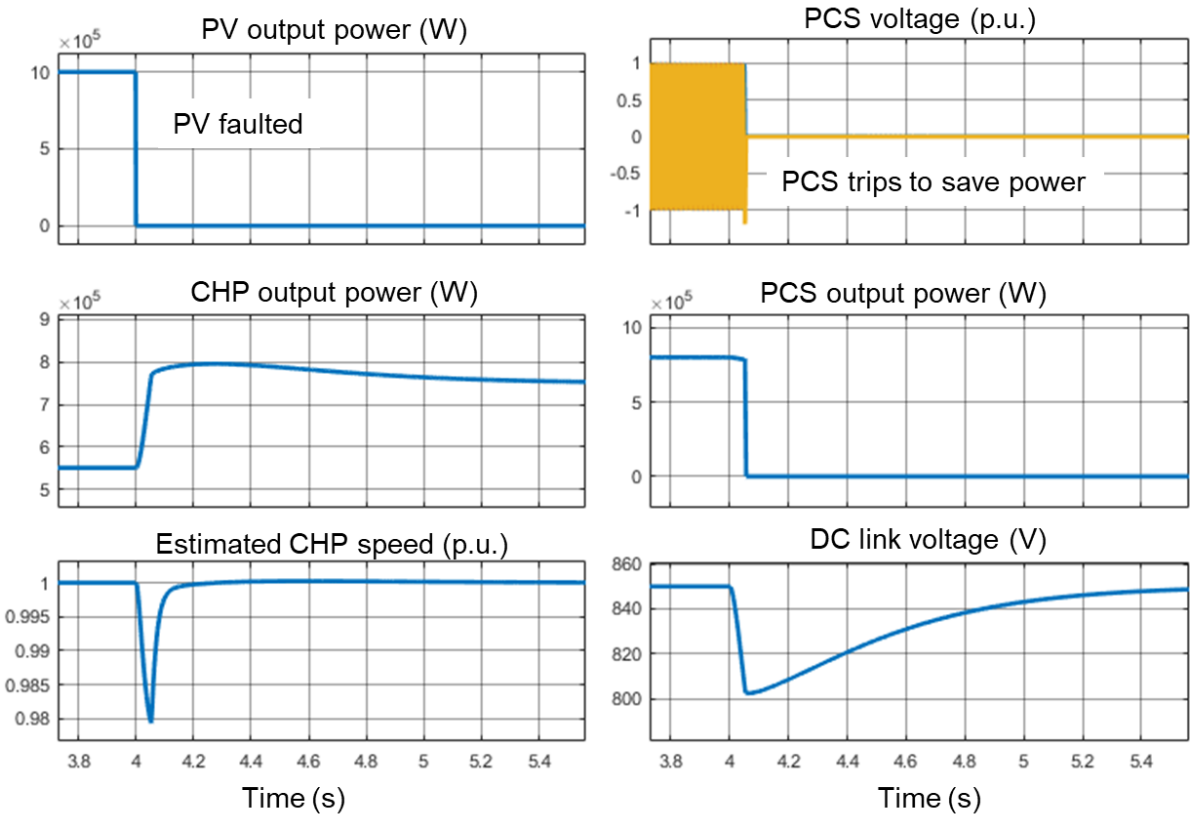


Fig. 3-12. Test case of internal PV fault

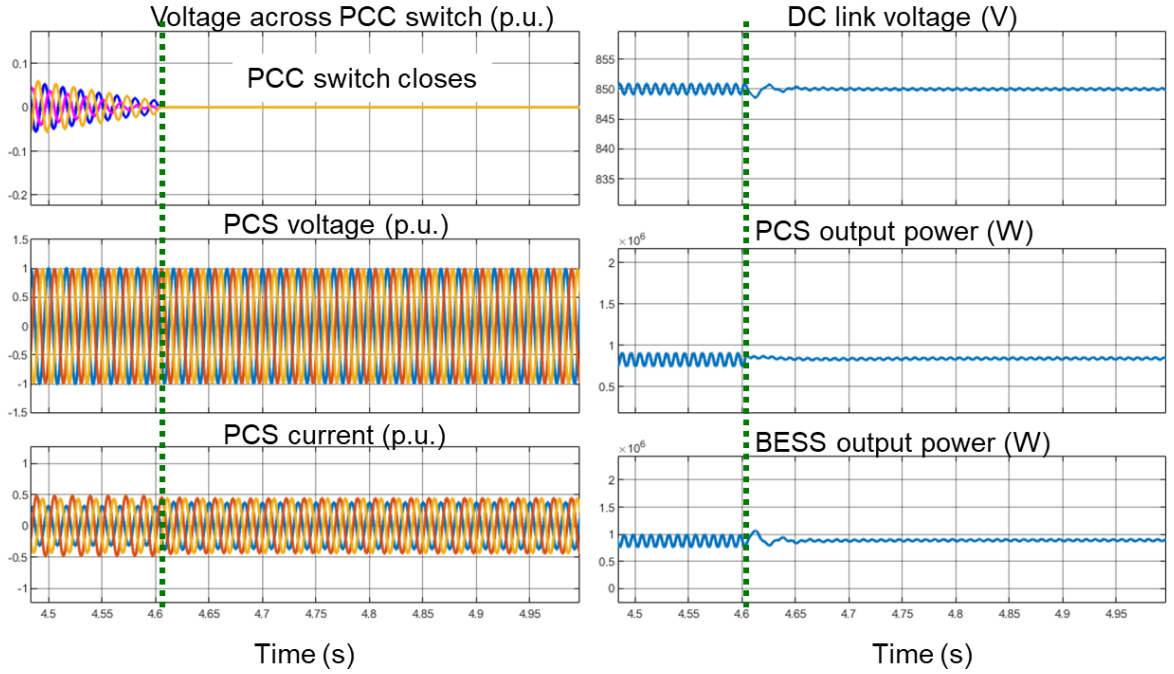
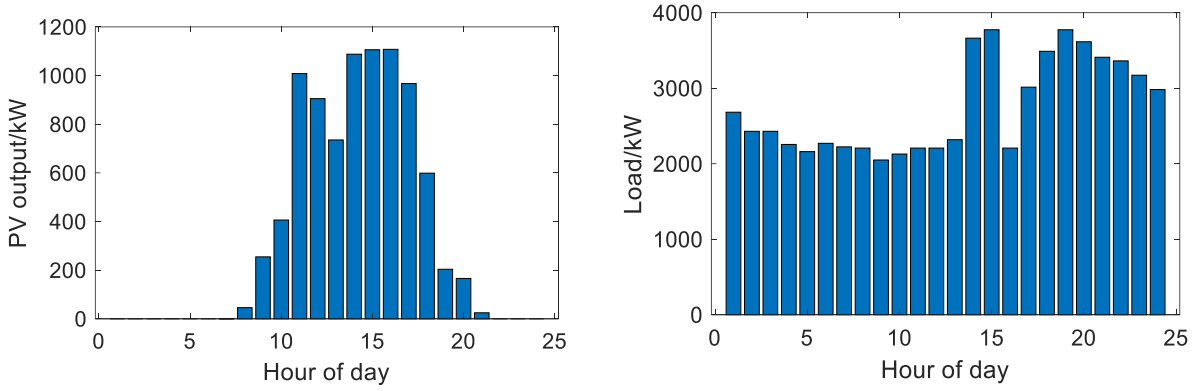


Fig. 3-13. Test case of resynchronization from islanded to grid-connected operation

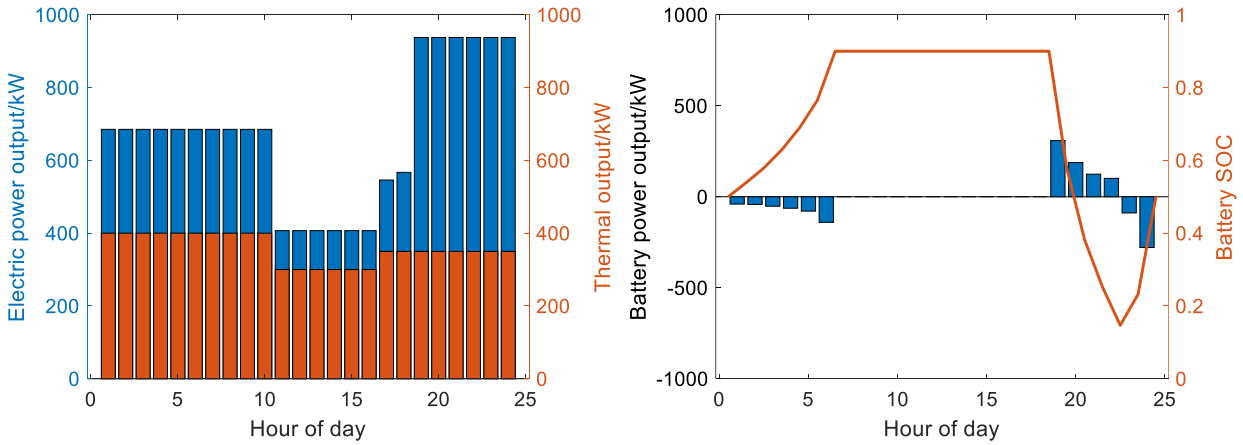
In the long-term model, the energy management function with demand response program modeling is validated.



(a) PV profile (b) Load profile

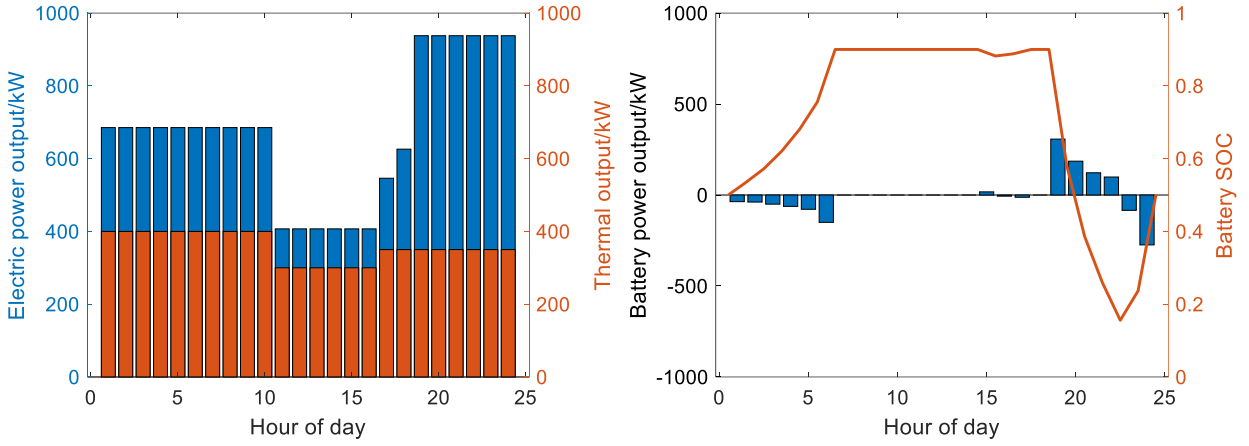
Fig. 3-14. Test case of energy management in grid-connected operation

Fig. 3-14 shows the PV profile and load profile assumed in the grid-connected operation model. The detailed model is reported in the previous quarter. The energy management function is able to generate an economic dispatch for the CHP and Battery Energy Storage System (BESS) based on the PV generation and load profiles, as well as the availability of a demand response program. Fig. 3-15 and 3-16 show the dispatch results without and with the demand response program, respectively. The difference in output powers is small, mainly due to the limited curtailment capacity assumed in the demand response program. Fig. 3-17 shows the hourly curtailment of loads as a result of the demand response program.



(a) CHP dispatch (b) BESS dispatch

Fig. 3-15. Dispatch results in the absence of a demand response program



(a) CHP dispatch (b) BESS dispatch

Fig. 3-16. Dispatch results in the presence of a demand response program

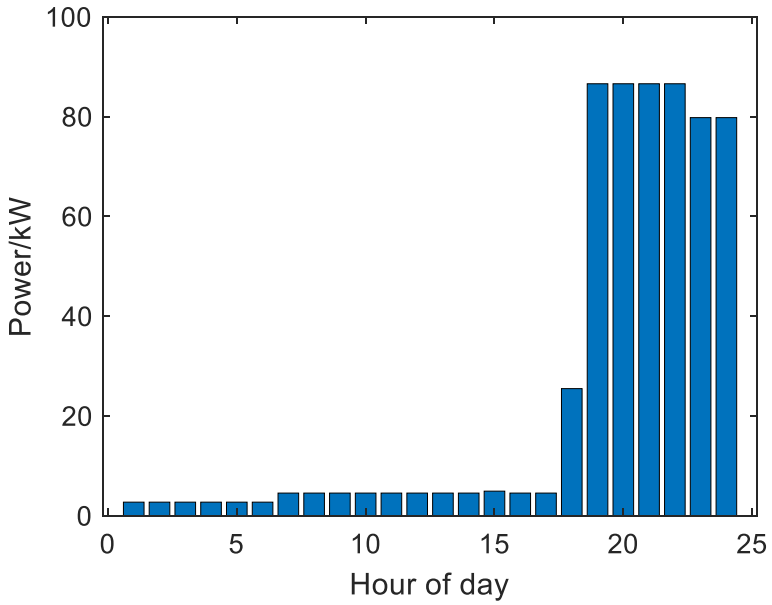
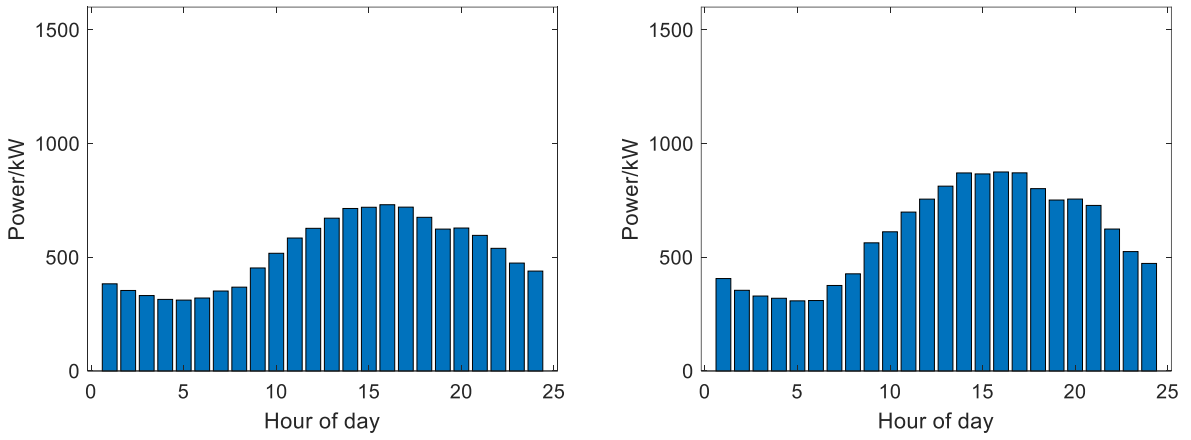


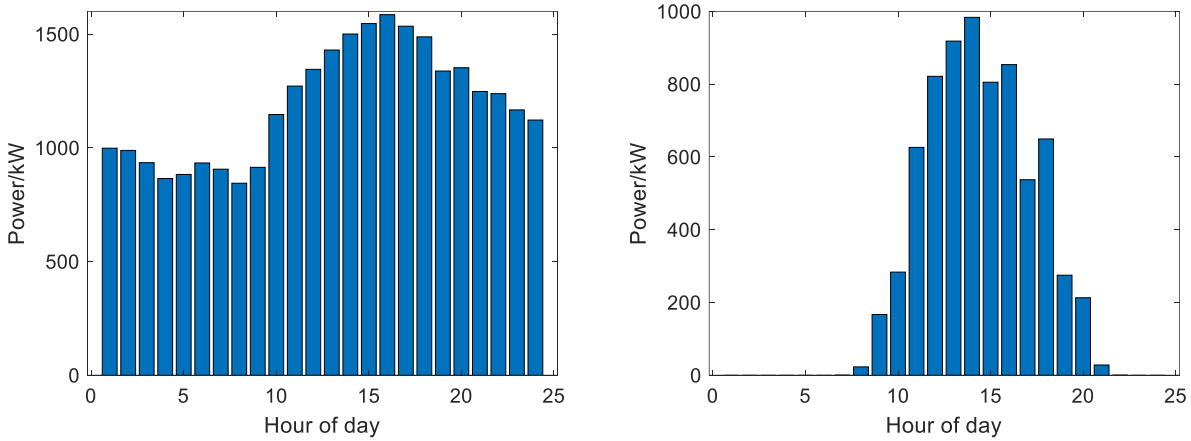
Fig. 3-17. Hourly load curtailment under the demand response program

In the islanded operation, we assume that the F-CHP system can extend or shrink its service area to neighboring load sections through the switching of remotely controlled smart switches. Fig. 3-18 (a)-(c) shows the load profiles of the load sections that are connected in series to the F-CHP system. Load section 1 is directly connected to the F-CHP system, while load section 2 is connected to load section 1. Load section 3 is connected to load section 2. The PV profile we used is shown in Fig. 3-18(d).

Fig. 3-19 shows the dispatch results in islanded operation. Compared to grid-connected operation, the CHP will output more power during the day, and the F-CHP system combined with the PV system will be able to service as many load sections as possible. The hourly dispatch of loads is shown in Table 2.2.

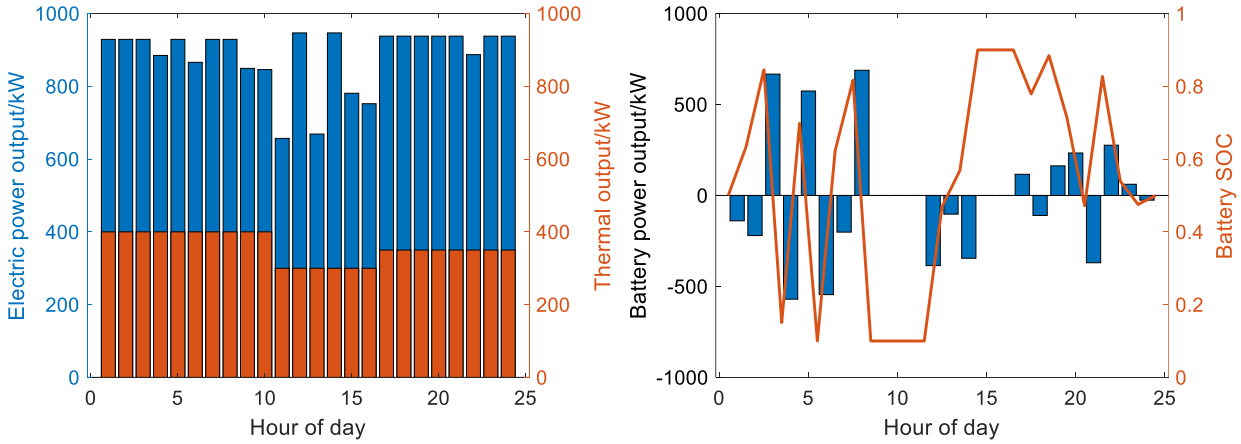


(a) Load Section 1 (b) Load Section 2



(c) Load Section 3 (d) PV profile

Fig. 3-18. Load profiles of the load sections connected to the F-CHP system



(a) CHP dispatch (b) BESS dispatch

Fig. 3-19. Dispatch results in islanded operation

Table 3-11. Hourly dispatch of load sections in islanded operation (1=connected)

Hour	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

Load1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Load2	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	
Load3	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Overall, the control algorithms are tested individually through different simulation platforms. A more thorough test with all functions implemented in the actual controller is conducted in HIL test.

3.4 F-CHP CONTROLLER TEST

Table 3-12 shows the system configuration and general test cases for HIL and HTB tests. In section 3.4.1, HIL tests will be introduced, and HTB test cases will be discussed in section 3.4.2.

Table 3-12. System configuration and general test cases for HIL and HTB tests

	HIL	HTB
System configuration	Simplified F-CHP system model, including • CHP (dc source with range/ramp constraints), • BESS (dc source with SOC constraints), • PV (dc source with predetermined output profile, can be curtailed), • LL (dc load, can be shed/restored partially) • PCS (2 level converter with average model) • AC circuit (2 sections, based on EPB model)	Downscaled PCS with • Actual CHB and DAB • AC circuit emulated by one HTB converter with transformer connection, 4 wire system • DC circuit emulated by one HTB converter, representing CHP, BESS, PV, LL
Test cases	Focus on system coordination • F-CHP system start • F-CHP system grid-connected operation • F-CHP system islanded operation • Resynchronization • Grid fault and islanding • Internal component fault handling	Focus on PCS operation • PCS start • PCS control power (grid-connected) • PCS control AC voltage (islanded) • PCS operating mode transitions • PCS operation under power system transients

3.4.1 HIL test

Opal-RT is used as the HIL testing platform to model the F-CHP system and study the coordination among the F-CHP system components. The planned system testing architecture is shown in Fig. 3-20. The controller will receive operating status from and issue control commands to the Opal-RT real-time simulator through a DNP3 communication protocol, which is commonly used among the distribution utilities' SCADA system.

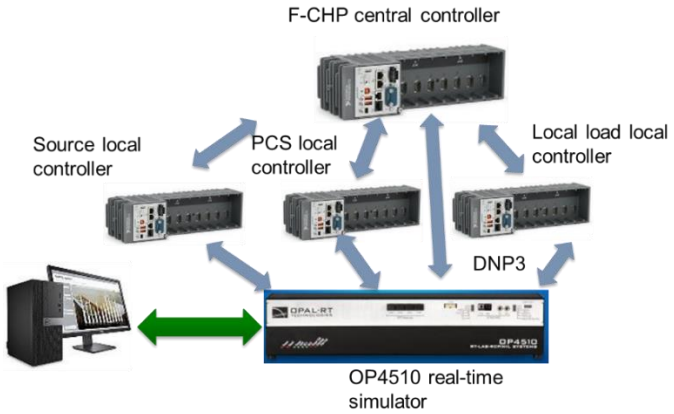


Fig. 3-20. Illustration for the HIL test architecture

3.4.1.1 Black Start

The black start test scenario includes two cases when the F-CHP system starts up from islanded and grid-connected conditions. Fig. 3-21 shows the system start-up sequence in islanded condition to demonstrate the system performance.

- At event 1, CHP starts to ramp up
- At event 2, CHP speed ramps to 1 p.u., and the F-CHP system recognizes the CHP is online, and has it to regulate DC link voltage. The power adjustment from the CHP source caused variations in its speed.
- At event 3, a 250 kW non-critical load is enabled.
- At event 4, BESS starts and takes over the DC-link control from CHP. Since then, CHP will not actively control the DC link voltage. The F-CHP controller controls its prime mover to supply power to the F-CHP system. Thus, its rotational speed will not have large transients.
- At event 5, the 500-kW critical load is enabled.
- At event 6, PV is enabled to output 500kW active power
- At event 7, with enough power, PCS starts and serves neighboring AC loads.
- At event 8, PV power increases to rated 1MW.
- At event 9, with enough power, F-CHP controller issues command to SCADA and pick-up additional loads from the AC system.

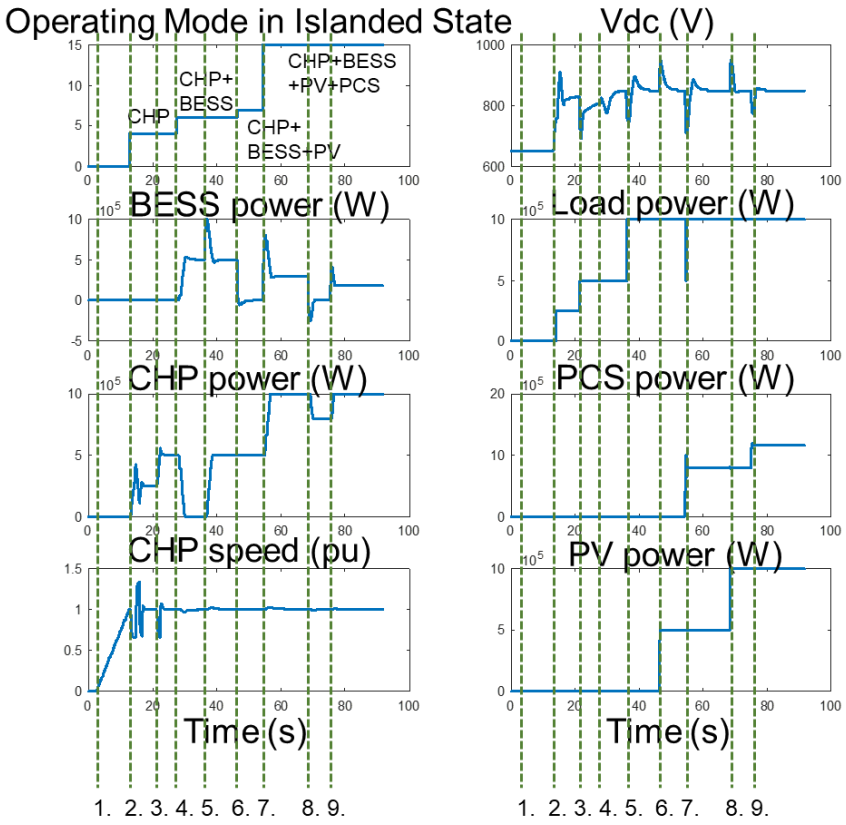


Fig. 3-21. Black start test in islanded condition

Fig.3-22 shows the system start-up sequence in grid-connected conditions to demonstrate system performance.

- At event 1, PCS starts and regulates the DC link voltage
- At event 2, CHP starts to ramp up. Local DC Loads are enabled. Without sources in the system, PCS can only absorb power from the grid to maintain the system power balance.
- At event 3, CHP speed ramps to 1 p.u. and becomes available to help with system dispatch. It ramps the power up to allow PCS to maintain 0 power exchange from the grid, as dispatch commands.
- At event 4, PV starts and generates 1MW active power. BESS starts to help with system dispatch.
- At event 5, the 500kW critical load is enabled. BESS power changes to maintain the system dispatch as 0 power exchange.
- At event 6, the system operator changed the dispatch command to let the F-CHP system generate 1MW active power. CHP ramps up to carry out the command.
- At event 7, the system operator changed the dispatch command again, to let F-CHP system absorb 1MW active power. CHP and BESS ramp down to carry out the command.

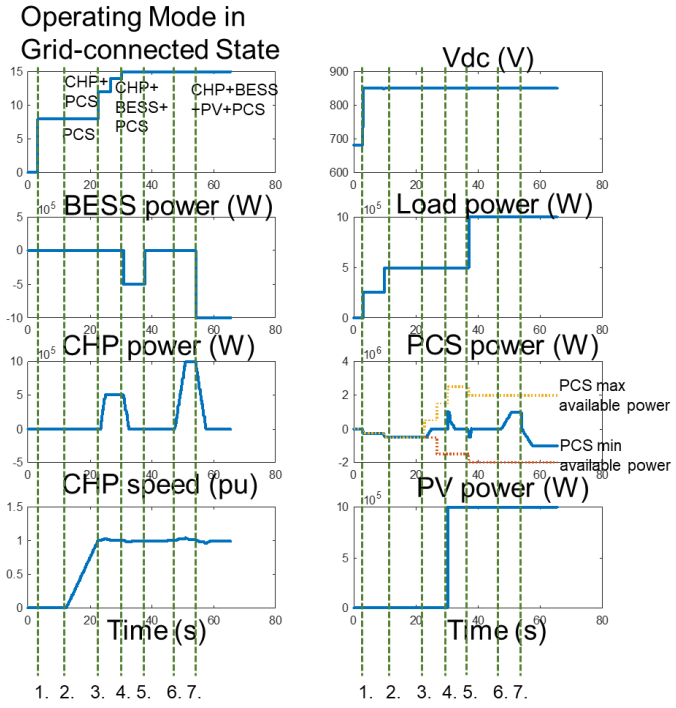


Fig. 3-22. Black start test in grid-connected condition

In both cases, the system Vdc is maintained to be higher than 700 V as the metrics defined in the previous quarter.

3.4.1.2 Grid-connected operation

Since the power dispatch function has been introduced in the black start function. The grid-connected operation test scenario will introduce the grid-support functions, as shown in Fig. 3-23 and Fig. 3-24.

Fig. 3-23 shows the active power support of inertia emulation. When the grid-frequency deviates down from the rated value 60 Hz. The BESS and CHP generate more power to the system, and PCS will output the additional power to the AC system, emulating the inertial response of the rotational machines. When the grid frequency goes back. The BESS and CHP similarly generate less power.

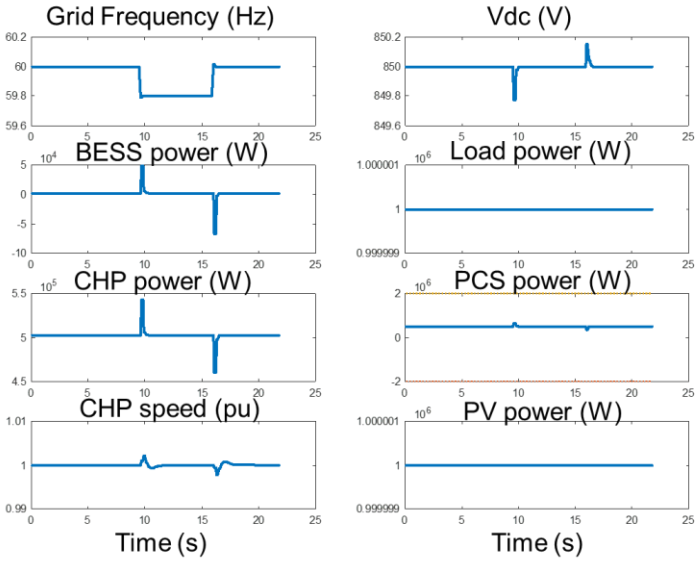


Fig. 3-23. Grid-connected test of frequency support

For voltage support, Fig. 3-24 shows different control modes from the PCS. In the first 15s, no reactive power support is demonstrated. When the PCS output active power changes, the reactive power is kept at 0. In the following 10s, constant power factor control is enabled. In this case, when the active power changes, the reactive power also changes. After that, Q-V droop control is enabled. The output reactive power from PCS actively reacts to system voltage change according to the preset droop curve.

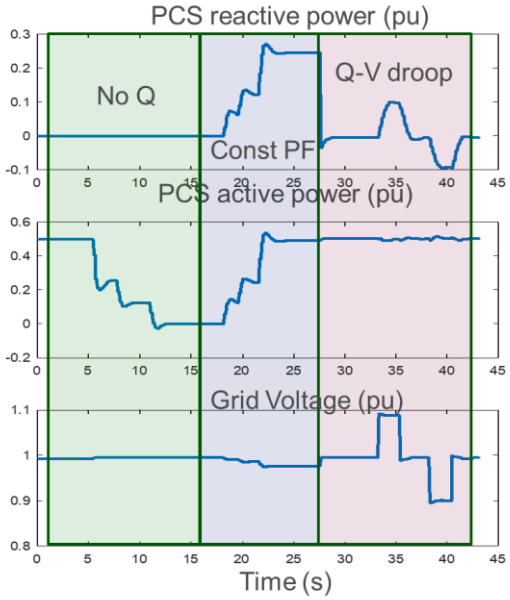


Fig. 3-24. Grid-connected test of voltage support

Fig. 3.2 shows the power outputs of the sources in the F-CHP system during the long-term grid-connected test. The data were obtained through the data logging function in the F-CHP central controller. The PV output followed a pre-programmed PV profile, and the CHP and BESS's outputs are dispatched by the energy management system. The combined output of the F-CHP system will minimize the peak load in the F-CHP system and minimize the total cost, including the demand charge.

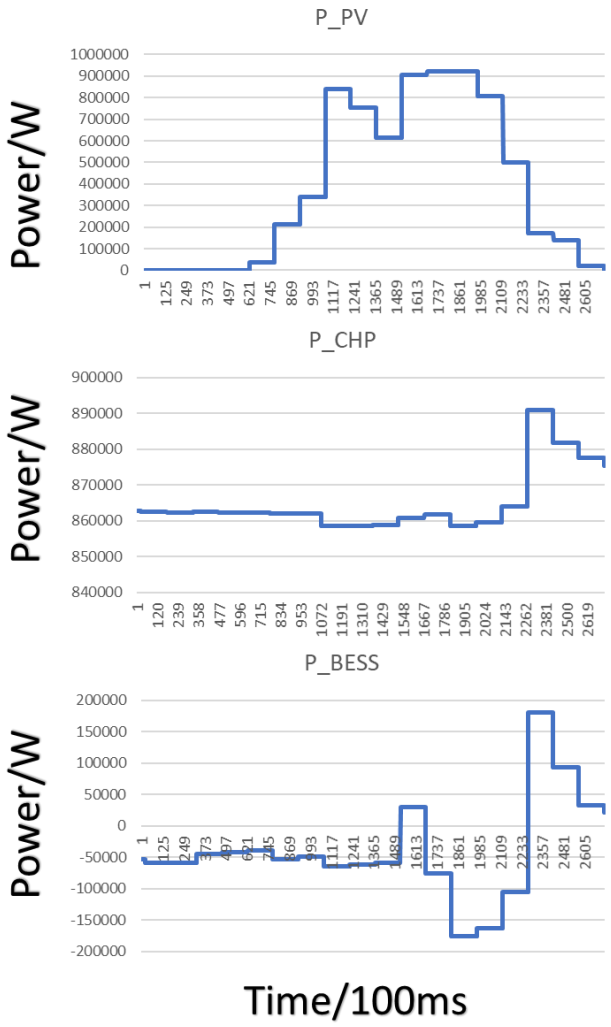


Fig. 3-25. Long term grid-connected test with energy management

3.4.1.3 Islanded operation

In the islanded operation test scenario, disturbances like load changes and source power changes are applied to check system performances, as shown in Fig. 3-26. The system starts with only CHP to provide a 250 kW non-critical load.

- At event 1, the 500-kW critical load is enabled. Since CHP is the only source in the system, it ramps up power to regulate DC link. Since the power is directly drawn from the source, the CHP speed drops to react to the disturbance.
- At event 2, the 500 kW critical load is disabled, creating a similar transient to the system.

- At event 3, BESS starts and takes over the DC link voltage regulation. From now on, CHP only helps with the DC-link regulation, and will not have large transients on its rotational speed.
- At event 4 and event 5, the 500 kW critical load and another 250 kW non-critical load are enabled. BESS provides the initial power needed, and CHP ramps up following that.
- At event 6, PV starts
- At event 7, PV power increases
- At event 8, PCS starts to serve AC loads
- At event 9, PV trips and PCS also trips by F-CHP controller to keep maintaining the system power balance.

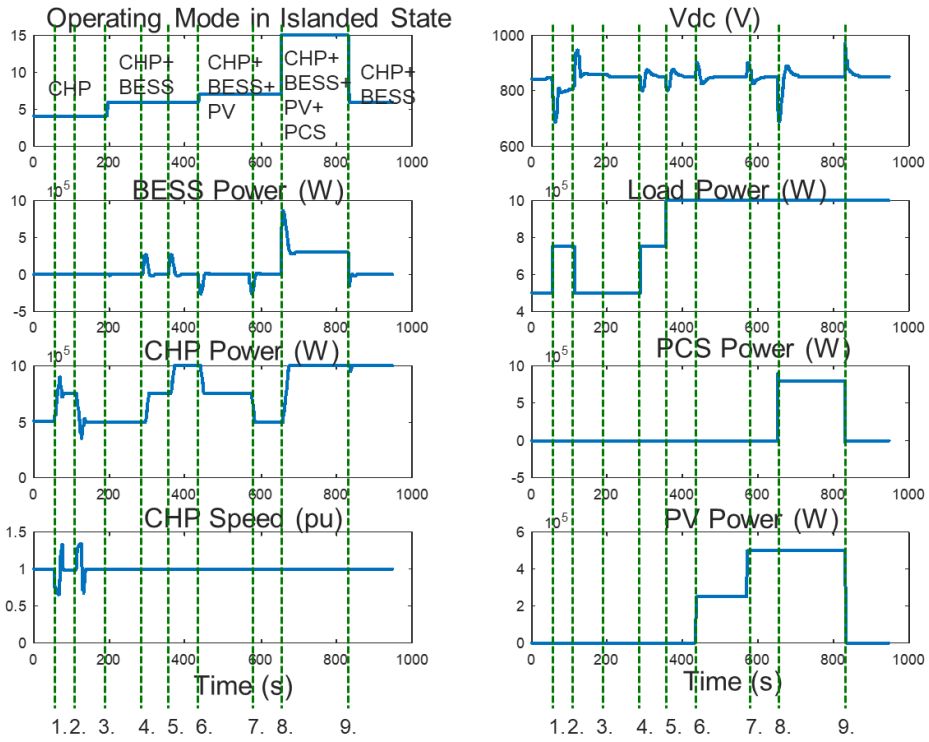


Fig. 3-26. Islanded test with system disturbances

Fig. 3-27 shows the output of the sources in the F-CHP system. The PV and CHP are the generating sources supporting the loads, and the BESS serves as emergency backup power and is standing by during the islanded operation.

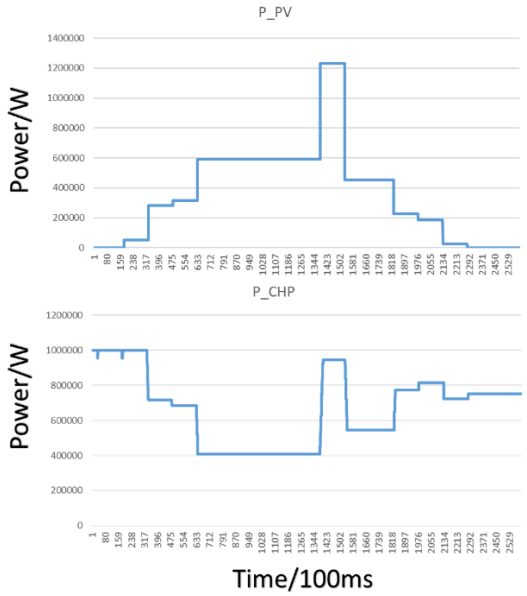


Fig. 3-27. Long term islanded mode test with energy management

Fig. 3-28 shows the voltage and frequency waveforms during the long-term islanded operation test. It is observed that the voltage stayed within its operational boundaries (0.95 p.u. to 1.05 p.u.), and the frequency also stayed within its operational boundaries (59.5 Hz to 60.5 Hz).

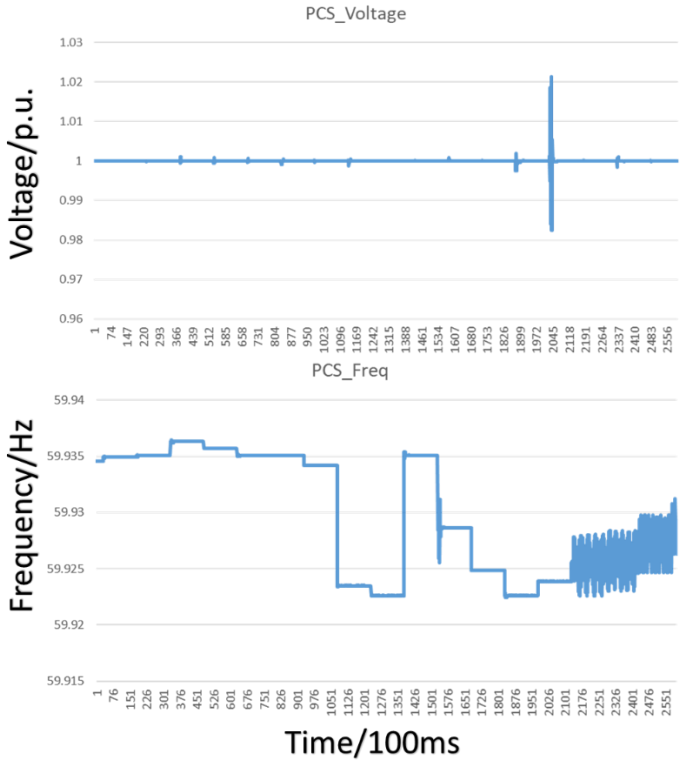


Fig. 3-28. Voltage and frequency during long term grid-connected test

3.4.1.4 Reconnection

The reconnection test scenario is to test the system transition from islanded operation to grid-connected operation. As shown in Fig. 3-29, once the grid becomes available, the central controller will issue commands to the PCS and let it to actively change its output voltage to match the grid voltage. Once the angle difference between the POI switch is small enough, it can be closed. The PCS transitions to grid-connected operation, and ramps down to carry out the system dispatch, to have 0 power exchange. This test is 100% completed.

Since the PCS model in the HIL test platform is highly reduced. More details on the system transition will be tested in the HTB test.

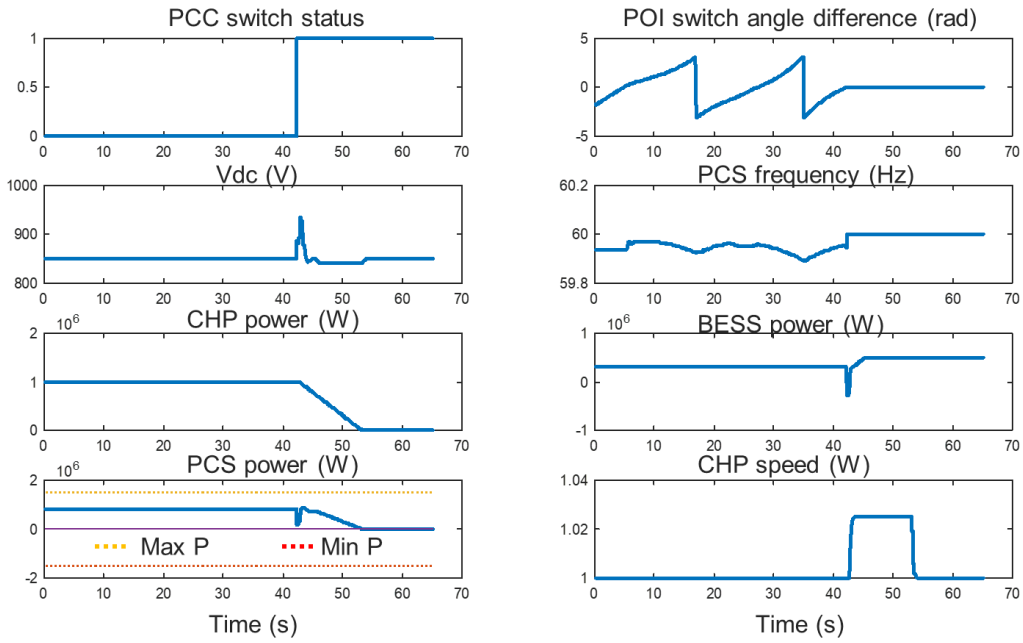


Fig. 3-29. Reconnection test

3.4.1.5 Grid fault and islanding

In grid fault and islanding test scenarios, grid short circuit faults are applied in both grid-connected operations and islanded operations. The results are shown in Fig. 3-30 to Fig. 3-32.

In Fig. 3-30, 2 grid faults are applied. In the first instance, the fault is cleared by itself in 100 ms, The PCS ride through the fault, and F-CHP system does not have large transients with the fault. In the second instance, the fault is persistent, and the relay opens the POI switch and triggers unplanned islanding. Since the system power is available, PCS continues to provide voltage to the AC system and serves neighboring AC loads.

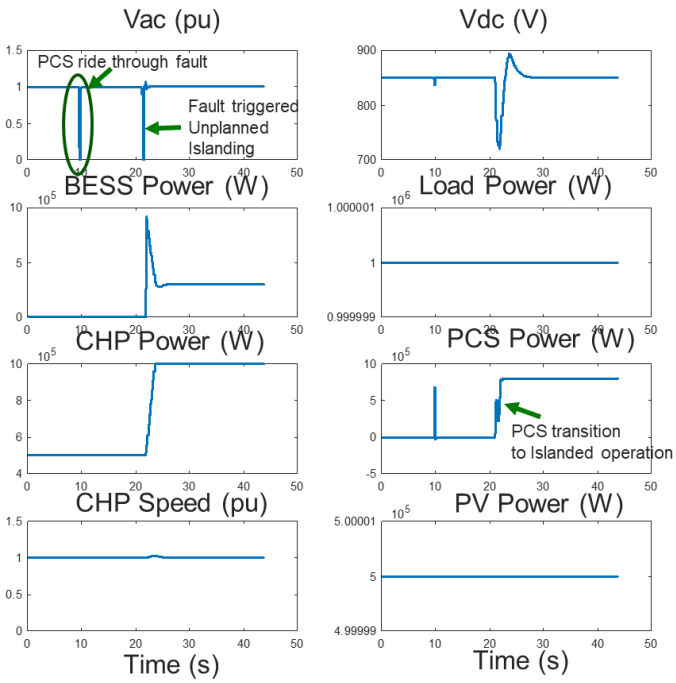


Fig. 3-30. Grid fault in grid-connected condition to trigger LVRT and unplanned islanding

In Fig. 3-31, another grid fault is applied. In this case, no power is available from BESS and PV. So, the PCS trips. Also, one 250kW non-critical load is also turned off by the F-CHP controllers to maintain the power balance.

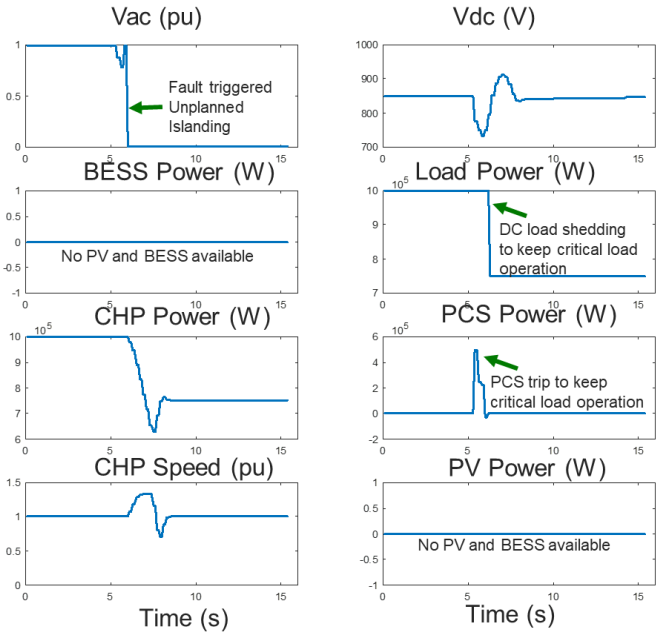


Fig. 3-31. Grid fault in grid-connected condition to trigger unplanned islanding and PCS trip

Fig. 3-32 shows the grid fault response in islanded operation. Similar to the case in Fig. 3-29, a first self-clearing fault happens but does not trigger relay action. The PCS ride through the fault.

The second permanent fault triggers the relay action to protect AC loads. The PCS power reduced. CHP and BESS ramp power down to maintain the power balance.

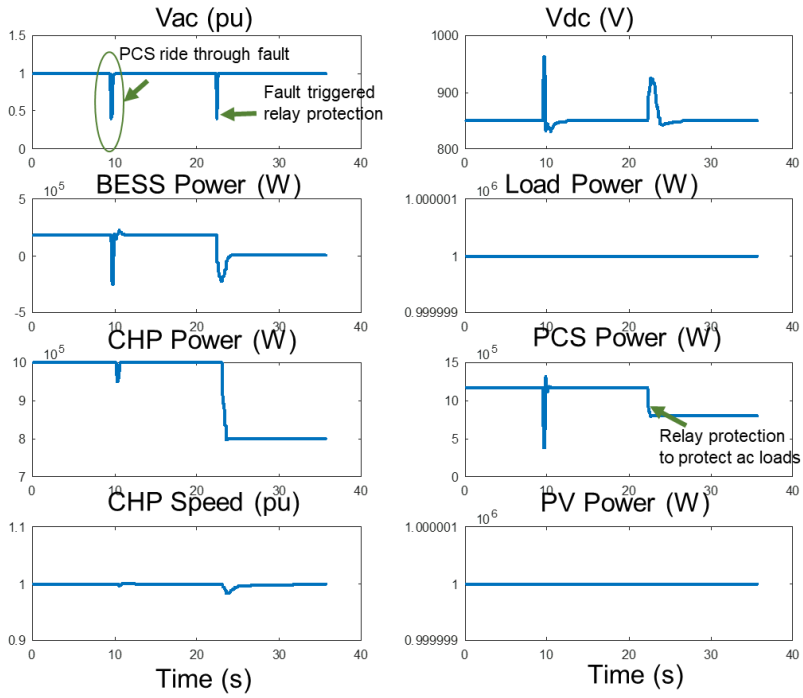


Fig. 3-32. Grid fault in islanded condition to trigger LVRT and load shedding

In all cases, LVDC voltage is maintained above the predefined metric 700V.

3.4.1.6 Internal Component Fault Handling

The internal component fault handling test scenario tests system response after the internal source failure specifically loads shedding performances to maintain the DC link voltage.

Fig. 3-33 shows the system response in grid-connected operation. When PV trips at around 4s, the system available power calculated by Active Power Coordination function is reduced. As it is still above the system dispatch, BESS and CHP can still ramp up to fulfill the command. After BESS trips at around 11s. The available power drops even more, and the F-CHP system outputs its maximum available power to the grid.

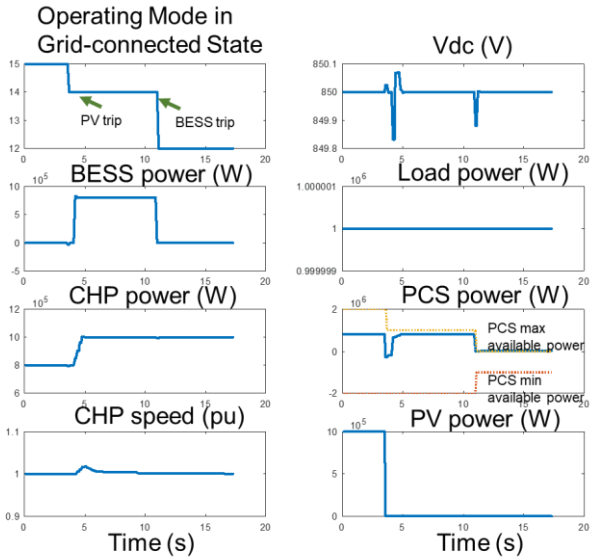


Fig. 3-33. Internal faults in grid-connected condition

Fig. 3-34 shows the internal fault response in islanded operation. When PV trips at around 5s, BESS ramps up to keep power balance. AC and DC loads are still served by the F-CHP system. When BESS trips at around 16s, the power from the only source CHP is not enough, PCS is turned off, and non-critical loads are shed by the F-CHP controller to help maintain the power balance.

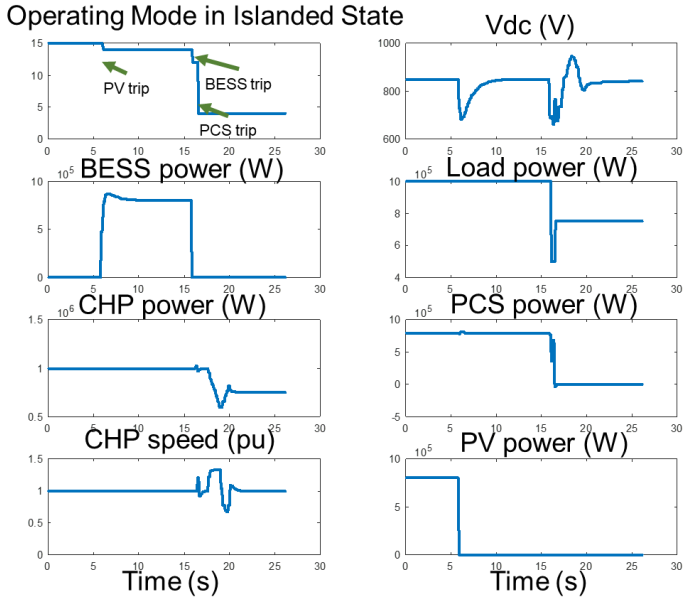


Fig. 3-34. Internal faults in islanded condition

In all cases, the DC link voltage is maintained. The F-CHP system tries to serve the loads and carry out the system command as much as possible.

3.4.2 HTB tests [3]

The HTB test setup configuration diagram is shown in Fig. 3-35. The setup is designed to test the F-CHP controller with circulating power. In the grid-connected mode, the grid emulator provides the three-phase four-wire grid, and the small-scale PCS converter works under grid-

connected mode. In the islanded mode, the grid emulator works as a load to imitate a three-phase balanced/unbalanced load. The DC emulator integrates modes of CHP sources, battery, PV, and local load. The central controller is implemented in a CompactRIO, and it communicates with converter controllers through a CAN bus.

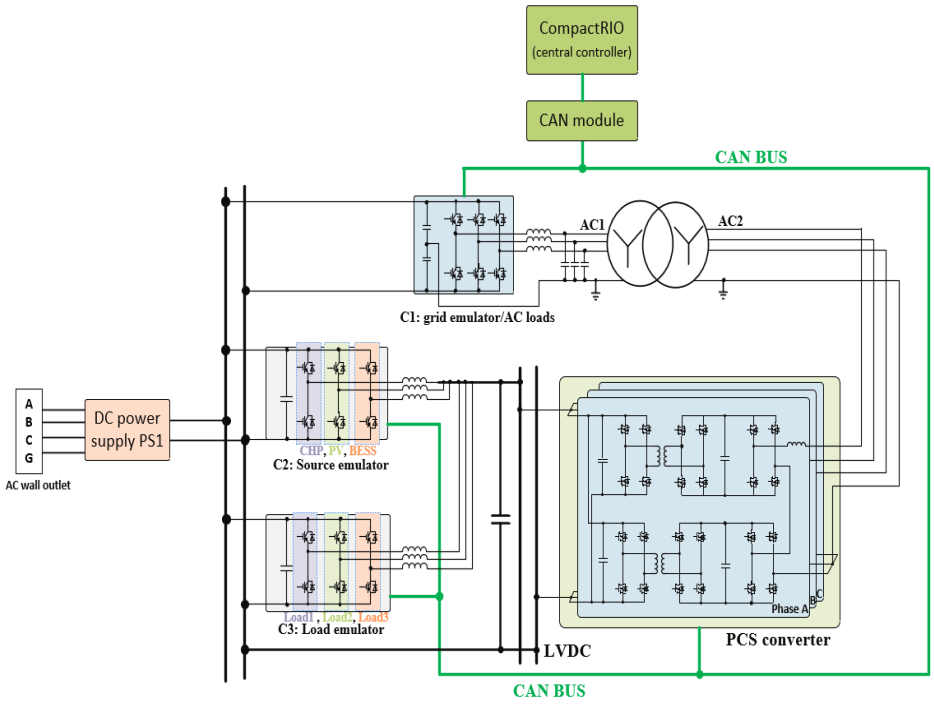


Fig. 3-35. F-CHP controller HTB test configuration

3.4.2.1 Human-machine interface

A human-machine interface (HMI) was developed for the F-CHP central controller test on the HTB platform. As shown in Fig. 3-36, the grid emulator, SCADA emulator, the F-CHP central controller command, and F-CHP system status and variables are shown on the HMI.

The grid emulator controls gird availability, voltage, frequency, as well as transient emulation command, such as faults. The SCADA emulator emulates the command from SCADA, including the power exchange command, external AC load support command, as well as PCS converter operation modes.

The F-CHP central controller command panel is used to send the command to initiate, start, or stop the F-CHP system, and display the system operation modes. The executed functions of the F-CHP central controller are indicated through a series of LED indicators. The F-CHP system configuration is shown at the bottom side of the HMI, and the status of each piece of equipment, including fault, stand by, or running, is indicated by two LEDs. Three scopes are located on the right side, and they are used to display the status and output power of each equipment.

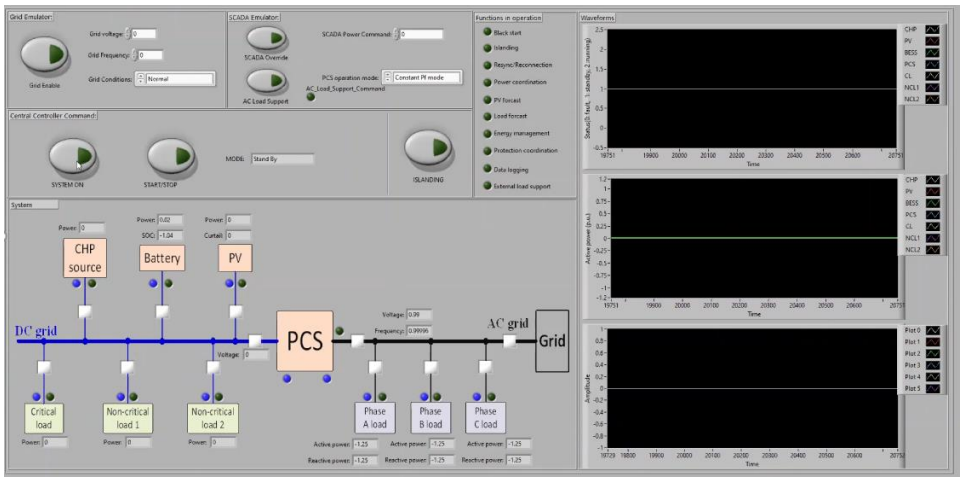


Fig. 3-36. Updated F-CHP central controller HTB test configuration

3.4.2.2 Grid-connected mode operation

The grid-connected operation was first conducted. The grid emulator was enabled to provide the AC grid, and the PCS converter was connected to the AC grid, exchanging power with the AC grid to stabilize the LV DC bus. The energy management, PV forecast, and load forecast functions were disabled, because these functions are long-term functions, and have also been tested in the HIL test.

The voltage and current waveforms of the HTB setup were measured. Fig. 3-37 shows the startup and steady-state operation waveforms in the grid-connected mode. In the beginning, the PCS converter starts first to establish the LV DC bus voltage. Then, the battery, PV, CHP source was started, followed by the local loads. In the grid-connected mode, the battery maintains its state of charge (SOC). PV outputs its power based on its PV profile. CHP outputs the remaining power for the local loads, and PCS provides the transient power demand.

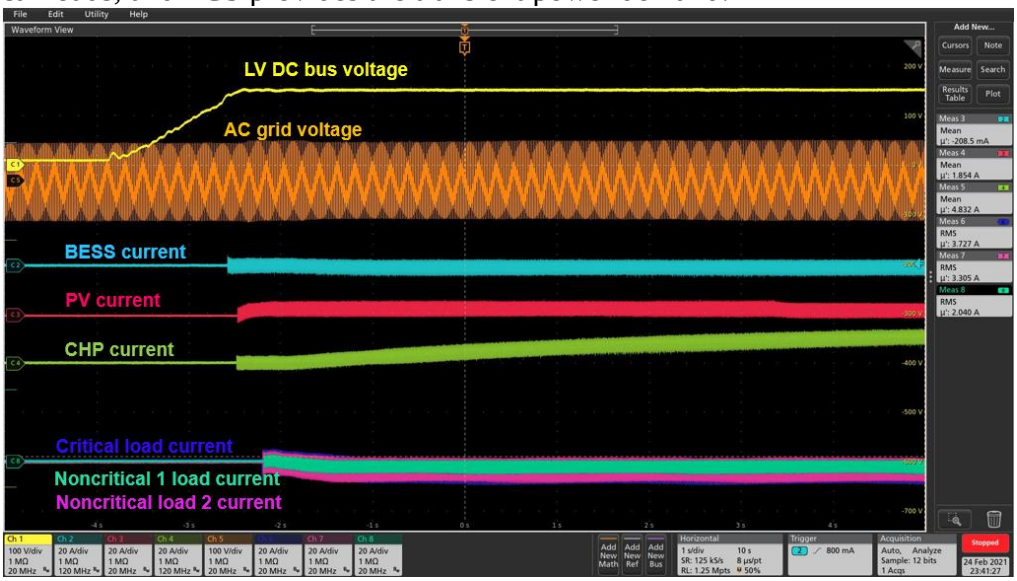


Fig. 3-37. Waveforms from the test setup in grid-connected mode operation

3.4.2.3 Islanded mode operation

Then, the islanded mode was tested. The F-CHP system detected the availability of the AC grid and was started to the islanded mode. Based on the SCADA command, the PCS converter was enabled to control the AC voltage and frequency, supporting the external AC loads.

The waveforms of voltage and current in islanded mode operation are shown in Fig. 3-38. The LV DC bus was controlled by the battery, and the PV output power based on its profile, and the loads consume power based on their load profile. When the balancing between the source and the loads was broken, the battery will provide transient power, and the CHP will regulate its power output to recover the power balancing between source and loads.

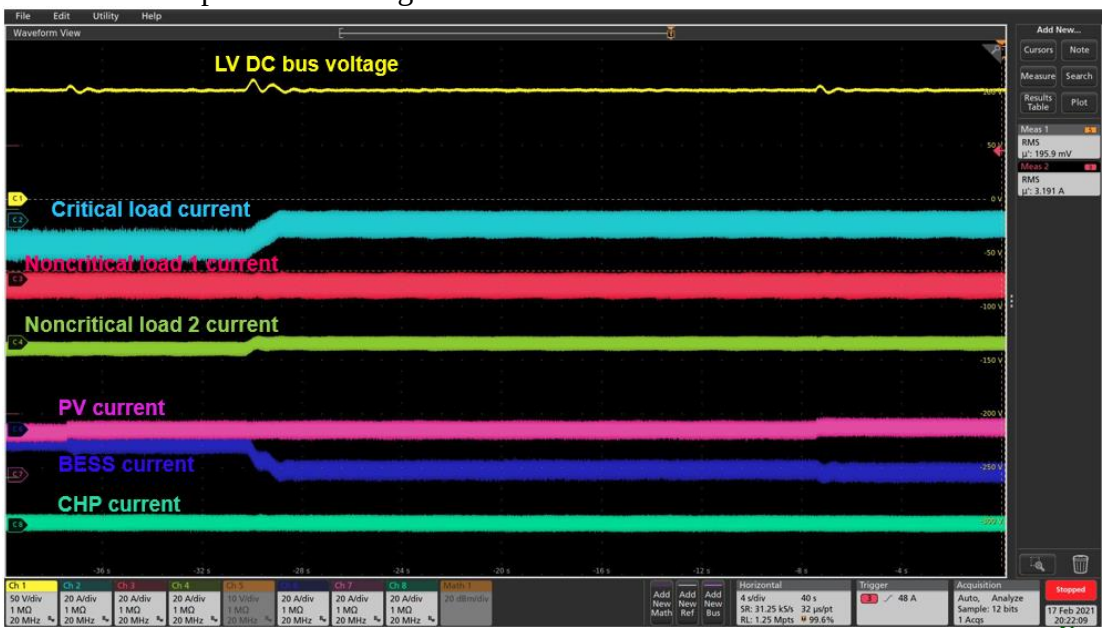


Fig. 3-38. Waveforms from the test setup in islanded mode operation

3.4.2.4 Mode transition (planned islanding, unplanned islanding, reconnection)

The F-CHP system operation mode transitions, including the planned islanding, unplanned islanding, as well as reconnection from the islanded mode back to the grid-connected mode were tested. Fig. 3-39 shows the waveforms of the voltages and currents during the transition tests. In the beginning, the AC grid did not exist, and the F-CHP system operated in the islanded mode. When the AC grid recovered, reconnection was conducted to connect the F-CHP system to the grid. The planned islanding was conducted by pushing the islanding button on the HMI. Even though the grid was available, the F-CHP system converted from grid-connected mode to the islanded mode after receiving the islanding command. After the islanding command was cleared, since the grid was still available, the system went back to the grid-connected mode. To emulate the unplanned transition, the grid emulator was suddenly disabled, and the grid lost. The F-CHP system converted from the grid-connected mode to the islanded mode when the grid was lost, and after the grid came back, the system reconnected itself to the grid. During the transition, the LVDC bus voltage had a short variation, but it was within the acceptable range.

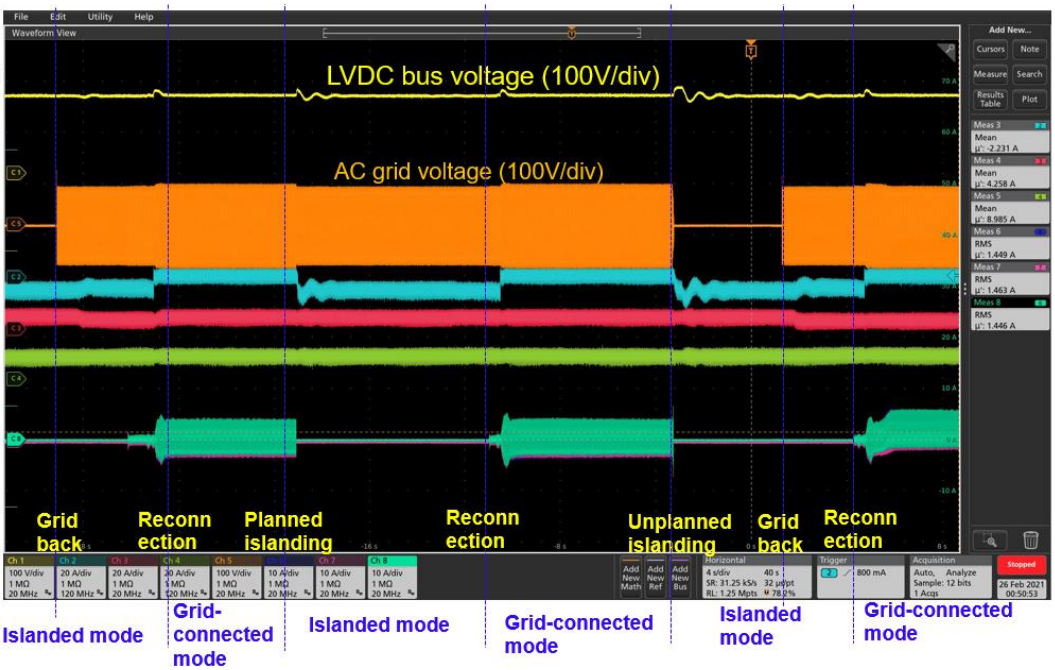


Fig. 3-39. Waveforms during mode transition

3.4.2.5 Grid transients

A single-phase-to-ground fault was conducted to test the response of the F-CHP system. As shown in Fig. 3-40, during the fault period, which is 1s in this test, one phase voltage was low, and one healthy phase had a small overvoltage. The PCS converter AC side current had a variation, but the LVDC bus voltage was still stabilized, which means the AC grid fault did not impact the F-CHP system.

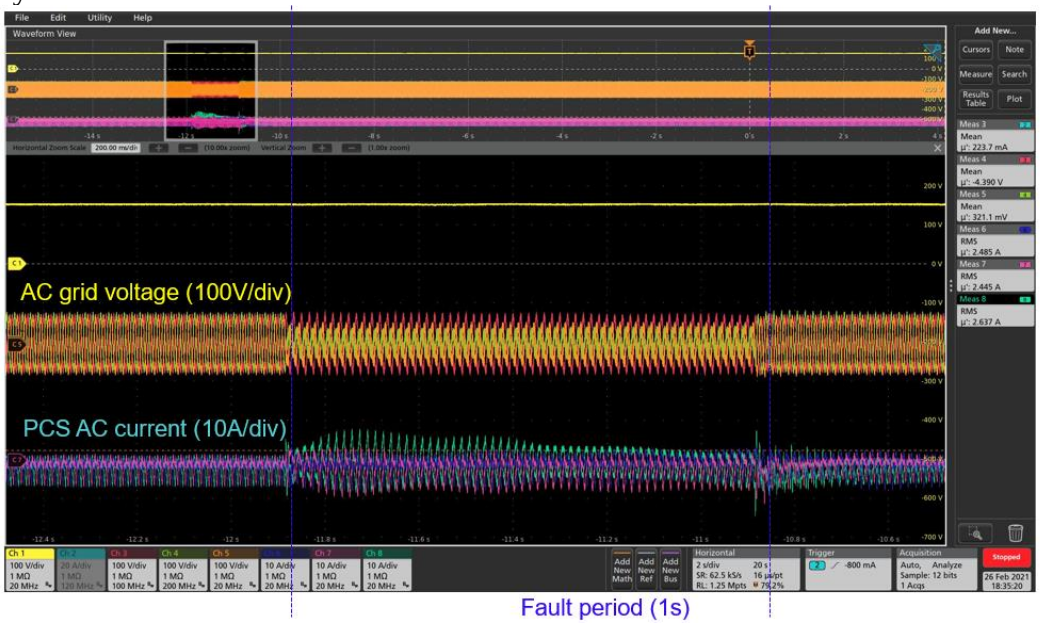


Fig. 3-40. Waveforms during AC grid fault

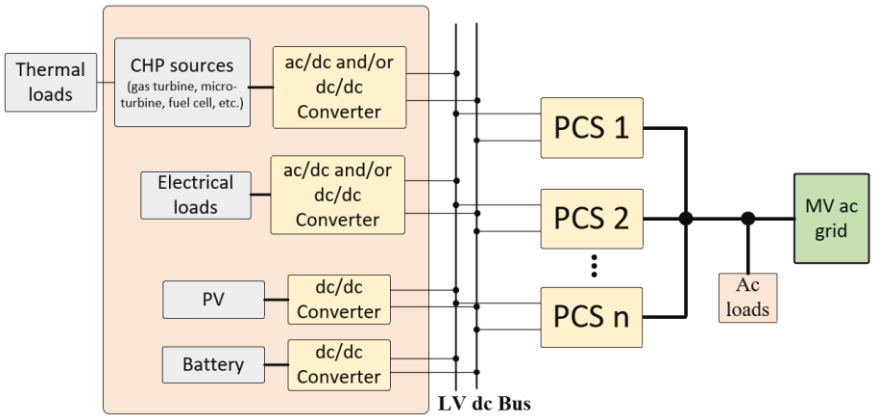
4. SCALABLE PCS DEVELOPMENT

As the single PCS operation and control have been demonstrated, the scalability of the F-CHP PCS is studied to verify that the proposed system can handle higher power for real applications. In this chapter, discussion on paralleling configuration, control, and protection is provided.

4.1 PCS PARALLELING TECHNIQUE

4.1.1 Paralleling scenarios

Three possible paralleling scenarios are shown in Fig. 4-1(a), (b), and (c), respectively. In Fig. 4-1(a), the F-CHP system only has one low voltage (LV) DC bus, and the PCS converters are paralleled at both the DC side and the AC side. In Fig. 4-1(b), the F-CHP system has multiple LV DC buses, and each DC bus has one PCS converter, connecting the DC bus to the same medium voltage (MV) AC grid. In Fig. 4-1(c), the F-CHP system has multiple LV DC buses, and each bus is connected to the MV AC grid by multiple PCS converters. In all three scenarios, the PCS converters are paralleled at the MV AC side, and the main difference is the LV DC side configuration. Fig. 4-1(a) can be easily extended to (b) and (c), and it needs almost all the techniques required for the paralleling control. Therefore Fig. 4-1(a) is selected as the main focus paralleling scenario in BP3.



(a)

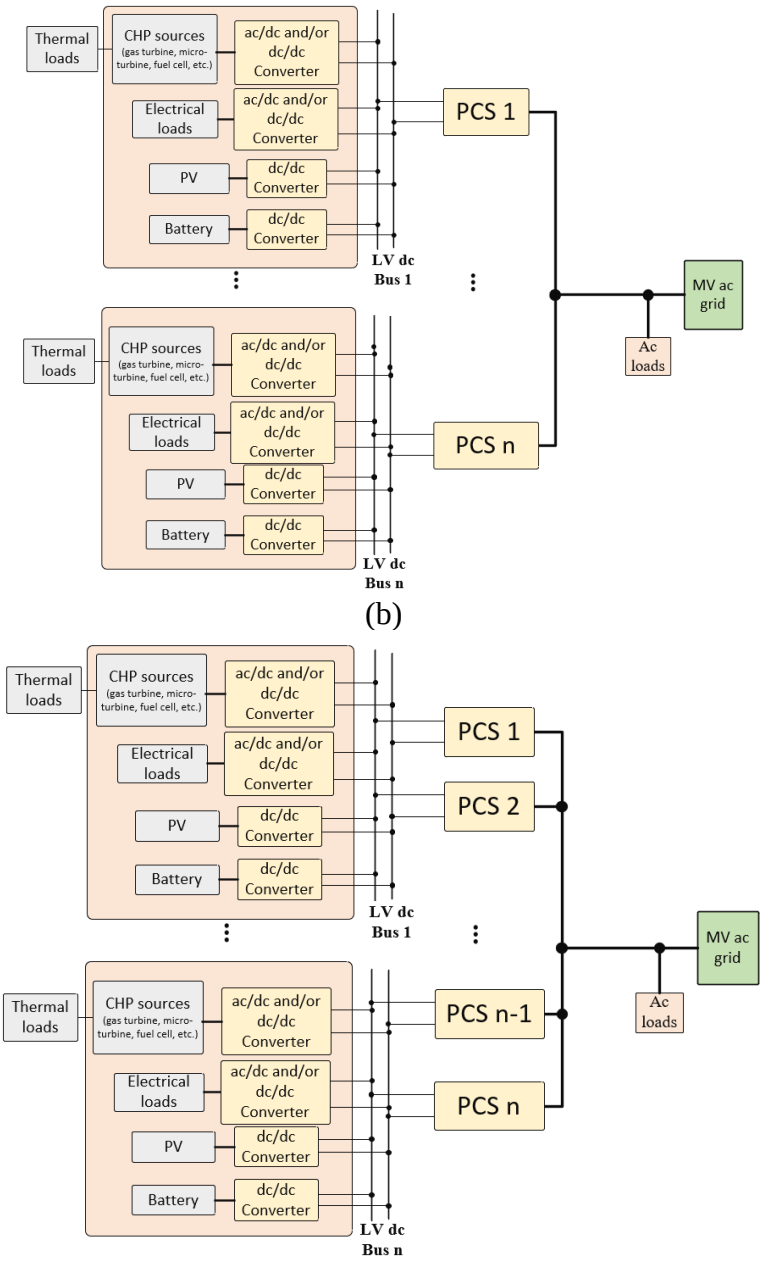


Fig. 4-1. Schematics of PCS converter (a) paralleling at both DC and AC sides, (b) paralleling only at the AC side, and (c) hybrid paralleling

4.1.2 DC/AC stage paralleling technique

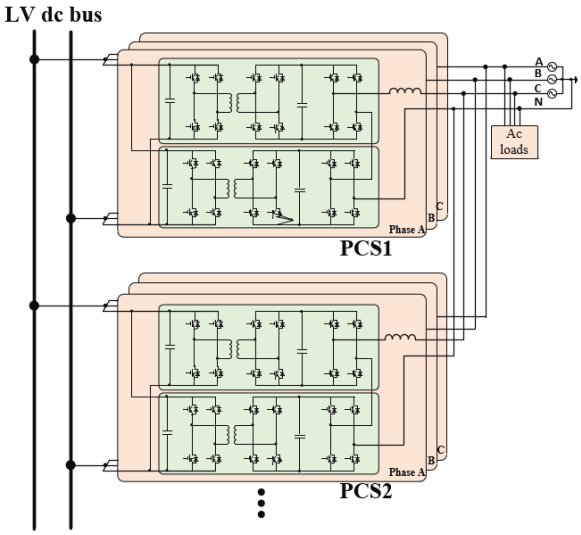
4.1.2.1 Circulating current under switching frequency

A more detailed PCS converter paralleling scheme is shown in Fig. 4-2 (a), and its DC/AC stage single-phase equivalent circuit in the grid-connected mode and the islanded mode are shown in Fig. 4-2(b) and (c), respectively. The two PCS converters output two PWM voltages. In the grid-connected mode, the AC voltage is formed by the grid, if the grid is strong (low impedance), the two PCS converters “see” a constant AC voltage, and they are decoupled from each other,

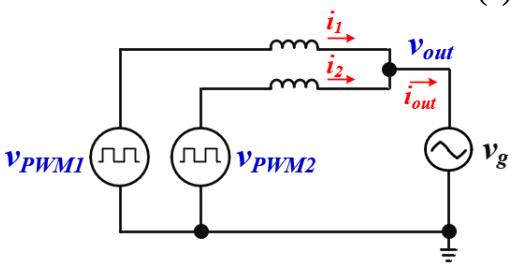
which mean the PWM voltage output from one PCS converter does not impact the current control of other PCS converters. However, if the grid is not strong, the PWM voltage output from one PCS converter changes the AC side voltage and impacts the other PCS converter current control. This is similar to the islanded mode case, which is shown in Fig. 1.2 (c). In the islanded mode, the AC voltage is formed by the PCS converters, supporting the external AC loads. In this case, the AC terminal voltage is determined by all PCS converters, which means the PCS converters are coupled with each other, and circulating current under switching frequency occurs. The worst case is when the load impedance is infinite and the angle difference of the two PWM voltages is 180 °, as shown in Fig. 1.3. In addition, the worst circulating current can be calculated as

$$\Delta i = \frac{V_{dc}}{2L}\Delta T = \frac{6.7\ kV}{2 \times 44mH} \times 12.5\mu s = 0.95A\ (\pm 8\%)$$

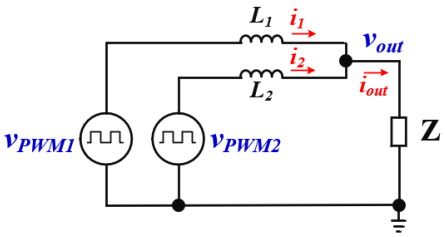
This current ripple is not high, so even if the carrier waveforms, used to generate the PWM pulses, of different PCS converters are not synchronized, the circulating current under switching frequency is acceptable. However, to get a better waveform, it is better to synchronize the carrier waveforms of different PCS converters.



(a)



(b)



(c)

Fig. 4-2. Schematics of (a) the PCS paralleling, (b) the DC/AC stage single-phase equivalent circuit in the grid-connected mode, and (c) the DC/AC stage single-phase equivalent circuit in the islanded mode

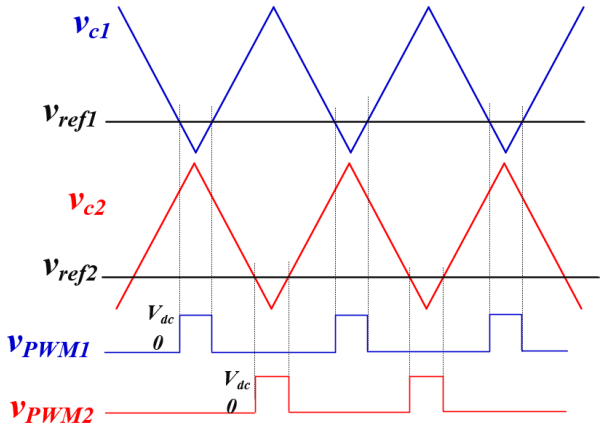


Fig. 4-3. PWM waveforms of different PCS converters

A simulation is conducted to verify the discussion about the islanded-mode operation. Two PCS converters are paralleled at the AC side, and the current waveforms of one PCS converter are shown in Fig. 4-4. The blue curves show the current when the two PCS converters use synchronized carrier waveforms, and the red curves show the current when the two PCS converter carrier waveforms are out of phase to the most (180º). From the waveform comparison under the resistive load, the capacitive load, and the inductive load, it can be found that even though in the worst case the converter current waveform does not show a big difference.

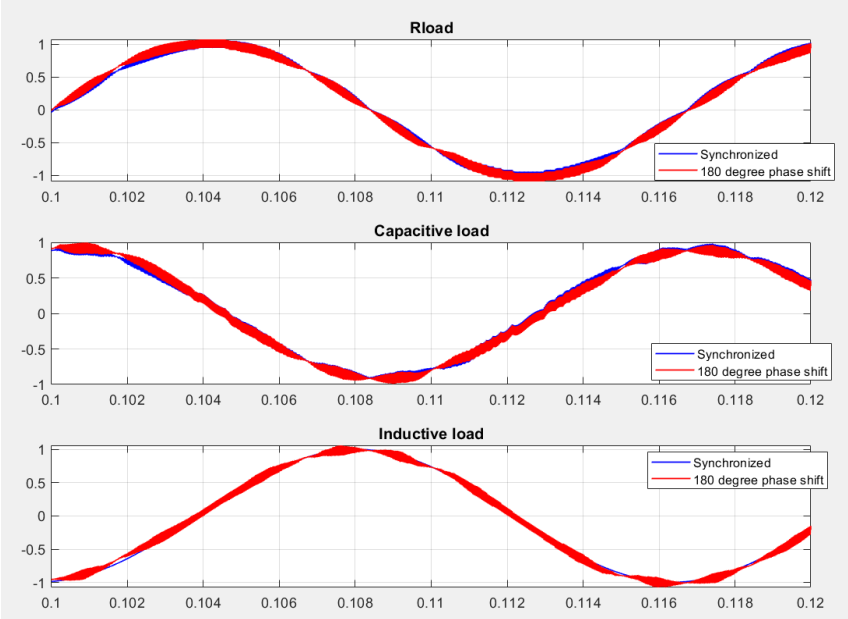


Fig. 4-4. Current waveforms of PCS paralleling under different load types and PWM synchronization conditions

4.1.2.2 Circulating current under fundamental frequency

In the grid-connected mode, all PCS converters will be synchronized with the grid voltage angle through their phase locked loop (PLL), so there should have no circulating current under the fundamental frequency during the steady-state operation. During the transient, due to PLL delay or limited response speed, circulating current under fundamental frequency may occur due to different output voltage phase angles. However, since the period is short in time, as long as the converter controls its current to be within its capability, the circulating current impact is negligible.

In the islanded mode, since the PCS converters form the AC voltage, if the output voltage of two PCS converters has different amplitudes or phase angles, a circulating current under fundamental frequency will be induced. Therefore, it is necessary to synchronize the voltage amplitude and angles of different PCS converters. The master-slave control scheme is adopted for the DC/AC stage to realize synchronization and the power sharing among different PCS converters in the islanded mode operation. As shown in Fig. 4-5, one PCS converter is the master, and it controls the AC terminal voltage and generates the total current commands. It divides the current command by the PCS converter number and then sends the current command for each PCS converter to the other converters. Also, the master PCS converter generates the angle information and sends the angle information to all slave PCS converters to realize angle synchronization. The slave PCS converters work in the current control mode.

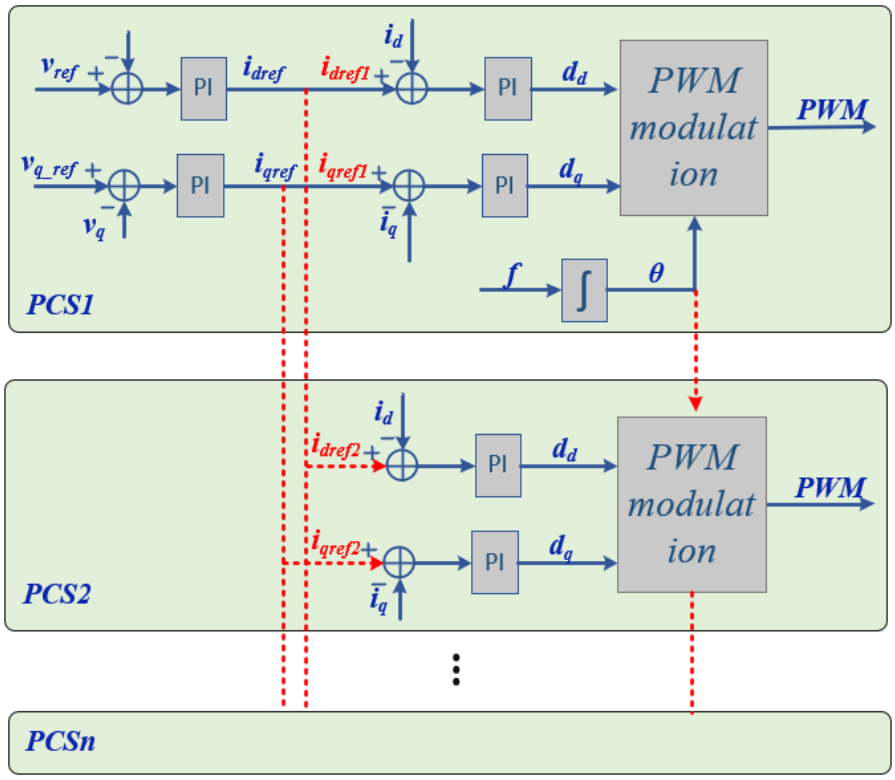
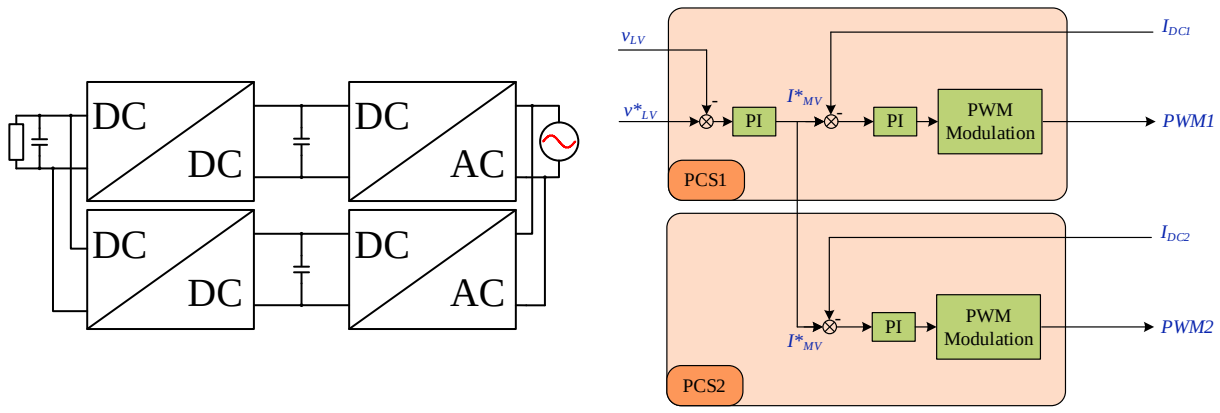


Fig. 4-5. The master-slave control scheme for the DC/AC stage in the islanded mode operation

4.1.2.3 DC/DC stage paralleling technique

Several PCS can also be paralleled at the LV DC link, which can be illustrated in Fig. 1.6(a). As the DC/DC converter may control the LV DC voltage, DC/DC converter controllers in different PCS converters should be coordinated to avoid control conflicts. Therefore, as shown in Fig. 1.6(b), a master-slave control is adopted for DC/DC converters in different PCS converters. The master converter (PCS1) controls the DC link voltage and sends the current reference to other slave converters, and the slave converters (PCS2, …) control their current. Therefore, the current can be evenly shared among the paralleled PCS converters.



(a) (b)

Fig. 4-6. Schematics of (a) PCS paralleled at DC side, (b) DC/DC paralleling control strategy

The paralleling strategy is verified in MATLAB/Simulink, and the simulation waveforms are shown in Fig. 4-7. Load steps are imposed on the LV DC side, and as the voltage drops by 20 V (2%), the DC/DC converters respond to the voltage change, and they realize the voltage and current balance within 0.5 millisecond. From the zoomed-in curve, it can be found that the slave converter has at most one cycle delay to the master converter, which is acceptable for the PCS operation and power balancing. Hence, the PCS can be paralleled on the DC side with the master-slave control strategy.

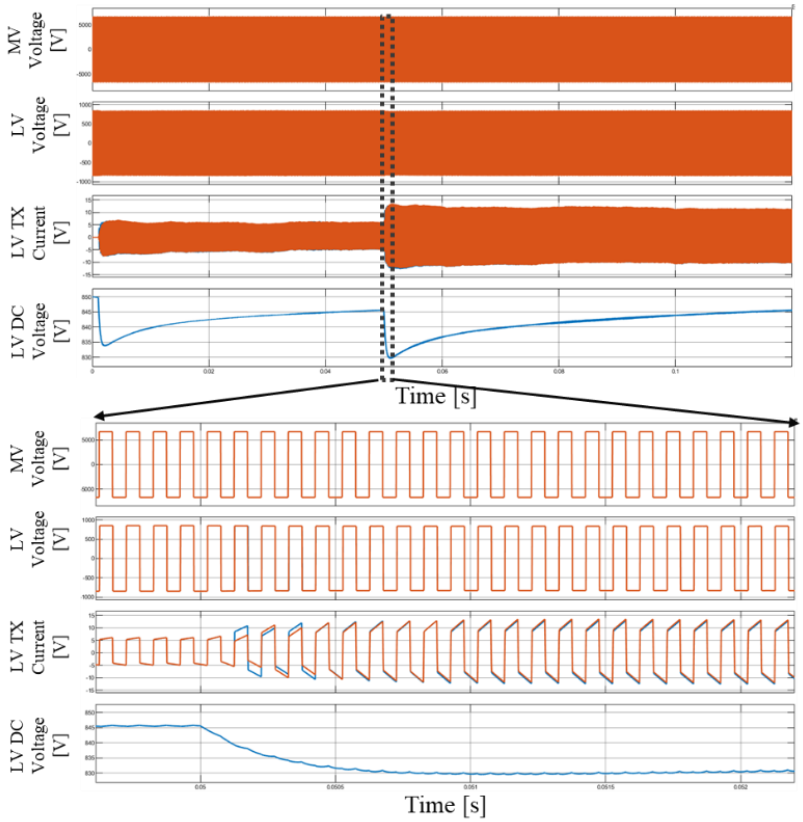
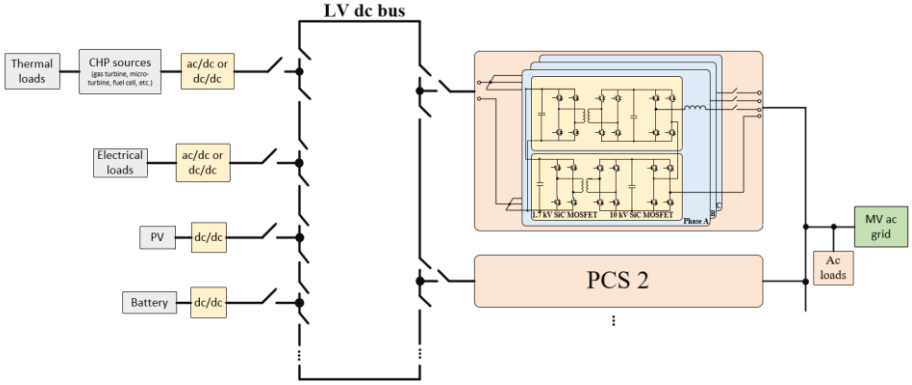


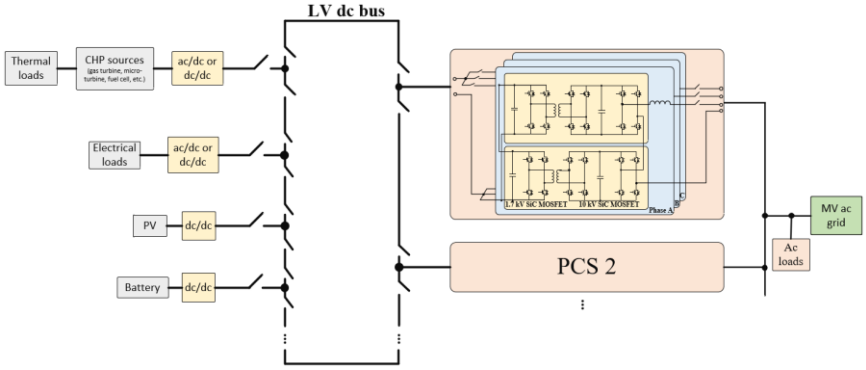
Fig. 4-7. Simulation waveform of PCS paralleling at DC side

4.1.2.4 Protection considerations

To increase the system resilience to LV DC bus faults, the ring bus configuration can be adopted. Each equipment connection point has three switches, and any single fault on the LV DC bus can be isolated by the adjacent two switches. For the PCS converter, it can use one switch for the whole converter, as shown in Fig. 4-8 (a), or use one switch for each phase, as shown in Fig. 4-8(b). For the latter configuration, the advantage is that when one phase is faulted, the other two phases can keep operating.



(a)



(b)

Fig. 4-8. System protection configuration: (a) protection on the whole PCS converter; (b) protection on each phase

4.2 HTB TEST

To validate the scalability of the PCS converter in the F-CHP system, two small-scale PCS converters are parallel connected between the DC bus of the F-CHP system and the AC grid. The central controller and the PCS local controller are updated to accommodate the operation of two PCS converters.

The HTB test platform is modified based on the test platform used in BP2. The previously developed five-level small-scale PCS converter is divided into two three-level PCS converters, and the two converters are parallel connected at both the DC and AC sides. As shown in Fig. 4-9, a similar setup to that in BP2 is used. A three-phase two-level converter is used as the grid emulator, generating the grid voltage, in the grid-connected mode test, and it is used as a load emulator, emulating the three-phase balanced/unbalanced loads, in the islanded mode test. Two three-phase two-level converters are used as the source and load emulator, respectively. The source emulator emulates the CHP source, PV, and battery, with each component emulated by one phase. Similarly, the load emulator emulates one critical load and two non-critical loads. The central controller is

implemented in a CompactRIO, and all equipment is integrated by a CAN bus to realize the communication between the central controller and the local controller.

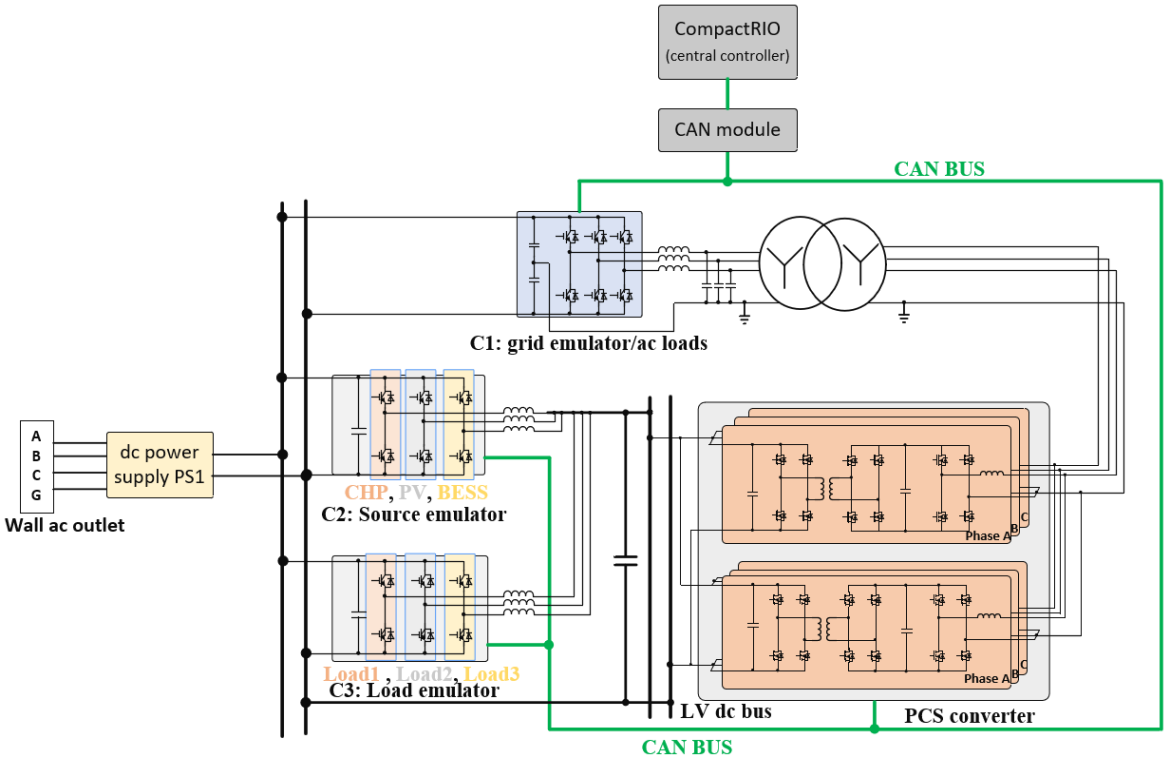


Fig. 4-9. The configuration of the HTB test platform

The islanded mode test is first completed. Without enabling the grid, the F-CHP system starts to the islanded mode operation. The start-up and steady-state waveforms are shown in Fig. 4-10. In the islanded mode the battery supports the DC bus voltage, so when the system is started, the battery starts first to establish the DC bus voltage. Then, the PV and CHP are started, followed by the local loads. The F-CHP system can also support the external AC loads when the grid is not available. The PCS converters will be started to provide the AC voltage and frequency, supporting the AC balanced/unbalanced loads.

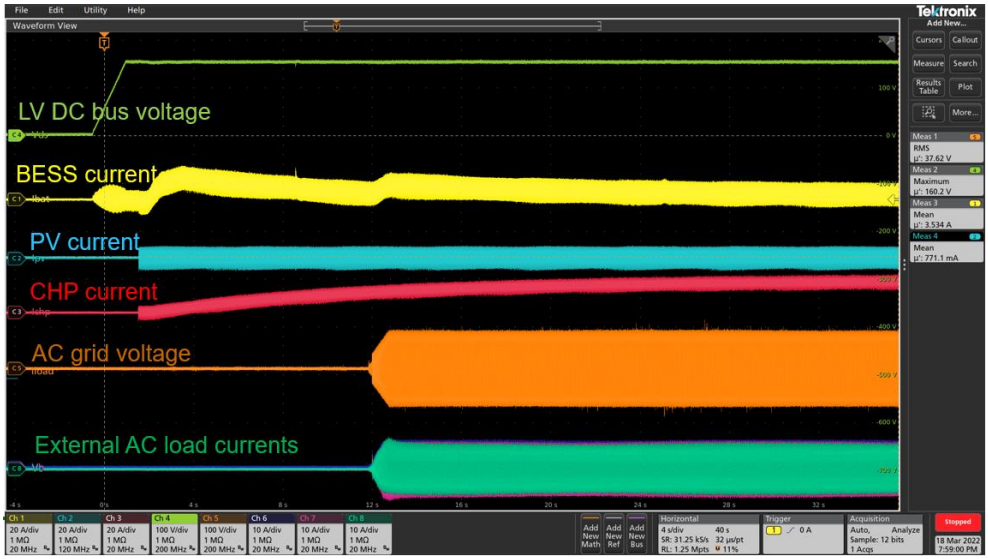


Fig. 4-10. The start-up and steady-state operation waveforms of the islanded-mode operation

Then, the grid-connected mode operation is tested. The grid is provided by the grid emulator, and the F-CHP system is started to the grid-connected mode since the grid is available. In the grid-connected mode, the DC bus voltage is supported by PCS converters. The screenshot of the HMI in the grid-connected mode is shown in Fig. 4-11. At this moment, each PCS converter delivers 0.22 p.u. power to the AC grid. The DC voltage waveform is shown in the right-middle oscilloscope, and it can be found that the voltage is quickly established by the PCS converters during the start-up process.

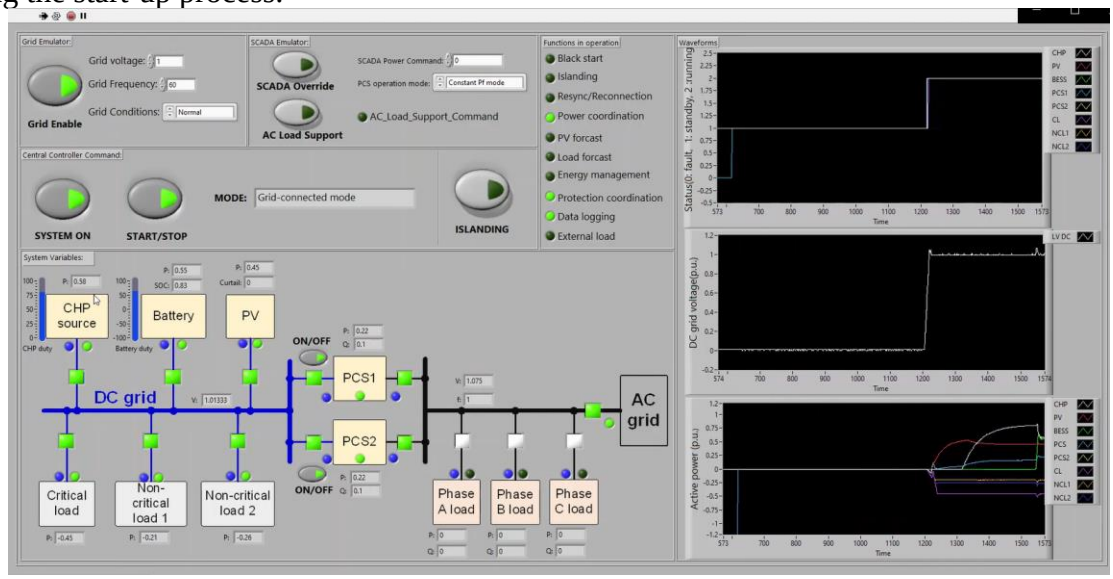


Fig. 4-11. The screenshot of the HMI in the grid-connected mode.

The waveforms of LV DC bus voltage, AC side grid voltage, battery current, PV current, CHP current, as well as the critical and non-critical load current in the mode transition tests are shown in Fig. 4-12. At the beginning, the grid is available, and the system operates in the grid-connected mode. At time t_1, although the grid is still available, the F-CHP system transferred from the grid-connected mode to the islanded mode because of the planned islanding command from the central controller. In the islanded mode, the battery controls the DC bus voltage, balancing the power between the generation and loads. The energy management function regulates the power generation from the CHP source and the PV curtail to achieve the best economic operation. At time t_2, the F-CHP system is converted back to the grid-connected mode by the central controller. At time t_3, the grid is suddenly lost, which corresponds to an unplanned islanding event, and the F-CHP system automatically converted to the islanded mode. At time t_4, the F-CHP system is requested to support the external AC loads by the SCADA, and the PCS converters start to operate, controlling the grid-side voltage and frequency to support the external AC loads. At time t_5, the AC loads support is stopped. At time t_6, the grid comes back, and at time t_7 the F-CHP system converted back to the grid-connected mode.

During all these mode transition tests, the LV DC bus voltage is regulated well, and the system does not show large disturbances, which verifies the design and control of the F-CHP system.

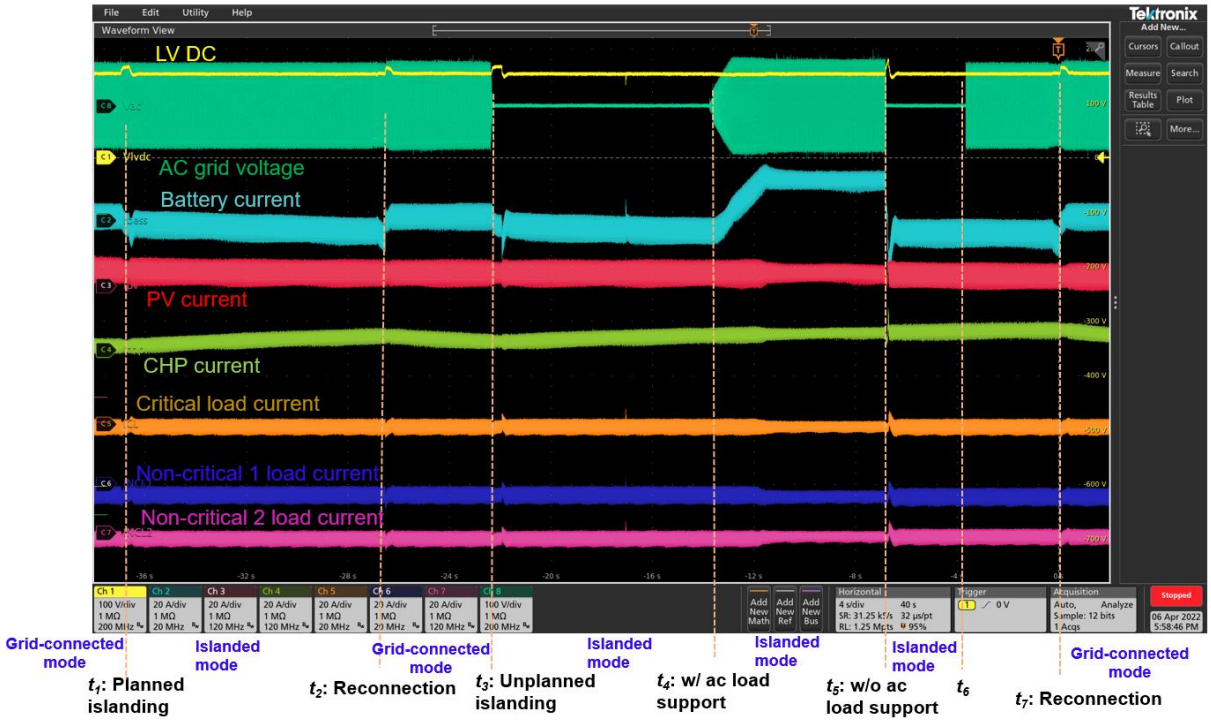


Fig. 4-12. Waveforms in mode transition Tests.

The circulating currents in both grid-connected mode and islanded mode are tested, and the current waveforms are shown in Fig. 4-13 and Fig. 4-14, respectively. In both operation modes, the PCS1 current and the PCS2 current align with each other quite well. The circulating current, which equals the current subtracting of PCS1 and PCS2, is quite small, compared to the fundamental current. Therefore, the circulating current is well controlled in the PCS converter.

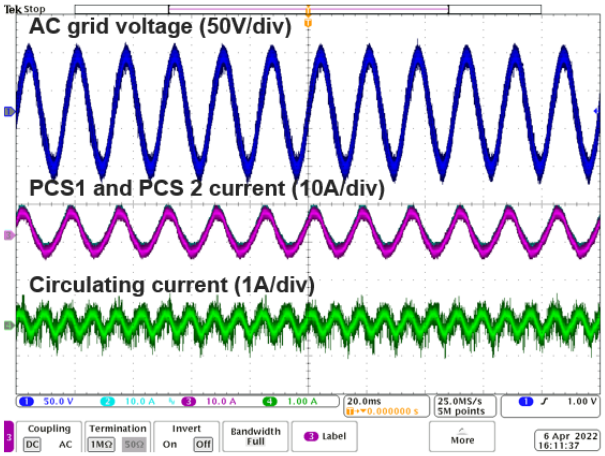


Fig. 4-13. Circulating current waveforms in the PCS converters in the grid-connected mode

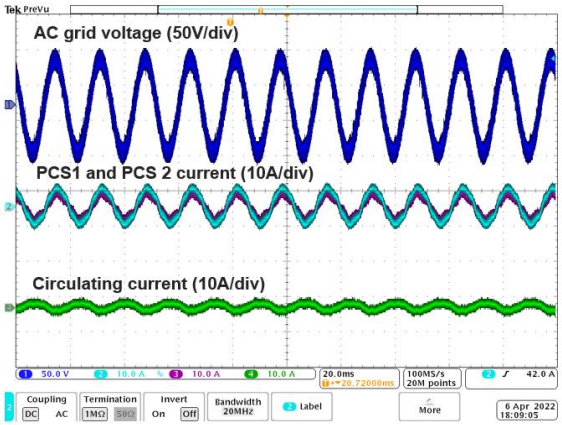


Fig. 4-14. Circulating current in the PCS converters in the islanded mode

4.3 MV PCS PARALLELING TEST

With Gen. I and II three-phase converters tested, the Gen. II (BP3) converter is paralleled with the Gen. I (BP2) converter for the converter scalability test. The hardware photo of the two PCS converters is shown in Fig. 4-15. Compared to Gen. I (BP2) converter, the Gen. II (BP3) converter achieves a size reduction of 49% and an efficiency improvement of 2.0 percentage points.

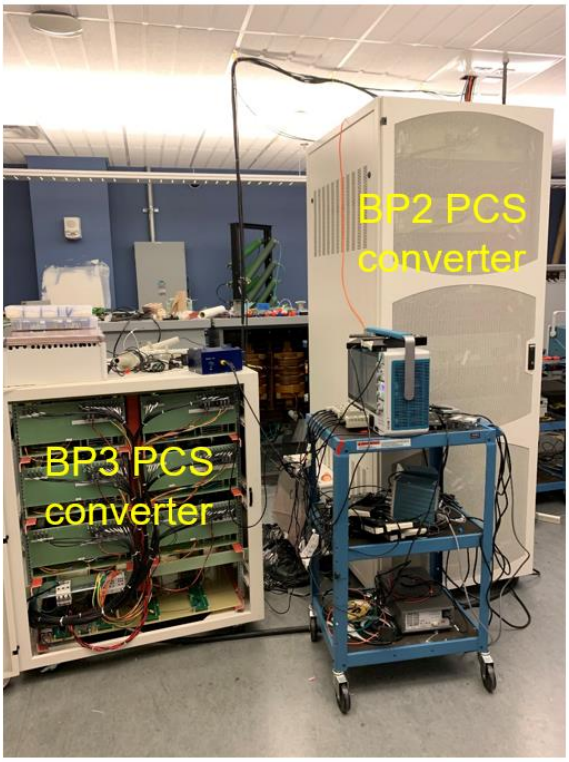


Fig. 4-15. Picture of the PCS paralleling test

Two different paralleling setups are used to test the paralleling operation and scalability in the islanded mode operation and grid-connected operation, respectively. The setup scheme for islanded mode operation is shown in Fig. 4-16. The two PCS converters are parallel connected at both the LV DC side and the MV AC side. The LV DC is supplied by a LV DC power supply, and the PCS converters control the MV AC voltage and frequency, supporting external AC loads. As discussed in section 4.1.2.2, one PCS converter operates as the master and the other converter as

the slave. The master converter regulates the AC voltage and frequency. It has an outer voltage loop, which generates the current reference. Also, the master converter generates the voltage angle. The slave converter only regulates the current, based on the current reference and angle command sent from the master converter. Moreover, the two converters share their operation status so that they can start and stop accordingly.

The MV AC side voltage and current waveforms at rated voltage (13.8 kV line-to-line) are shown in Fig. 4-16. The MV AC voltages are controlled to be the reference, and the load current is equally shared between PCS 1 and PCS2, which also shows that the circulating current is small.

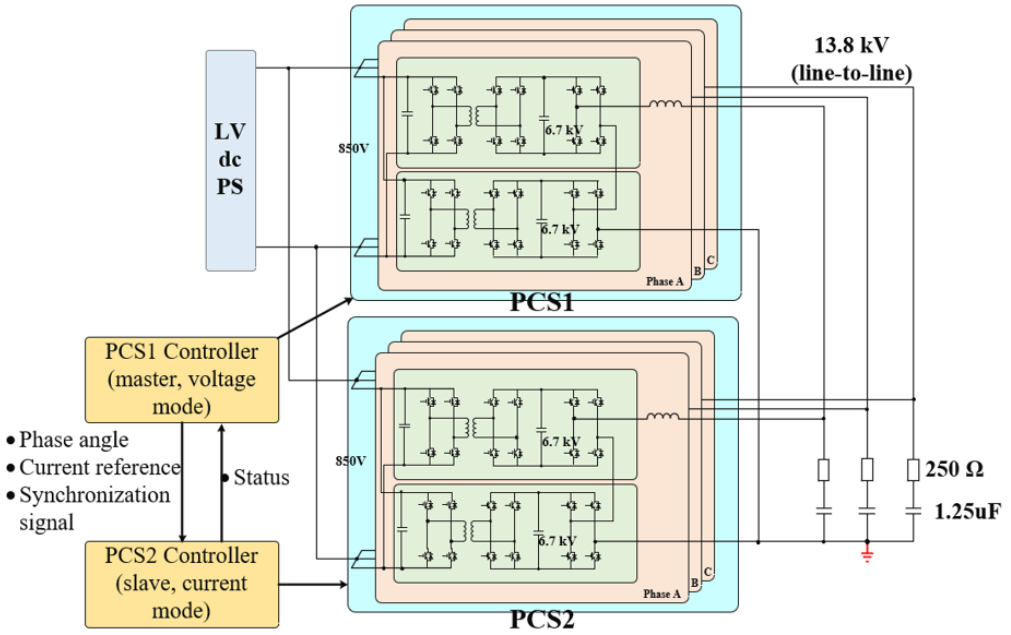


Fig. 4-16. Scheme of the PCS paralleling test setup for islanded mode operation

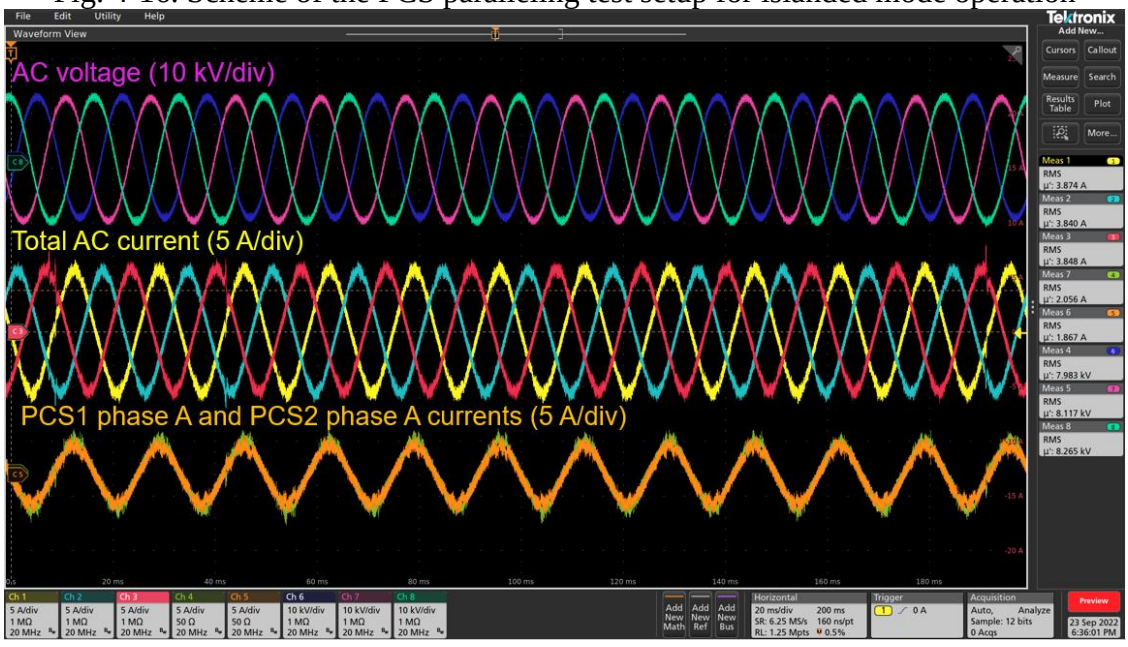


Fig. 4-17. MV AC voltage and current waveforms under the paralleling setup for islanded mode operation

The setup scheme for the grid-connected mode operation is shown in Fig. 4-18. The two PCS converters are still parallel connected at both the LV DC side and the MV AC side. A 1.7 kV Si IGBT-based three-phase two-level converter is used as the grid emulator, generating the AC voltage and frequency. The AC output of the grid emulator is connected to the MV AC output of the two PCS converters through three single-phase 277 V/0-277 V VARIAC three single-phase 120 V/8 kV transformers. The DC input of the grid emulator is connected to the PCS LV DC input, so the power can circulate between the PCS converters and the grid emulator. In this setup, the PCS converters operate in the current mode, controlling the AC side current (power). The MV AC voltage and current waveforms are shown in Fig. 4-19. The current waveforms of PCS 1 and PCS 2 almost match with each other, which means the current sharing between the two converters is achieved and the circulating current is small.

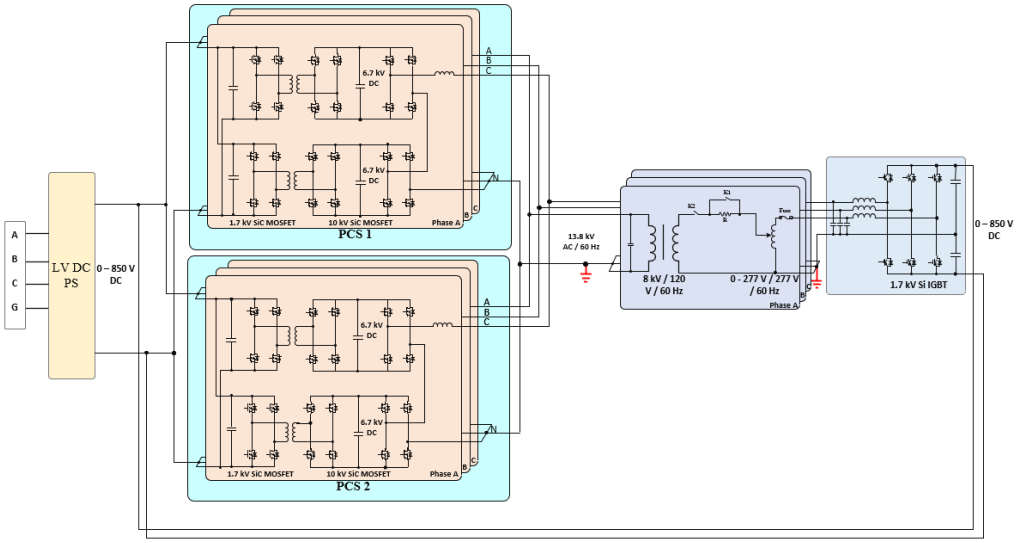


Fig. 4-18. Scheme of the PCS paralleling test setup for grid-connected mode operation

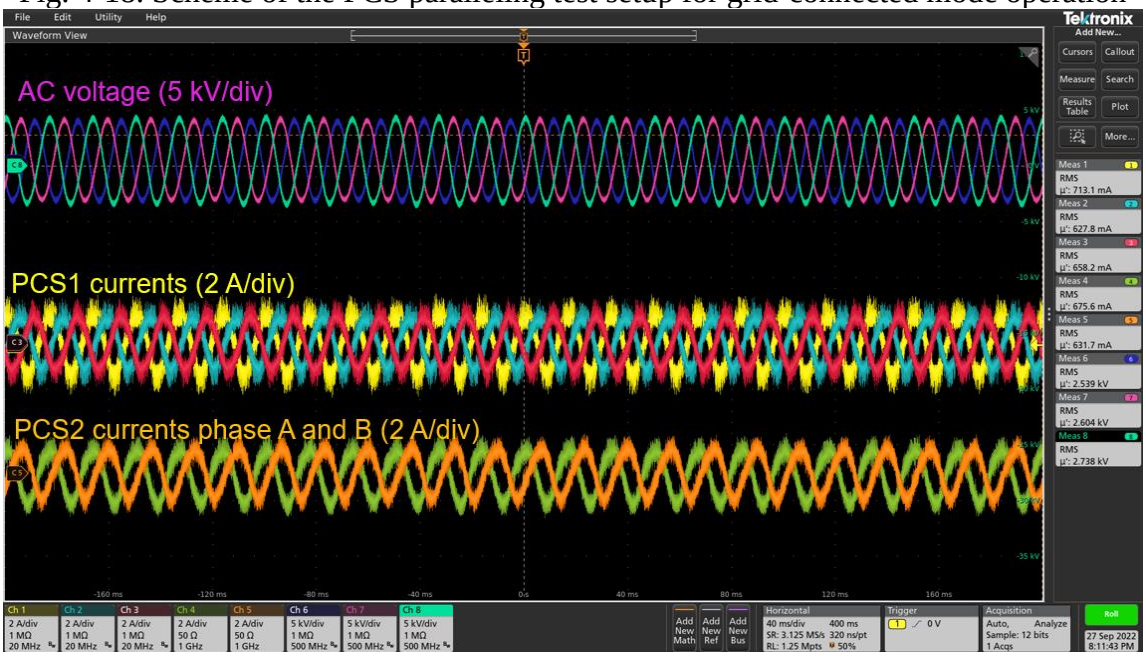


Fig. 4-19. MV AC voltage and current waveforms under the paralleling setup for grid-connected mode operation

5. SUMMARY

5.1 F-CHP PCS CONVERTER DESIGN

PCS specification and grid requirements have been identified. The grid and standard impact have been studied on the control and power stage design of the F-CHP PCS, considering multiple modes, LVRT/HVRT, faults, unbalance, transients, etc.

The PCS has been designed with high power density and efficiency, considering grid impact, insulation ratings, the effects of parasitics, etc.

Tests have been performed and verified the functionalities of the PCS hardware design considering grid requirement.

5.2 F-CHP CONTROLLER DESIGN

The needs of the controller for the F-CHP system have been identified to operate in both islanded and grid-connected scenarios.

Designed the controller architecture and control algorithms have been designed considering different CHP characteristics. And the controller has been tested in three simulation models (i.e., simulation, HIL and HTB) in different time scales.

Implemented and HIL-tested the control algorithms in NI's general purpose controller.

Small-scale PCS has been designed and implemented with the HTB to verify the F-CHP controller.

6. REFERENCE

[1] "SiC-Based Modular Transformer-less MW-Scale Power Conditioning System and Control for Flexible CHP System," Advanced Manufacturing Office U.S. Department of Energy 2020. [Online]. Available: https://www.energy.gov/eere/amo/articles/sic-based-modular-transformer-less-mw-scale-power-conditioning-system-and-control

[2] J. Wang *et al.*, "Economic Benefits of Integrating Solar-Powered Heat Pumps Into a CHP System," *IEEE Transactions on Sustainable Energy,* vol. 9, no. 4, pp. 1702-1712, 2018, doi: 10.1109/TSTE.2018.2810137.

[3] H. Li *et al.*, "Development of a Power Electronics-based Testbed for a Flexible Combined Heat and Power System," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 10-14 Oct. 2021 2021, pp. 764-770, doi: 10.1109/ECCE47101.2021.9595994.

[4] H. Li, Z. Gao, S. Ji, Y. Ma, and F. Wang, "An Inrush Current Limit Method for SiC-based Multi-level Grid-connected Converter During Low-Voltage Ride-Through," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 14-17 June 2021 2021, pp. 2044-2049, doi: 10.1109/APEC42165.2021.9487192.

[5] H. Li, Z. Gao, S. Ji, Y. Ma, and F. Wang, "An Inrush Current Limiting Method for Grid-Connected Converters Considering Grid Voltage Disturbances," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 10, no. 2, pp. 2608-2618, 2022, doi: 10.1109/JESTPE.2022.3147515.

[6] H. Li, Y. Ma, S. Ji, and F. Wang, "The Impact of the Lightning Surge on SiC-based Medium-voltage Three-phase Four-wire Grid-connected Converters," in *2021 IEEE*

Applied Power Electronics Conference and Exposition (APEC), 14-17 June 2021 2021, pp. 2037-2043, doi: 10.1109/APEC42165.2021.9487166.

[7] H. Li, P. Yao, Z. Gao, and F. Wang, "Medium Voltage Converter Inductor Insulation Design Considering Grid Requirements," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 2339-2350, 2022, doi: 10.1109/JESTPE.2021.3131602.

[8] Z. Gao, H. Li, and F. Wang, "A Medium-Voltage Transformer with Integrated Leakage Inductance for 10 kV SiC-Based Dual-Active-Bridge Converter," in *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, 7-9 Nov. 2022 2022, pp. 221-226, doi: 10.1109/WiPDA56483.2022.9955258.

[9] H. Li, Z. Gao, and F. Wang, "A PWM Strategy for Cascaded H-bridges to Reduce the Loss Caused by Parasitic Capacitances of Medium Voltage Dual Active Bridge Transformers," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 9-13 Oct. 2022 2022, pp. 1-6, doi: 10.1109/ECCE50734.2022.9947550.

[10] H. Li, Z. Gao, Z. Yang, C. Nie, and F. Wang, "A Medium Voltage Testbed for the Performance and Function Tests of a 13.8 kV Power Conditioning System Converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 20-24 March 2022 2022, pp. 757-763, doi: 10.1109/APEC43599.2022.9773522.

[11] H. Li, Z. Gao, and F. Wang, "Medium Voltage Isolated Auxiliary Power Supply Design for High Insulation Capability, Ultra-Low Coupling Capacitance, and Small Size," *IEEE Transactions on Power Electronics*, pp. 1-14, 2023, doi: 10.1109/TPEL.2023.3244855.

[12] H. Shyh-Jier and S. Kuang-Rong, "Short-term load forecasting via ARMA model identification including non-Gaussian process considerations," *IEEE Transactions on Power Systems*, vol. 18, no. 2, pp. 673-679, 2003, doi: 10.1109/TPWRS.2003.811010.