Feed-Forward Compensation for Model Predictive Control in Tri-port Current-Source Medium-Voltage String Inverters for PV-Plus-Storage Farms

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***Abstract*— The novel tri-port current-source medium-voltage string inverter (TCS-MVSI) is a promising candidate for large-scale PV-plus-storage (PVS) farms owing to its galvanic isolation, easy storage integration, soft-switching capability across entire load range, controlled low dv/dt and EMI, benign fault tolerance, etc. Due to its low inertia feature, traditional PI-based control cannot manage large transients effectively. Instead, a model-based predictive control (MPC) is proposed to achieve robust and stable operation. As is well known, the control performance of MPC is compromised by the sampling and computational delay during implementation significantly, if not well addressed. This paper analyzed and quantified these delays and then proposes feed-forward compensation (FFC) for the MPC method to compensate the delays and the large parameter variations due to the low-inertia nature. In addition, this method also compensates for the high dc-link ripple within each switching cycle, a unique issue for low-inertia converters. The proposed method requires low computational effort, allowing it to be extended for multiple ports. The effectiveness of the proposed method has been validated in experiments. In 10 kW test, the proposed method decreases the average dc-link current by 17%, leading to ~20% conduction losses and ~0.5% increase in converter efficiency. In addition, the peak dc-link current also decreases by 15%, resulting in reduced transformer size. As a result, an increased power density can be achieved with the proposed method. Similar improvements have been observed across the power range from 2 kW to 10 kW.**

Keywords*— *tri-port, low-inertia, current-source converters, medium voltage string inverters (MVSI), soft-switching, low EMI, PV-plus-storage (PVS), solar-plus-storage, model predictive control (MPC), sampling and computational delay, feed-forward compensation, ripple compensation.

I. INTRODUCTION

PVS is becoming a favored configuration for newly commissioned large-scale PV projects since integrated storage can provide energy dispatchability and auxiliary grid support services [1]. To integrate the storage, additional converters are required in traditional central and string inverters, which increases the cost, installation, and O&M efforts [2-4]. Instead, the recently proposed tri-port current-source medium-voltage string inverters (TCS-MVSI), which is derived from the soft-switching solid-state transformer (S4T), can integrate the storage easily and eliminates the additional converters [5, 6]. Besides, it provides several additional attractive features like single-stage conversion, galvanic isolation, soft-switching capability across entire load range, controlled low dv/dt and EMI, and benign fault tolerance, making it a promising candidate for large-scale PVS applications [5].

However, the reduced dc-link inductance of S4T converters brings low inertia and high dc-link ripple, posing great challenges to traditional PI-based control and causing control saturation under large transients. To address this challenge, a model-based predictive control was proposed in [7]. As is well known, the performance of model predictive control (MPC) is highly dependent on an accurate system model and is easily degraded by control delays and parameter mismatches, especially in high-frequency applications [8, 9]. In [7], compensation based on second-order terms has been proposed and verified.

This paper proposes feed-forward compensation (FFC) for MPC to be used in a tri-port current-source medium-voltage string inverter (TCS-MVSI). The objective of the FFC is to compensate for both the sampling and computational delays and the high dc-link ripple dynamics with low computational effort, allowing it to be extended for an *N*-port converter. First, the induced sampling and computational delays of MPC control during implementation are analyzed and quantified. Next, the scheme of proposed FFC for MPC will be discussed in detail. In the end, the effectiveness of the proposed control is validated in experiments at different power levels. In 10 kW experiments, the average and peak dc-link magnetizing currents are reduced by >15%, leading to reductions in converter losses and transformer size. Consequently, an increased efficiency and power density of the TCS-MVSI can be achieved.

II. TRI-PORT CURRENT-SOURCE MEDIUM-VOLTAGE STRING INVERTERS

The tri-port current-source medium-voltage string inverter (TCS-MVSI) is derived from a novel topology called soft-switching solid-state transformer (S4T) [5, 6, 10]. As shown in Fig. 1, the TCS-MVSI consists of twelve 25 kVA TCS-MVSI power electronics building blocks (PEBBs) connected in the input-parallel-output-series (IPOS) manner. Each TCS-MVSI PEBB is configured as a tri-port with PV and storage connected to the LV bridge. On the MV bridge, the TCS-MVSI PEBB is configured as a single-phase AC output for series stacking and four of them are connected in series to achieve 2.4 kV MV on

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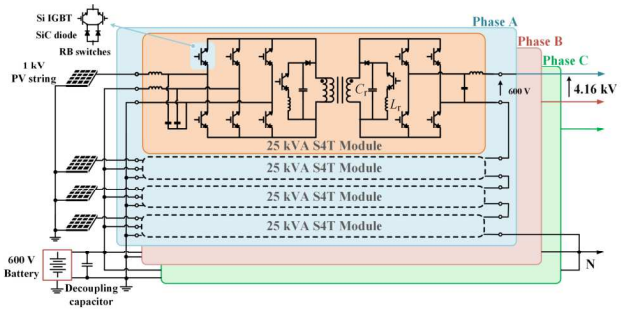


Fig. 1. Schematic of proposed 4 kV/300 kVA TCS-MVSI.

the AC side. The three-phase system contains three of them in the same structure and is able to achieve 4 kV MVAC output.

A common storage/capacitor is connected across all the modules, where the decoupling capacitor is required to eliminate double-line frequency pulsating power for single-phase ac output but not for the three-phase system. Besides, the common storage/capacitor allows the power exchange across all modules, which guarantees a balanced output across the series-connected modules even under unbalanced inputs [5].

III. Delays in Model-Predictive Control

The compact high-frequency transformer of the TCS-MVSI features a reduced dc-link magnetizing inductance and consequent low inertia of the converter. But the low inertia poses great challenges to traditional PI-based control and causes control saturation under large transients. To address this challenge, a model-based predictive control (MPC) was proposed in [7]. The compensation based on second-order terms proposed in [7], is disabled in this paper to show the efficacy of the proposed compensation block.

A. Control Diagram of MPC

Fig. 2 presents the control diagram of MPC based on a controller integrating both DSP and FPGA. The DSP communicates with FPGA at 16 kHz interrupt frequency and the FPGA interfaces with the hardware prototype with 50 MHz clock frequency. The FPGA samples voltage/current sensor measurements and send data to the DSP for time calculation and state sequence determination in each switching cycle, which will be sent back to the FPGA to generate gate signals for control.

The principle of MPC control is to control the dc-link magnetizing current I_m to its reference value $I_{m,ref}$ with (1) by maintaining the volt-sec balance of the magnetizing inductance L_m in the high-frequency transformer. In practical, the power mismatch between PV and grid port is balanced out by the decoupling port, the common storage/capacitor.

$$\Delta I_{m,error,comp} = I_{m,ref} - I_m = \sum V_{port,n} \cdot t_{port,n} / L_m \quad (1)$$

B. Sampling and Computational Delay

Time delays from sampling and computation during implementation are inevitable in MPC based control. In the proposed implementation, the delay can be estimated according to the event sequences of the MPC control shown in Fig. 3:

- t_1 - t_2: at the beginning of the k^{th} switching cycle, all voltage/current sensor measurements including I_m are sampled with 4-sample moving averaging technique in the FPGA. The sampling frequency is set as 320 kHz and the 4-sample moving averaging process takes around 12 us.
- t_2 - t_3: sensor sampling finishes at t_2 and the FPGA triggers DSP interrupt immediately to write processed values to the DSP. This process takes only a few FPGA clock cycles (< 0.1 us).

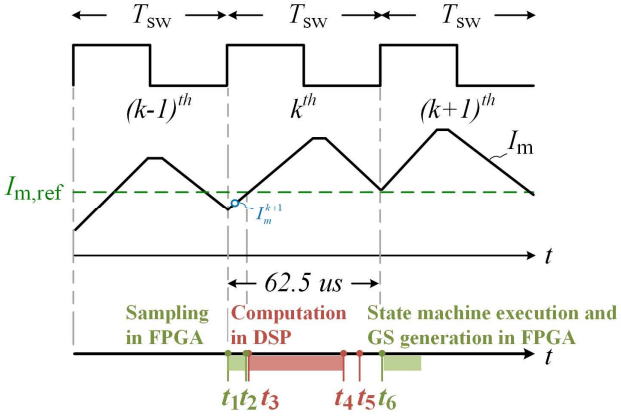


Fig. 3. Event sequences of MPC control.

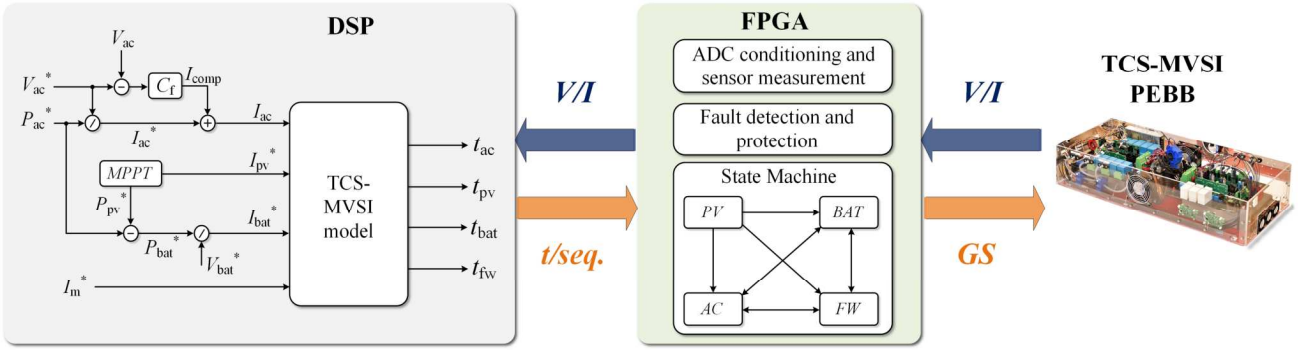


Fig. 2. Control digram of MPC control.

- $t_3 - t_4$: DSP determines state sequences and calculates time durations for each state in the $(k+1)^{th}$ cycle based on TCS-MVSI model.
- $t_4 - t_5$: DSP writes state sequences and time durations into DSP memory. It usually takes several microseconds.
- $t_5 - t_6$: idling stage, DSP memory is waiting to be read by the FPGA at the upcoming interrupt at t_6.
- t_6: at the beginning of the $(k+1)^{th}$ switching cycle, the FPGA reads values from DSP memory, executes the state machine, and generate gate signals to control the hardware prototype.

It can be observed that one switching cycle of sampling and computational delay is introduced, where FPGA sampling takes ~12 us while DSP computation takes ~ 40 us. Hence, with uncompensated MPC, the duty cycles for $(k+1)^{th}$ switching cycle are calculated in k^{th} cycle. More importantly, the calculations are based on the measurements done at the start of k^{th} cycle. Of all the parameters, the most important one is the magnetizing current. Essentially, the calculations for $(k+1)^{th}$ cycle are based on I_m^k, instead of I_m^{k+1}. The error compensation done in the $(k+1)^{th}$ cycle under the case of MPC without delay compensation is given by (3).

$$\Delta I_{m\_error\_comp}^{k+1} = I_{m\_ref} - I_{m,meas}^{k} \tag{2}$$

whereas ideally it should have been

$$\Delta I_{m\_error\_comp}^{k+1} = I_{m\_ref} - I_{m,meas}^{k+1} \tag{3}$$

As expected, this may lead to over or under compensation resulting in oscillations in I_m, causing increased power losses in semiconductors, transformers, filters, snubbers, etc. Under large transients, the deviation could be large enough for the controller to become unstable.

IV. Proposed Feed-Forward Compensation For Model-Predictive Control

To mitigate the negative impact of time delays, a feed-forward compensation (FFC) for model-predictive control (MPC) is proposed. It shares the same event sequence as the MPC without compensation shown in Fig. 3. The FFC comprises two parts, one-switching-cycle sampling and computational delay compensation and high dc-link ripple compensation, where the high dc-link ripple is a unique issue for low-inertia converters with reduced dc link. The proposed method addresses the issue with reduced implementation effort and computation cost, especially for N-port low-inertia converters.

A. Sampling and Computational Delay Compensation

Fig. 4 demonstrates an implementation example of I_m in the k^{th} cycle of converter. One of the primary control objectives is to estimate time durations for various states in the $(k+1)^{th}$ cycle as accurately as possible based on TCS-MVSI model. To achieve this goal, an accurate estimation of the initial I_m in the $(k+1)^{th}$ cycle, $I_{m,est,FFC0}^{k+1}$, is critical.

In the MPC without compensation, owing to the one-switching-cycle delay quantified in the last section, DSP assumes the sampled $I_{m,meas}^{k}$ in the k^{th} cycle is equal to the $I_{m,est,FFC0}^{k+1}$ in the $(k+1)^{th}$ cycle, inducing a large error in $I_{m,meas}^{k+2}$. Instead, with MPC with FFC, $I_{m,est,FFC0}^{k+1}$ is estimated using the following equation:

$$I_{m,est,FFC0}^{k+1} = I_{m,meas}^{k} + \Delta I_{m\_error\_comp}^{k} \tag{4}$$

$$\Delta I_{m\_error\_comp}^{k} = I_{m\_ref} - I_{m,est,FFC0}^{k} \tag{5}$$

The error compensation for $(k+1)^{th}$ cycle is now given as

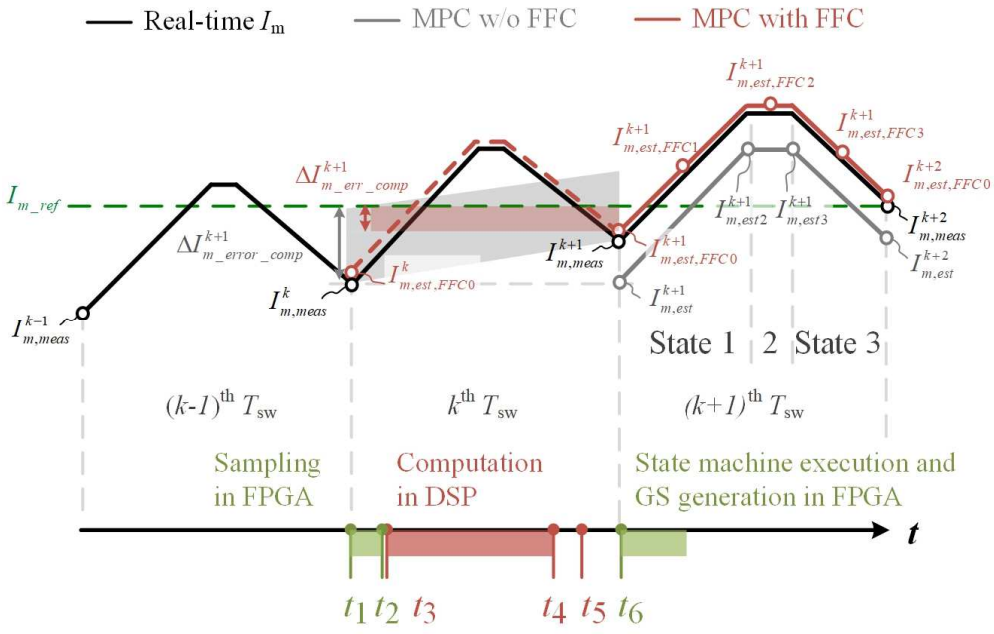


Fig. 4. Proposed MPC with FFC.

$$\Delta I_{m\_error\_comp}^{k+1} = I_{m\_ref} - I_{m,est,FFC0}^{k+1} \quad (6)$$

which can also be written as

$$\Delta I_{m\_error\_comp}^{k+1} = I_{m\_ref} - I_{m,meas}^{k} - \Delta I_{m\_error\_comp}^{k} \quad (7)$$

Please note that the $\Delta I_{m\_err\_comp}^{k}$ is available from the calculations done in the *(k-1)*th switching cycle. Comparing (2) with (7), it is clear that the delay compensation is achieved just by a single arithmetic operation using the error compensation value from the previous cycle. As a result of using the estimated value, over/under compensation of the $I_{m,meas}^{k}$ is reduced, thereby avoiding oscillations and instability in I_m.

In a more accurate implementation of delay compensation, the estimated $I_{m,est,FFC0}^{k+1}$, can be calculated using the $I_{m,meas}^{k}$, duty cycles of all states as calculated in the *(k-1)*th cycle, the plant model, and new voltage samples available at the start of k^{th} cycle. However, this can lead to significant computational effort. In the proposed method, the estimation is done through $I_{m,meas}^{k}$ and the model calculations done in *(k-1)*th cycle, which provide $I_{m,est,FFC0}^{k}$. Essentially, compared to the detailed delay compensation scheme, the simplification is achieved through ignoring the filter capacitor voltage dynamics, which is acceptable as the capacitive filter is designed to limit the voltage peak-to-peak ripple to < 10%.

Please note that $I_{m,est,FFC0}^{k+1}$ is still an estimate and could be different from the actual value $I_{m,meas}^{k+1}$. The error in the estimate could be because the following approximations:

1) Neglected sensor delays and offsets
2) Computational errors
3) Neglected dynamcis of filter capacitor voltages
4) Inaccurate plant model

To address the delays and the associated dynamics caused by these approximations, a compensation coefficient, k_{comp}, is used in the error compensation equation.

$$\Delta I_{m\_err\_comp}^{k+1} = k_{comp} \cdot \left(I_{m\_ref} - I_{m,est,FFC0}^{k+1}\right) \quad (8)$$

where $0 \le k_{comp} \le 1$. The error compensation will be finished in one switching cycle if $k_{comp} = 1$, which is the traditional dead-beat control. But it might incite instability issues with aforementioned approximations. With $k_{comp} < 1$, the error will be reduced to <10% in N cycles with (9), where *N* is the number of switching cycles for compensation.

$$e = (1 - k_{comp})^{N} \quad (9)$$

$k_{comp} = 0.6$ is selected to distribute the error compensation burden to three switching cycles.

B. I_m Ripple Compensation

Different from traditional converters with bulky dc link, the low inertia converters with multiple ports/states suffer an increased ripple on their DC links. As a current-source low-inertia converter, the dc-link current of TCS-MVSI, I_m, varies by 60% in different states within each switching cycle. As a result, each state has a significantly different I_m to start with and over the time of its state. Therefore, I_m has to be estimated separately for each state within the same single switching cycle to minimize the negative impact of high I_m ripple. This issue does not exist in traditional high-inertia converters but prevails in low-inertia converters such as TCS-MVSI.

To address this issue in TCS-MVSI, a computationally inexpensive method to estimate the average I_m for each state is proposed, which can be easily scaled to an *N*-port converter. Instead of using the initial currents $I_{m,est}^{k+1}$, $I_{m,est2}^{k+1}$, and $I_{m,est3}^{k+1}$ for each state without any compensation, the MPC with FFC uses the average currents $I_{m,est,FFC1}^{k+1}$, $I_{m,est,FFC2}^{k+1}$, and $I_{m,est,FFC3}^{k+1}$ in each state to approximate the real-time values in the $(k+1)^{th}$ cycle. These average currents are calculated with (10), where the time periods $t_{port,n}$ are computed based on the initial currents $I_{m,est,FFC0}^{k+1}$ after FFC with (11). Here the variations in filtering capacitor voltages of different ports are neglected intentionally to simplify the calculation since these capacitors are designed to limit the voltage peak-to-peak ripple to < 10%, while the peak-to-peak ripple in I_m is 40%-60%.

$$I_{m,est,FFCn}^{k+1} = I_{m,est,FFC0}^{k+1} + \sum_{i=0}^{n-1} \frac{V_{port,i} \cdot t_{port,i}}{L_m} + \frac{V_{port,n} \cdot t_{port,n}}{2L_m}, \quad n = 1,2,3 \quad (10)$$

$$t_{port,n} = \begin{cases} 0, & n = 0 \\ I_{port,n} \cdot T_{sw} / (I_{m,est,FFC0}^{k+1} + \sum_{i=0}^{n-1} \frac{V_{port,i} \cdot t_{port,i}}{L_m}), & n = 1,2,3 \end{cases} \quad (11)$$

The selected parameters in MPC without compensation and MPC with FFC are summarized in Table I.

TABLE I. SELECTED PARAMETERS IN MPC W/O COMPENSATION AND MPC WITH FFC

Cal. in the k^{th} switching cycle	**MPC w/o compensation**	**MPC with FFC**
FFC-compensated I_m - $\Delta I_{m,comp}^{k+1}$	--	$k_{comp} \cdot (I_{m\_ref} - I_{m,est,FFC0}^{k})$
Estimated initial I_m in the $(k+1)^{th}$ cycle	$I_{m,meas}^{k+1}$	$I_{m,FFC0}^{k+1}$
I_m for time duration of state 1	$I_{m,meas}^{k+1}$	$I_{m,FFC1}^{k+1}$
I_m for time duration of state 2	$I_{m,est2}^{k+1}$	$I_{m,FFC2}^{k+1}$
I_m for time duration of state 3	$I_{m,est3}^{k+1}$	$I_{m,FFC3}^{k+1}$
I_m used for error compensation	$I_{m,meas}^{k+1}$	$I_{m,FFC0}^{k+1}$

V. EXPERIMENTAL VALIDATION

The hardware prototype of 25 kVA TCS-MVSI PEBB is presented in Fig. 5. And the test bench to validate the performance of the proposed method is shown in Fig. 6. The system specifications of the TCS-MVSI and the test bench are summarized in TABLE II.

Fig. 7 shows the comparative performances with two methods at 10 kW test. Compared with 117 A with the MPC without compensation, the FFC-MPC reduces the average I_m by 17% to 97 A. According to [10], the conduction losses in semiconductor devices account for > 60% of the total power losses of the converter (~3%). As a result, the 17% reduction in I_m can save at least 17% conduction losses in semiconductors and the savings would expand to >20% when taking the transformer and snubbers losses into account. As a result, the converter efficiency can be enhanced by ~ 0.5% considering the quadratic relationship of conduction losses to the flowing current.

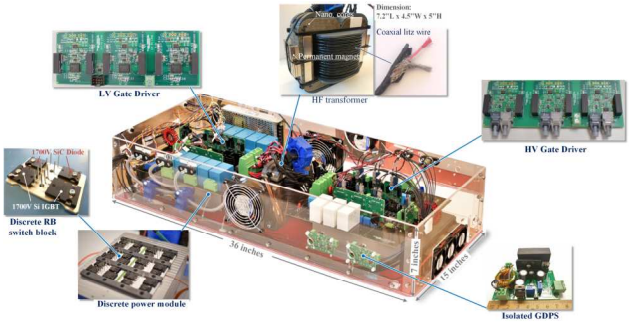


Fig. 5. Hardware prototype of 25 kVA TCS-MVSI PEBB.

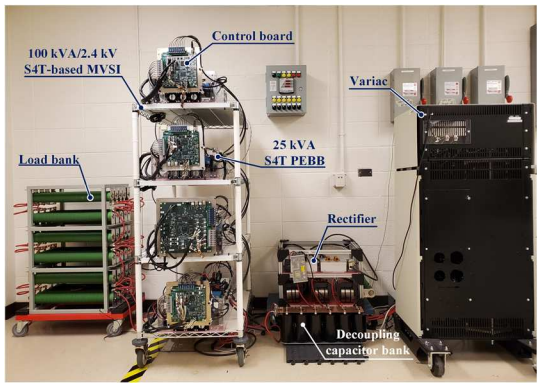


Fig. 6. Experiment setup.

TABLE II. SYSTEM SPECIFICATION OF TCS-MVSI AND TEST BENCH

Parameters	***Values***	**Parameters**	***Values***
PV voltage	1000 V	AC voltage	600 Vrms
Battery voltage	650 V	Decoupling capacitor	1.1 mF
Switching freq.	16 kHz	Magnetizing ind.	350 uH
Resonant capacitor	50 nF	Resonant inductor	2 uH

In addition, the peak I_m drops from 151 A to 129 A, a 15% reduction with the proposed method. This reduction decreases the saturation current limit of the transformer core and results in reduced core size. As a result, an increased power density of the TCS-MVSI can be achieved with the proposed method thanks to the improved converter efficiency and reduced transformer size.

Similar improvements have also been observed across the power range from 2 kW to 10 kW, as presented in Fig. 8.

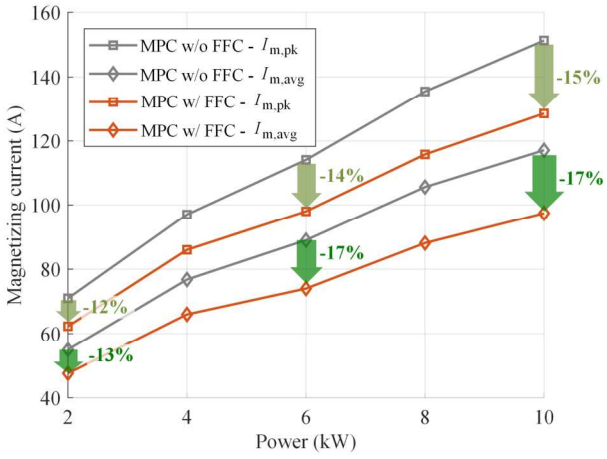
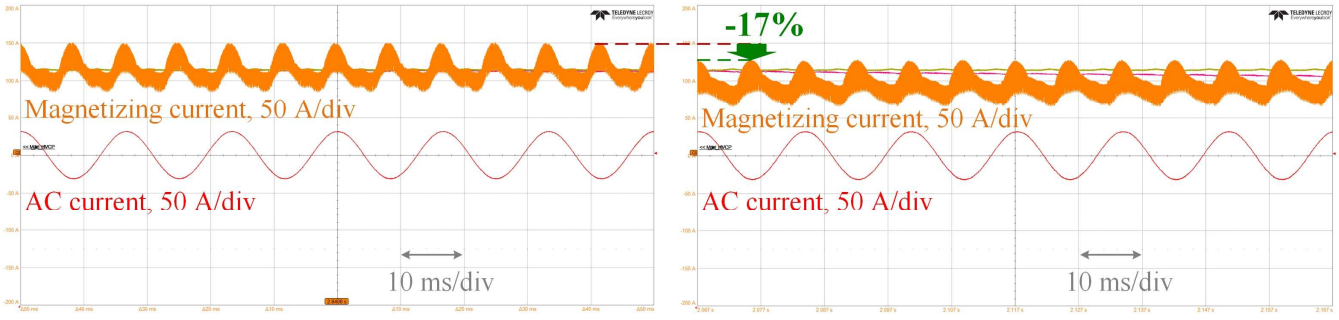


Fig. 8. Performance improvements of proposed method across 2 kW to 10 kW.



(a) MPC without compensation

(b) Proposed MPC with FFC

Fig. 7. Performance comparison of MPC without compensation and proposed MPC with FFC at 10 kW experiments.

VI. CONCLUSION

This paper proposed a feed-forward compensation for Model Predictive Control to be used with the novel TCS-MVSI in large-scale PVS farms. The proposed method compensates for the sampling and computational delay and high dc-link ripple in low-inertia TCS-MVSI. Firstly, one switching cycle of sampling and computational delay in the MPC method is analyzed and quantified. Next, the scheme of the proposed FFC for MPC is explained. It is shown that the proposed method addresses the delay and low-inertia related issues with low implementation effort and computational cost, which is especially beneficial for extending it to N-port low-inertia converters ($N \geqslant 3$). In the end, the effectiveness of the proposed method has been validated in experiments. It reduces both the average and peak dc-link current at different power levels. In 10 kW tests, the average magnetizing current decreases by 17%, leading to >20% conduction loss reduction and ~0.5% converter efficiency enhancement. In addition, the 15% reduction in peak magnetizing current reduces the saturation current limit of the transformer core and results in reduced core size. As a result, an increased power density of TCS-MVSI can be achieved with the proposed method. Similar improvements have also been observed across the power range from 2 kW to 10 kW.

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