Power Electronic Hardware-in-the-Loop (PE-HIL): Testing Individual Controllers in Large-Scale Power Electronics Systems

Suman Debnath
Oak Ridge National Laboratory
Knoxville, TN, USA
debnaths@ornl.gov

Phani R.V. Marthi
Oak Ridge National Laboratory
Knoxville, TN, USA
marthip@ornl.gov

Zerui Dong
OPAL-RT Corporation
Wheat Ridge, CO, USA
zerui.dong@opal-rt.com

Qianxue Xia
Georgia Institute of Technology
Atlanta, GA, USA
qxia@gatech.edu

Sudipta Chakraborty
OPAL-RT Corporation
Wheat Ridge, CO, USA
sudipta.chakraborty@opal-rt.com

***Abstract*—Large power electronics systems like multi-port autonomous reconfigurable solar power plant (MARS) are increasingly being researched upon to integrate emerging energy sources. MARS connects photovoltaic (PV) systems and energy storage systems (ESSs) to high-voltage direct current (HVdc) links/grids and high-voltage alternating current (ac) transmission grids. As these large power electronics systems incorporate complex hierarchical control systems that are close-by and communicate fast, the control systems require an unique power electronic hardware-in-the-loop (PE-HIL) real-time architecture to evaluate individual controllers. In this paper, a PE-HIL real-time architecture is proposed to evaluate one of the hundreds to thousands of digital signal processors (DSPs) that are a part of the complex hierarchical control system. The DSP connects to a central processing unit (CPU) and a field programmable gate array (FPGA) that form a part of the upper levels of the control system. The DSP is part of the lower level of the control system. The proposed PE-HIL architecture is tested and evaluated. Preliminary test results are presented to showcase the concept.**

***Index Terms*—MARS, DSP, Control, HIL**

I. Introduction

Large power electronics (PE) systems like high-voltage direct current (HVdc) converters, flexible alternating current transmission systems (FACTS), multi-port power electronics, among others, have been or are being developed. These large power electronics systems incorporate complex control architectures that are often hierarchical with high-speed communication links with very low latencies (in the order of micro-seconds or lower). The control architectures may require significant number of control devices (in the order of hundreds to thousands) that may be difficult to evaluate in research stage.

There is existing literature to evaluate higher level controllers in large-scale PE systems like in modular multilevel converters (MMCs) [1] or full-scale hierarchical control system in MMCs [2]–[5]. There is also existing literature to evaluate one PE's controller in a power grid with the rest of PEs in the power grid simulated in real-time simulators. In these types of systems, there are examples where the one PE controller interacts with higher level controllers like a microgrid controller or aggregated controllers or distribution management system [6], [7]. These interactions typically happen in the seconds to minutes time-scale. However, the interaction between one PE module's controller with the rest of the hierarchical control system in a large-scale PE system happens at a much faster time-scale (typically in the order of micro-seconds). One example of a large PE system in research is a multi-port autonomous reconfigurable solar power plant (MARS) that connects photovoltaic (PV) systems and energy storage systems (ESSs) to high-voltage direct current (HVdc) links/grids and high-voltage alternating current (ac) transmission grids [8]. The control system in MARS includes three hierarchical levels - L1, L2, and L3. While L1 controller is implemented in a central processing unit (CPU) and L2 controller(s) is implemented in one or more (up to 6) field programmable gate arrays (FPGAs), the L3 controllers are implemented in hundreds to thousands of digital signal processors (DSPs). Implementing such a complex control system in early-stage research is challenging. To overcome this challenge and effectively test and characterize the hierarchical control ar-

Research sponsored by Solar Energy Technologies Office of U.S. Department of Energy. This material is based upon work supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under the Solar Energy Technologies Office Award Number 34019. The views expressed herein do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

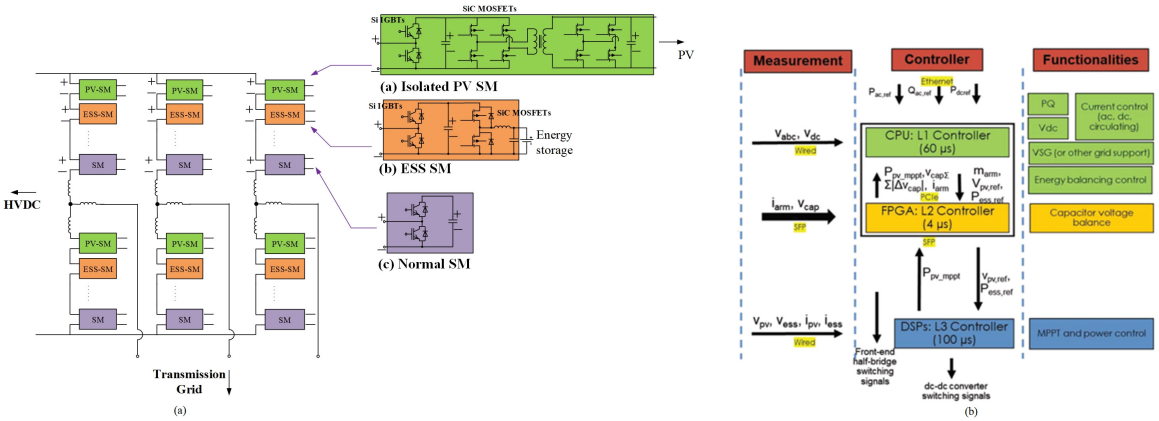

Fig. 1. MARS: (a) circuit architecture; (b) control system

chitecture, in this paper, the power electronic hardware-in-the-loop (PE-HIL) architecture for evaluating modules proposed in [9] is extended to test individual PE controllers in large-scale PE systems. In this paper, one L3 controller is tested along with L1 and L2 controller in MARS with a real-time PE-HIL test setup. This process enables the testing of stability and performance of the hierarchical control system. This process can be extended to other large PE systems in research that use fast communication in their hierarchical control systems with latencies in the order of micro-seconds.

II. MARS Architecture

The MARS' circuit architecture is shown in Fig. 1a [8]. The circuit comprises of 3 phase-legs consisting of 2 arms, namely, upper and lower arms. The phase-legs connect to HVdc and transmission ac grids. There are several submodules (SMs) connected in series with an inductor in each arm. There are three types of SMs in each arm: (i) PV-SM that connects to PV arrays, (ii) ESS-SM that connects to energy storage, and (iii) normal SM that is not connected to any PV array or energy storage. All three types of SMs consist of a silicon (Si) insulated-gate bipolar junction transistor (IGBT)-based front-end half-bridge. Additionally, the PV SM includes a silicon carbide (SiC) metal-oxide semicondutor field-effect transistor (MOSFET)-based unidirectional isolated or non-isolated boost converter that connects to the dc-link of the Si IGBT-based front-end half-bridge. The ESS SM includes a SiC MOSFET-based bidirectional non-isolated boost converter that connects to the dc-link of the Si IGBT-based front-end half-bridge. In each arm, there are N_{norm} normal SMs, N_{pv} PV-SMs, and N_{ess} number of ESS-SMs. The number of each type of SM is determined by the individual power rating of PV and ESS as well as the total power rating of PV and ESS in MARS. Further description on MARS maybe found in [8].

A. Control System

The hierarchical control system for MARS is shown in Fig. 1b. It consists of: (i) L1 controller in CPU, (ii) L2 controller in FPGA, and (iii) L3 controller in DSP. The communication between CPU and FPGA happens through peripheral component interconnect express (PCIe) and between FPGA and DSPs happens through small form factor pluggable (SFP) optical channels.

B. L1 Controller

The L1 controller is implemented in the CPU of the control system. It controls ac-side grid states like voltages, currents, active/reactive power, and frequency, and dc-side states like voltage and current. L1 controller also balances the energy between different types of SMs in an arm. Power dispatch commands that include power transferred to ac side ($P_{\text{ac,ref}}$), power transferred to dc side ($P_{\text{dc,ref}}$), and reactive power provided to ac side ($Q_{\text{ac,ref}}$) are sent by the system operator to L1 controller in MARS through ethernet communication. Based on the power dispatch commands and voltage (v_{abc})/frequency control of the ac grid, the L1 controller controls ac/dc currents and dc-link voltage (v_{dc}). It also provides energy balancing between different types of SMs (PV SMs, ESS SMs, and normal SMs) based on internal capacitor voltage and circulating current control through the energy balancing controller (EBC) [8]. Based on testing the system under different operating conditions, the EBC controller is activated under certain operating conditions where balancing between different types of SMs is not feasible otherwise. This minimizes the circulating current requirements. The voltage/frequency control of the ac grid in L1 controller is based on virtual synchronous generator (VSG), which is explained in detail in [8]. Based on these controllers, the L1 controller determines arm modulation indices (marm). The L1 controller also determines the reference voltage and power commands of PV and ESS in MARS ($v_{\text{pv,ref}}$ and ($P_{\text{ess,ref}}$)), respectively. The reference voltage of PV is determined based on the power transfer identified from PV and using the characteristics of PV to identify the voltage reference at its terminals. It sends the arm modulation indices, PV reference command, and ESS reference command to L2 controller through PCIe. It receives the summation of the capacitor voltages from each arm ($v_{\text{cap}\sum}$), summation of the absolute value of the difference between individual capacitor voltages from the average of the capacitor voltages in each arm ($\sum |v_{\text{cap}}|$), arm currents (i_{arm}), and the maximum power that can be generated from PV (P_{pvmppt}) from L2 controller

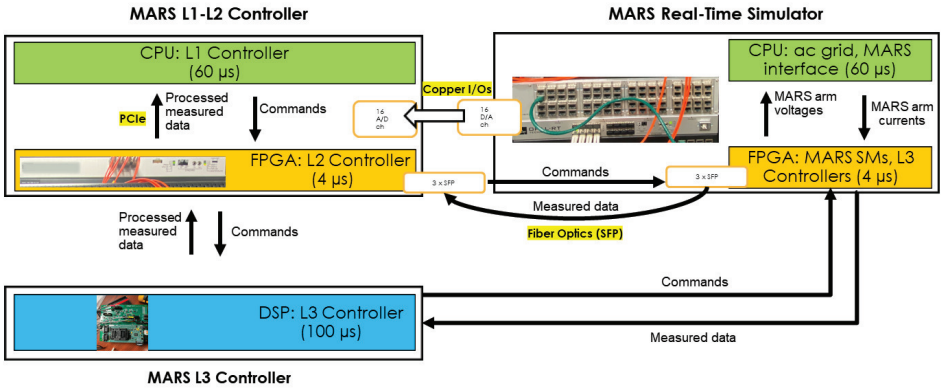

Fig. 2. PE-HIL setup to evaluate hierarchical control system of MARS.

through PCIe. It also receives measured ac-side voltages, dc-side voltage, and arm currents as inputs.

C. L2 Controller

The L2 controller maintains the capacitor voltages balanced across different SMs in each arm based on the existing SM capacitor voltage balancing algorithm [10]. It is implemented in the Xilinx Kintex-7 FPGA of the control system. The L2 controller receives the maximum power that can be generated by PV (P_{pvmppt}) from L3 controller and sends the PV/ESS reference ($v_{\text{pv,ref}}$ and ($P_{\text{ess,ref}}$)) to the L3 controller. It also generates the switching signals for the front-end half-bridges of all the SMs. The L2 controller is implemented in the FPGA of the control system by modifying a generic voltage balancing algorithm as presented in [11]. The L2 controller receives modulation indices from L1 controller to control the voltage in the arm of MARS. It also receives the measured arm currents and SMs front-end half-bridge capacitor voltages from MARS. It determines the number of front-end half-bridges that need to be turned ON at each L1 controller time-step in each arm of MARS. Based on the already turned ON front-end half-bridges prior to the current L1 controller time-step, the number of additional front-end half-bridges that need to be turned ON/OFF are identified. The L2 controller turns additional front-end half-bridges ON/OFF depending on the direction of the arm current and status of the capacitor voltages [10]. Furthermore, the status of a pair of front-end half-bridges in each arm may be swapped based on the direction of arm current and if the minimum or maximum SMs front-end half-bridge capacitor voltage violates a pre-defined lower or upper limit. The L2 controller repeats the whole process to maintain the SMs front-end half-bridge capacitor voltages in the required range. After finishing the implementation of the L2 controller in the FPGA, six L2 controllers are instantiated, with one for each arm.

D. L3 Controller

The local control in PV and ESS SMs, termed as the L3 controller, regulates the power transferred from PV and ESS. The power commands received from L2 controller are in digital form and need to be converted within the DSP. For example, frequency modulation technique may be used to transfer the power/voltage command and the corresponding demodulation scheme needs to be implemented in the DSP to determine the commands. The power transfered from PV is regulated through the control of the PV voltage and the power from ESS through direct control of the power transfered. The L3 control algorithm has been implemented in the digital signal processor (DSP) using Code Composer Studio (CCS) for one ESS SM and one PV SM. Each PV and ESS SM's dc-dc converter L3 controller is tested independently. Typically, there will be hundreds to thousands of DSPs required based on the total number of PV and ESS SMs in MARS ($6 \times (N_{\text{pv}} + N_{\text{ess}})$).

III. PE-HIL Setup

The PE-HIL setup to evaluate the hierarchical control system of MARS is shown in Fig. 2. The PE-HIL setup consists of MARS real-time simulator in OPAL-RT's OP5707 platform and the MARS L1-L2 controller in CPU-FPGA with one PE controller (L3 controller) in DSP.

A. Real-Time Simulation Model

The MARS real-time simulator in the PE-HIL setup includes real-time simulation of the high-fidelity switched system model of MARS described in detail in [12]. The real-time simulation model includes ac grid and MARS interface simulated in the CPU. MARS SMs including the dc-dc converters and L3 controllers are simulated in the FPGA. The ac grid model of MARS is based on the high-fidelity electromagnetic transient (EMT) model of the grid developed in [13]. The arm currents in the MARS interface are simulated in the real-time simulation platform in the CPU. The front-end half-bridges in all SMs are modeled in the FPGA of the real-time simulation platform by using the generic MMC toolbox as presented in [14], [15]. The real-time simulation model developed in OPAL-RT's OP5707 simulator is described in detail in [16]. All the PV and ESS SMs' dc-dc converter models are developed in the FPGA of the real-time simulation platform and are integrated with the front-end half-bridge models along with their respective L3 controllers. The simulated L3 controllers incorporate the parameters like the sampling time, control time-step, and control delays incorporated in the controller implementation. The parameters like sampling time, control

time-step, and control delays are identified based on stand-alone controller hardware-in-the-loop (cHIL) evaluation of the L3 controller in DSP with a real-time simulation model of the dc-dc converters (in PV and ESS SMs). In the PE-HIL setup, the real-time simulation model also incorporates the capability to receive the switching signals for one PV dc-dc converter and one ESS dc-dc converter from the L3 controller in the DSP. The rest of the L3 controllers (that is in the order of several hundreds to thousands) is simulated in the real-time simulator. This provides the capability to not only evaluate the L1-L2 hierarchical controllers, but also evaluate the L1-L2 hierarchical controllers with one L3 controller in physical implementation. This process enables the characterization of the complete hierarchical control system of MARS through evaluating the stability of the one PV or ESS SM that is controlled by the physical L3 controller.

B. Hierarchical L1 - L2 Control System cHIL Test setup

The cHIL test setup to evaluate the hierarchical L1-L2 control system is shown in Fig. 5 with both L1 and L2 control algorithms of MARS incorporated in the control system. The high-fidelity real-time simulation model of MARS incorporated in the control system. The high-fidelity real-time simulation model of MARS without any external interface requirements is described in III-A and is used in the real-time simulation platform.

C. Real-Time MARS SM Model Development

In the PV and ESS-SMs, the dc-dc converters are used to connect the PV and ESS system to the Si-based front-end half-bridge in MARS. The front-end half-bridges in SMs are modeled in the FPGA of the real-time simulation platform by using OPAL-RT's generic MMC toolbox as presented in [16]. To connect with the dc-dc converter in SMs, the MMC toolbox is modified by sending the SM's capacitor voltage to the dc-dc converter model and receiving the injection current from dc-dc converter model as shown in Fig. 3. The high-speed SFP communication protocol is deployed to exchange the data between the MARS real-time simulation platform and control platform. The developments of PV and ESS dc-dc boost converter models and their L3 controllers in the FPGA of the real-time simulation platform are presented in [16]. In the PV

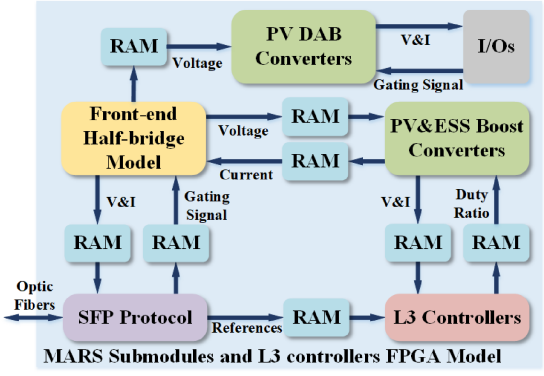

Fig. 3. Diagram of MARS SMs and L3 controllers FPGA model

isolated converters' development, as the first step, the Simulink Simscape Electrical model of dual active bridge (DAB) based PV dc-dc converter is developed. Based on this model, the discrete model of PV isolated dc-dc converter is developed as the second step. The discretization method used in developing the discrete model is introduced in [12] [17]. This method is the numerical stiffness-based hybrid discretization that could segregate stiff and non-stiff states in the PV converter. In this model, the numerical stiffness is observed in inductor current dynamics of the converter and not observed in capacitor voltage dynamics of the converter. As a result, the backward Euler and forward Euler are used to discretize the inductor current dynamics and capacitor voltage dynamics, respectively. The discretized form of capacitor voltage dynamics and inductor current dynamics are given by

$$I_{\mathrm{L}}[t] = \frac{L}{L + R_{\mathrm{L}} T_{\mathrm{s}}} \left(I_{\mathrm{L}}[t - T_{\mathrm{s}}] + \frac{T_{\mathrm{s}}}{L} \left(S_2 S_3 - S_1 S_4 \right) V_{\mathrm{sm}}[t] - \frac{T_{\mathrm{s}}}{L} a \left(S_6 S_7 - S_5 S_8 \right) V_{\mathrm{c}}[t] \right) \tag{1}$$

$$V_{\mathrm{c}}[t] = V_{\mathrm{c}}[t - T_{\mathrm{s}}] \left(1 - \frac{T_{\mathrm{s}}}{R_{\mathrm{c}} C} \right) + \frac{T_{\mathrm{s}}}{C} I_{\mathrm{pv}}[t - T_{\mathrm{s}}] + \frac{T_{\mathrm{s}}}{C} a \left(S_6 S_7 - S_5 S_8 \right) I_{\mathrm{L}}[t - T_{\mathrm{s}}] \tag{2}$$

where I_{L} is inductor current, L is DAB inductor's inductance, R_{L} is the series resistance of inductor, I_{pv} is the injection current of PV panel, S_1 to S_8 are semiconductor switching states, V_{sm} is PV-SM capacitor voltage, a is transformer turns ratio, V_{c} is capacitor voltage, C is converter capacitance, R_{C} is the parallel resistance of capacitor, and T_{s} is time step of simulation. Based on these discrete functions, the discrete model of PV isolated dc-dc converter is developed by converting Simulink Simscape Electrical model to the numerical function based model. To generate the FPGA firmware, the Simulink blocks in the discrete model are replaced by Xilinx Blockset to get the Xilinx block-based discrete model as shown in Fig. 4. In order to simulate up to one hundred PV isolated converters in real-time, a pipelining process is used to make the FPGA model utilize parallel computation capability that could save FPGA resources and make real-time simulation possible with a large number of dc-dc converters and sub-microsecond time step [16]. After deploying the pipelining process, the model of PV isolated dc-dc converter could simulate the 100 converters' dynamics of the states in each 500 ns which is the same as PV and ESS boost converter model. After the development, the PV isolated dc-dc converter model is deployed into the MARS to interact with front-end half-bridge model. However, these models could not be connected directly, since they are executed in different time-steps. The random-access memories (RAMs) are used as buffers to exchange the data between the isolated dc-dc converter model and front-end half-bridge model asynchronously. The rate transition is implemented in the RAM control logic to enable the RAM process the data executing in different time-steps. Additionally, to interact with

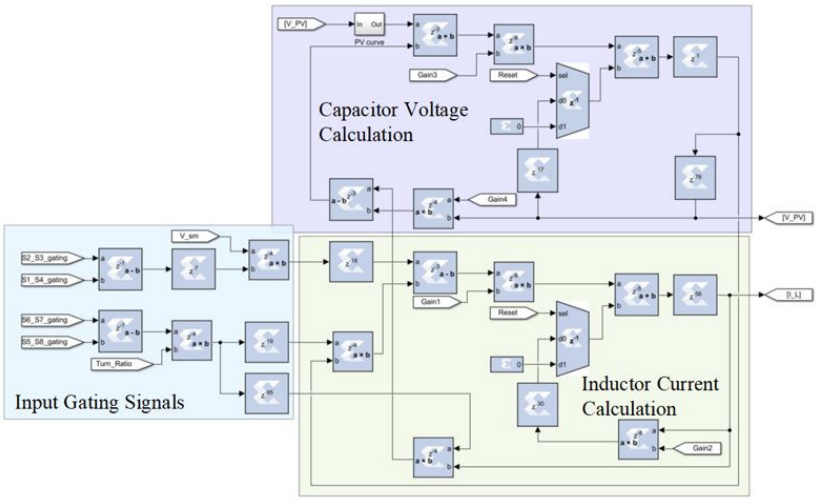

Fig. 4. Block diagram of PV isolated dc-dc converter FPGA model

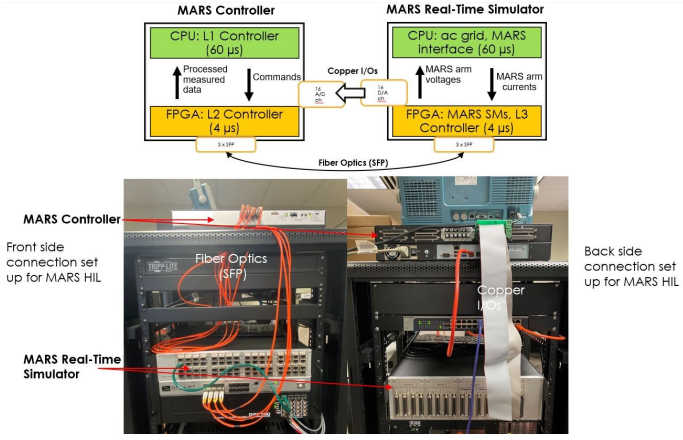

Fig. 5. MARS L1-L2 hierarchical controller cHIL setup

the external PE controller, which is running outside of the real-time simulation platform, the analog output channels are mapped to send the voltage and current measurements from one of the isolated converters to the external controller. And the digital input channels are mapped to receive the gating signals from the external controller. The dynamic model of the MARS system (including the three types of SMs) and L3 controller is implemented in the Xilinx Virtex-7 FPGA of the OP5707 real-time simulation platform.

D. Hierarchical PE Control System Under Test

While the real-world implementation of the hierarchical control system of MARS consists of L1-L2 controller in CPU-FPGA with hundreds-thousands of L3 controllers in DSPs, for low-cost early-stage research evaluation, it helps to characterize the interactions between L1-L2 controller in CPU-FPGA with at least one L3 controller in DSP for controlling PEs in the dc-dc converter of the PV or ESS SM. The hierarchical PE control system under test in this paper includes CPU-FPGA connected to one DSP.

E. PE-HIL Setup

The MARS real-time simulator sends ac-side voltages and arm current measurements to the L1 controller in CPU through analog copper inputs/outputs (I/Os). It also sends the measured front-end half-bridge capacitor voltages in each SM, arm currents, and maximum power available in PV to the control system (L2 controller) in FPGA through SFP. Through the SFP communication, SM capacitor voltages and arm currents measured from MARS hardware (in the real-time simulation platform) are sent to the L2 controller (in the control system). In addition, the switching commands, active power reference to the simulated L3 controllers in ESS SMs, and voltage reference to the simulated L3 controllers in PV SMs from the L2 controller are sent to MARS real-time simulator through the SFP. In the SFP communication, three channels, one channel for each phase, are used to exchange data. Eight SMs gating signals or two analog signals are packed in one 32-bit word in this communication. The dual-port RAMs are used as buffer to exchange data asynchronously between the SFP communication algorithm and the subsystems receiving the data. Additionally, 10 channels of analog I/Os are mapped to exchange system-level signals between the control system and real-time simulation platform. These channels are used to send measured arm currents, dc-side voltage, and ac-side voltages from real-time simulation platform. The real-time simulation platform includes the high-fidelity model of MARS that includes the power electronics hardware except for one L3 controller and is described in Section III-A. The L2 controller sends active power/voltage reference to the one L3 controller in DSP based on if ESS or PV SM's L3 controller is being tested. The power/voltage command reference is sent through digital communication.

The one L3 controller in DSP receives (through analog copper I/Os) the measured input voltage and inductor current from the ESS or the measured voltages from the PV dc-dc converter simulated in real-time in the FPGA of the real-time simulator.

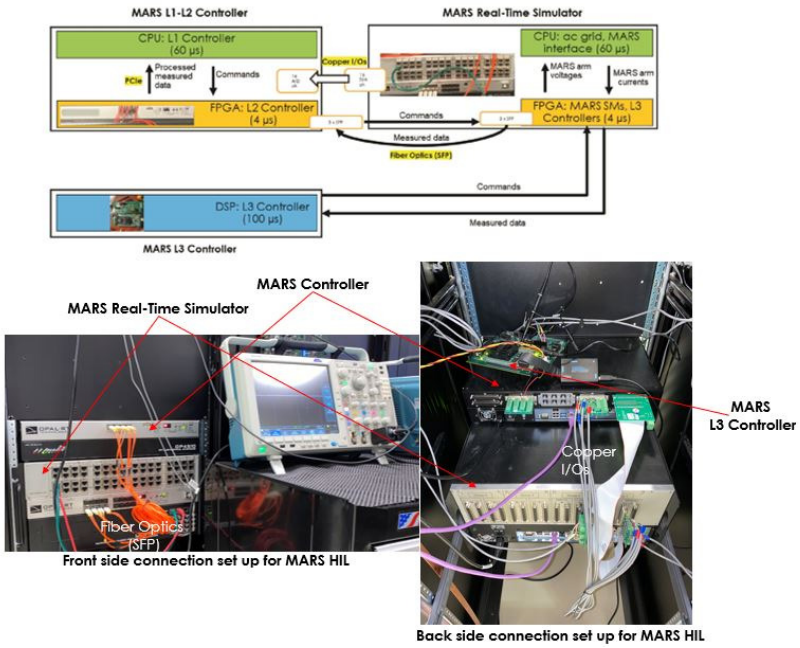

Fig. 6. PE-HIL test setup with open loop PE-HIL test layout

IV. Experimental Results

The case-study to evaluate the control algorithms is based on upgrading the HVdc substation at Pittsburg, CA. to MARS [8]. The HVdc substation at Pittsburg, CA, is a part of the Trans Bay Cable (TBC) link. The parameters of MARS are presented in [8]. The high-fidelity real-time simulation model, L1 controller, L2 controller, and L3 controller are developed in this study. The hierarchical L1-L2 control system system is tested in its cHIL test setup. In addition, the open-loop PE-cHIL control system is tested in its open-loop test setup. The PE-HIL test setup is shown in Fig. 6 along with open-loop PE-HIL test layout. This set-up is used in evaluation of both open loop PE-HIL tests and PE-HIL tests. In PE-HIL test setup, the active power/voltage reference (based on if ESS or PV SM's L3 controller is being tested) to the one L3 controller in DSP is sent from MARS L1-L2 controller as shown in Fig. 2. In this case, the active power/voltage command is received by the L3 controller from the L2 controller as a frequency modulated signal. In the case of open loop PE-HIL test, the active power/voltage reference (based on if ESS or PV SM's L3 controller is being tested) is not sent to the one L3 controller in DSP as shown in Fig. 6.

A. Hierarchical L1 - L2 Control system cHIL Test Results

The dispatch commands sent to MARS include variation of ac-side and dc-side powers: (1) $P_{\mathrm{ac,ref}}$, $P_{\mathrm{dc,ref}}$ = 100 MW and (2) $P_{\mathrm{ac,ref}}$, $P_{\mathrm{dc,ref}}$ = 300 MW. In operating condition 1, energy balancing control (EBC) described in [8] is required. EBC is not required in operating condition 2. The PV power produced in operating conditions 1 and 2 is used to charge the ESS. The test results for the different dispatch commands given to the hierarchical controllers are shown in Fig. 7. From the Fig. 7d, the front-end half-bridge capacitor voltages are observed to be balanced. This shows the successful operation of the EBC in L1 controller and the SM capacitor voltage balancing algorithm in L2 controller under different normal in the hierarchical control system of MARS.

B. Open loop PE-HIL test results

The open loop PE-HIL test results for operating condition of $P_{\mathrm{ac,ref}}$, $P_{\mathrm{dc,ref}}$ = 100 MW are shown in Fig. 8. In this case, the PV-DAB module voltage reference ($V_{\mathrm{cpv,ref}}$) is not sent from MARS L1-L2 controller and is generated from the power command in the L3 controller itself. From Fig. 8e, for

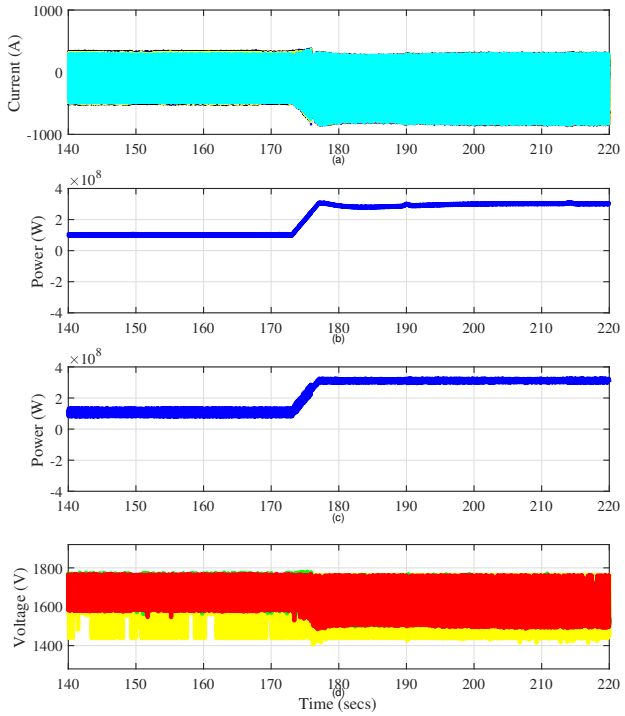

Fig. 7. cHIL test results: a) iarm currents; b) ac-side active power; c) dc-side power; d) different SM voltages (ESS, PV, Normal)

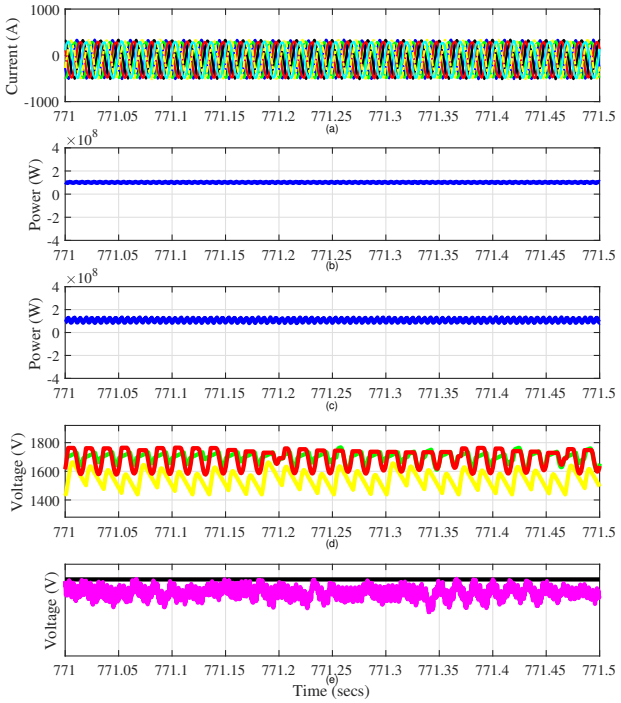

Fig. 8. Open loop PE-HIL test results: a) iarm currents; b) ac-side active power; c) dc-side power; d) different SM voltages (ESS, PV, Normal); e) DAB module $V_{\mathrm{cpv,ref}}$ and $V_{\mathrm{cpv,DAB}}$

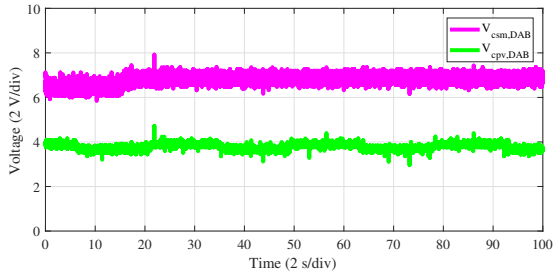

Fig. 9. PV-DAB module states from oscilloscope: $V_{\mathrm{cpv,DAB}}$ and $V_{\mathrm{csm,DAB}}$ on L3 controller for operating condition $P_{\mathrm{ac,ref}}$, $P_{\mathrm{dc,ref}}$ = 100 MW

the given PV power dispatch command, the PV input capacitor voltage ($V_{\mathrm{cpv,DAB}}$) is following its reference $V_{\mathrm{cpv,ref}}$ and is also stable. In addition to the DAB states, from Fig. 8a-d, other states in the system such as iarm currents, different front-end half bridge SM voltages are stable and the ac side power from MARS is following the dispatch commands accurately. Furthermore, the measured data (PV-DAB module states) sent from MARS real-time simulator are also shown in Fig. 9 indicating the stable communication between MARS L3 controller and MARS real-time simulator. A gain of 250 needs to be multiplied to the values observed in Fig. 9 due to the corresponding factor considered while sending the measured values to the DSP.

C. PE-HIL test results

The PE-HIL test results for operating conditions of $P_{\mathrm{ac,ref}}$, $P_{\mathrm{dc,ref}}$ = 100 MW and step change from $P_{\mathrm{ac,ref}}$ = -50 MW, $P_{\mathrm{dc,ref}}$ = -74 MW to $P_{\mathrm{ac,ref}}$ = 250 MW, $P_{\mathrm{dc,ref}}$ = 116 MW are shown in Fig. 10 - Fig. 11. In this case, the MARS L1-L2 controller sends the $V_{\mathrm{cpv,ref}}$ to the L3 controller. After receiving the $V_{\mathrm{cpv,ref}}$ from MARS L1-L2 controller, the L3

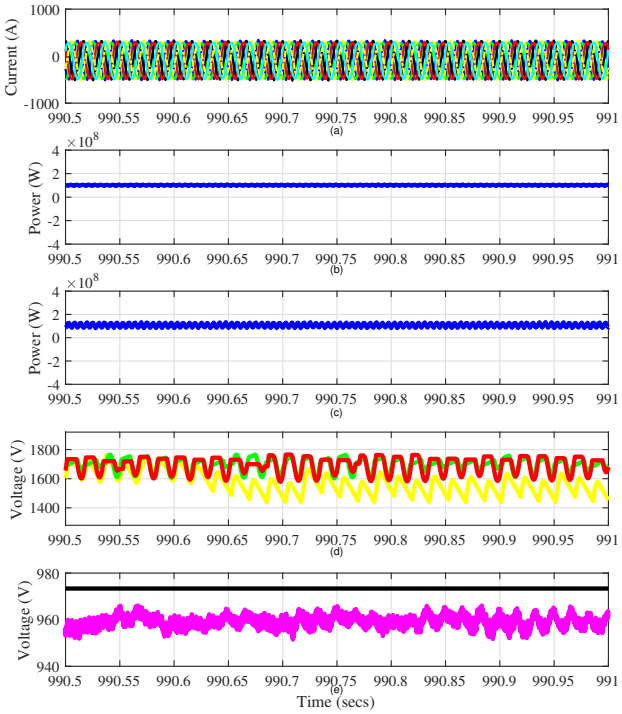

Fig. 10. PE-HIL test results for operating condition of $P_{\mathrm{ac,ref}}$, $P_{\mathrm{dc,ref}}$ = 100 MW: a) iarm currents; b) ac-side active power; c) d- side power; d) different SM voltages (ESS, PV, Normal); e) DAB module $V_{\mathrm{cpv,ref}}$ and $V_{\mathrm{cpv,DAB}}$

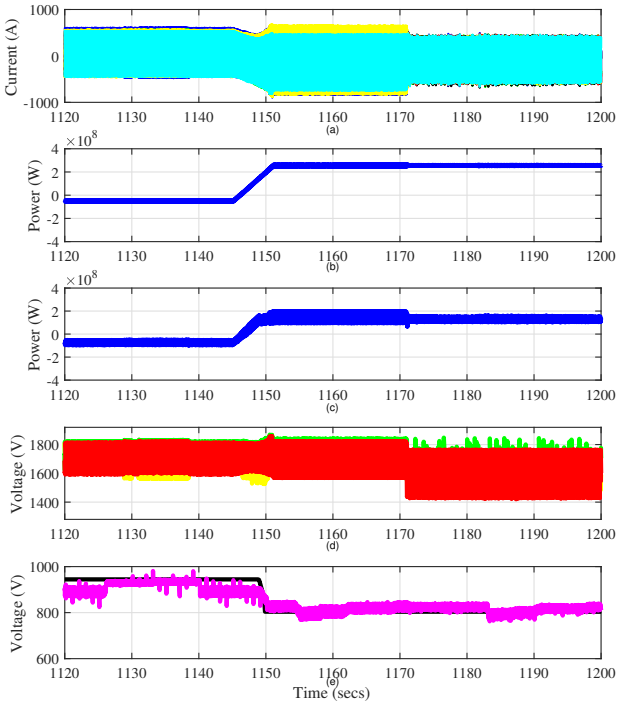

Fig. 11. PE-HIL test results for step change from $P_{\mathrm{ac,ref}}$ = -50 MW, $P_{\mathrm{dc,ref}}$ = -74 MW to $P_{\mathrm{ac,ref}}$ = 250 MW, $P_{\mathrm{dc,ref}}$ = 116 MW: a) iarm currents; b) ac-side active power; c) dc-side power; d) different SM voltages (ESS, PV, Normal); e) DAB module $V_{\mathrm{cpv,ref}}$ and $V_{\mathrm{cpv,DAB}}$

controller sends switching signals to the DAB module in the MARS real-time simulator. The results shown in Fig. 10 - Fig. 12 reinforce the successful evaluation of the PE-HIL testing of MARS system at Pittsburg, CA. From Fig. 10a-d and Fig. 11a-d, it is observed that the dispatch commands

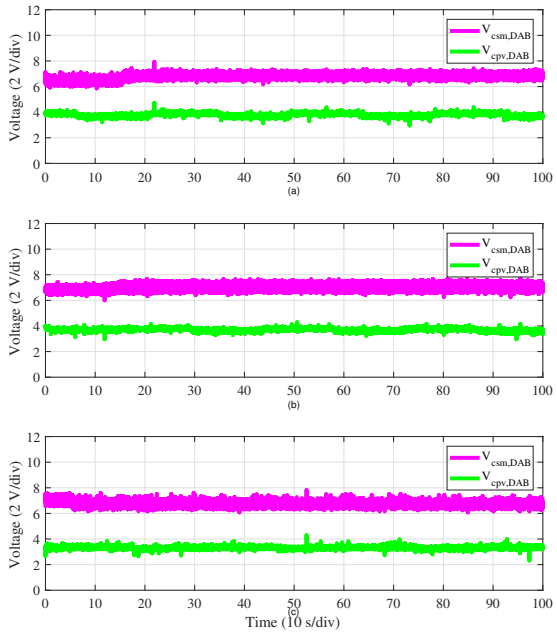

Fig. 12. PV-DAB module states from oscilloscope: $V_{\mathrm{cpv,DAB}}$ and $V_{\mathrm{csm,DAB}}$ on L3 controller for operating conditions a) $P_{\mathrm{ac,ref}}$, $P_{\mathrm{dc,ref}}$ = 100 MW; b) $P_{\mathrm{ac,ref}}$ = -50 MW, $P_{\mathrm{dc,ref}}$ = -74 MW; and c) $P_{\mathrm{ac,ref}}$ = 250 MW, $P_{\mathrm{dc,ref}}$ = 116 MW

for $P_{\mathrm{ac,ref}}$, and $P_{\mathrm{dc,ref}}$ are being accurately followed. In addition, it can be observed that the iarm currents, different front-end half bridge SM voltages are stable and within their respective limits. From Fig. 10e and Fig. 11e, it is observed that the $V_{\mathrm{cpv,DAB}}$ of the PV-DAB module in MARS real-time simulator is following its reference $V_{\mathrm{cpv,ref}}$ (which is sent to L3 controller from MARS L1-L2 controller) closely during steady state and step change conditions. The PV-DAB module states sent to L3 controller from MARS real-time simulator are shown in Fig. 12a-c. From the figure, it can be observed that the $V_{\mathrm{cpv,DAB}}$ and front-end half bridge capacitor voltage of PV DAB module ($V_{\mathrm{csm,DAB}}$) in MARS real-time simulator are stable and within their respective limits. A gain of 250 needs to be multiplied to the values observed in Fig. 12 due to the corresponding factor considered while sending the measured values to the DSP.

V. Conclusions

In this paper, an unique PE-HIL setup to evaluate one PE module's controller with the upper-level controllers in a large-scale PE system is described. The PE-HIL setup is applied to MARS at Pittsburg to evaluate one L3 controller interacting with L1-L2 controllers in MARS. The evaluation helps with characterizing the stability of the hierarchical control system (L1-L2-L3) of MARS and characterize its performance under different operating conditions. It also enables to identify resource constraints in individual controllers and/or challenges with communication (if any) between controllers.

Acknowledgement

Authors would also like to thank Dr. John Seuss from SETO for overseeing the project developments and providing guidance.

References

[1] C. Lin, D. Liu, X. Wu, Z. He, W. Wang, and W. Li, "Setup and performance of a combined hardware-in-loop and software-in-loop test for mmc-hvdc control and protection system," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 1333–1338.

[2] X. Ma, X. Fei, Z. Chu, Z. Li, F. Gao, M. Lei, Z. Wang, W. Wang, P. Wang, and Y. Li, "Full-scale physical control system real-time digital simulator design for mmc-hvdc simulation and testing," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 4518–4523.

[3] G. Li, D. Zhang, Y. Xin, S. Jiang, W. Wang, and J. Du, "Design of mmc hardware-in-the-loop platform and controller test scheme," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 2, pp. 143–151, 2019.

[4] Z. Zhu, X. Li, H. Rao, W. Wang, and W. Li, "Testing a complete control and protection system for multi-terminal mmc hvdc links using hardware-in-the-loop simulation," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 4402–4408.

[5] R. Wierckx and S. Elimban, "Real-time performance of fpga-based mmc valves for hvdc systems," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, 2015, pp. 004 506–004 512.

[6] H. Tu, Y. Du, H. Yu, S. Lukic, M. Metelko, P. Volgyesi, A. Dubey, and G. Karsai, "A hardware-in-the-loop real-time testbed for microgrid hierarchical control," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 2053–2059.

[7] Y. Du, X. Lu, H. Tu, J. Wang, and S. Lukic, "Dynamic microgrids with self-organized grid-forming inverters in unbalanced distribution feeders," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1097–1107, 2020.

[8] S. Debnath, P. R. V. Marthi, Q. Xia, J. Pan, M. Saeedifard, V. N. Vipin, S. Chakraborty, and M. Arifujjaman, "Renewable integration in hybrid ac/dc systems using a multi-port autonomous reconfigurable solar power plant (mars)," vol. 36, no. 1, pp. 603–612, 2021.

[9] S. Debnath, S. Zheng, N. Watson, S. Campbell, R. Zeng, and M. Chinthavali, "Flexible intelligent real-time dc-ac grid emulator (fire): Power electronic hardware-in-the-loop (pe-hil) amplifier," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1060–1067.

[10] S. Debnath and M. Chinthavali, "Mmc-hvdc: Simulation and control system," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8.

[11] W. Li, L.-A. Grégoire, and J. Bélanger, "A modular multilevel converter pulse generation and capacitor voltage balance method optimized for fpga implementation," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2859–2867, 2015.

[12] P. R. V. Marthi, S. Debnath, Q. Xia, and M. Saeedifard, "Advanced models and fast simulation algorithms for mars plants," in *2020 IEEE/PES Transmission and Distribution Conference and Exposition (T D)*, 2020, pp. 1–5.

[13] S. Debnath, Q. Xia, M. Saeedifard, and M. Arifujjaman, "Advanced high-fidelity lumped emt grid modelling & comparison,," *CIGRE Grid of the Future*, 2019.

[14] W. Li, L.-A. Grégoire, S. Souvanlasy, and J. Bélanger, "An fpga-based real-time simulator for hil testing of modular multilevel converter controller," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2088–2094.

[15] W. Li and J. Bélanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time hil test bench," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2401–2409, 2016.

[16] Z. Dong, S. Debnath, W. Li, Q. Xia, P. R. Marthi, and S. Chakraborty, "Real-time simulation framework for hardware-in-the-loop testing of multi-port autonomous reconfigurable solar power plant (mars)," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 3160–3167.

[17] Q. Xia, S. Debnath, P. R. V. Marthi, S. Marti, and M. Saeedifard, "High-fidelity models and fast emt simulation algorithms for isolated multi-port autonomous reconfigurable solar power plant (mars)," in *2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2021, pp. 1–7.