SAND2022-17068R

U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Electrification

2022 Annual Progress Report

Vehicle Technologies Office

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

(This page intentionally left blank)

I Electric Drive Technologies

I.1 Electric Drive Technologies Research

I.1.1 Power Electronics: Vertical GaN Device Development (Sandia National Laboratories)

Andrew Binder, Principal Investigator
Sandia National Laboratories
P.O. Box 5800, MS 1086
Albuquerque, NM 87185
E-mail: abinder@sandia.gov

Susan Rogers, DOE Technology Development Manager
U.S. Department of Energy
E-mail: susan.rogers@ee.doe.gov

Start Date October 1, 2018: End Date: September 30, 2024
Project Funding (FY22): $800,000 DOE share: $800,000 Non-DOE share: $0

Project Introduction

This project is part of a multi-lab consortium that leverages U.S. research expertise and facilities at national labs and universities to significantly advance electric drive power density and reliability, while simultaneously reducing cost. The final objective of the consortium is to develop a 100 kW traction drive system that achieves 33 kW/L, has an operational life of 300,000 miles, and a cost of less than $6/kW. One element of the system is a 100 kW inverter with a power density of 100 kW/L and a cost of $2.7/kW. New materials such as wide-bandgap semiconductors, soft magnetic materials, and ceramic dielectrics, integrated using multi-objective co-optimization design techniques, will be utilized to achieve these program goals. This project focuses on a subset of the power electronics work within the consortium, specifically the design, fabrication, and evaluation of vertical GaN power devices suitable for automotive applications.

Objectives

Gallium Nitride (GaN) is a promising wide-bandgap (WBG) semiconductor material that could enable higher-performance power electronic devices than traditional Silicon (Si) or even its WBG counterpart, Silicon Carbide (SiC). This is based on the increased critical electric field of GaN, which would enable lower-resistance devices with the same hold-off voltage as devices fabricated from the other materials. This is a key performance metric for power devices. Laterally-oriented, High Electron Mobility Transistors (HEMTs) based on AlGaN and GaN materials are common in high-frequency applications and are being established in lower-voltage power switching applications (approximately 600 V and below). However, with the emerging commercial maturation of GaN substrates, traditional vertically-oriented device structures (such as are common in Si and SiC) can now be realized in GaN, with several promising demonstrations of high-voltage pn diodes and vertical transistors appearing in the literature [1]–[3]. While GaN pn diodes may be of interest, the ~3 V turn-on voltage, determined mainly by the bandgap of the material, discourages their use in some power-switching circuits due to the loss of power conversion efficiency resulting from this high turn-on voltage. Instead, more promising candidates for these power conversion systems, including automotive inverters, are GaN Schottky barrier diodes (SBDs) and Junction Barrier Schottky (JBS) diodes, shown in Figure I.1.1.1 (a), which have turn on voltages of ~1 V as determined by the Schottky barrier height of the metal to the semiconductor material, rather than the semiconductor bandgap.

Similarly, vertically-oriented GaN transistors promise high-performance as power electronic devices if several key growth and fabrication challenges are overcome for the GaN material system. Interestingly, several different types of vertical GaN transistors have been demonstrated including Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) in the trench configuration (T-MOSFET, shown in Figure I.1.1.1 b), the double-well

(D-MOSFET) configuration (shown in Figure I.1.1.1 c), and the Current Aperture Vertical Electron Transistor (CAVET) configuration [4]–[6]. Each of these device topologies has benefits and challenges associated with fabrication and performance, but the MOSFET designs show the most promise for power switching applications and are being investigated during this effort. With the MOSFET device designs, challenges exist in making the semiconductor/insulator (or oxide) interface due to the lack of a good native oxide for GaN (Si and SiC both have native oxides). In addition, selective-area doping control, which is needed to form lateral pn junctions, cannot be easily achieved in GaN. Current state-of-the-art GaN devices use techniques such as ion implantation with special anneal processes (high-pressure and high-temperature) [7] or epitaxial regrowth [8] to realize selective-area doping control. Both techniques are relatively immature in GaN, and their behavior needs to be studied and techniques need to be developed to control these processes for eventual use in power systems for electric vehicles.

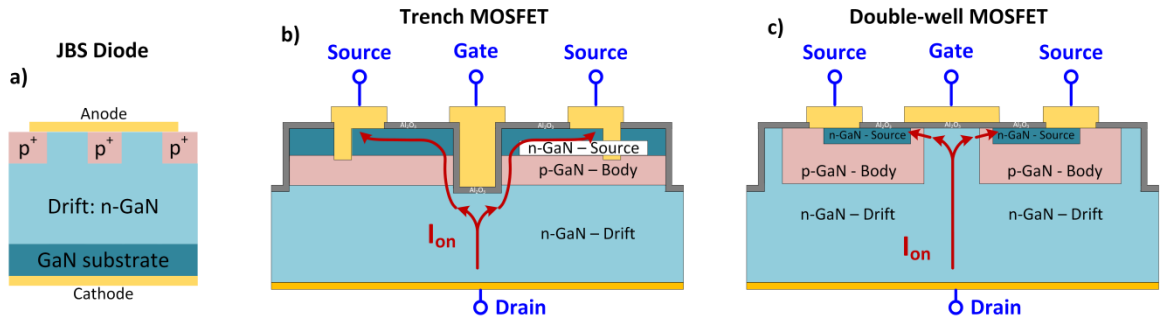

Figure I.1.1.1. (a) Schematic drawing of JBS diode, (b) schematic drawing of Trench MOSFET, and (c) schematic drawing of a Double-well MOSFET.

The first year of this effort focused on the development of simulation and modeling capabilities to help drive the designs of future GaN diodes and transistors. In parallel, epitaxial growth and fabrication processes were initiated toward realizing and demonstrating these devices. The second year of this effort has focused on fabrication and a first-generation demonstration of these devices. With demonstrators for both the JBS and trench MOSFET complete, the third year of the program focused on improving the baseline performance by improving passivation quality, tackling challenges related to etch-and-regrowth, and improving off-state characteristics for both the JBS and MOSFET devices. This year's effort is focused again on improving baseline performance. These efforts resulted in doubling the MOSFET blocking voltage, further improvements in etch-and-regrowth processes, and an optimization for the edge termination process. In the future, once devices of sufficient performance are achieved these will be further characterized in a performance and reliability test-bed (created under a different project within the consortium) to evaluate their suitability for electric drive applications, especially regarding their ability to meet the DOE consortium targets. Also, with increasing maturity, the devices can be shared with the consortium partners, who will evaluate them in electric drive systems and provide feedback to us for further improvement in their performance for power electronics.

Approach

The focus of this past year has been on improving baseline performance for both the JBS and MOSFET device. In many cases, challenges faced by both devices can more easily be addressed through cycles of learning on a simpler device. For instance, the pn diode platform can be used to benchmark passivation quality and to evaluate edge termination effectiveness, a simple Schottky Barrier diode can be used to understand the influence of etch damage and etch-damage recovery procedures on n-type GaN, and the MOSCAP can be used to evaluate gate dielectric performance on m-plane GaN. Experiments on these three devices were heavily leveraged in the past year to improve device performance for the JBS and MOSFET platforms. Examples of the three devices are shown in Figure I.1.1.2.

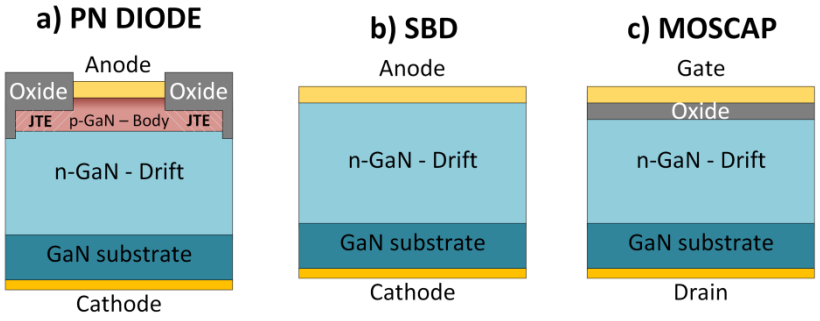

Figure I.1.1.2. Studies on these three devices, the pn diode, the Schottky Barrier diode, and the MOSCAP lends insight into improving performance for the JBS and MOSFET devices.

Results

Vertical GaN PN Diodes

Last year (FY21) we established a new passivation process for GaN pn diodes using a bilayer film consisting of 100 nm of atomic layer deposited (ALD) alumina (Al_2O_3) and 2 µm of silicon nitride (SiN) by plasma enhanced chemical vapor deposition (PECVD). Compared to early attempts to establish a passivation process, this new film resulted in low leakage diodes and the ALD-Al_2O_3 film appears robust to the addition of PECVD-SiN as a subsequent layer. This bilayer passivation has been robust across multiple device lots and has even been successfully deployed to other diode projects at Sandia. With a new and robust passivation process established, it is critical to consider how the passivation can affect the edge termination and breakdown performance of the device. When examining reverse IV curves from a select few devices, it is apparent at first glance that the addition of a passivation film causes a reduction in breakdown voltage as seen in Figure I.1.1.3a. Further statistical analysis demonstrates a similar trend, where three varieties of passivation all established a nominal reduction in breakdown voltage of 300V compared to the unpassivated sample (Figure I.1.1.3b). According to theory, a 200-300 V drop in breakdown voltage corresponds with a reduction of charge of 4×10^{12} cm^{-2} in the step-etched JTE (junction termination extension) which is a reasonable amount of charge to expect at the

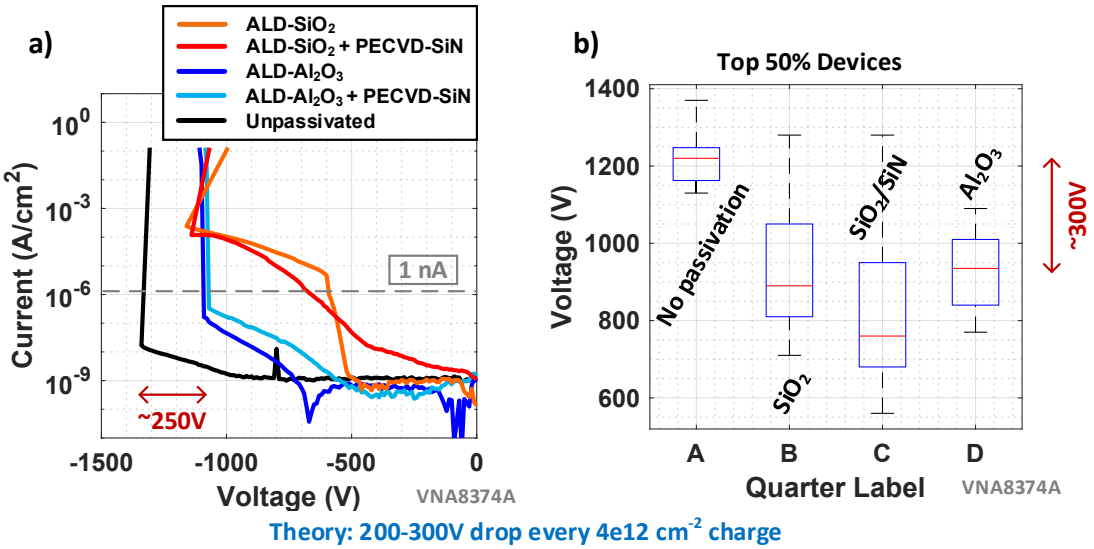

Figure I.1.1.3. Sandia's recent progress for GaN passivation and the impact passivation has on breakdown voltage: showing (a) the reverse IV performance for diodes with various passivations, and (b) the statistical breakdown for the top 50% of yielding devices. Note, all devices are tested under flourinert during high voltage testing.

interface between the passivation and semiconductor and is consistent with some preliminary models and data from the GaN MOSFET and MOSCAP work.

The results from the passivation work highlights a need to optimize the design of the edge termination to account for non-idealities such as the charge from the passivation, epitaxy and doping variations, and other factors that impact the effectiveness of the edge termination. An edge termination is designed to minimize and distribute the peak electric field at the edge of the device where the junction has been terminated. In the case of a step-etched JTE, proper management of the surface electric field requires precise control of the charge in the JTE. This charge is set primarily by the product of doping and thickness for the JTE but many factors can alter the charge in the JTE including charge from the passivation layer as seen in Figure I.1.1.3. According to theoretical calculations the breakdown voltage can be quite sensitive to the dose in the JTE, and when considering the unknowns, it is near impossible to know the optimal etch depth to achieve the required dose. Therefore, we ran a multivariable JTE experiment to pinpoint the optimal JTE thickness target. These results presented are the first multipoint step-etched JTE study reported in GaN. The diode and single-zone step-etched JTE are presented in Figure I.1.1.4a. Three experiments were carried out on separate quarters of the same wafer, each with a different JTE etch depth target. The statistical data shown in Figure I.1.1.4b represents the results after screening for yield of the top 50% of devices with the highest breakdown. This data demonstrates a clear trend of increasing breakdown voltage with increasing JTE thickness. Compared to the simulation data (Figure I.1.1.4c), the shape of the data matches well to a theoretical prediction with some offset in terms of total charge (shift in the x-axis). This data serves to guide future designs and indicates a shift in total dose of approximately 1×10^{13} cm^{-2} to reach the optimal JTE target compared to an ideal simulation scenario. This shift is consistent with several non-ideal conditions such as: (1) plasma damage on the surface from ICP etching, (2) non-idealities in the doping profile near the junction, (3) surface charge, and others. The results of this study clearly highlight the need to account for these non-idealities when designing the edge termination, and the impact on breakdown voltage as a direct result of the quality of the termination strategy.

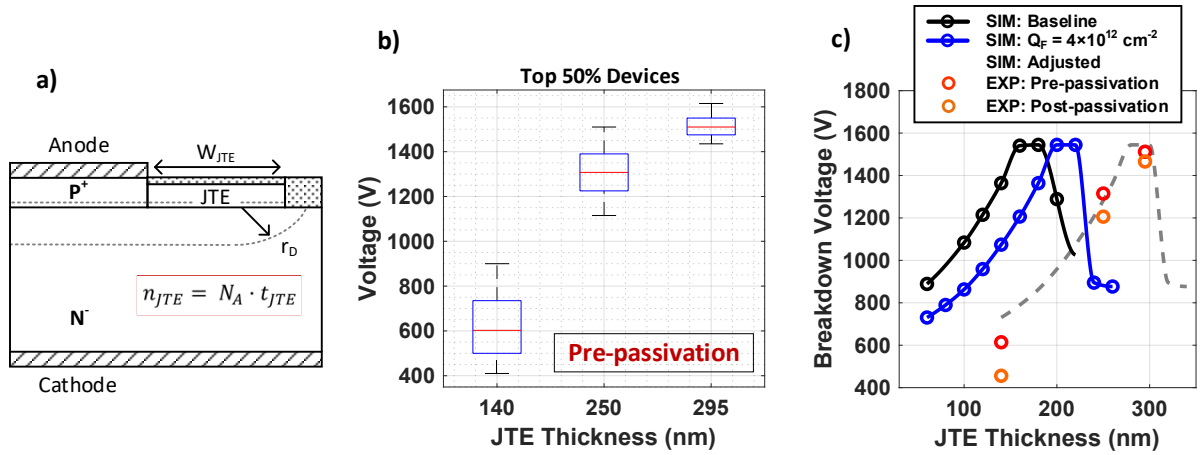

Figure I.1.1.4. A diagram of the single-zone step-etched JTE is shown in (a) and is the baseline device for the etch depth experiment. After screening for yield, a statistical representation of the top 50% highest breakdown devices is shown in (b). This data is then superimposed with simulation data in (c) demonstrating an excellent match to the theoretical data with an offset in the x-axis representing a difference in total charge.

Vertical GaN Schottky Barrier Diodes

The vertical GaN Junction Barrier Schottky (JBS) process that we are developing utilizes an etch-and-regrowth process to form the selective-area doped regions. Similarly, advanced trench-MOSFET and double-well MOSFETs require one or more selective-area doped regions. This selective-area doping process by etch-and-regrowth generally results in a junction with considerably more leakage than a continuously grown sample. To tackle this challenge, we have been developing a process that can reduce the etch damage that contributes to leakage. Last year we showed considerable success in removing residual ICP etch damage for Schottky Barrier

diodes. This year we have worked towards finding a solution that results in etched-and-regrown PN diodes with low reverse leakage current. Although our understanding of the etch-and-regrowth process has improved, we are still working to identify a process that can improve on the leakage characteristic compared to what was shown for our JBS devices in Ref. [9]. This effort is expected to continue into the next year.

Vertical GaN MOSFETs

In the previous years we demonstrated a 1st generation process for the vertical GaN trench MOSFET, then identified several key challenges [10] to address based on that result. Last year we demonstrated a 2nd generation gate dielectric process that improved on the leakage and breakdown strength for ALD-SiO_2 gate dielectrics. This year we incorporated all those revisions into the 2nd generation MOSFET process resulting in doubling the MOSFET blocking voltage. The first generation MOSFETs suffered from surface and channel leakage that dominated the off-state characteristics and resulted in a 250V breakdown with high leakage current. Revisions to the design and incorporation of new processes developed in the last year resulted in a 500V breakdown with nearly six orders of magnitude reduction in leakage current (Figure I.1.1.5 a). Failure at 500V is attributed to rupture of the gate dielectric at the bottom of the trench due to high electric-fields during the blocking state as depicted in Figure I.1.1.5 b. This is in agreement with TCAD modeling which predicts that for a device with an avalanche voltage of 1400V, an early failure will occur in the 450-550V range due to high fields in the gate dielectric at the trench bottom (Figure I.1.1.5 c). The agreement between TCAD and experimental results is a positive outcome which highlights that many early failure points for the MOSFET have been solved and the device behavior is as expected. From this point the blocking voltage can be further improved by applying conventional rules of scaling.

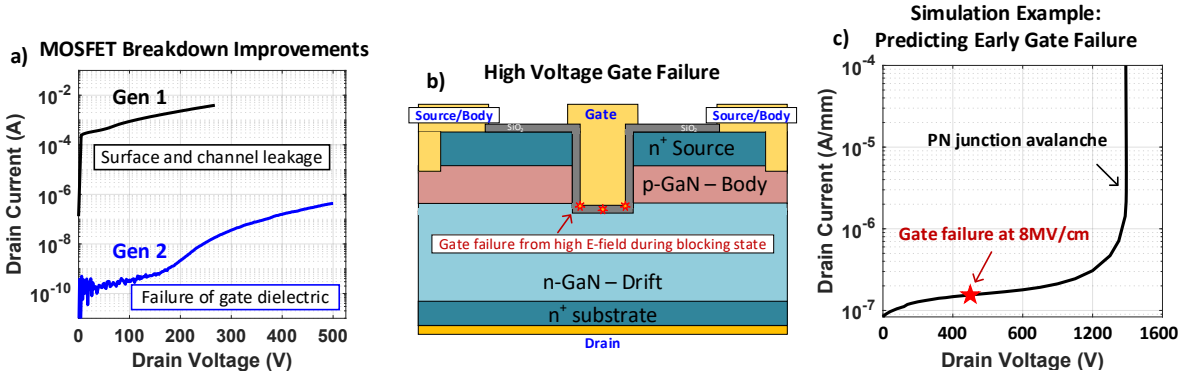

Figure I.1.1.5. Generational improvements for the MOSFET continue, showing (a) a doubling of breakdown voltage from generation 1 to generation 2 and several orders of magnitude reduction in leakage current. The failure point of the new generation of MOSFETs is due to failure of the gate dielectric at the bottom of the trench (b). TCAD simulations (c) show good agreement with failure mechanism and give insight into improving breakdown voltage further.

Several techniques can be employed to improve breakdown voltage for future MOSFET generations. First, the magnitude of electric-field strength in the gate dielectric below the trench is proportional to the depth that the trench protrudes below the body/drift pn junction. To ensure the trench etch fully penetrates through the junction we use a margin of 10% over-etch into the drift. For our 1st generation epitaxy design with a source and body total thickness of 1.7 µm the over-etch into the drift is on average 170 nm. If the combination of the source and body thickness is reduced, then the over-etch can be reduced and the field-strength in the gate dielectric will be less for the same applied blocking voltage. Additionally, reducing the thickness of the p-GaN body layer reduces the channel length, which is a significant portion of the total device resistance. For these reasons we have designed a 2nd generation epitaxy design (Figure I.1.1.7) with a total source and body thickness of 700 nm, half the body thickness of the 1st generation epi, and 40% of the total source and body thickness. This brings the trench over-etch depth target from 170 nm in gen-1 epi to 70 nm in gen-2 epi which will serve to reduce high electric-fields in the gate dielectric.

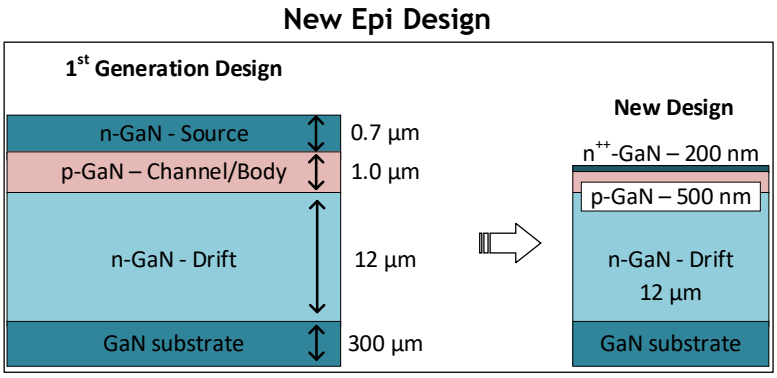

Figure I.1.1.7. MOSFET epitaxy has been redesigned to accommodate a thinner channel region, and a more highly doped and thinner n-GaN source region. This will not only improve on-state performance metrics but allows for better tolerance on the trench etch which will improve breakdown voltage when the etch depth past the channel is minimized.

Although the breakdown voltage can be improved by reducing trench etch depth below the junction, or by over designing the drift region by lowering doping and increasing thickness, the better method is to design a structure that will protect the gate dielectric from high electric-fields during blocking. Due to difficulty of selective-area doping in GaN, conventional techniques for forming a structure to protect the gate dielectric are not viable. We developed a new method to form a buried field shield by an etch-and-regrowth process. This field shield serves to protect the gate dielectric during the blocking state from high electric fields. The method devised is outlined in the provisional patent [11] and an example of one possible topology of the field shield is shown in Figure I.1.1.6. This structure relies heavily on our developed etch-and-regrowth processes, and as such it will be difficult to demonstrate until the etch-and-regrowth process matures. However, this method is in theory one of the best ways to protect the gate and to achieve the theoretical maximum performance from GaN.

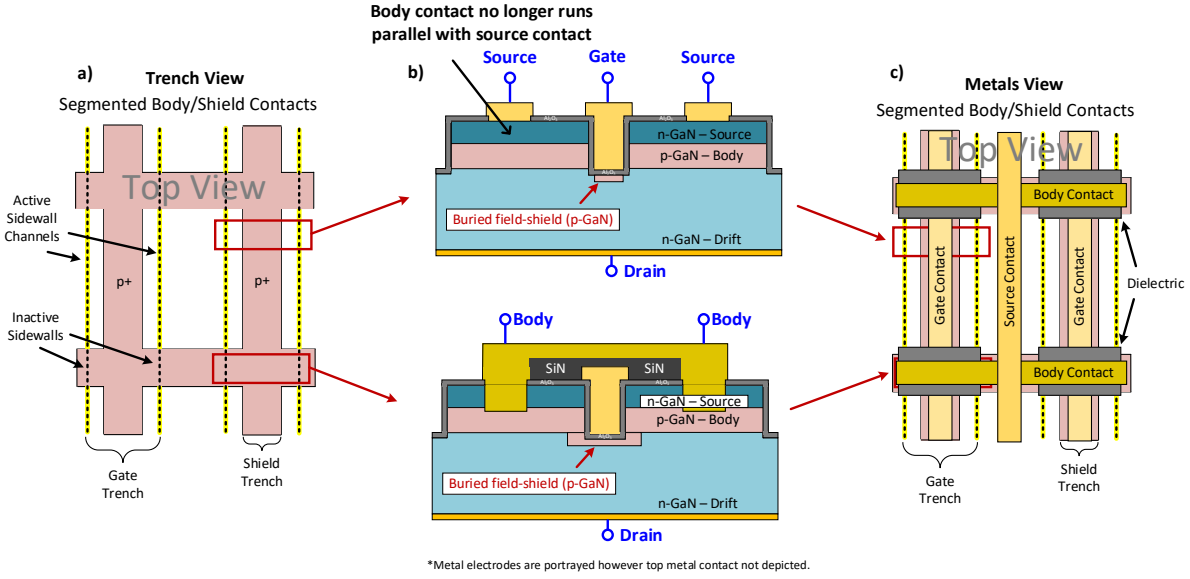

Figure I.1.1.6. Method for forming a buried field shield via etch and regrowth showing a) the trench view, b) the cross-section view, and c) the metals view of a segmented body contact approach. More details are available in Ref. [11].

Conclusions

GaN offers the promise of power electronic devices with performance that exceeds conventional Si and even SiC-based devices. This is due to its advantageous material properties, chiefly its higher breakdown electric field. Due to the increased maturity of GaN substrates, vertical GaN devices showing promising performance are being demonstrated and are being considered for insertion into power conversion applications. This project has focused on the design, simulation, and fabrication processes needed to build vertical GaN diodes and transistors for use in electric drive traction systems. This year we developed a process for edge termination in vertical GaN power devices and our group is the first to report a multipoint fit from theory to experiment, which serves to mark a milestone of maturity for these devices. For the GaN MOSFET the second-generation device demonstrated double the blocking voltage (500 V) compared to the previous generation and a reduction of leakage current by six orders of magnitude. The groundwork has been set to increase blocking voltage further for next device generations, including a new method for protecting the gate dielectric by way of an etched-and-regrown buried field shield. With substantial improvements in device maturity, especially for GaN diodes, we anticipate an increased effort for device packaging and evaluation of packaged parts performance next year.

Key Publications

1. A. Binder and J.A. Cooper, "Buried Field Shield in GaN Trench MOSFETs via Etch and Regrowth," US Provisional Patent 63/208,119.
2. A. T. Binder *et al*., "Etched and Regrown Vertical GaN Junction Barrier Schottky Diodes," in *The 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2021),* 2021.
3. C. E. Glaser, A. T. Binder, L. Yates, A. A. Allerman, D. F. Feezell, and R. J. Kaplar, "Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices," in *The 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2021),* 2021.
4. L. Yates, A. Binder, J. Dickerson, G. Pickrell, and R. Kaplar, "Electro-thermal Simulation and Performance Comparison of 1.2 kV, 10 A Vertical GaN MOSFETs," Rio Grande Symposium on Advanced Materials, Albuquerque, NM (September 2019).

References

[1] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical power p-n diodes based on bulk GaN," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 414–422, Feb. 2015.

[2] A. Armstrong *et al.*, "High voltage and high current density vertical GaN power diodes," 2016.

[3] H. Ohta, K. Hayashi, F. Horikiri, M. Yoshino, T. Nakamura, and T. Mishima, "5.0kV breakdown-voltage vertical GaN p-n junction diodes," *Jpn. J. Appl. Phys.*, vol. 57, no. 4, pp. 4–09, 2018.

[4] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV," *Appl. Phys. Express*, vol. 7, no. 2, p. 021002, Feb. 2014.

[5] H. Otake, S. Egami, H. Ohta, Y. Nanishi, and H. Takasu, "GaN-based trench gate metal oxide semiconductor field effect transistors with over 100cm2/(Vs) channel mobility," *Japanese J. Appl. Physics, Part 2 Lett.*, vol. 46, no. 25–28, p. L599, Jul. 2007.

[6] S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, "CAVET on bulk GaN substrates achieved with MBE-regrown AlGaN/GaN layers to suppress dispersion," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 41–43, Jan. 2012.

[7] T. J. Anderson *et al.*, "Activation of Mg implanted in GaN by multicycle rapid thermal annealing," *Electron. Lett.*, vol. 50, no. 3, pp. 197–198, Jan. 2014.

[8] G. W. Pickrell *et al.*, "Regrown Vertical GaN p–n Diodes with Low Reverse Leakage Current," *J. Electron. Mater. 2019 485*, vol. 48, no. 5, pp. 3311–3316, Mar. 2019.

[9] A. T. Binder *et al.*, "Etched and Regrown Vertical GaN Junction Barrier Schottky Diodes," in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2021, pp. 288–292.

[10] C. E. Glaser, A. T. Binder, L. Yates, A. A. Allerman, D. F. Feezell, and R. J. Kaplar, "Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices," in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2021, pp. 268–272.

[11] A. Binder and J.A. Cooper, "Buried Field Shield in GaN Trench MOSFETs via Etch and Regrowth," US Provisional Patent 63/208,119.

Acknowledgements

This work is supported by the DOE Office of Energy Efficiency and Renewable Energy, Vehicle Technologies Office. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. The views expressed in the article do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

(This page intentionally left blank)

U.S. DEPARTMENT OF
ENERGY

Office of
ENERGY EFFICIENCY &
RENEWABLE ENERGY

For more information, visit:
energy.gov/vehicles

DOE/EE-#### April 2022