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Understanding the Initial Stages of Time Dependent Dielectric Breakdown in Si/SiO_2 MOSFETs Utilizing EDMR and NZFMR

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***Abstract*— We investigate the initial stages of time-dependent dielectric breakdown (TDDB) in high-field stressed Si/SiO_2 MOSFETs via electrically detected magnetic resonance (EDMR). As anticipated, we find that the defects dominating the initial stages of TDDB include silicon dangling bonds at the (100) Si/SiO_2 interface (P_{b0} and P_{b1} centers). We find that the densities of these defects increase with stress time. With similar stressing and optimized measurement temperature, we do observe EDMR of generated oxide defects known as E' centers. The results indicate that the initial stages of TDDB in the Si/SiO_2 system involves a rate limiting step of tunneling between a silicon dangling bond and an oxide defect. Additionally, we have made near-zero field magnetoresistance spectroscopy measurements, which show clear differences with stressing time; these differences are almost certainly due to a redistribution of hydrogen atoms in the oxide.**

Keywords*— *silicon dioxide, electrical stressing, TDDB, EDMR, NZFMR, SILC, interface traps, MOSFET.

I. Introduction

The reliability of SiO_2 films in metal oxide semiconductor (MOS) technology is a major concern for device manufacturers. Accelerated reliability tests—such as high constant-voltage stressing and voltage ramping—are routinely used to simulate aging of MOS oxides through statistical analysis of oxide breakdown conditions. This time-dependent dielectric breakdown (TDDB) phenomenon is one of the most important reliability problems in solid-state electronics [1-4].

As device structures age, whether it be through use or due to accelerated high-field stressing, their leakage current characteristics as a function of gate bias will change. For the most part, the leakage currents due to TDDB will have two main components associated with different tunneling mechanisms: trap-assisted tunneling and Fowler-Nordheim tunneling [3,4]. At lower values of applied electrical field, the leakage currents will be dominated by trap-assisted tunneling, in which charge tunnels through energy minima due to deep-level traps scattered throughout the oxide. As the oxide is damaged throughout high-field stressing, the amount of these traps increases [4], resulting in a higher amount of leakage current at equivalent values of electric field in comparison to unstressed devices, known as stress-induced leakage current (SILC). At higher values of applied electrical field, band-bending in the oxide will reach a point at which the TDDB process will begin; at this time, the tunneling current through the oxide will decrease in magnitude throughout the lifetime of the device [5]. This phenomenon can be seen in the constant voltage stressing characteristics shown in Fig. 1.

While there is plenty of literature demonstrating the purely electronic aspects of these phenomena in high-field stressed Si/SiO2, the atomic-scale physical and chemical phenomena for TDDB in oxides is not yet fully understood. Arguably, the most powerful method for identifying the chemical and physical nature of electrical defects in semiconductor devices is electrically detected magnetic resonance (EDMR). EDMR operates on the same physical principles as conventional

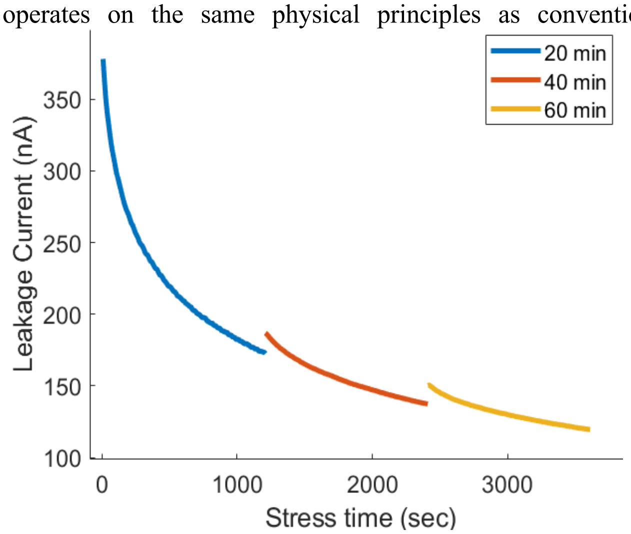

Fig. 1. Leakage current characteristics for the Si/SiO_2 MOSFET stressed at a constant gate bias of -9 V, demonstrating the trapping of charge throughout the TDDB process in Si/SiO_2. As the stress bias is removed to run the EDMR experiments, some positive charge leaves the oxides, which leads to the discontinuities in the leakage current.

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electron paramagnetic resonance (EPR) [6] in that the defect identification takes place through observation of the effects of spin-orbit coupling and electron-nuclear hyperfine interactions on the magnetic resonance spectra of the defects involved. EDMR differs from EPR in its detection scheme. It directly measures spin-dependent phenomena via changes in device current or voltage. EDMR is much more sensitive than conventional EPR: it can detect 1000 or fewer defects in a device structure under study [7], whereas conventional EPR sensitivity requires a minimum of about ten billion defects under ideal circumstances.

In this study, we utilize EDMR via spin dependent trap assisted tunneling (SDTAT) [8,9,11] and spin dependent recombination (SDR) [7,10,12]. SDTAT exploits the spin dependence of trap assisted tunneling; the flipping of spins at the resonance condition allows for once forbidden tunneling events to occur. SDR involves the spin dependence of recombination through deep level defects. By flipping electron spins at the defects, previously forbidden recombination can occur, causing a change in device current. In addition, we utilize a new related spectroscopic technique: near-zero field magnetoresistance (NZFMR) spectroscopy [10]. The NZFMR measurement can provide information about electron-nuclear hyperfine interactions, as well as the kinetics of trap-to-trap tunneling and electron-hole recombination [11].

The biasing scheme used for the SDR measurements was the Fitzgerald-Grove gated diode technique, commonly referred to as the dc I-V technique [13]. In the dc I-V approach, the body is held at virtual ground and the source/drain to body diodes are slightly forward biased to inject minority carriers into the channel, while the gate is swept from inversion to accumulation. At a certain gate voltage, the source/drain to body current will reach a maximum value, corresponding to a maximum recombination of traps at the interface. This peak in the current is given by the expression:

$$\Delta I_{DCIV} = \frac{1}{2} q n_i \sigma v_{th} D_{it} A q |V_f| \exp\left(\frac{q|V_f|}{2k_B T}\right), \quad (1)$$

where D_{it} is the density of traps per unit area near the middle of the silicon band gap at the Si/SiO_2 interface as a function of the source/drain forward bias V_f, n_i corresponds to the intrinsic carrier concentration, σ is the geometric mean of the capture cross section for holes and electrons, A is the gate area, and v_{th} is the thermal velocity. The values of q, k_B, and T correspond to the elementary charge, Boltzmann's constant, and absolute temperature, respectively. The use of the dc I-V technique allows for the calculations of interface trap densities within the high-field stressed devices, allowing for a quantitative measure of the defect densities measured in the EDMR experiments.

II. Experimental

The devices used in this study were Si/SiO_2 n-type MOSFET structures with 7.5 nm thick oxides. The MOS structures consisted of 126 devices, with 15 µm × 1 µm channel dimensions. During stressing and SDTAT, these devices were shorted at the drain, source, and substrate. High-field stressing and electrical characterization of these devices were accomplished using a Hewlett-Packard 4145A Semiconductor Parameter Analyzer. The high-field SDTAT and SDR measurements were done on a custom-modified spectrometer outlined elsewhere [8,12]. Likewise, the NZFMR measurements were made on another custom-built low-field spectrometer [11]. Low temperature measurements were accomplished using a Bruker ER 4111 VT IBM Instruments Variable Temperature Unit with liquid nitrogen.

III. Results

The leakage current vs. time characteristics for the -9 V high-field stress can be seen in Fig. 1. The dc I-V experimentally calculated interface density measurements for these stressing conditions are shown in Table 1 (corresponding to the density of states near mid-gap). Comparisons of high-frequency SDTAT EDMR results on an array of Si/SiO_2 devices for various stress times at a constant bias of – 9 V is shown in Fig. 2. The dc I-V EDMR results at 200 K are shown in Fig. 3. In all EDMR measurements, devices were oriented with magnetic field perpendicular to the (100) interface plane. Comparisons of NZFMR dc I-V measurements for a Si/SiO_2 MOSFET at various stress times is shown in Fig. 4. NZFMR SDTAT spectra at various gate biases for a device stressed for an hour at -9 V are shown in Fig. 5.

Table I
Calculated interface trap densities using Dc I-V

	Unstressed	20 min	40 min	60 min
Mid-gap D_{it} (10^{11} cm^{-2} eV)	.117	10.9	14.8	18.2

Interface trap densities near the middle of the band gap for the unstressed, 20 min, 40 min, and 60 min constant gate voltage stressed device (-9 V).

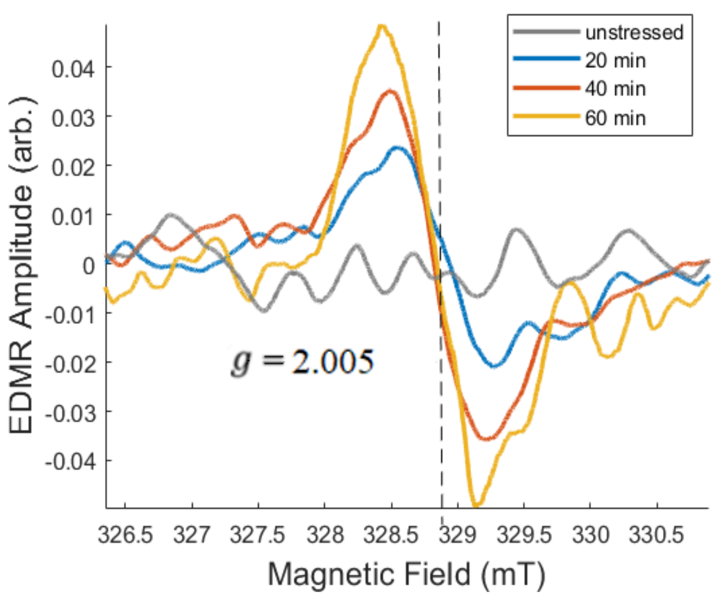

Fig. 2. SDTAT EDMR comparisons of Si/SiO_2 MOSFETs stressed at -9 V for 20, 40, and 60 minutes. The dominating defect are P_b center—silicon dangling bonds at the (100) interface — with a zero-crossing $g \approx 2.005$. This signal is almost certainly dominated by the P_{b0} center: the measured linewidth and existence of the P_{b1} in our SDR data suggests a weaker P_{b1} contribution.

IV. Discussion

The SDTAT EDMR measurements on the unstressed devices in Fig. 2 were below our detection limit. As the devices were high-field stressed for increasing periods of time, a signal began to resolve corresponding to a zero-crossing g=2.0050. With the magnetic field perpendicular to the (100) interface plane, this signal is due to a response from silicon dangling bonds known as P_b centers: almost certainly the (100) interface P_{b0} ($g = 2.0059$) and a potential P_{b1} ($g = 2.0032$) center contribution [14,15].

As the high-field stressing time increased, the signal amplitude of the SDTAT response also increased. Perhaps surprisingly, the increase in amplitude of the SDTAT P_b center response is consistent with the measured dc I-V interface densities for the stress times provided in Table 1. As shown elsewhere, the SDR P_b response from the dc I-V EDMR measurements show a comparable increase [12]. The pre-stress interface density for these devices were nearly two orders of magnitude below the high-field stressed interface densities, whereas the difference between the 20 min, 40 min, and 60 min high-field stressed devices were within a factor of two. The drastic change in interface densities between the unstressed and high-field stressed device is consistent with our observation of rapid interface defect generation in MOSFETs in the early stages of TDDB [4,12].

Unfortunately, due to the much lower sensitivity of the SDTAT measurement in these devices, it is difficult to make an accurate quantitative assessment of the amplitudes of the resonant spectra. EDMR is made more powerful through the use of signal averaging, but due to the low levels of leakage currents in these devices, it was still difficult to fully resolve the spectra over the course of days. However, the clear increase in interface signal amplitude throughout the duration of the high-field stressing does qualitatively correspond with our calculated interface densities with respect to stress time.

The dc I-V spectra for a high-field stressed device at 200 K is shown in Fig. 3. Like the SDTAT spectra, the low-temperature dc I-V spectra contains both the P_{b0} and P_{b1} signal at $g = 2.0065$ and $g = 2.0032$, respectively. However, there is an additional response located at g=2.000 corresponding to what could only be an E' center [16,17]. It should be noted that this g-value is slightly lower than what is generally reported in literature (g = 2.0007). However, this deviation is most likely due to the significant overlap of the E' center response with the larger amplitude P_{b1} center, which would result in a 'shift' of the perceived observation of the zero-crossing magnetic field.

As previously mentioned, the dc I-V biasing scheme is only sensitive to defects very near the interface. For this measurement to detect an E' center response—the E' centers can exist anywhere in the oxide—there must be a significant amount of E' centers being generated throughout the oxide from the high-field stressing. However, this result is not clear from the SDTAT spectra; the SDTAT results in Fig. 2 clearly show that the dominant defect in the SDTAT EDMR response is the interface silicon dangling bonds. This result is perplexing, considering that the physical process involved in SDTAT is trap-assisted tunneling throughout oxide states.

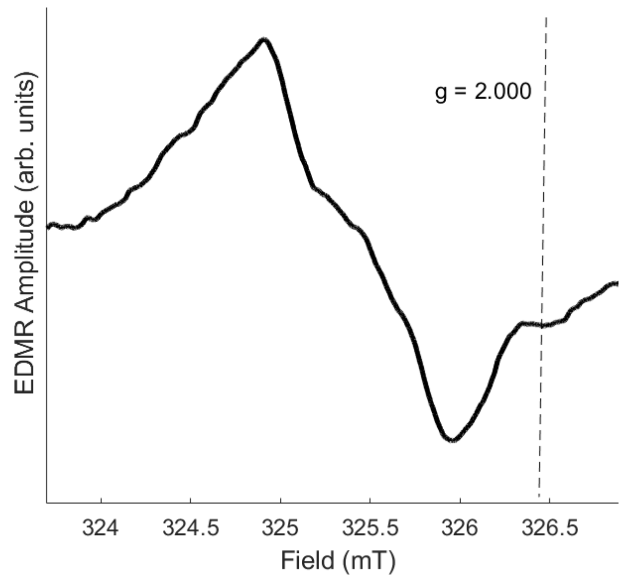

Fig. 3. SDR EDMR results at 200 K for a high-field stressed Si/SiO_2 MOSFET that with an additional E' center (g = 2.000) response at the interface.

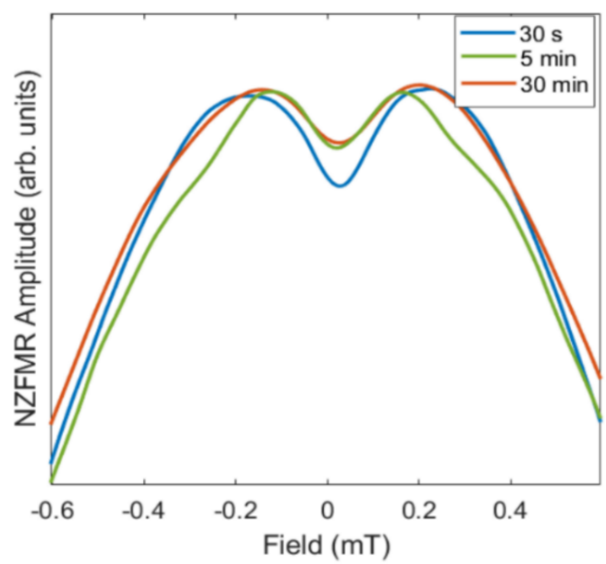

Fig. 4. Comparisons of the integrated NZFMR dc I-V response in Si/SiO_2 MOSFETs stressed at -9 V for 30 seconds, 5 minutes, and 30 minutes. The changes in the central response is due to changes in the hyperfine interactions near the interface due to the duration of the high-field stress, indicating a redistribution of hydrogen throughout the stressing process.

Previous EPR experiments on high-field stressed Si/SiO_2 have demonstrated that high-field stressing results in the generation of E' centers [17]. Additionally, electrical characterization of leakage currents in Si/SiO_2 MOSFETs clearly show an increase in trap-assisted-tunneling events due to high-field stressing [1-3]: a result that must involve the generation of oxide traps [4]. And lastly, the low-temperature dc I-V results on these structures indicate that E' defects within the oxide are generated by the high-field stressing of these MOSFETs. The known existence of these defects, paired with the clear domination of interface defects in the SDTAT

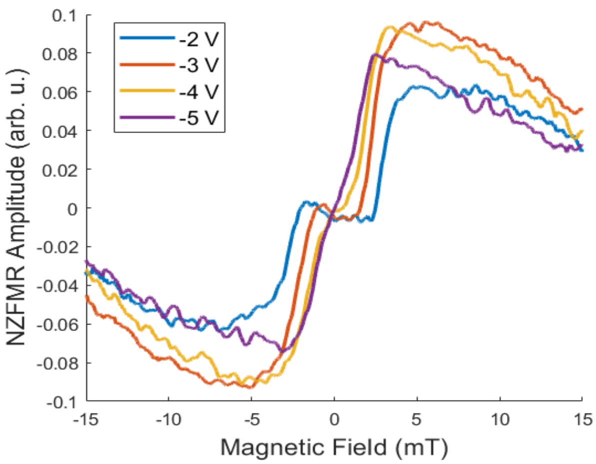

Fig. 5. Comparisons of NZFMR SDTAT in Si/SiO_2 MOSFETs stressed at -9 V for 60 minutes at various gate biases. The significant change in linewidths (5-16 mT) is due to the kinetics of the trap assisted tunneling process.

response, strongly indicates that in the early stages of TDDB, the Si/SiO_2 interface to oxide tunneling process acts as a rate-limiting step [11].

Additional information about the effect of high-field stressing at the Si/SiO_2 interface can be gleaned in the normalized dc I-V NZFMR spectra for various stress times shown in Fig. 4. NZFMR spectra can be modeled using the stochastic quantum Liouville equation (SLE) [10] in terms of hyperfine interactions and the kinetics involved in both recombination and tunneling processes [11]. In the case of a dc I-V measurement with essentially identical devices with identical biasing conditions, the kinetics of the recombination process must be constant. Thus, any changes in the observed NZFMR line shape will be entirely due to changes in the hyperfine interactions from mobile magnetic nuclei near the interface.

The NZFMR spectra in Fig. 4 show clear changes in the line shape throughout the duration of the high-field stress. In the case of a Si/SiO_2 MOSFET, the only magnetic nuclei within the system will be ^{29}Si nuclei (4.7% abundance) and hydrogen nuclei (100% abundance). However, only hydrogen nuclei are mobile. Thus, these SDR results provide evidence that throughout the early stages of TDDB, there must be a redistribution of hydrogen throughout the interface.

Fig. 5 shows the SDTAT NZFMR spectra for a Si/SiO_2 MOSFET that was high-field stressed for an hour as a function of applied gate bias. In this case, in which the chemical structure of the already stressed device will not be changing in any significant manner, the differences in the NZFMR line shape will be due to the kinetics of the trap-assisted tunneling process as a function of applied electric field. One could argue that the application of these biases serves to further stress these devices. However, the equivalent stress times [1] for these biases would be effectively negligible. Additionally, the most dramatic effects of high-field stressing occur early on in the device's lifetime [4,12]. The already negligible effects of these biases would produce a miniscule effect on changes in the hyperfine spectra.

The changes in NZFMR line shape in Fig. 5 are much larger. Note the changes in the linewidths; between -2 to -5 V, the linewidth of this feature changes from 5 to 16 mT. These large changes indicate a significant change in the kinetic rates involved in the trap-assisted tunneling processes in these stressed Si/SiO_2 MOSFETs. The random nature of the formation of percolation paths in TDDB makes quantitative analysis of the NZFMR spectra difficult. However, the broadening is consistent with an increase in tunneling kinetics. The results suggest that, at least in principle, NZFMR spectroscopy using modeling via the SLE could potentially provide a fundamental understanding of the TDDB breakdown process in Si/SiO_2.

V. Conclusion

Our study of the atomic-scale defects involved in TDDB in Si/SiO_2 MOSFETs yields important information about the Si/SiO_2 interface. We find, consistent with earlier work, that the dominant defect in the SDTAT spectra of high-field stressed (100) Si/SiO_2 to be the interface dangling bond centers: the P_{b0} and P_{b1}center. However, we also show evidence of the generation of paramagnetic oxide traps called E' centers near the Si/SiO_2 interface in low-temperature dc I-V measurements. These results likely indicate that there may be a rate-limiting step involving the interface-to-oxide tunneling event, a result that would be consistent with previous findings [9,11].

We also provide NZFMR spectra that show changes in hyperfine interactions that indicate the motion of hydrogen at the interface throughout high-field stressing. Additionally, we provide experimental evidence of significant changes in the kinetic rates due to biasing in high-field stressed devices. These findings could likely be used to further understand the importance of the kinetic rates and provide information about percolation paths in future TDDB experiments.

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References

[1] A. Berman, "Time-Zero Dielectric Reliability Test by a Ramp Method," *19th International Reliability Physics Symposium,* pp. 204-209, Apr. 1981.

[2] D. J. DiMaria and J. H. Stathis, "Anode hole injection, defect generation, and breakdown in ultrathin silicon dioxide films," *J. Appl. Phys.*, vol. 89, no. 9, pp. 5051-5024, May 2001.

[3] J. W. McPherson, "Reliability physics and engineering: time-to-failure modeling," *2nd ed., Springer, New York*, 2013.

[4] J. Blauew, J. van Houdt, D. Wellkens, G. Groesenken, and H. E. Maes, “SILC-related effect in flash E²PROM’s-Part I: A quantiative model for steady-state SILC,” *IEEE Trans. Electron Devices*, vol. 45, no. 8, pp. 1745-1750, Aug. 1998.

[5] C. Zener, “A theory of electrical breakdown of solid dielectrics,” *Proc. R. Soc. London Ser. A*, 143, pp 523-529, 1934.

[6] J. H. Weil, J. R. Bolton, and J. E. Wertz, “Electron Paramagnetic Resonance: Elementary Theory and Practical Applications,” *Wiley Interscience, New York,* 1994.

[7] G. Kawachi, C. F. O. Grae, M. S. Brandt, and M. Stutzmann, “Spin-dependent transport in amorphous silicon thin-film transistors,” *J. Non-Cryst. Solids.* vol 198-200, no. 2, pp. 1117-1120, May 1996.

[8] M. A. Anders, P. M. Lenahan, C. J. Cochrane, J. van Tol, “Physical nature of electrically detected magnetic resonance through spin dependent trap assisted tunneling in insulators,” *J. Appl. Phys.*, vol. 124, no. 21, Dec. 2018, Art. no. 215105.

[9] S. J. Moxim, J. P. Ashton, P. M. Lenahan, M. E. Flatte, N. J. Harmon, S. W. King, “Observation of Radiation-Induced Leakage Current Defects in MOS Oxides with Multifrequency Electrically Detected Magnetic Resonance and Near-Zero-Field Magnetoresistance,” *IEEE Trans. Nuc. Sci.*, vol. 67, no. 1, pp. 228-233, Jan. 2020.

[10] N. J. Harmon, S. R. McMillan, J. P. Ashton, P. M. Lenahan, M. E. Flatte, “Modeling of Near Zero-Field Magnetoresistance and Electrically Detected Magnetic Resonance in Irradiated Si/SiO_2 MOSFETs,” *IEEE Trans. Nuc. Sci.*, vol. 67, no. 7, pp. 1669-1673, Jul. 2020.

[11] E. B. Frantz, D. J. Michalak, N. J. Harmon, E. M. Henry, S. J. Moxim, M. E. Flatte, S. W. King, J. S. Clarke, P. M. Lenahan, “Electrically Detected Magnetic Resonance & Near-Zero Field Magnetoresistance in ^{28}Si/$^{28}SiO_2$,” Submitted to *J. Appl. Phys.,* May 25th , 2021.

[12] S. J. Moxim, F. V. Sharov, D. R. Hughart, G. S. Haase, C. G. McKay, P. M. Lenahan, “Atomic-scale Defects Generated in the Early/Intermediate Stages of Dielectric Breakdown in Si/SiO_2 Transistors,” Unreleased, 2021.

[13] D. J. Fitzgerald, A. S. Grove, “Surface recombination in semiconductors,” *Surface Sci.*, vol. 9, pp. 347-369, 1968.

[14] Y. Nishi, T. Tanaka, A. Ohwada, “Study of Silicon-Silicon Dioxide Structure by Electron Spin Resonance II,” *Jpn. J. Appl. Phys.* vol. 11, no. 85, Jan. 1972.

[15] E. H. Poindexter, P. J. Caplan, B. E. Deal, R. R. Razouk, “Interface states and electron spin resonance centers in thermally oxidized (111) and (100) silicon wafers,” *J. Appl. Phys.* vol. 52, no. 879, pp. 879-884, Feb. 1981.

[16] F. J. Feigl, W. B. Fowler, K. L. Yip, “Oxygen Vacancy model for the E' center center in SiO_2,” *Solid State Commun*, vol. 14, no. 3, pp. 225-229, Feb. 1974.

[17] W. L. Warren, P. M. Lenahan, “Electron spin resonance study of high field stressing in metal-oxide-silicon device oxides,” *Appl. Phys. Lett.* vol. 49, no. 19, pp. 1296-1298, Nov. 1986.