Isolating *p*- and *n*- Doped Fingers with Intrinsic *poly*-Si in Passivated Interdigitated Back Contact Silicon Solar Cells

Matthew B. Hartenstein,[1,2] William Nemeth,[2] Vincenzo LaSalvia,[2] Steve Harvey,[2] Harvey Guthrey,[2] San Theingi,[2] Matthew Page,[2] David L. Young[2], Paul Stradins,[2,*] and Sumit Agarwal[1,*]
[1]Colorado School of Mines, Golden, CO, 80401, USA, [2]National Renewable Energy Laboratory, Golden, CO, 80401, USA.

***Abstract* – Polycrystalline silicon on silicon oxide (*poly*-Si/SiO_x) passivating contacts enable ultra-high-efficiency interdigitated back contact silicon solar cells. To prevent shunt between *n*- and *p*-type doped fingers, an insulating region is required between them. We evaluate the use of intrinsic *poly*-Si for this isolation region. Interdigitated fingers were formed by plasma deposition of doped hydrogenated amorphous silicon through mechanically-aligned shadow masks, on top of a full-area intrinsic amorphous silicon layer. High-temperature annealing then crystallized the *a*-Si:H to *poly*-Si and drove in the dopants. Two mechanisms were identified which cause contamination of the intrinsic *poly*-Si gap during processing. During deposition of doped fingers, we show using secondary ion mass spectrometry and conductivity measurements that the intrinsic gap becomes contaminated by doped *a*-Si:H tails several nanometers thick to concentrations of ~10^{20} cm^{-3}. Another source of contamination occurs during high-temperature annealing, where dopants desorb from doped regions and readsorb onto intrinsic *a*-Si:H. Both pathways reduce the resistivity of the intrinsic gap from ~10^5 Ω·cm to ~10^{-1} Ω·cm. We show that plasma etching of the *a*-Si:H surface before crystallizing with a capping layer can eliminate the contamination of the intrinsic *poly*-Si, maintaining a resistivity of ~10^5 Ω·cm. This demonstrates masked plasma deposition as a dopant patterning method for Si solar cells.**

***Index Terms*—Interdigitated-back-contact, passivating contacts, silicon solar cells**

Manuscript received April 1, 2020. This work was supported by the U.S. Department of Energy under SETP DE-EE0007553 and Contract No. DE-AC36-08GO28308 with Alliance for Sustainable Energy, LLC, the Manager and Operator of the National Renewable Energy Laboratory. Funding provided by U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office under Agreement Number 34359. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes (Corresponding authors: Paul Stradins and Sumit Agarwal)

M. B. Hartenstein is with the Department of Chemical and Biological Engineering at Colorado School of Mines, Golden, CO 80401, USA, and also with the National Renewable Energy Laboratory, Golden CO 80401, USA. (email: hartenstein@mymail.mines.edu)

W. Nemeth, V. LaSalvia, S. Harvey, H. Guthrey, S. Theigni, M. Page, D. L. Young, and P. Stradins are with the National Renewable Energy Laboratory, Golden CO 80401, USA. (email: William.Nemeth@nrel.gov, Vincenzo.LaSalvia@nrel.gov, Steve.Harvey@nrel.gov, Harvey.Guthrey@nrel.gov, San.Theingi@nrel.gov, Matthew.Page@nrel.gov, David.Young@nrel.gov, Pauls.Stradins@nrel.gov)

S. Agarwal is with the Department of Chemical and Biological Engineering at The Colorado School of Mines, Golden, CO 80401, USA. (email: sagarwal@mines.edu)

I. Introduction

Solar energy is one of the most promising technologies for meeting the world's clean energy needs and Si-based photovoltaics (PV) dominate the solar industry in terms of market share [1]. To expand the use of PV worldwide, it is essential to decrease the net cost of electricity from solar power by increasing the efficiency of devices. For device fabrication using monocrystalline silicon (*c*-Si), efficiency has been improved greatly by moving from the Al-back surface field (20.3%) [2] to the *p*-type passivated emitter rear contact [3, 4] (25.0%) cells. Further improvements in device efficiency can be achieved with passivated contacts based either on polycrystalline Si with silicon oxide (*poly*-Si/SiO_x) (26.1%) [5, 6] or amorphous hydrogenated Si (*a*-Si:H) as in the Si heterojunction cells (SHJ) (26.7%) [7]. Passivated contacts greatly reduce recombination at the silicon surface by preventing direct contact with the metal thereby increasing the cell's open-circuit voltage, V_{oc}. *Poly*-Si/SiO_x contacts passivate the *c*-Si surface with ~1.4–2.2 nm SiO_x layer [8-10], which is either thin enough to allow for quantum mechanical tunneling [11-13] or may contain pinholes [14] to enable carrier transport from bulk *c*-Si to the heavily-doped *poly*-Si contacts [5, 11, 15-18]. In SHJ structures [19-22] the hydrogen during plasma deposition of a few nanometers *a*-Si:H layer provides excellent passivation of the *c*-Si surface [23]. Doped *a*-Si:H is then deposited on the intrinsic *a*-Si:H layer followed by a transparent conducting oxide (TCO), which acts as the carrier transport layer to the contacts. Unlike *poly*-Si/SiO_x contacts, a TCO is required in SHJ devices due to the low lateral conductivity of doped *a*-Si:H compared to doped *poly*-Si.

The record efficiencies, >26%, of *c*-Si solar cells are for the interdigitated back contact (IBC) cell architecture with passivated contacts [5, 7]. IBC solar cells allow for high-efficiency devices not only because they eliminate shading and reflection losses due to the absence of the front metal grid, but also enable the use of passivating contacts on both contact polarities without parasitic absorption at the front of the device. This generally allows for higher short-circuit current, I_{sc} [24]. The passivated IBC architecture has been demonstrated using either *poly*-Si/SiO_x (see Fig. 1a) or *a*-Si:H [7, 22, 25] contacting schemes. Although passivated IBC cells have high efficiency, and currently hold the world record for *c*-Si [7], complicated processing steps required for the patterning of the passivated rear contacts limit their widespread adoption in the Si PV industry. One common method of patterning the plasma-

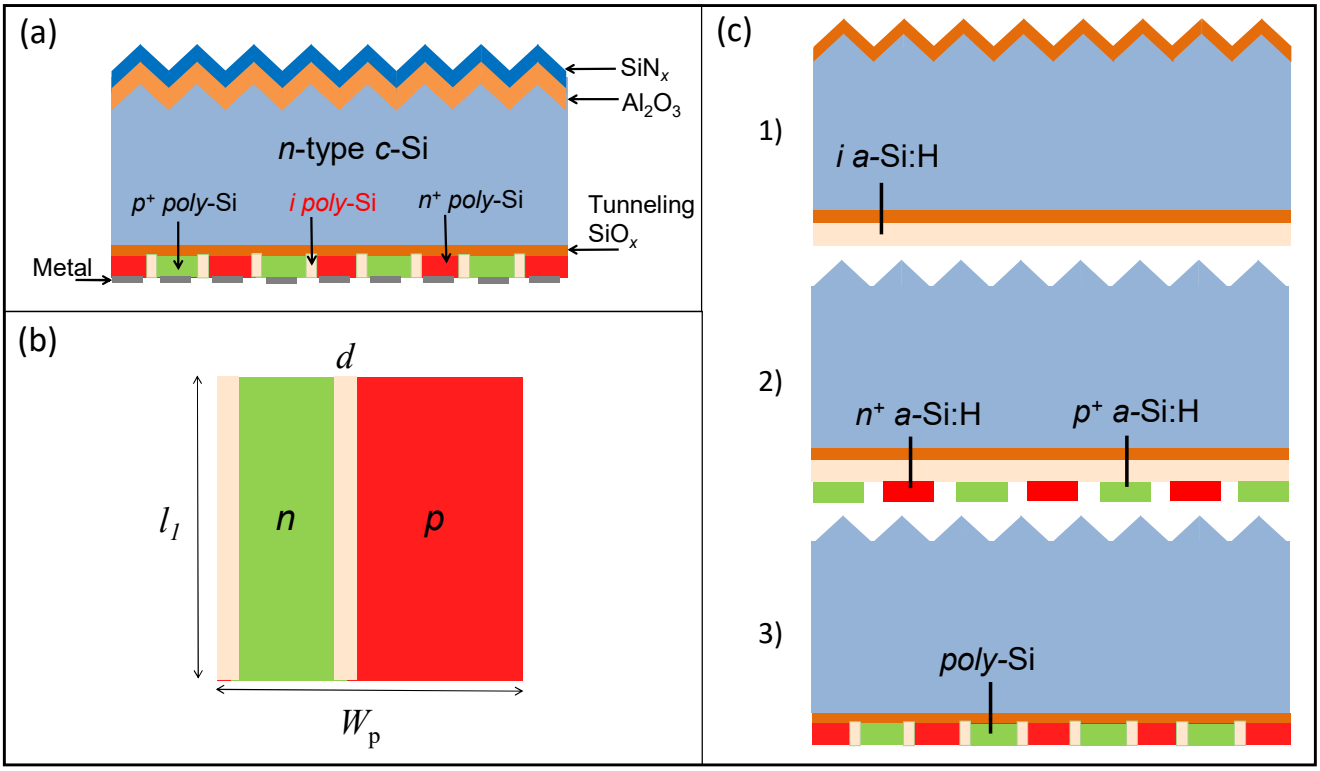

Fig. 1. (a) Schematic of the IBC cell structure of interest. A thin SiO_x film separates the *poly*-Si fingers at the rear of the cell from the bulk *c*-Si, while the doped *poly*-Si fingers are separated by intrinsic *poly*-Si. (b) A schematic representation of one pitch at the rear side of an IBC cell. Fingers of length l_1 are separated by an intrinsic region of width δ, resulting in a total pitch width *W*p. (c) The process of creating doped *poly*-Si contacts of an IBC cell. Beginning with full-area intrinsic *a*-Si:H, doped *a*-Si:H films are plasma deposited through contact masks onto the intrinsic *a*-Si:H before a high-temperature anneal converts the *a*-Si:H to *poly*-Si and drives dopants into the intrinsic film, finalizing the dopant patterning.

deposited [7, 25, 26] *poly*-Si or *a*-Si:H films on the rear side is with photolithography [27], which requires many processing steps leading to increased costs [28]. Other dopant patterning methods for IBC cells include ion implantation [29-32], laser drive-in [33], and laser ablation [34], but require high capital investment into equipment with complicated processing still involved.

The complicated patterning steps for fabricating *poly*-Si based passivated IBC cells are necessary in large part due to the requirement of a highly insulating region between the *n*- and *p*-type *poly*-Si fingers [2, 35, 36]. In doped *c*-Si IBCs, direct contact between *p*- and *n*-type regions forms an ideal diode, while in *a*-Si doped fingers, the lateral conductivity is too low to allow for high levels of recombination at the *p*- and *n*-type finger interface. In *poly*-Si IBC cells, however, direct contact of the *n*- and *p*-type doped *poly*-Si fingers leads to significant shunting by enabling direct recombination through defect states or a tunnel junction between the heavily doped regions [37]. Green shows that for any solar cell [38], the fill factor is related to the total shunt resistance through the following relation

$$FF = FF_0\left[1 - \frac{0.84}{R_{shunt}/R_{ch}}\right], \qquad (1)$$

where *FF* is the cell fill factor, FF_0 is the ideal fill factor without any resistance effects, R_{shunt} is the cell shunt resistance, and R_{ch} is the characteristic cell resistance defined as $R_{ch} = V_{oc}/I_{sc}$. (1) shows that to limit the reduction in fill factor to less than 1% of FF_0, R_{shunt} must be ~100 times greater than the characteristic cell resistance. For an IBC cell with *N* number of *p*- and *n*-type fingers, there will be $2{\cdot}N$ isolation lines in the cell, as shown in Fig. 1b. Adding these $2{\cdot}N$ resistors in parallel, each with a resistance of R_i, the total shunt resistance is given by $R_{shunt} = R_i/2N$. For a single pitch of width W_p on the back side of the IBC as shown in Fig. 1b, R_i can be expressed as $\rho_i \cdot d/t \cdot l_1$, where l_1, d, t, and ρ_i are respectively the length, width, thickness, and resistivity of the insulating line. The total shunt resistance can then be expressed as $R_{shunt} = \rho_i \cdot d/2 \cdot N \cdot l_1 \cdot t$. For a total cell width of $l_2 = W_p{\cdot}N$, we can rewrite,

$$R_{shunt} = \rho_i \cdot d \cdot W_p/2 \cdot A \cdot t, \qquad (2)$$

where $A = l_1{\cdot}l_2$ is the total surface area of the cell. Therefore, for the above 1% FF loss, or $R_{shunt} = 100{\cdot}R_{ch}$ we obtain the following criterion for a sufficiently insulating intrinsic gap:

$$\rho_i = 200 \cdot t \cdot V_{oc}/d \cdot W_p \cdot J_{sc}. \qquad (3)$$

Although a large *d* will provide high R_{shunt}, this isolation region should be kept very narrow to ensure that the majority carriers in the wafer can easily reach the contacted fingers, minimizing the series resistance of the device. For these reasons a highly insulating but narrow isolating region must be maintained between the doped fingers. Assuming W_p = 1 mm and t = 50

nm, for a V_{oc} of 700 mV and a short-circuit current density J_{sc} of 40 mA/cm^2, this corresponds to ρ_i ~ 100 Ω·cm for an isolation line width of d =10 μm (a reasonable order of magnitude estimate for the best IBCs [37]), corresponding to a dopant atom concentration in the *poly*-Si of ~10^{17} – 10^{18} cm^{-3} [39]. According to (3), proportionally lower resistivities are acceptable for isolation lines wider than 10 μm.

One method to isolate the *n*- and *p*-type doped regions in an IBC device is to create a physical gap between the two types of doped fingers. However, this requires additional steps such as selective etching of the region between the doped fingers and passivation of the underlying *c*-Si wafer in the gap to prevent loss in V_{oc} [37]. Utilizing highly resistive intrinsic *poly*-Si in the isolation region can prevent direct shunt between the fingers and can passivate the underlying *c*-Si wafer (see Fig. 1a). The focus of this study is to demonstrate the possibility of using an intrinsic *poly*-Si region to separate doped *poly*-Si fingers in passivated contacts based on *poly*-Si/SiO_x. A recent study by Hollemann *et al.* has also explored this topic [17] and demonstrated IBCs with *poly*-Si contacts on ~2.2 nm SiO_x, fabricated using ion implantation [17, 40]. In this work, precisely-patterned *a*-Si:H fingers were directly deposited through plasma-enhanced chemical vapor deposition (PECVD) using mechanically-aligned shadow masks. The doped fingers were deposited on full-area intrinsic *a*-Si:H deposited on a thin ~1.5 nm tunneling SiO_x layer (see Fig. 1a), before crystallization into *poly*-Si. Using intrinsic *poly*-Si as the insulating material between doped *poly*-Si fingers is a natural choice in this architecture as intrinsic *poly*-Si in a *poly*-Si/SiO_x stack provides excellent passivation of the *n*-type *c*-Si surface, with J_0 < 30 fA/cm^2 on symmetric test structures of intrinsic *poly*-Si/SiO_x stacks on *n*-Si. Additionally, we show that the use of intrinsic *poly*-Si as the insulating gap combined with direct deposition of the doped fingers allows for fewer fabrication steps, greatly simplifying the process. However, we show that plasma deposition of doped *a*-Si:H fingers through a shadow mask and subsequent annealing of *a*-Si:H to *poly*-Si causes increased conductivity in the isolation region due to contamination with dopants leading to shunting. We identify the mechanisms that lead to contamination of the gap region and develop mitigation strategies to maintain high resistivity of the intrinsic isolation region.

II. Experiment

A. Fabrication of test structures to characterize the intrinsic poly-Si isolation region

As-sawn *n*-type Czochralski (*n*-Cz) Si (100) wafers with 3.5 Ω·cm resistivity, ~180 μm in thickness, were cut into 40 mm × 60 mm pieces and etched in 22.5% aqueous KOH to planarize the surface and remove the saw damage. The *c*-Si wafers then underwent standard cleaning steps of piranha, RCA 1, and RCA 2 followed by etching in 1% HF to remove the oxide formed by the RCA 2 step. A dry, thermal, ~70 nm thick SiO_x film was then grown for 30 min in a quartz tube furnace at 1100 °C at atmospheric pressure in an O_2 ambient at a flow rate of 3000 standard cm^3/min (sccm). Subsequently, on one side of the wafer, a ~50 nm film of intrinsic *a*-Si:H was deposited on the thick, insulating SiO_x via a SiH_4/H_2 capacitively-coupled, radio-frequency (rf) plasma operated at 13.56 MHz at a pressure of 1 Torr. The oxidized *c*-Si wafers were placed on the grounded electrode kept at 300 °C. The input power to the plasma was 8 W, with the gas flow rates set to 2 and 100 sccm for SiH_4 and H_2, respectively. Following deposition, the *a*-Si:H films were annealed in a quartz tube furnace in an N_2 ambient. The furnace temperature was ramped from 200 to 850 °C over 3 hr, followed by a 30 min annealing step at 850 °C to convert the *a*-Si:H to *poly*-Si via solid-phase crystallization. The films then underwent a passivation step, which entails a ~15 nm film of Al_2O_3 grown by atomic layer deposition at a temperature of 150 °C from trimethyl aluminum and water, followed by annealing for 20 min at 400 °C in forming gas (1:9 H_2:N_2), and subsequent removal of alumina film by an HF dip as described in [26].

Test structures with patterned, doped fingers were created identically to the above full-area intrinsic *poly*-Si structures, with the addition of doped *a*-Si:H fingers on top of the intrinsic *a*-Si:H by masked PECVD, then crystallizing the structures at 850 °C as described above. Phosphorus- or boron-doped *a*-Si:H fingers, with different gap spacings between them, were plasma-deposited through the Si contact masks at the same conditions as the intrinsic *a*-Si:H above, but with the addition of 1 sccm of B_2H_6 (2.6% in H_2) or 1 sccm of PH_3 (3% in H_2). Some samples were etched for 2–5 s immediately after the deposition of *p*- or *n*-type doped *a*-Si:H fingers, in a reactive ion etcher (Samco RIE-1C) using an SF_6 plasma at a pressure of 100 mTorr with an SF_6 flow rate of 5 sccm at 5 W of rf power (13.56 MHz). Dopant depth profiles were measured with dynamic secondary ion mass spectrometry (SIMS) (Cameca IMS 7f) with an oxygen primary ion beam at 3.5 kV and a sample potential of 2 kV. Three-dimensional dopant concentration on top of the intrinsic *a*-Si:H layer was mapped prior to crystallization and metallization using time-of-flight SIMS (ION-TOF TOF-SIMS V). The primary ion beam was a 30 keV BiMn source, with a pulsed beam current of 1 pA. Measurements were performed in negative polarity utilizing a Cs^+ gun for sputtering, operating at 3 kV at a current of 25 nA. The data was quantified using relative sensitivity factors for phosphorous and boron in silicon obtained from separate measurements of an ion-implanted standard.

Electrical contacts to the intrinsic *poly*-Si film or patterned doped *poly*-Si fingers were formed by thermal evaporation of 1 μm thick Al in a tool with a base pressure of ~10^{-7} Torr via a Si mask matching the plasma-deposited 2D doping patterns. Following metallization, the coplanar resistance of the intrinsic film or between the *p*- or *n*-type doped fingers, was determined by applying a voltage across each pair of adjacent pads and measuring the current.

B. Contact mask fabrication

Contact masks for patterning of doped regions and Al metal contacts were fabricated from as-sawn *n*-Cz wafers by laser scribing. A 532 nm Nd-YAG laser was used to divide them into 40 mm ×60 mm pieces and to scribe a physical mask pattern, removed via KOH etching, onto each piece. These *c*-Si wafers were used as contact masks to deposit patterned doped *a*-Si:H and Al. The spacings between the finger openings varied

between 150 to 500 µm. These contact masks were aligned to the samples with fidelity of ~10 µm by precision-made ceramic pins put into matching, laser-scribed openings in the samples and the masks.

III. Results and Discussion

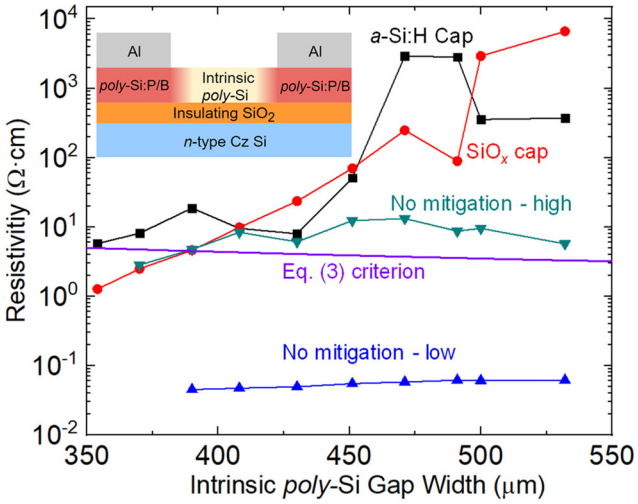

Fig. 2. Resistivity of the intrinsic *poly*-Si isolation region as a function of isolation region width with and without a capping layer. Addition of a *a*-Si:H or SiO_x capping layer improves resistivity by multiple orders of magnitude for wide spacings but remains low for narrower spacings. The inset shows the test structure used for these resistivity measurements.

The resistivity of intrinsic *poly*-Si deposited on quartz substrates or on *c*-Si wafers with >100 nm thermally grown SiO_2 was ~10^5 Ω·cm, which meets the criterion of (3) that $R_{shunt} > 100 \cdot R_{ch}$. After fabrication of the doped finger test structures (see inset of Fig. 2) with *p*- or *n*-type doped fingers were fabricated. The resistivity of the intrinsic *poly*-Si isolation region in these test structures, shown by the blue and teal curves of Fig. 2, decreased by several orders of magnitude to a range of 0.1 – 10 Ω·cm. This suggests that the addition of the doped fingers resulted in contamination of the intrinsic *poly*-Si between the doped fingers. Dynamic SIMS depth profiling measurements were performed at the center of the region between the two *n*-type doped fingers to detect the phosphorous levels. These measurements, shown in Fig. 3, confirmed that phosphorus was present in the insulating *poly*-Si gap at concentrations of 10^{20}–10^{21} cm^{-3}, close to the phosphorous concentration of ~2×10^{21} cm^{-3} in doped fingers. The phosphorous concentration was roughly the same for the entire ~40 nm thickness of the undoped region. The peak at ~40 nm corresponds to the depth of the SiO_x layer between the *poly*-Si and the *c*-Si, where dopants pile up before diffusing into the bulk Si [41]. This clearly indicates that one or more of the processing steps causes the dopants to migrate from the intentionally doped region to the isolating *poly*-Si lines.

Based on the processing sequence of the test structures (see Fig. 1c) we posit three mechanisms for contamination of the intrinsic *poly*-Si isolation region. First, it is possible that the dopants can migrate during plasma deposition of the doped *p*- and *n*-type *a*-Si:H fingers into the region blocked by the contact

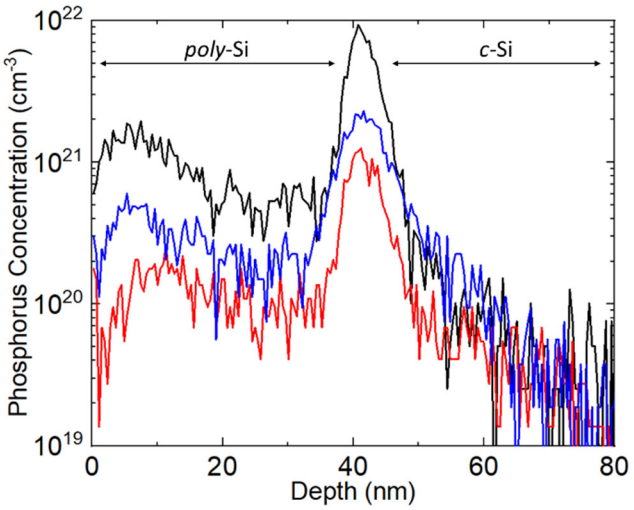

Fig. 3. SIMS depth profiling of phosphorus in regions of a patterned *n*-type *a*-Si:H on intrinsic *a*-Si:H, similar to those shown in Fig. 4. The black curve represents the depth profile within the phosphorus doped finger, red shows the depth profile in an undoped isolation region between two *n*-type regions separated by ~220 µm. The blue curve represents the depth profile in an undoped isolation region between two *n*-type fingers separated by ~40 µm gap.

mask. This could occur due to the migration of radicals generated from the parent molecules of the dopant gases in between the physical spacing between the *c*-Si mask and the substrate wafer. These masks were simply in contact with each other with the weight of the masking wafer with no additional applied pressure. Moreover, both wafers were saw-damage etched with a surface roughness of ~10 µm, which leads to imperfect contact between the mask and the substrate (see Fig. 4a). Second, migration of dopants from the doped fingers to the isolating intrinsic *poly*-Si region could occur during the crystallization and dopant drive-in step at 850 °C in the quartz furnace. During this step, dopants can desorb from the surface redeposit onto and diffuse into the undoped regions (see Fig. 4b). Third, the dopants can also diffuse laterally through the grain boundaries in intrinsic *poly*-Si layer during this 850 °C anneal to contaminate the isolation region [40]. Below, we address these mechanisms in detail experimentally.

A. Leakage of Dopants Underneath Shadow Mask

Dopant spreading from the edge of the patterning mask was measured for samples with ~30 nm thick phosphorous or boron doped *a*-Si:H fingers deposited on ~50 nm thick intrinsic *a*-Si:H. No annealing at 850 °C was performed. The lateral surface dopant concentration profiles are shown in Fig. 5 and were extracted from 3-dimensional TOF-SIMS maps over an area of 500 µm × 500 µm and 100 nm depth (see example inset for P in Fig. 5), by averaging the top ~50 nm of the 3-D maps. These include a 50 µm wide intentionally doped region near the edge of the finger, and the rest of the profile captures the dopant tail in the intrinsic *a*-Si:H region under the shadow mask. The P and B dopant lateral profiles and the P-dopant 3D map in Fig. 5 correspond to doped fingers at the outside edge of the pattern to prevent any overlap from the tail of an adjacent finger. Figure 5 shows that P dopant indeed spreads into the masked intrinsic

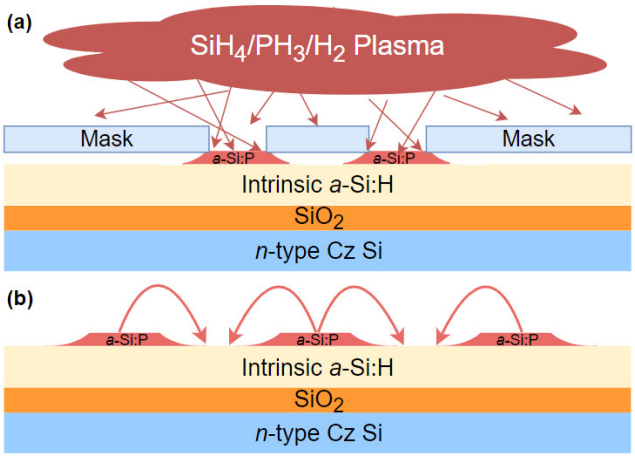

Fig. 4. Schematic showing the contamination of the intrinsic *poly*-Si isolation region. (a) spreading of dopant radicals under the contact mask during plasma deposition of doped *a*-Si:H (a) and (b) desorption/ readsorption of dopants during crystallization.

a-Si:H region by up to ~150 µm, while the boron concentration drops sharply past the mask edge.

During deposition of doped *a*-Si:H, B_2H_6 and PH_3 dissociate in the plasma forming radical species. Most radicals in a plasma environment have a finite sticking coefficient to the growth surface. As shown in Fig. 4a, these radicals have random trajectories as they impinge on to the growth surface. The plasma itself cannot penetrate the gap between the mask and the substrate as the spacing is ~10 µm while a typical Debye length in the plasma is typically ~100 µm [42]. The neutral-neutral mean free path in the plasma at our chamber pressure is ~50 µm. Thus, radicals must have a sticking coefficient <<1 to migrate long distances in the space between the mask and the substrate, colliding with their surfaces many times and ultimately leading to long dopant tails. Low sticking coefficient between dopant radicals and the *a*-Si:H surface is most likely in the absence of dangling bonds sites [43]. Underneath the mask, there is no ion bombardment from the plasma to create dangling bonds and thermal hydrogen desorption from the *a*-Si:H surface does not occur appreciably at temperatures <350 °C [44]. For these reasons, a low sticking coefficient is to be expected and the long dopant tails seen in Fig. 5 are not surprising at the temperatures used for deposition. The fact that we witness phosphorus spreading much further into the gap than boron could possibly be due to a lower sticking coefficient on the *a*-Si:H surface of radicals generated in a PH_3 plasma compared to those generated in a B_2H_6 plasma, though sticking coefficients of individual species within a plasma are difficult to quantify.

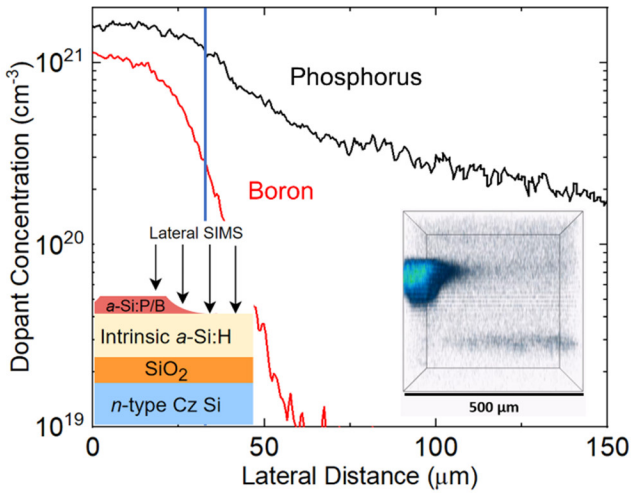

Fig. 5. Lateral SIMS profiles extending outward from *p*- and *n*-type fingers. The mask edge is located at ~25 µm (blue line). The left inset shows a representative test structure for lateral TOF-SIMS profiling. The second inset shows a 3-D map of phosphorus atoms at the edge of an *n*-type finger. The map is approximately 500 µm × 500 µm in area and ~100 nm in depth.

B. Contamination by Gas Phase/ Solid-Phase Transport of Dopants

To test gas-phase dopant transport, a full-area layer of heavily doped *a*-Si:H was deposited onto both sides of a Si wafer and full-area layers of intrinsic *a*-Si:H were deposited onto four other Si wafers that had a ~60 nm thick thermal SiO_2. These samples were loaded into a quartz boat with the doped *a*-Si:H wafer placed at the center with two intrinsic *a*-Si:H wafers on each side of this doped wafer. The intrinsic films were crystallized simultaneously at 850 °C, but not in direct contact with the doped sample. After metallization with Al, conductivity measurements of the intrinsic films were performed as previously described. Intrinsic *poly*-Si films annealed with the phosphorus doped *a*-Si:H show resistivities ranging from ~0.1 – 100 Ω·cm, with higher resistivities for samples upstream of the doped *a*-Si:H coated sample. This range of resistivities is several orders of magnitude lower than the resistivity of intrinsic *poly*-Si (~10^5 Ω·cm) processed under identical condition without a doped wafer in the furnace. Because the intrinsic films were only exposed to phosphorus when co-annealed with the phosphorous doped *a*-Si:H sample, their much lower resistivity can only be attributed to the transfer of P through the gas phase during the high-temperature step. Indeed, this solid-source dopant transfer mechanism is used for doping *c*-Si wafers [45]. Additionally, [46] describes the *in situ* single-side doping of Si wafers by annealing of a test wafer between phosphorus and boron source wafers. Though our setup and annealing conditions are quite different from those described in [45] and [46], we experimentally confirmed this dopant transfer for the crystallization annealing step.

The as-deposited, *n*-type *a*-Si:H films used in this study contain ~3–4 ×10^{21} cm^{-3} phosphorus. However, the solid solubility limit of phosphorus in *c*-Si is ~5×10^{20} cm^{-3} [47]. Therefore, crystallization of *a*-Si:H forces excess phosphorus atoms out of the crystalline matrix into the grain boundaries or surface of *poly*-Si, with most P dopants being inactive. Khandekar used phosphorus-doped *a*-Si:H as the substrate for low-pressure chemical vapor deposition of SiN_x at 760 °C. During the growth of SiN_x, the underlying phosphorous-doped *a*-Si:H underwent crystallization to *poly*-Si. Elemental mapping of the interface between *poly*-Si and SiN_x using energy dispersive x-ray spectroscopy showed that phosphorus segregated to the surface of *poly*-Si during the crystallization step [48]. Additionally, other studies show that the presence of excess phosphorous atoms on a Si(100) surface leads to the

formation of phosphorus dimer rows which can form P_2 species that can desorb at temperatures >550 °C [43, 49]. Previously, Kipp *et al.* investigated the absorption and decomposition of phosphine radicals on the Si(100) using surface spectroscopy and density functional theory. This study shows that phosphine adsorption and decomposition depends strongly on the temperature and, for temperatures between 200-400 °C, phosphorus atoms are likely to diffuse along the Si(100) surface to form P_2 dimer rows [50]. Another study using Auger electron spectroscopy shows that coverage of phosphorus on the Si(100) surface increases with temperature for temperatures up to 550 °C but begins to decrease at higher temperatures as P_2 molecules desorb from the surface. Based on these previous studies, we hypothesize that the contamination of the intrinsic *poly*-Si region during crystallization is due to the desorption of P_2 from the doped regions, and readsorption onto intrinsic *poly*-Si followed by diffusion into the previously intrinsic *poly*-Si.

A similar experiment was performed where intrinsic *a*-Si:H films were annealed alongside boron-doped films. However, only a small drop in resistivity from ~10^5 to ~10^4 Ω·cm was observed, which indicates that boron does not effuse from the heavily-doped *poly*-Si to the same degree as phosphorus. This is likely due the high stability of boron atoms on Si surfaces even up to temperatures of 1000 °C [49].

Lastly, it is possible that dopant atoms could diffuse from the doped *poly*-Si finger edges into intrinsic *poly*-Si film to contaminate the isolation region between doped fingers as suggested in [40]. Reported diffusion coefficients for boron and phosphorous in *poly*-Si vary greatly depending on deposition method, deposition temperature, dopant concentration, and grain size. Kamins *et al.* showed that the effective diffusivity of phosphorus and boron through *poly*-Si depends strongly not only on the diffusion temperature, but also on the deposition temperature of the *poly*-Si films grown via chemical vapor deposition [51]. The values reported in the literature at ~850 °C range from ~10^{-15}–10^{-12} and ~10^{-14}–10^{-13} cm^2/s for boron and phosphorus, respectively [51-56]. Values as high as ~10^{-9} cm^2/s were reported in [57], but at much higher temperatures and much larger grain sizes than those in our experiments (~5-100 µm in [57] compared to ~20 nm). The authors in [40] calculated diffusion coefficients ~10^{-10} cm^2/s for boron and phosphorus. While these diffusion coefficients are outside the range reported in [51-56], they are below ~10^{-9} cm^2/s reported in [57]. The reason for the higher diffusion coefficient is unclear, and the higher annealing temperature of 1035 °C in [57] cannot alone explain such high diffusion coefficients. Based on the activation energy barriers and preexponential factors reported in [53, 54] for phosphorus and boron results in an estimated diffusion coefficient of ~10^{-12} cm^2/s at 1035 °C. Since the authors in [40] used ion implantation for patterning, it is possible that dopants near the surface of their *a*-Si:H films also entered the intrinsic region during their 900 °C oxidation anneal via the gas-phase transfer mechanism described above before the oxide could form to completely prevent gas phase transfer. For an ion implantation energy of 20 keV, the projected range into *a*-Si:H is estimated as ~25 nm with a straggle of ~12 nm [58], assuming a Gaussian implantation profile, this corresponds to ~2% of the implanted phosphorus remaining at or near the surface of *a*-Si:H after implantation, which could participate in gas-phase transfer during the 900 °C oxidation anneal. To determine whether lateral diffusion would have an impact for our samples, we perform a simple calculation. Using the upper estimates for the effective diffusion coefficients D_{eff}, calculated from [53, 54], and an upper estimate of the diffusion time, t = 3.5 hr, at 850 °C, the effective diffusion length, $l_{eff} = \sqrt{D_{eff} \cdot t}$, is estimated to be only ~ 0.1 µm and ~0.05 µm for boron and phosphorus, respectively. Therefore, it is expected that solid-phase diffusion plays a negligible role in any conductivity changes of the intrinsic *poly*-Si isolation region in our studies compared to the two primary mechanisms discussed above.

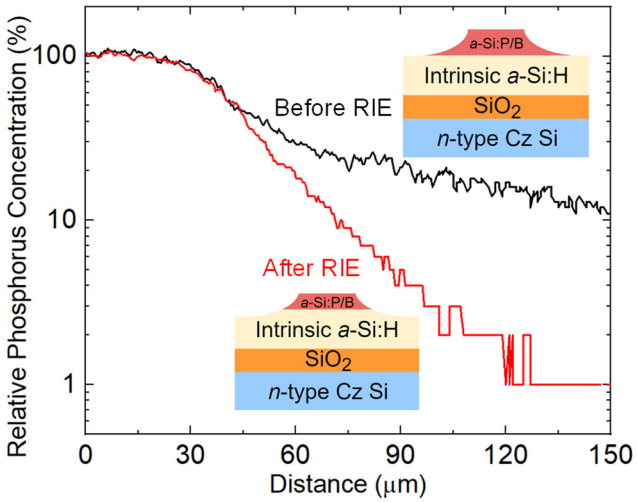

Fig. 6. Lateral SIMS profiles of relative phosphorus concentration at finger edges before (black) and after (red) SF_6 etching of *a*-Si:H. Both profiles were normalized for comparison.

C. Mitigation of isolation region contamination

To mitigate the issue of gas-phase dopant transfer during the crystallization annealing of doped *a*-Si:H to *poly*-Si, we tested the effectiveness of using a capping layer on top of doped *a*-Si:H. This capping layer is expected to reduce the effect of gas-phase dopant transfer as the dopants would have to diffuse through this capping layer into the gas phase and then diffuse again into the adjacent regions through the same capping layer. Two capping layers were tested for the test structure shown in Fig. 2: (a) ~40 nm plasma-deposited intrinsic *a*-Si:H and (b) an SiO_x layer formed due to oxidation during crystallization of the *a*-Si:H film to *poly*-Si in an O_2 ambient. Our measurements in Fig. 2 show that these capping layers are clearly effective in maintaining resistivities that are much higher than the target resistivity, at least for spacings >350 µm. Because no gas-phase dopant transfer was observed during the annealing of boron-doped films *a*-Si:H films, no additional mitigation strategy was deemed necessary.

Next, to mitigate the effect of dopant spreading during plasma deposition, we etched back a thin surface layer of the *a*-Si:H after the deposition of *a*-Si:H doped fingers. We used SF_6 plasma reactive ion etching. Since it is expected that the dopant tail in the *a*-Si:H film underneath the masked region will decay rapidly beyond the line edge (see Fig. 4), the thickness of the dopant tail in most of the intrinsic *a*-Si:H gap will be much

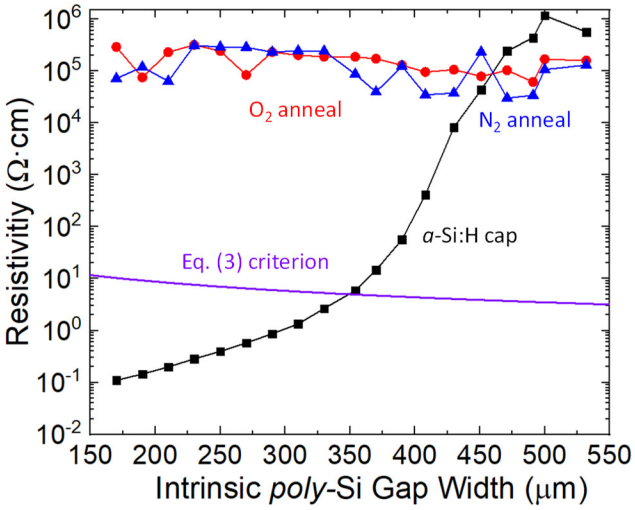

Fig. 7. Resistivity of the intrinsic *poly*-Si isolation region as a function of isolation region width. The samples were processed identically to those shown in Fig. 2, but with an additional SF_6 plasma etch following deposition of doped *a*-Si:H fingers. Note that the scale for this graph extends to much narrower spacings than that of Fig. 2.

thinner than the intentionally doped region. Therefore, uniform plasma etching of the top surface can remove dopants from the intrinsic gap, with minimal effect on the intentionally doped region. Fig. 6 shows the relative lateral concentration profiles of a sample before and after SF_6 plasma etching. By removing a uniformly thick layer of *a*-Si:H after doped *a*-Si:H deposition, the dopant concentration drops by two orders of magnitude over a shorter distance.

This etch back strategy, combined with a capping layer during the crystallization annealing step is thus expected to mitigate dopant transfer into the intrinsic *poly*-Si region better than the capping layers alone. We conducted a similar experiment to the one previously described (see Fig. 2) but extended it to narrower spacings and reevaluated the use of each capping layer. Fig. 7 shows the resistivity for three samples after etch back in an SF_6 plasma: (a) annealed in O_2 to intentionally grow an SiO_x capping layer, (b) annealed in N_2 following by plasma deposition of intrinsic *a*-Si:H capping layer, and (c) annealed in N_2 with no capping layer. For samples that were annealed in O_2, we measured resistivities over the range of ~10^4–10^5 Ω·cm. Surprisingly, for samples that were annealed in an N_2 ambient where we do not expect the growth of a capping layer, we observed resistivity values that were almost identical to the samples annealed in O_2 (see Fig. 7). However, even in an N_2 atmosphere, enough background oxidants such as O_2 and H_2O are present in our system, evidenced by a thin oxide formation on *poly*-Si observed routinely under N_2. Apparently, even this thin SiO_x layer is sufficient to suppress gas-phase dopant transfer. In contrast, the samples with an *a*-Si:H capping layer showed a drastic drop in resistivity, by up to six orders of magnitude, for spacings <450 μm and thus, addition of an *a*-Si:H capping layer is not a good mitigation strategy even with the addition of the plasma etch-back post-deposition. We propose that the decrease in resistivity is related to the chemical transport in our PECVD tool: hydrogen radicals in the plasma etch [59, 60] the heavily doped *a*-Si:H from the chamber walls, substrate holder, and doped fingers nearby, forming gas-phase etch products that contain P and B. These gas-phase species dissociate in the H_2 plasma creating radicals that redeposit the dopant atoms on top of the intrinsic *a*-Si:H regions. Therefore, the most robust strategy to mitigate the contamination of the intrinsic *poly*-Si region with dopants is an etch back in an SF_6 plasma after deposition of *a*-Si:H through the contact mask, followed by annealing in an O_2 ambient to crystallize *a*-Si:H to *poly*-Si.

IV. Conclusions

A low isolation region resistivity significantly hinders IBC cell performance. To limit loss in fill factor due to shunt, the resistivity between the *n*- and *p*-type fingers should be ≥100 Ω·cm. Intrinsic *poly*-Si fits this criterion, but device processing can lead to shunting via two pathways: spreading of dopant radicals during plasma deposition as shown via TOF-SIMS dopant mapping, and phosphorus desorption from the doped film surface during high-temperature crystallization as demonstrated with conductivity tests. Both pathways lower the isolation region resistivity to ~10^{-1} Ω·cm, which is orders of magnitude lower than the acceptable limit. Plasma etching of the *a*-Si:H surface following doped *a*-Si:H deposition removes the dopants which spread during plasma deposition. This combined with the formation of a surface SiO_x during crystallization in O_2 ambient prevents dopant desorption during crystallization. When both mitigation strategies are implemented, resistivities comparable to uncontaminated intrinsic *poly*-Si, ~10^5 Ω·cm, are achieved. These findings are expected to lead to improved processing strategies for efficient and inexpensive IBC cells produced by shadow masked PECVD and physical vapor deposition.

Acknowledgment

This research was supported by US DOE EERE under the Photovoltaic Research and Development (PVRD) program of the Solar Energy Technology Office under Award Number DE-EE0007553 as well as US DOE EERE contract SETP DE-EE00030301 (SuNLaMP) and under Contract No. DE-AC36-08GO28308.

VI. References

[1] A. Metz, M. Fischer, and J. Trube, "International technology roadmap for photovoltaics (ITRPV): Crystalline silicon technology-current status and outlook," in *Proceedings of the PV Manufacturing in Europe Conference, Brussels, Belgium*, 2017, pp. 18-19.

[2] M. A. Green, Y. Hishikawa, E. D. Dunlop, D. H. Levi, J. Hohl-Ebinger, and A. W. Y. Ho-Baillie, "Solar cell efficiency tables (version 52)," *Progress in Photovoltaics: Research and Applications,* vol. 26, no. 7, pp. 427-436, 2018, doi: 10.1002/pip.3040.

[3] A. Morisset *et al.*, "Highly passivating and blister-free hole selective poly-silicon based

contact for large area crystalline silicon solar cells," *Solar Energy Materials and Solar Cells,* vol. 200, p. 109912, 2019.

[4] H. Huang *et al.*, "20.8% industrial PERC solar cell: ALD Al 2 O 3 rear surface passivation, efficiency loss mechanisms analysis and roadmap to 24%," *Solar Energy Materials and Solar Cells,* vol. 161, pp. 14-30, 2017, doi: 10.1016/j.solmat.2016.11.018.

[5] F. Haase, "Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells," *Solar Energy Materials and Solar Cells,* vol. 186, pp. 184-193, 2018, doi: 10.1016/j.solmat.2018.06.020.

[6] F. Lindholm, A. Neugroschel, M. Arienzo, and P. Iles, "Heavily doped polysilicon-contact solar cells," *IEEE electron device letters,* vol. 6, no. 7, pp. 363-365, 1985.

[7] K. Yoshikawa *et al.*, "Exceeding conversion efficiency of 26% by heterojunction interdigitated back contact solar cell with thin film Si technology," *Solar Energy Materials and Solar Cells,* vol. 173, pp. 37-42, 2017/12/01/ 2017, doi: https://doi.org/10.1016/j.solmat.2017.06.024.

[8] A. G. Aberle, "Surface passivation of crystalline silicon solar cells: a review," *Progress in Photovoltaics: Research and Applications,* vol. 8, no. 5, pp. 473-487, 2000, doi: 10.1002/1099-159x(200009/10)8:5<473::Aid-pip337>3.0.Co;2-d.

[9] A. G. Aberle, S. W. Glunz, A. W. Stephens, and M. A. Green, "High-eficiency silicon solar cells: Si/SiO2, interface parameters and their impact on device performance," *Progress in Photovoltaics: Research and Applications,* vol. 2, no. 4, pp. 265-273, 1994, doi: 10.1002/pip.4670020402.

[10] M. Rienäcker *et al.*, "Junction resistivity of carrier-selective polysilicon on oxide junctions and its impact on solar cell performance," *IEEE Journal of Photovoltaics,* vol. 7, no. 1, pp. 11-18, 2016.

[11] R. Peibst *et al.*, "Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?," *Solar Energy Materials and Solar Cells,* vol. 158, pp. 60-67, 2016, doi: 10.1016/j.solmat.2016.05.045.

[12] R. van der Vossen, F. Feldmann, A. Moldovan, and M. Hermle, "Comparative study of differently grown tunnel oxides for p-type passivating contacts," *Energy Procedia,* vol. 124, pp. 448-454, 2017/09/01/ 2017, doi: https://doi.org/10.1016/j.egypro.2017.09.273.

[13] A. S. Kale *et al.*, "Understanding the charge transport mechanisms through ultrathin SiO x layers in passivated contacts for high-efficiency silicon solar cells," *Applied Physics Letters,* vol. 114, no. 8, p. 083902, 2019.

[14] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, "Carrier-selective contacts for Si solar cells," *Applied Physics Letters,* vol. 104, no. 18, 2014, doi: 10.1063/1.4875904.

[15] F. Haase, "Interdigitated back contact solar cells with polycrystalline silicon on oxide passivating contacts for both polarities," *Jpn J Appl Phys 1,* vol. 56, 2017, doi: 10.7567/JJAP.56.08MB15.

[16] F. Haase *et al.*, "Perimeter Recombination in 25%-Efficient IBC Solar Cells With Passivating POLO Contacts for Both Polarities," *IEEE Journal of Photovoltaics,* vol. 8, no. 1, pp. 23-29, 2018, doi: 10.1109/jphotov.2017.2762592.

[17] C. Hollemann, F. Haase, S. Schäfer, J. Krügener, R. Brendel, and R. Peibst, "26.1%-efficient POLO-IBC cells: Quantification of electrical and optical loss mechanisms," *Progress in Photovoltaics: Research and Applications,* 2019, doi: 10.1002/pip.3098.

[18] M. Rienäcker *et al.*, "Recombination Behavior of Photolithography-free Back Junction Back Contact Solar Cells with Carrier-selective Polysilicon on Oxide Junctions for Both Polarities," *Energy Procedia,* vol. 92, pp. 412-418, 2016, doi: 10.1016/j.egypro.2016.07.121.

[19] J. Bullock *et al.*, "Efficient silicon solar cells with dopant-free asymmetric heterocontacts," (in English), *Nature Energy,* vol. 1, no. 3, Jan 25 2016, doi: 10.1038/nenergy.2015.31.

[20] S. Harrison, O. Nos, G. D'Alonzo, C. Denis, A. Coll, and D. Munoz, "Back Contact Heterojunction Solar Cells Patterned by Laser Ablation," *Energy Procedia,* vol. 92, pp. 730-737, 2016, doi: 10.1016/j.egypro.2016.07.051.

[21] T. Desrues, S. De Vecchi, G. D'Alonzo, D. Munoz, and P. J. Ribeyron, "Influence of the emitter coverage on interdigitated back contact (IBC) silicon heterojunction (SHJ) solar cells," 2014, pp. 857-861, doi: 10.1109/PVSC.2014.6925050.

[22] M. Lu, U. Das, S. Bowden, S. Hegedus, and R. Birkmire, "Optimization of interdigitated back contact silicon heterojunction solar cells: tailoring hetero-interface band structures while maintaining surface passivation," *Progress in Photovoltaics: Research and Applications,* vol. 19, no. 3, pp. 326-338, 2011, doi: 10.1002/pip.1032.

[23] Y. Lee, C. Park, N. Balaji, Y.-J. Lee, and V. A. Dao, "High-efficiency Silicon Solar Cells: A Review," *Israel Journal of Chemistry,* vol. 55, no. 10, pp. 1050-1063, 2015, doi: 10.1002/ijch.201400210.

[24] J. Liu, Y. Yao, S. Xiao, and X. Gu, "Review of status developments of high-efficiency crystalline silicon solar cells," *Journal of Physics D: Applied Physics,* vol. 51, no. 12, 2018, doi: 10.1088/1361-6463/aaac6d.

[25] A. Tomasi *et al.*, "Simple processing of back-contacted silicon heterojunction solar cells using selective-area crystalline growth," *Nature Energy,* vol. 2, no. 5, pp. 17062-17062, 2017, doi: 10.1038/nenergy.2017.62.

[26] W. Nemeth *et al.*, "Polycrystalline silicon passivated tunneling contacts for high efficiency silicon solar cells," (in English), *Journal of Materials Research,* vol. 31, no. 6, pp. 671-681, Mar 28 2016, doi: 10.1557/jmr.2016.77.

[27] J. Nakamura, N. Asano, T. Hieda, C. Okamoto, H. Katayama, and K. Nakamura, "Development of heterojunction back contact Si solar cells," (in English), *IEEE Journal of Photovoltaics,* vol. 4, no. 6, pp. 1491-1495, Nov 2014, doi: 10.1109/JPHOTOV.2014.2358377.

[28] R. Vasudevan *et al.*, "Laser-induced BSF: A new approach to simplify IBC-SHJ solar cell fabrication," 2018.

[29] D. L. Young *et al.*, "Low-cost plasma immersion ion implantation doping for Interdigitated back passivated contact (IBPC) solar cells," *Solar Energy Materials and Solar Cells,* vol. 158, pp. 68-76, 2016, doi: 10.1016/j.solmat.2016.05.044.

[30] D. L. Young, W. Nemeth, V. Lasalvia, R. Reedy, N. Bateman, and P. Stradins, "Ion implanted passivated contacts for interdigitated back contacted solar cells," (in English), *2015 IEEE 42nd Photovoltaic Specialist Conference, PVSC 2015,* pp. 1-5, 2015, doi: 10.1109/PVSC.2015.7356141.

[31] D. L. Young *et al.*, "Interdigitated Back Passivated Contact (IBPC) Solar Cells Formed by Ion Implantation," *IEEE Journal of Photovoltaics,* vol. 6, no. 1, pp. 41-47, 2016, doi: 10.1109/jphotov.2015.2483364.

[32] C. Reichel *et al.*, "Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells," *Journal of Applied Physics,* vol. 118, no. 20, 2015, doi: 10.1063/1.4936223.

[33] E. Franklin *et al.*, "Design, fabrication and characterisation of a 24.4% efficient interdigitated back contact solar cell," *Progress in Photovoltaics: Research and Applications,* vol. 24, no. 4, pp. 411-427, 2016, doi: 10.1002/pip.2556.

[34] D. Walter *et al.*, "Damage-free ultraviolet nanosecond laser ablation for high efficiency back contact solar cell fabrication," *Solar Energy Materials and Solar Cells,* vol. 136, pp. 1-10, 2015, doi: 10.1016/j.solmat.2014.12.030.

[35] D. D. Smith, "Backside contact solar cell with formed polysilicon doped regions," Patent US8242354B2

Patent Appl. 12/626483, 2009. [Online]. Available: https://patents.google.com/patent/US8242354B2/en?oq=US8242354B2

[36] R. M. Swanson, "Back side contact solar cell with doped polysilicon regions," ed: Google Patents, 2009.

[37] C. Reichel, R. Müller, F. Feldmann, A. Richter, M. Hermle, and S. W. Glunz, "Influence of the transition region between p- and n-type polycrystalline silicon passivating contacts on the performance of interdigitated back contact silicon solar cells," (in English), *Journal of Applied Physics,* vol. 122, no. 18, Nov 14 2017, doi: 10.1063/1.5004331.

[38] M. A. Green, *Solar cells : operating principles, technology, and system applications / Martin A. Green* (Prentice-Hall series in solid state physical electronics., no. Accessed from https://nla.gov.au/nla.cat-vn1555330). Englewood Cliffs, N.J: Prentice-Hall, 1982.

[39] B. Tyagi and K. Sen, "On the resistivity of polycrystalline silicon," *physica status solidi (a),* vol. 80, no. 2, pp. 679-684, 1983.

[40] C. Hollemann *et al.*, "Separating the two polarities of the POLO contacts of an 26.1%-efficient IBC solar cell," *Scientific Reports,* vol.

10, no. 1, p. 658, 2020/01/20 2020, doi: 10.1038/s41598-019-57310-0.
[41] T. Matsuura, J. Murota, N. Mikoshiba, I. Kawashima, and T. Sawai, "Diffusion of As, P, and B from doped polysilicon through thin SiO2 films into Si substrates," *Journal of The Electrochemical Society,* vol. 138, no. 11, p. 3474, 1991.
[42] A. J. L. a. M. A. Lieberman, "Basic Plasma Equations and Equilibrium," in *Principles of Plasma Discharges and Materials Processing*, 2005, pp. 23-42.
[43] S. R. Schofield *et al.*, "Phosphine Dissociation and Diffusion on Si(001) Observed at the Atomic Scale," *The Journal of Physical Chemistry B,* vol. 110, no. 7, pp. 3173-3179, 2006/02/01 2006, doi: 10.1021/jp054646v.
[44] W. Beyer and H. Wagner, "Determination of the hydrogen diffusion coefficient in hydrogenated amorphous silicon from hydrogen effusion experiments," *Journal of Applied Physics,* vol. 53, no. 12, pp. 8745-8750, 1982.
[45] B.-J. Cho, S.-K. Park, and C.-K. Kim, "Estimation of effective diffusion time in a rapid thermal diffusion using a solid diffusion source," *IEEE Transactions on Electron Devices,* vol. 39, no. 1, pp. 111-117, 1992.
[46] A. Rohatgi and D. Meier, "Developing novel low-cost, high-throughput processing techniques for 20%-efficient monocrystalline silicon solar cells," *Photovoltaics International,* vol. 10, pp. 87-93, 01/01 2010.
[47] M. Sarret, A. Liba, F. L. Bihan, P. Joubert, and B. Fortin, "n-type polycrystalline silicon films obtained by crystallization of in situ phosphorus-doped amorphous silicon films deposited at low pressure," *Journal of Applied Physics,* vol. 76, no. 9, pp. 5492-5497, 1994, doi: 10.1063/1.357167.
[48] A. Khandekar, S. Surthi, V. Hou, N. Rana, and B. Williams, "Mechanism of Surface Bump Defect Formation in Phosphorus Doped Polysilicon-Silicon Nitride Film Stack," in *2008 IEEE Workshop on Microelectronics and Electron Devices*, 18-18 April 2008 2008, pp. 26-29, doi: 10.1109/WMED.2008.4510660. [Online]. Available: https://ieeexplore.ieee.org/ielx5/4509989/4510639/04510660.pdf?tp=&arnumber=4510660&isnumber=4510639&ref=
[49] M. L. Yu, D. J. Vitkavage, and B. S. Meyerson, "Doping reaction of PH3 and B2H6 with Si(100)," *Journal of Applied Physics,* vol. 59, no. 12, pp. 4032-4037, 1986, doi: 10.1063/1.336708.
[50] L. Kipp, R. D. Bringans, D. K. Biegelsen, J. E. Northrup, A. Garcia, and L. Swartz, "Phosphine adsorption and decomposition on Si(100) 2 x 1 studied by STM," *Phys Rev B Condens Matter,* vol. 52, no. 8, pp. 5843-5850, Aug 15 1995, doi: 10.1103/physrevb.52.5843.
[51] T. I. Kamins, J. Manoliu, and R. N. Tucker, "Diffusion of Impurities in Polycrystalline Silicon," *Journal of Applied Physics,* vol. 43, no. 1, pp. 83-91, 1972, doi: 10.1063/1.1660842.
[52] D. J. Coe, "The lateral diffusion of boron in polycrystalline silicon and its influence on the fabrication of sub-micron MOSTs," *Solid-State Electronics,* vol. 20, no. 12, pp. 985-992, 1977/12/01/ 1977, doi: https://doi.org/10.1016/0038-1101(77)90208-8.
[53] D. Losee, J. Lavine, E. Trabka, S. T. Lee, and C. Jarman, "Phosphorus diffusion in polycrystalline silicon," *Journal of applied physics,* vol. 55, no. 4, pp. 1218-1220, 1984.
[54] I. C. Post and P. Ashburn, "Investigation of boron diffusion in polysilicon and its application to the design of pnp polysilicon emitter bipolar transistors with shallow emitter junctions," *IEEE transactions on electron devices,* vol. 38, no. 11, pp. 2442-2451, 1991.
[55] B. Han *et al.*, "Phosphorus and boron diffusion paths in polycrystalline silicon gate of a trench-type three-dimensional metal-oxide-semiconductor field effect transistor investigated by atom probe tomography," *Applied Physics Letters,* vol. 107, no. 2, 2015, doi: 10.1063/1.4926970.
[56] S. Nédélec, D. Mathiot, and M. Gauneau, "Diffusion of boron in polycrystalline silicon," in *ESSDERC'96: Proceedings of the 26th European Solid State Device Research Conference*, 1996: IEEE, pp. 153-156.
[57] F. H. M. Spit and H. Bakker, "Diffusion of donor elements (125Sb, 82P, 74(73)As) in polycrystalline silicon," *physica status solidi (a),* vol. 97, no. 1, pp. 135-142, 1986, doi: 10.1002/pssa.2210970111.

[58] I. M. Lab. "ION IMPLANTATION: PROJECTED RANGE & STRAGGLE CALCULATOR." Brigham Young University. https://cleanroom.byu.edu/rangestraggle (accessed.

[59] R. Van Oort, M. Geerts, J. Van Den Heuvel, and J. Metselaar, "Hydrogen plasma etching of amorphous and microcrystalline silicon," *Electronics Letters,* vol. 23, no. 18, pp. 967-968, 1987.

[60] R. P. H. Chang, C. C. Chang, and S. Darack, "Hydrogen plasma etching of semiconductors and their oxides," *Journal of Vacuum Science and Technology,* vol. 20, no. 1, pp. 45-50, 1982, doi: 10.1116/1.571307.