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Fly-Buck Converter Parametric Analysis and ZVS Operation for Multiple Outputs

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***Abstract*—The Fly-buck converter provides a simple, low-cost solution to generating multiple isolated or non-isolated output voltage rails using secondary windings of the coupled inductor. Under certain operating conditions, the high side (HS) and low side (LS) switches can realize zero-voltage-switching (ZVS) at turn-ON, reducing switching losses and electromagnetic interference (EMI). However, several factors play a critical role in determining the soft-switching criteria. Therefore, this paper presents an in-depth analysis and evaluation of the ZVS operation through developing equivalent circuit models of the fly-buck converter along with a parametric study of the design variables, including leakage inductance, output current ratio, and dead time.**

***Index Terms*—fly-buck, flybuck, isolated buck, isolated converters, multi-output converters, ZVS, soft-switching, coupled inductor buck**

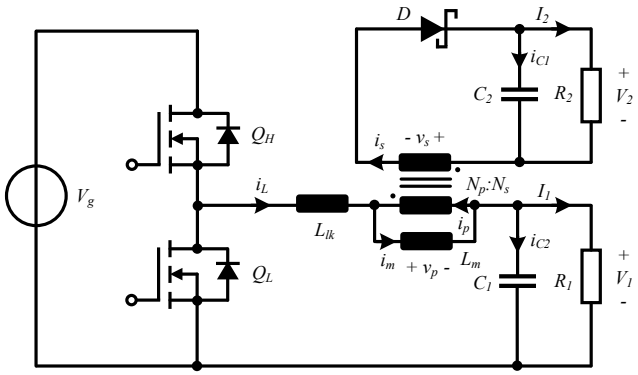


Fig. 1: Fly-buck Converter Circuit Topology

I. Introduction

Several systems that rely on power electronic power delivery and conversion demand multiple voltage rails to supply power to several apparatus with unique loading characteristics. These include telecommunication equipment [1], medical devices [2], data centers [3], distributed sensing [4], aerospace electronic systems [5], [6], and more. While design priorities vary, most applications favor power conversion solutions with lower cost, higher efficiency, higher power density or specific power, and/or improved reliability. In general, this motivates the realization of designs with fewer components, where power is processed through fewer stages and using fewer converters. To realize these improvements, multiple output converters may be incorporated that supply more than one voltage using a single circuit.

There is a variety of circuit topologies and system architectures to enable multiple voltage outputs [7]–[13]. Compared to the traditional isolated converter topologies like Flyback, Forward, and Push-Pull, Fly-buck is an alternative solution to generating the desired number of output voltages through a coupled inductor in replacement of the filter inductor in the synchronous buck converter [14]. The fly-buck topology is shown in Fig. 1 where the primary voltage, V_1 is non-isolated and produced by the buck whereas the secondary voltage, V_2 can be isolated and generated by the additional winding of the coupled inductor, similar to the Flyback.

This topology has several advantages: multiple isolated output voltages can be realized through the secondary windings. It is relatively cost-effective due to low number of components required and simple compensation design without needing a signal isolation for feedback [15]. Such advantages are desirable characteristics for various applications like isolated gate driver bias supplies for power transistor switching operation [16]–[19].

Nonetheless, there are several unique challenges associated with the topology, such as cross-regulation on multiple output voltages [20], [21], output capacitor sizing requirement [22], and modelling of the converter [23]. Despite the converter's known control strategy to enable zero-voltage-switching (ZVS) operation [24], [25], information is lacking on a detailed ZVS analysis and the effects of the converter parameters influencing the soft-switching conditions. Thus, this paper provides an in-depth analysis, describing the ZVS operation based on varying design parameters, including the leakage inductance of the coupled inductor, secondary to primary output current ratio, and the required dead-time for the switching devices.

The paper is outlined as follows – Section II details the converter's theory of operation. Section III describes the equivalent circuit models and the derived equations, governing the ZVS criteria. Section IV provides detailed ZVS analysis based on the selected design parameters. Section V presents the ZVS validation approach through both simulation and hardware results. Lastly, Section VI present conclusions and future work.

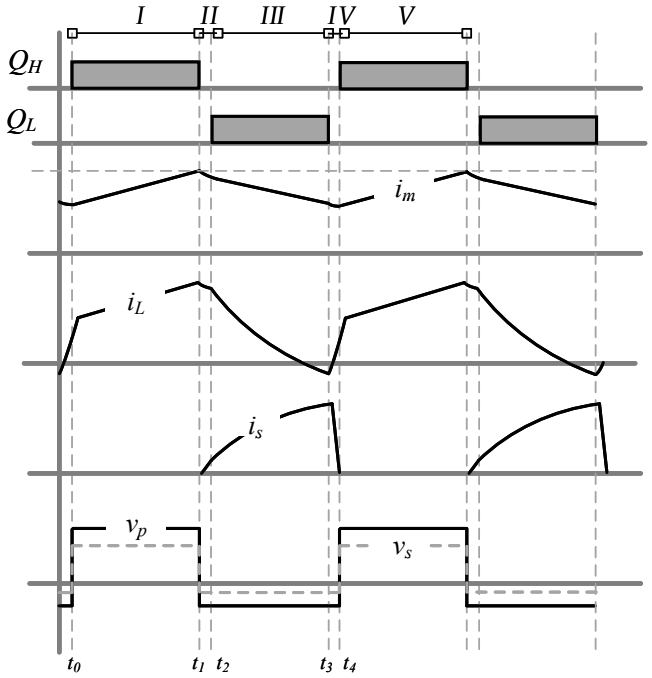


Fig. 2: Fly-buck Steady State Operation Waveforms

II. Fly-Buck Converter Operating Modes

The operation of the fly-buck converter can be described by the four stages denoted as I-IV in Fig. 2. The figure depicts the primary (v_p) and secondary (v_s) voltages of the coupled inductor, magnetizing current (i_m), and primary (i_L) and secondary (i_s) side current waveforms during each time interval. The fly-buck operation principles can be largely explained in two distinct modes of operation – buck mode (I-II) and flyback mode (III-IV).

A. Buck Converter Mode (I-II)

The first two intervals, I and II describe the traditional synchronous buck converter mode of operation. Mode I $[t_1 - t_0]$ is when the high-side (HS) switch, Q_H is ON and low-side (LS) switch, Q_L is OFF. The magnetizing inductance, L_m is charged by the source minus the primary output voltage, i.e. $V_g - V_1$ much like the conventional buck converter. The primary side current follows the magnetizing current, expressed in (1) while the secondary winding current remains zero as the diode, D is reverse biased. Fig. 3(a) describes such an operation mode.

Mode II $[t_2 - t_1]$, illustrated in Fig. 3(b), is the dead time interval when both Q_H and Q_L are OFF. The magnetizing current conducts through the body diode of Q_L, resonating between the transistors' output capacitances, C_{oss} (not shown), primary side output capacitance, C_1 and the equivalent inductance, $L_m + L_{lk}$, where L_{lk} is the leakage inductance. As with the conventional buck converter, the fly-buck can expect the same soft-switching mechanism for Q_L during this period.

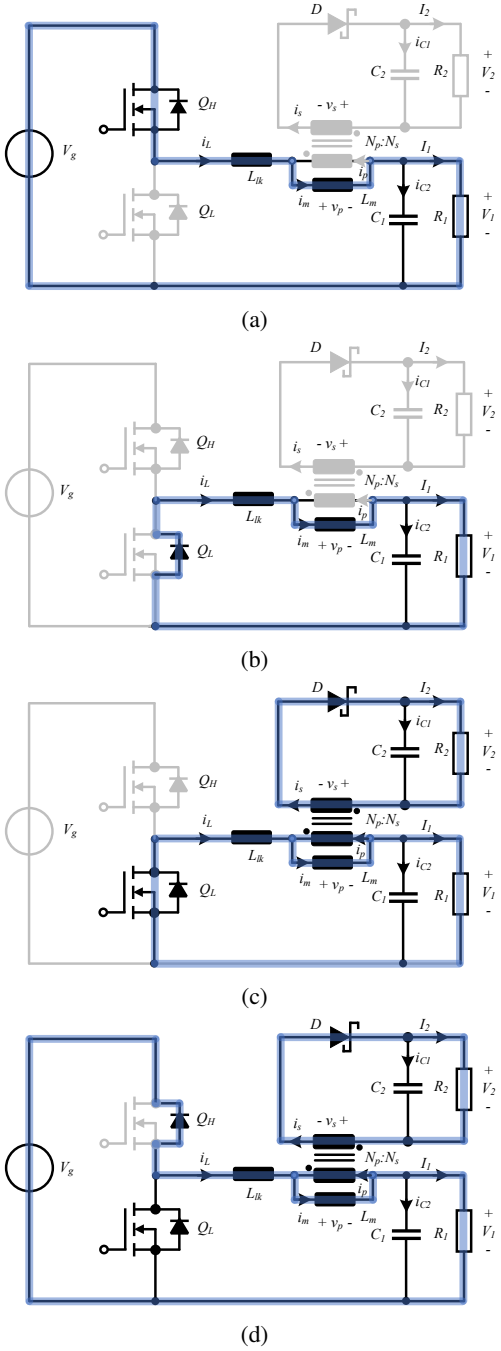


Fig. 3: Fly-buck Modes of Operation: (a) Mode I $[t_1 - t_0]$, (b) Mode II $[t_2 - t_1]$, (c) Mode III $[t_3 - t_2]$, (d) Mode IV $[t_4 - t_3]$

B. Flyback Converter Mode (III-IV)

The last two intervals, III and IV describe the mode of operation analogous to the flyback converter. Mode III $[t_4 - t_2]$ is when Q_L is ON and Q_H is OFF. During this period, v_s is negative, forward biasing D and allowing i_s to conduct to the secondary output capacitor, C_2 and the load, R_2. The circuit for this time-interval is shown in Fig. 3(c). Unlike the buck converter, i_L in Fly-buck decreases at a faster rate, owing to the supply of current to both output loads, I_1 and I_2.

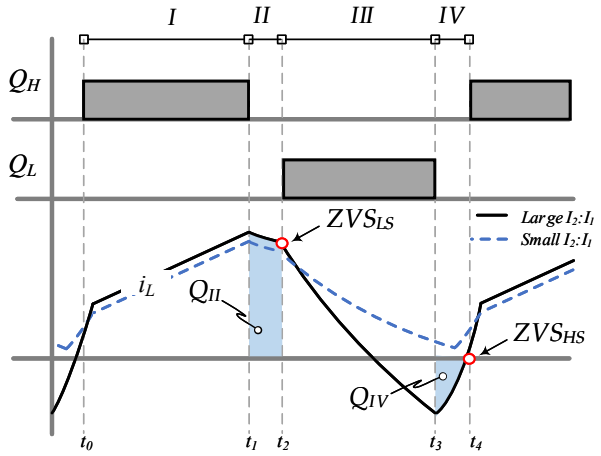


Fig. 4: Fly-buck Primary Current Waveforms with Small and Large Output Current Ratio ($I_2 : I_1$) Cases

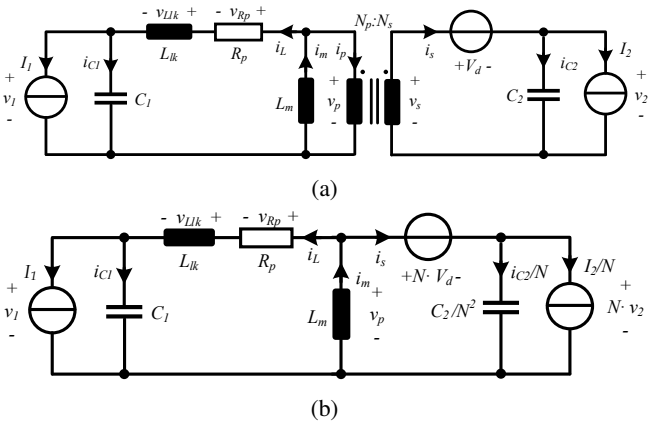


Fig. 5: Fly-buck Equivalent Circuit Models – (a) lumped element based circuit and (b) reduced form with reflection to primary

Depending on the output current ratio, $I_2 : I_1$ along with other factors, such as the current ripple, the peak primary current at t_3, i.e. $i_L(t_3)$ and the current direction (positive or negative) are determined during this time interval, which are essential factors to realize ZVS on Q_H.

Mode IV $[t_2 - t_1]$, described in Fig. 3(d) is the dead time when both Q_H and Q_L are OFF. The primary side current continues to flow through the body diode of Q_L, resonating between the output capacitances, C_{oss}, primary and secondary output capacitance, C_1 and C_2, and the leakage inductance, L_{lk}. During this period, the current direction can change, allowing the circulating current through the body diode of Q_H. Therefore, the viability of ZVS on Q_H largely depends on the current direction, the peak amplitude, and the total charge dissipated on Q_H.

III. Zero-Voltage-Switching (ZVS) Analysis

It is critical to evaluate the circulating current characteristics during the commutation of the bridge-leg to assess ZVS conditions on the switches [26], [27]. As indicated in the previous section, Fly-buck topology can operate at ZVS for both Q_H and Q_L under specific criteria. The conditions for soft-switching depend on the circuit parameters that determine the peak current amplitude, the total dissipating charge, and the current direction.

Fig. 4 compares i_L between a small and a large value of $I_2 : I_1$ ratio. With the smaller ratio, the average magnetizing current, I_m is smaller and vice versa for the larger ratio. This relationship is expressed in (1) where N is the turns ratio, i.e. $N = N_p/N_s$. The ratio, $I_2 : I_1$ is, in fact, a driving factor in successful operation of ZVS because it not only shifts the DC offset of I_m and hence, changing the initial peak current at t_2, $i_L(t_3)$, but also allows the current direction to change during Mode III. The higher the secondary output current, the lower the primary peak current at t_3.

During the dead times, II and IV, the total net charge commutated by i_L is represented as Q_{II} and Q_{IV}. Following the charge-based ZVS analysis in [27], (2) must hold true to realize ZVS on Q_H and Q_L.

$$I_m = I_1 + \frac{I_2}{N} \tag{1}$$

$$Q_{II} \text{ and } Q_{IV} > \int_0^{V_g} 2C_{oss}(v)d(v) = 2Q_{oss} \tag{2}$$

$$i_L(t_3) > 0 \tag{3}$$

The ZVS on Q_L, ZVS_{LS} annotated in Fig. 4 can be generally assumed in Fly-buck as it is in buck. However, ZVS on Q_H, ZVS_{HS} can be challenging as there are many factors that control the likelihood of it. Along with (2), to realize ZVS_{HS} (3) must be also met or assumed, which is not feasible when I_2 is not greater than a certain value of I_1, as illustrated with the smaller case in Fig. 4. The illustration provides recognition that investigating ZVS_{HS} requires careful modeling of the converter operation, especially the current through the HS switch. Thus, further evaluation of ZVS_{HS} is provided in the following section through constructing proper equivalent circuit models and deducing the analytical solution for the primary current.

IV. Fly-buck Equivalent Circuit Model Analysis

To carefully address the ZVS_{HS} conditions, it is paramount to evaluate the circuit operation during the flyback mode (III-IV) and examine the parameter ranges at which (2)-(3) are met. Fig. 5 illustrates the succession of the equivalent circuit model development process specific to the time interval III.

To simplify the equivalent circuit modeling approach, the primary and secondary load resistors, R_1 and R_2 have been replaced by the current sources, I_1 and I_2, respectively. The secondary side diode voltage drop is accounted for and represented as V_d. Furthermore, the parasitic resistance, R_p represents the winding loss as well as the ON-resistance of Q_L. The lumped element circuit based transformer model [28] is used to represent the coupled inductor with the leakage inductor on the primary side. Fig. 5(a) includes these elements in the model and Fig. 5(b) shows the reduced form of Fig. 5(a)

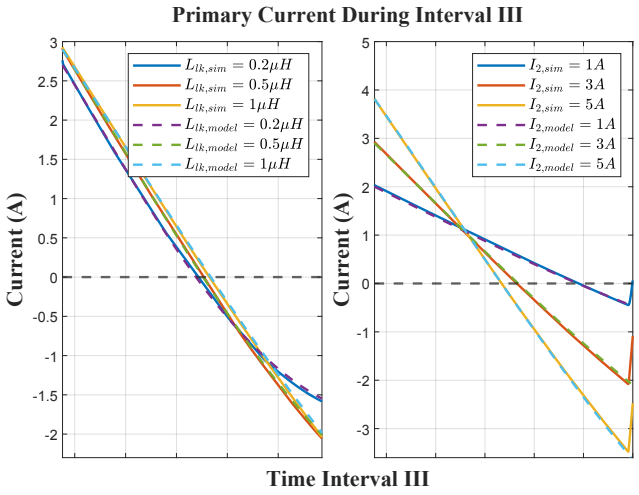


Fig. 6: Fly-buck equivalent circuit model validation between the simulation and analytical solution with different L_{lk} and I_2

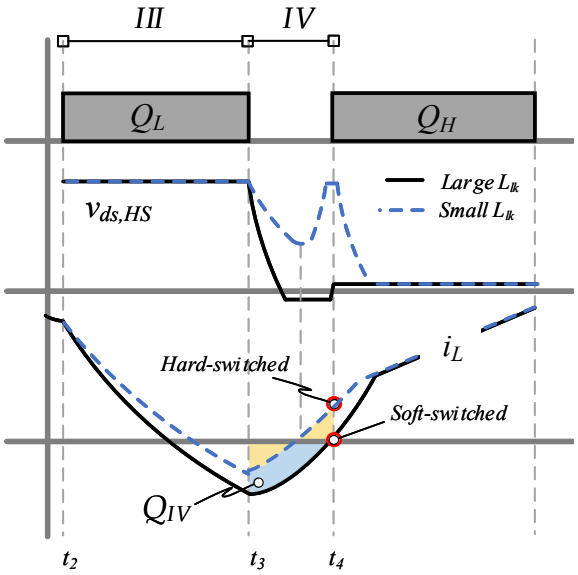


Fig. 7: Effects of L_{lk} on the HS drain voltage, $v_{ds,HS}$. Large L_{lk} can support soft-switching whereas small L_{lk} results in hard-switching

with the secondary side elements reflected to the primary side of the ideal transformer with the turns ratio, N.

Note that the equivalent circuit in Fig. 5(b) shows the primary output capacitance and the primary load on the left hand side, the secondary output capacitance and output load on the right hand side, and the energy transfer elements (coupled inductor) in the middle. Assuming that $L_m >> L_{lk}$, L_m can be treated as an open circuit, allowing the leakage inductance, L_{lk} to be the main element for the current circulation and energy transfer between the primary and the secondary side.

With the equivalent circuit model defined, $i_L(t-t_3)$ can be derived and solved for using (4)-(5); (6) shows the exact form of the solution and the derivation process has been omitted for brevity. Equation (6) provides a useful insight to the current direction and the peak current during III, which can be used for the ZVS criteria (2)-(3).

$$i_L = i_{C1} + I_1 = -(i_{C2} + I_2)/N \tag{4}$$

$$v_{R_p} + v_{L_{lk}} + V_1 - N \cdot V_2 - N \cdot V_d = 0 \tag{5}$$

$$i_L = e^{-\frac{\alpha t}{2}} \left(\cosh\left(\frac{rt}{2}\right)(\gamma + \delta) + \sinh\left(\frac{rt}{2}\right)\frac{\gamma\alpha + 2\epsilon + \alpha\delta}{r} \right) - \gamma \tag{6}$$

where

$$\alpha = \frac{R_p}{L_{lk}}$$

$$\beta = \frac{1}{L_{lk}C_{eq}}$$

$$\gamma = I_1 - \frac{I_2}{N}$$

$$\delta = I_1 + \frac{I_2}{N} + \frac{V_1(V_g - V_1)}{2V_g f_{sw} L_m} = i(t_2)$$

$$\epsilon = \frac{N(V_2 + V_d) - V_1 - \delta R_p}{L_{lk}} = i'_L(t_2)$$

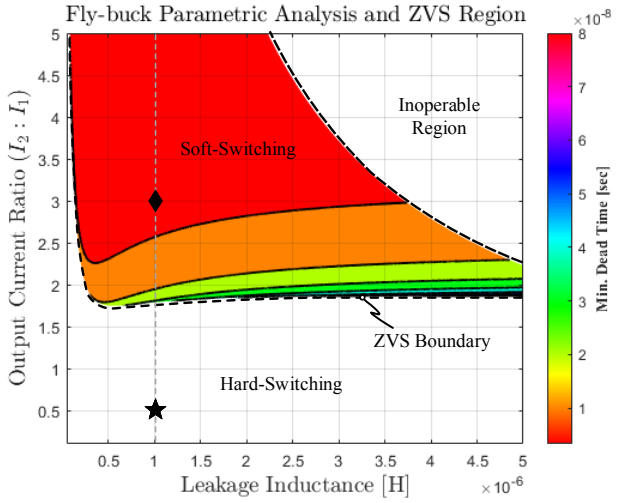
$$r = \sqrt{\alpha^2 - 4\beta}$$

To ensure the validity of the derived equation in (6), Fig. 6 compares $i_L(t-t_3)$ between the Fly-buck converter simulation model and the analytical solution with different L_{lk} and I_2 values. It shows closely matching waveforms between the simulation and the model across the varying range of test cases.

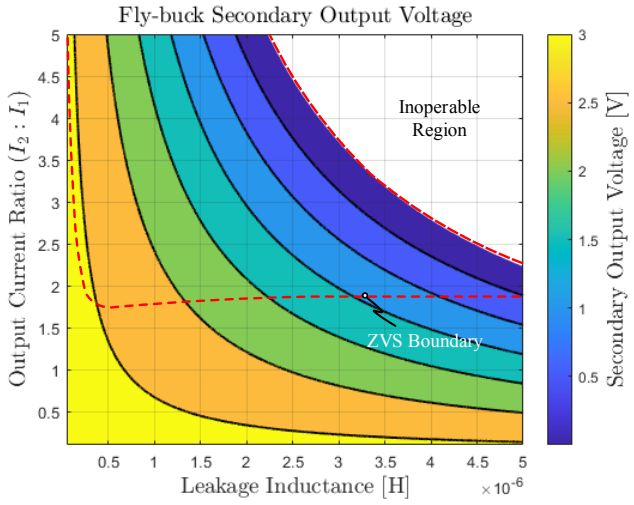
V. Fly-buck High Side ZVS Analysis

Examining (6) and Fig. 6 alludes to some salient factors impacting the current characteristics during III. With different combinations of L_{lk} and $I_2 : I_1$, the peak current and direction can vary considerably during the commutation. Consequently, the successful ZVS_{HS} operation depends on the total charge, Q_{IV} during the dead time in IV, given that (3) is met. To provide a visual aid to the soft-switching and hard-switching cases based on two separate arbitrary values of the leakage inductance, Fig. 7 illustrates the effects on a small and large leakage inductance.

Given that $i_L(t_3)$ is negative for both cases, with the smaller value of L_{lk}, the slope at which $i_L(t-t_4)$ increases is faster than that of the large L_{lk} due to the inverse relationship between the slew rate and the leakage inductance. Such a rate of change can be approximated by (7). The smaller L_{lk} case can drive the current to the positive direction during IV, causing insufficient net charge to fully discharge C_{oss}, which eventually results in hard-switching. On the other hand, with the large L_{lk}, higher energy stored is expected and thus, the circulating current is maintained longer during t_{IV}, ultimately discharging the output capacitance before the turn-ON at t_4 and prompting ZVS. Equation (8) can be used to



(a)



(b)

Fig. 8: Fly-buck parametric study on (a) ZVS boundary region and (b) secondary voltage drop based on L_{lk} and I_2 combinations

characterize the primary current with the initial condition of $i_L(t_3)$ calculated from (6). Equation (9) is the integral form of (8), expressing the total charge equal to $2Q_{oss}$. Thus, (9) can be used to derive the time when the circulating charge is equal to the output capacitances.

$$\frac{di_L(t_3)}{t_{IV}} \approx \frac{V_g - NV_d}{L_{lk}} \tag{7}$$

$$i_L(t-t_4) \approx \frac{V_g - NV_d}{L_{lk}}(t-t_4) - i_L(t_3) \tag{8}$$

$$\frac{V_g - NV_d}{2L_{lk}}(t-t_4)^2 - i_L(t_3)t - 2Q_{oss} = 0 \tag{9}$$

To conceptualize the degrees of freedom, especially L_{lk} and $I_2 : I_1$, effecting the ZVS operation, Fig. 8(a) is generated by parametrically varying the elements and determining the minimum dead time requirement. The hard-switching region as indicated in the figure, is where ZVS cannot be achieve due to

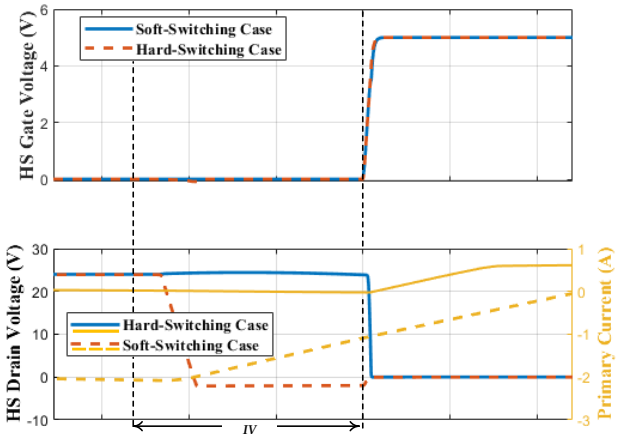


Fig. 9: Simulation validation results showing soft-switching and hard-switching cases, which correspond to the symbols '♦' and '★' in Fig. 8(a). The solid blue and yellow lines are for the hard-switching case whereas the dashed red and yellow lines are for the soft-switching case.

either i_L remaining positive direction or the circulating charge, $Q_{IV} < 2Q_{oss}$. In other words, high coupling coefficient of the coupled inductor or small current ratio can indeed inhibit the ZVS operation.

The soft-switching region is when full ZVS can be realized on Q_H. In the soft-switching region, the minimum dead time requirement is presented. In practice, too large dead time can reduce the overall efficiency while operating at below the required dead time results in partial ZVS or hard-switching.

In addition, it is noteworthy to mention that the inoperable region is defined as the area where the secondary voltage, V_2 has dropped to nearly zero; the region can widen depending on what the user-defined value is for the application-specific regulation requirement.

The voltage drop on the secondary side can be calculated using (10). It can be inferred that V_2 drop also depends on L_{lk} and I_2, given that the rest of the parameters are fixed. Fig. 8(b) depicts the voltage drop in V_2 within the same parametrically evaluated range between L_{lk} and $I_2 : I_1$ in Fig. 8(a).

$$V_2 = \frac{L_m \cdot \Delta i_m \cdot f_{sw}}{N(1-D)} - \frac{2L_{lk} \cdot f_{sw}}{N^2(1-D)^2} \cdot I_2 - (V_d + R_p \cdot I_2) \tag{10}$$

The larger the L_{lk} and $I_2 : I_1$, the higher the voltage drop on V_2. The inoperable region in Fig. 8 indicates that it is important to choose the converter operation point(s) based on not only the ZVS operation, but also the minimum voltage requirement.

VI. Evaluation of ZVS Operation and Validation

Fig. 9 presents the simulation results showing the expected outcomes of the soft-switching and hard-switching cases, which are marked by '♦' and '★', respectively. The hard-switching case is when $I_1 = I_2 = 0.5A$ and $L_{lk} = 1\mu H$

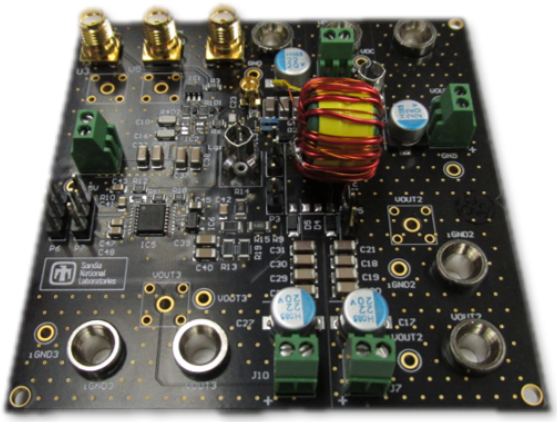


Fig. 10: Picture of the Fly-buck converter Hardware Prototype

whereas the soft-switching case is when $I_1 = 0.5A$, $I_1 = 3A$, and $L_{lk} = 1\mu H$. It can be noted that by the end of the interval IV, the current is slightly positive or nearly zero for the hard-switching case while it is approximately $-2A$ for the soft-switching case. Both (2)-(3) are satisfied for the soft-switching case due to the larger current peak value from I_2.

Fig. 10 shows a picture of the Fly-buck converter hardware. The hardware prototype has been used to validate the Fly-buck converter ZVS operation. The prototype uses a custom designed coupled inductor in order to control both the magnetizing inductance and the leakage inductance.

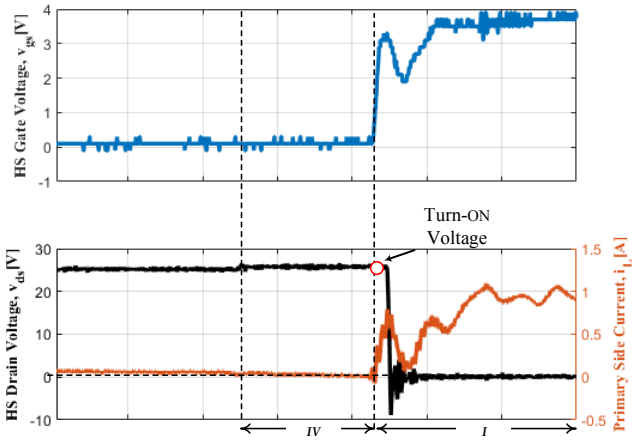
Fig. 11(a) presents the hard-switching case when $I_2 : I_1 = 1$ whereas Fig. 11(b) reproduced the soft-switching case where the test case is $I_2 : I_1 = 3$. Note that the leakage inductance is fixed and the output current varied between $0.5A$ and $3A$. The higher I_2 allowed larger peak current during III and IV; this resulted in approximately $-2A$ peak current through Q_H for the $I_2 : I_1 = 3$ case. Q_{IV} shows the total charge circulated during the commutation period in IV, satisfying (2)-(3) conditions and thus, soft-switching is realized. On the other hand, the current is nearly zero for the hard-switching case and the energy stored in the leakage inductor is not able to discharge the output capactiance, causing hard-switching.

The experimental test cases are not the same as the selected operating points for simulation due to the transformer construction and the margin of error in the leakage inductance measurement.

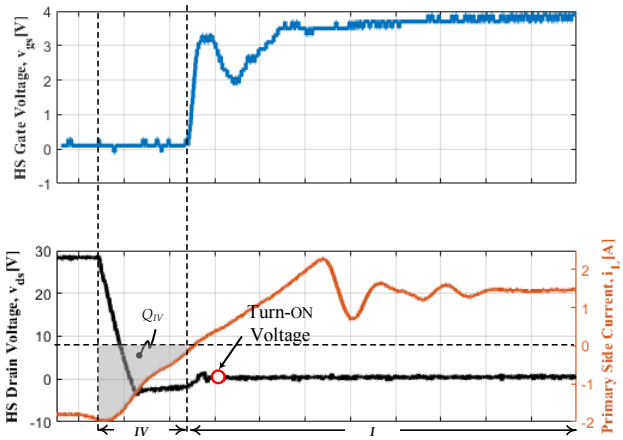
Based on the simulation and experimental results provided, though not an exhaustive approach, it can be believed that the ZVS region analyzed in Fig. 8(a) can be corroborated by the selected test cases in simulation and experiment showing the anticipated switching characteristics.

VII. Conclusion and Future Work

Fly-buck converter is an attractive option to supporting multi-output voltage rails. It's versatile and flexible due to its simple design along with other notable performance metrics, including realizing ZVS for both HS and LS switches. However, it requires a careful selection of the leakage inductance, the output current ratio, and the dead time in order to enhance the performance of the converter under the ZVS operation.



(a)



(b)

Fig. 11: Experimental results showing: (a) hard-switching case and (b) soft-switching case

One of the challenges observed with ensuring a wide range of ZVS operation is determining the optimal operating point(s) based on the source and load requirements. Thus, the authors recommend a further study on evaluating multi-dimensional design of the Fly-buck converter with the specific loading and regulation requirement. Moreover, it is insightful to account for the efficiency calculation across the soft-switching and hard-switching areas to expand on the current analyses. Lastly, designing a custom coupled inductor with a precise control of the leakage inductance requires a comprehensive design evaluation of the magnetic construction.

Last but not least, there have been various buck derived topologies found in literature [29]- [30]. It would provide interesting work, if detailed comparisons are explored between

the Fly-buck and other circuit topologies that enable multi-output voltage rails.

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