Final Technical Report

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1 Executive Summary

In this project, we attempted to make CdTe homojunctions using single crystal *p*-type doped substrates and closed-space sublimation epitaxy (CSSE) *n*-type doped films. The project included modeling which determined the ideal thickness for the *n*-type layer as being <200 nm.

Boules of high concentration indium-doped CdTe and $CdSe_{0.4}Te_{0.6}$ (CST) were grown using modified vertical Bridgman (MVB) methods. Similarly, iodine-doped CdTe crystals were grown for the first time. Washington State University (WSU) stock phosphorus-doped CdTe was used as the p-type substrate layer. The crystals were characterized by Hall effect and time-resolved photoluminescence (TRPL, for electrical properties), photoluminescence microscopy (for uniformity), X-ray diffraction (for crystal structure), and glow discharge mass spectrometry (GDMS, for dopant and impurity concentration). CdTe:I crystals were also characterized by visible and infrared transmission measurements, and various Cd or Te heat treatments were performed to assess changes in optical and electrical properties. A Master's thesis in Materials Science and Engineering was completed focusing on the CdTe:I crystals. According to GDMS, about 5-10% of intended indium dopant was incorporated in the CdTe and CST crystals, and about 2-22% of intended iodine dopant was incorporated into the CdTe crystals.

The grown *n*-type materials – CdTe:In, $CdSe_{0.4}Te_{0.6}$:In, and CdTe:I – were provided to the National Renewable Energy Laboratory (NREL) for growth of CSSE thick films for characterization by two photon TRPL (for carrier lifetime), electron back-scatter diffraction (EBSD, to assess epitaxy), and Hall effect. The thick films were necessary for the TRPL measurements to avoid surface and interface recombination effects to ensure the bulk film lifetime was being measured. A few thinner films were grown and characterized, and have similar properties to the thick films. All films were shown by EBSD to be epitaxial.

Several measurements of secondary ion mass spectroscopy (SIMS) were performed. Nearly 100% of the indium from the crystal was incorporated into the measured thick films, while only ~2-22% of the iodine from the crystal was incorporated. Additionally, significant diffusion of the indium during CSSE, but perhaps less diffusion of iodine, was observed. The substrate (*p*-type crystal) temperature cannot easily be decoupled from the source (n-type powdered material) in CSSE, resulting in high temperatures >500°C which likely lead to the large diffusion effects. The SIMS results were ambiguous as to whether the phosphorus from the substrate also diffuses into the films.

The net result of the diffusion issue is that homojunction devices created using CSSE have a buried homojunction, as indicated by the near infrared peak in the external quantum efficiency (EQE). Various parameterization of front and back contacts suggested that the poor device performance was primarily a result of this buried junction and not due to other effects. However, one experiment where indium metal was diffused into an undoped CdTe single crystal suggested much better performance than the same indium diffused into a CSSE undoped CdTe layer (which still had a buried junction), suggesting that there may also be an issue with the CSSE film lifetime in addition to the dopant profile. Future work should assess whether there is any way to make the substrate temperatures lower in the CSSE process, to slow or halt the process of dopant diffusion from the films.

2 Participants and Collaborators

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- Prof. John McCloy, Principal Investigator
- Dr. Santosh Swain, Research Assistant Professor
- Dr. Magesh Murugesan, Post-doctoral Research Associate
- Dr. Rubi Gul, Research Assistant Professor
- Mr. Samuel Bigbee-Hansen, MS student – CdTe:I growth and characterization
- Ms. Jing Shang, PhD student – investigation into RTA effects; help with electrical char.
- Mr. Raine Antonio, undergraduate student – polishing
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National Renewable Energy Laboratory

- Dr. Joel Duenow, co-Principal Investigator
- Dr. Steven Johnston – TRPL measurements
- Dr. Helio Moutinho – EBSD measurements
- Mr. Bart Stevens

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4 Background and Introduction

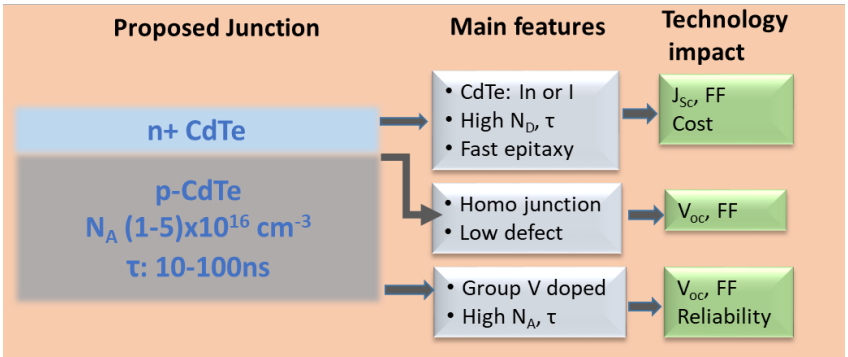


Figure 1: Features of the proposed devices and expected impact on performance parameters ($J_{ShortCircuit}$, $V_{OpenCircuit}$, and Fill Factor), cost, and reliability.

CdTe is the only photovoltaic (PV) solar technology competing with Chinese Si panels on both performance and cost. CdTe technology has already reached levelized costs less than conventional fuels. For the past 25 years, polycrystalline CdTe solar cells have been made using a p-n semiconductor heterojunction. V_{oc} has been limited to about 800-900 mV, though carrier lifetime and interface improvements have helped increase efficiency from 16% to 22% in recent years. Critically, *in-situ* Group V (GrV) doping has increased absorber hole density limits from 10^{14} cm^{-3} to 10^{16}–10^{17} cm^{-3}. This has already improved energy yield relative to that of longstanding Cu-doped devices, and now provides a platform for higher efficiency. However, as the absorber hole density increases, the interface recombination becomes more deleterious and evidence indicates this is now limiting next-generation CdTe performance (Metzger et al., 2019). In addition, common n-type layers such as CdS and MgZnO (MZO) have one or more issues related to parasitic absorption, non-ideal band offset, lattice mismatch-induced defects, dopability, or chemical stability. Shifting from a heterointerface to a homojunction provides a clear path to remove *deleterious interface defects* from the critical p-n junction. The project aims to combine the low-cost manufacturing advantage of CdTe technology with strategies to increase efficiency and reliability, which may enable reaching the ambitious levelized cost of electricity (LCOE) target of $0.02/kWh, since state-of-the art (SOTA) CdTe PV cost is already <$0.05 kWh, and is the lowest among all PV. The proposed device structure and expected technological impact are illustrated in Figure 1. The technical barrier is to develop a high-quality n-type emitter for CdTe solar cells.

Prior to this project, very little work has been done on n-type doping in polycrystalline solar cells. Molecular beam epitaxy (MBE) work has shown that CdTe is much easier to dope n-type, reaching carrier density values as high as 10^{18} cm^{-3} (Zhao et al., 2016). A single-crystal p-n homojunction solar cell made in 1987 held the world record V_{oc} for almost 30 years (Nakazawa et al., 1987) until Washington State University (WSU) and NREL teamed together and exceeded 1 V for the first time by using p-type doping with GrV elements (P, As, Sb) in single crystals (Burst et al., 2016). While n-type CdS has been used for high-efficiency and high-voltage solar cells, the extraordinarily short carrier lifetime in CdS leads to current loss. Addtionally, finding a lattice-matched n-type emitter for a CdTe heterojunction is difficult; MZO, for example, creates stability and control issues. In our preliminary studies with n-type doping with In, we have demonstrated electron densities ~10^{18} cm^{-3} in single crystals of CdTe and CdSeTe. Figure 2 shows activation efficiency of p-type doped (Burst et al., 2016), and n-type CdTe/CdSeTe recently grown at WSU. The properties are promising to the extent that we propose to use thin indium or iodine-doped n-

type CdTe as a low series resistance emitter, paired with a p-type CdTe:P absorber. NREL has recently demonstrated epitaxy using the close-spaced sublimation (CSS) process where single crystal (sX) films could be grown at commercial manufacturing rates simultaneously doped by source materials (Colegrove et al., 2020). Here, we propose to further advance the scientific understanding of n-type doping and thin film methods to fabricate CdTe-based homojunction solar cells and characterize how they modify interface recombination and solar cell attributes.

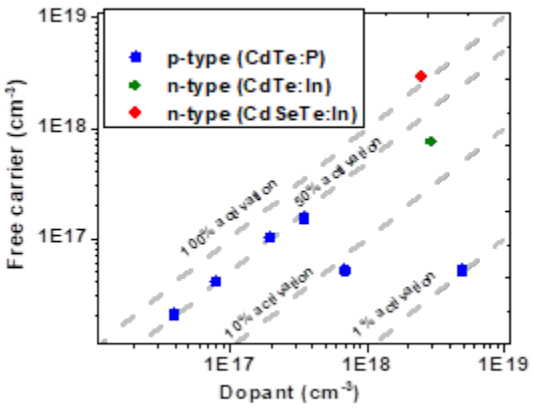


Figure 2: Dopant activation in p-type doping (CdTe:P, from (Nakazawa et al., 1987)) and n-type CdTe (CdSeTe) recently grown at WSU.

5 Major Goals & Objectives

CdTe is the leading thin-film photovoltaic (PV) technology with the lowest cost per Watt due to low-cost manufacturing and comparable efficiency with multicrystalline-Si. Cost can be further reduced by improving efficiency without significantly changing manufacturing processes. Fabricating homojunctions with ideal CdTe material properties can alleviate some of the major efficiency-limiting factors in state-of-the-art heterojunctions. Project success will positively impact the US solar industry, manufacturing, and energy security, since the US is the leading manufacturer of CdTe PV. The completion of the project is expected to lead to further research aimed at studying dopant behavior under various process conditions, doping large area films and modules, surface passivation, compatibility with existing contact technology, and doping in combination with Se alloying.

In order to fabricate homojunctions, we will develop indium (In) and iodine (I)-doped n-type CdTe that is compatible with a GrV-doped p-type CdTe absorber. In this project, we will design, fabricate, and study CdTe homojunctions, combining modeling, bulk and thin film growth of doped CdTe, and material and device characterization. The junction will be made by depositing highly n-type epitaxial films on p-type single crystal substrates. The substrates will be prepared from phosphorus-doped bulk crystals with hole density (10^{15} - 10^{16} cm^{-3}) and lifetime (5-55 ns) that have shown high V_{oc} (~900-1000+ mV). A fast close-space sublimation epitaxy (CSSE) process, which has been shown to produce single crystal films, will be used to make n-type films by in-situ doping. As source material, pre-doped CdTe:In and CdTe:I materials, grown by the Bridgman method, will be used. Device modeling will be performed, which will guide desired optimization of material properties and device design for making efficient junctions. To

characterize single crystals, films, electron density, junction formation, and devices, we will apply the following techniques: Hall effect, glow discharge mass spectrometry (GDMS), SIMS (secondary ion mass spectrometry), J-V, C-V, electron backscatter diffraction (EBSD), and scanning electron microscopy (SEM). Final project target is to achieve a CdTe p-n homojunction with V_{oc} of 875±25 mV, efficiency > 10%.

6 Project Results and Discussion

Milestone status is shown in Table 1.

Table 1. Status of milestones

#	Anticipated Month (STATUS)	Performance Metric	Success Value	Assessment Tool / Method of Measuring Success Value	Metric Justification, Additional Notes
1.1.1	1 (COMPLETE)	Perform initial modeling to determine acceptable thickness and electron concentration in n-layer for junction	Thickness range and doping range determined	Parameterized Sentaurus model	Provides early targets for n-layer thin film thickness and carrier concentration
1.2.1	2 (COMPLETE)	Thin single crystal n-type layers of In-doped CdTe grown by CSSE on p-type CdTe	Films of CdTe:In on CdTe:P wafer, verified single crystal	Thickness by electron microscopy or profilometry; single crystal by EBSD; SIMS profile for indium incorporation (target 10^{18} cm^{-3} In in film); measured TRPL, target lifetime >1 ns.	Proof of concept homojunction with existing source material crystals of CdTe:P and CdTe:In
1.3.1	3 (COMPLETE)	Carrier density and lifetime in CdTe:In bulk single crystal	$5x10^{17}$ cm^{-3}; minority carrier lifetime > 1 ns (this is 10% radiative recombination)	Crystal quality by IR microscopy; Carrier concentration by Hall Effect; Lifetime by TRPL	The success value was chosen considering the state of the art in absorber material carrier density
1.2.2	4 (TEAM DECIDED NOT TO PERFORM)	Thin n-type layer of n-type CdTe grown by TE on p-type CdTe	Films of CdTe:In on CdTe:P wafer, $CdCl_2$ passivated, lifetime measured	Thickness by electron microscopy or profilometry; lifetime by TRPL; SIMS profile for indium incorporation	RISK MITIGATION: only needed if 1.2.1 does not work right away; $CdCl_2$ treatment will likely be necessary
1.3.2	4 (COMPLETE)	Carrier density and lifetime in CdTe:I bulk single crystal	$5x10^{17}$ $cm^{-3;}$ minority carrier lifetime > 1 ns (this is 10% radiative recombination)	Crystal quality by IR microscopy; Carrier concentration by Hall Effect; Lifetime by TRPL	The success value was chosen considering the state of the art in absorber material carrier density

Table 2. (continued) Status of milestones

1.4.1	5 (COMPLETE)	Film thickness, carrier density, and lifetime in CdTe:In film on CdTe:P	$5x10^{15}$ $cm^{-3;}$ minority carrier lifetime > 1 ns	Thickness by electron microscopy or profilometry; carrier concentration by Hall effect (on undoped CdTe) or C-V; lifetime by TRPL	This electron concentration should be achievable given 2020 results on CdTe:In films; lifetimes assumed similar to bulk crystals
1.4.2	7 (COMPLETE)	Film thickness, carrier density, and lifetime in CdTe:I film on CdTe:P	$5x10^{15}$ $cm^{-3;}$ minority carrier lifetime > 1 ns	Thickness by electron microscopy or profilometry; carrier concentration by Hall effect (on undoped CdTe) or C-V; lifetime by TRPL	Assuming similar performance for iodine dopant as for indium dopant.
1.4.3	10 (COMPLETE)	Characterized CdTe p-n homojunction	*n*-CdTe:(In or I)/*p*-CdTe:P devices (ITO front contact and Cu/Mo or Au back contact) with measured $n > 5\times10^{15}$ cm^{-3}, V_{oc} of >750 mV	Characterization by J-V (T), C-V, EQE Fabrication complete; desired performance not yet realized	The success value was chosen considering the state of the art in CdTe *p-n* homojunctions
EOP-A	12 (COMPLETE)	Measured device parameters, V_{oc}, efficiency	V_{oc} of 875±25 mV, efficiency > 10% Performance not achieved for efficiency, though V_{oc} was close for some devices	Average, standard deviation. At least 5 cells measured under standard conditions.	For V_{oc}, greater than observed in literature for homojunction, and is indicator that interface combination is low and junction is of good quality. Efficiency part assuming non-optimized thickness and contacts, but otherwise good junction and carrier lifetime.

6.1 Device modeling

In order to predict and understand homojunction device performance within the bounds of experimentally achievable material properties, we established a solar cell device model using Sentaurus Device software (Figure 3). By simultaneously solving the Poisson and electron and hole continuity equations, we were able to examine the relative benefits of growth parameter changes such as film thickness, surface preparation, and source and substrate temperatures that can have measurable effects on values such as J_{sc}, recombination velocity, carrier lifetime, and dopant incorporation and activation. In initial results, we found that, because we are placing the back contact on the opposite side of the *p*-type wafer from the emitter and front contact, greater wafer thicknesses lead to a reduction in photovoltaic (PV) device fill factor due to increased series resistance; as a result, wafers of thickness < 2 mm are preferred for use in device structures. We also examined device performance parameters as a function of Cd(Se)Te:In emitter thickness for different combinations of surface recombination velocity at the front interface (S_f), *n-p* junction interface (S_{int}), and back interface (S_b), as shown in Figure 4 (parameters used in the model are shown in Table 3). We found that J_{sc}, in particular, is increasingly adversely affected for emitter thicknesses exceeding ~200 nm for typically observed S values (as indicated by the green and red markers).

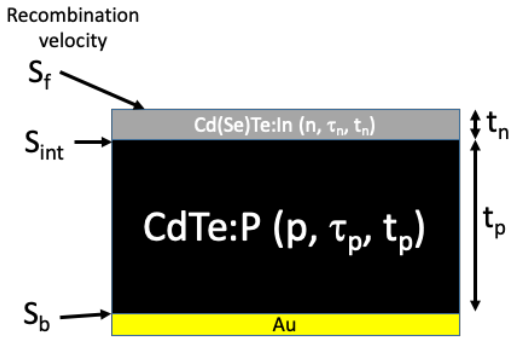


Figure 3: Cross-section of the homojunction device model structure established in Sentaurus Device software. Carrier concentration (n, p), carrier lifetime (τ_n, τ_p), and film thickness (t_n, t_p) were specified for the n-type and p-type semiconductor layers. Surface recombination velocities at the front (S_f), n-p junction interface (S_{int}), and back (S_b) were also specified.

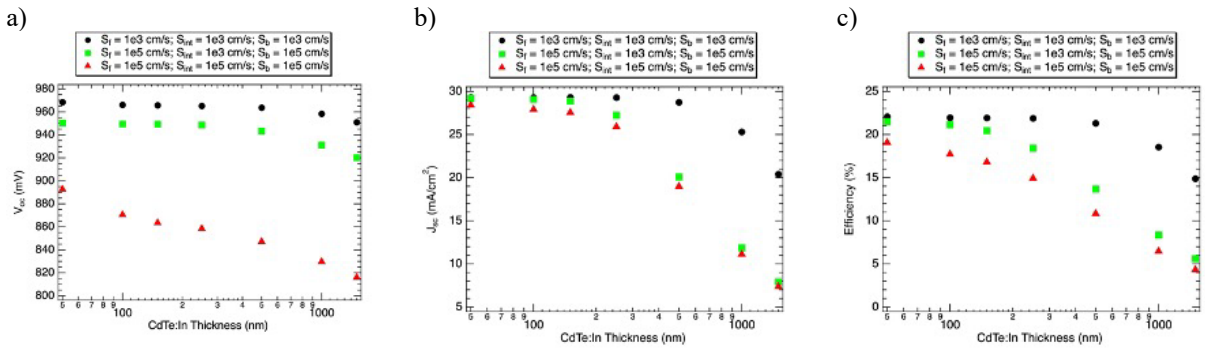


Figure 4: Device parameters as a function of film thickness for combinations of S_f, S_{int}, and S_b.

Table 3: Model input values used in generating the data shown in Figure 2.

Parameter	Value	Source
N	$9.15x10^{15}$ cm^{-3}	CdSeTe:In post-rapid thermal anneal measured Hall value
τ_n	10 ns	Film lifetime estimate
t_n	varied	Emitter thickness
p	$3x10^{15}$ cm^{-3}	CG168 CdTe:P wafer, measured Hall value
τ_p	20 ns	CG168 CdTe:P lower bound of measured carrier lifetime
t_p	1 mm	p-type wafer thickness
S_f	$1x10^3$, $1x10^5$ cm/s	Near-ideal and typical values
S_{int}	$1x10^3$, $1x10^5$ cm/s	Near-ideal and typical values
S_b	$1x10^3$, $1x10^5$ cm/s	Near-ideal and typical values

6.2 Film growth and characterization (CdTe:In, CdSeTi:In, CdTe:I films)

Cd(Se)Te:In films were deposited by close-spaced sublimation epitaxy (CSSE). A graphite boat was filled with Cd(Se)Te:In source material sieved to an approximate size of 250-1100 µm. Quartz spacers were used to suspend a CdTe wafer 2 mm above the source material. Finally, a graphite plate susceptor was positioned to be in thermal contact with the back surface of the CdTe wafer. The chamber was evacuated to ~$1x10^{-4}$ torr using an oil-sealed mechanical pump with a liquid nitrogen trap to prevent oil backstreaming into the deposition chamber. After evacuation, the chamber was backfilled with one of two growth ambients. When using a growth ambient of 8 torr N_2, the temperature of the source was ramped to 670-700°C while the setpoint of the substrate (wafer) was set to 200°C and allowed to warm naturally through thermal coupling with the source, reaching a temperature of ~550°C by the time of completion of the film deposition. Deposition times for thicker films, used for Hall and carrier lifetime measurements, were of 15 min. duration, leading to film thicknesses of 10-50 µm. For comparison, films were also grown in an ambient of 20 torr H_2. Lower source temperatures (645-665°C) and a higher substrate setpoint (625°C) were chosen based on previous experience with this growth technique and ambient. After growth, some films were subjected to additional rapid thermal annealing (RTA) to determine whether the In dopant could be further activated. These anneals were performed in Ar ambient for 2-5 min. at temperatures from 500-600°C using a 1 min ramp from room temperature to the setpoint.

Initially, thicker films were grown to facilitate two-photon excitation time-resolved photoluminescence (2PE TRPL) measurements. These films were also used to measure Hall effect. In general, it was found that films grown in H_2 ambient were of lower resistivity and higher carrier concentration than those grown in N_2 ambient. Characteristics of selected films are shown in Table 5. The resistivity and carrier concentration values of the thin CdTe:In film shown in Figure 5 are comparable to those obtained for the thicker films. This high carrier concentration for thin films is important when using these thin films in device structures. For the CdSeTe:In, (Figure 8) however, the thin film showed higher resistivity and lower carrier concentration values than those observed in thicker films.

6.2.1 CdTe:In films

Hall measurements were performed on Cd(Se)Te:In films to determine the carrier concentration and mobility of these films. In the case of the thicker films, soldered In contacts were used.

Pressed In contacts were used for thinner films (those <500 nm) to prevent thermal damage to the films. Hall results for CdTe:In are in Figure 5.

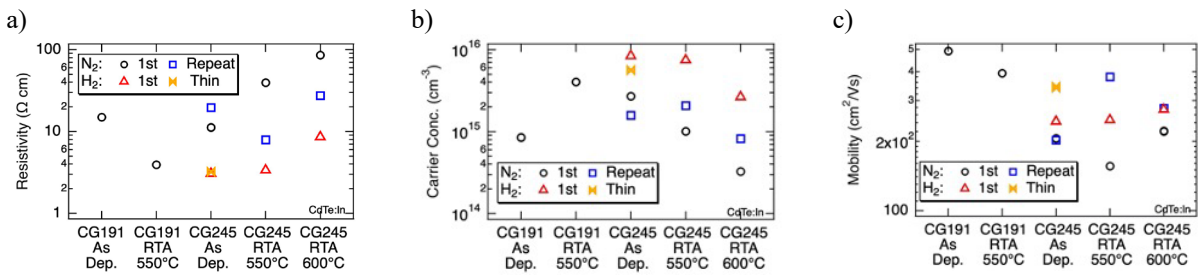


Figure 5: Hall results for CdTe:In films grown by CSSE on high-resistivity CdTe wafers. Resistivity, n-type carrier concentration, and carrier mobility are shown for as-deposited and RTA-treated films. CG191 and CG245 indicate that the films were grown using two different source materials. The symbols indicate different growth ambients (N_2 vs. H_2) and growth trials. "Thin" indicates films of thickness <500 nm, whereas other films were of 10-50 µm thickness.

Secondary Ion Mass Spectrometry (SIMS) was collected on two films to ascertain whether the desired amount of dopant was transferred from the crystal to the film during CSS. Films measured were those grown from CG245 (CdTe:In), deposited in N_2 or H_2 environments, and having or not having a rapid thermal annealing (RTA) treatment at 550°C. The results are shown in Figure 6. It can be seen that the In incorporation into the films is ~100%, slightly better with the H_2 environment. Therefore, the cause of poor electrical properties of these films cannot be dopant incorporation, but must be poor activation or contact issues. There is an apparent decrease in measured In near the substrate (dotted line based on the measured thicknesses of the films) which might indicate some interdiffusion, especially for the thicker film deposited in H_2.

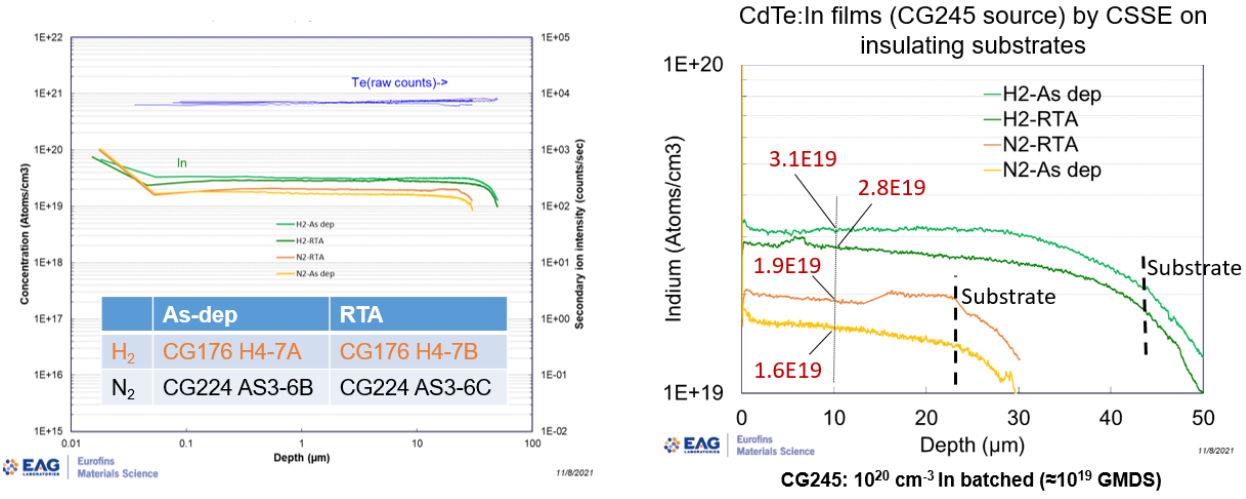


Figure 6: SIMS collected on 4 CdTe:In films. The sample name in the left Figure indicates the substrate (CG176 is high resistivity $Cd_{0.9}Zn_{0.1}Te$ and CG224 is CdTe). Note that the background In levels for both substrates is ~10^{17} cm^{-3}.

Previously, SIMS measurements were performed to verify the depth of In diffusion for a thin *n*-type CdTe:In film (~0.9 µm) deposited onto a p-type CdTe:P wafer, matching the general structure that was used in homojunction devices (though this test structure did incorporate a somewhat

thicker CdTe:In film than that typically used in devices). As discussed previously, In was found to diffuse to a depth of several µm (Figure 7), consistent with the observed buried homojunction behavior observed in JV and QE data (see section 6.5). The P profile was not presented at that time because of unexpected nonuniformity that was observed in the P depth profile. This nonuniformity has been confirmed through two additional repeated measurements (Figure 7). In all three cases, the P profile oscillates between P concentrations in the low-mid 10^{17} cm^{-3} range to values as low as the P detection limit of ~10^{15} cm^{-3}. Reasons for these significant changes in P concentration with depth remain unclear. The P concentration observed has not been correlated to any changes in crystallinity of the wafer (for example, grain boundaries or twinning), though this type of dependence is possible. Since the doping level of this crystal was ~10^{17} cm^{-3}, and it was grown Te-rich (sample #D in (McCoy et al., 2018); #3 in (Duenow et al., 2016)), it is possible that the fluctuations in P are from inclusions, either P segregating into the Te inclusions, or else P concentrating in the CdTe between the Te inclusions. The spatial extent of the fluctuations, ~1 µm by SIMS, is consistent with some of the precipitate sizes previously observed by infrared microscopy.

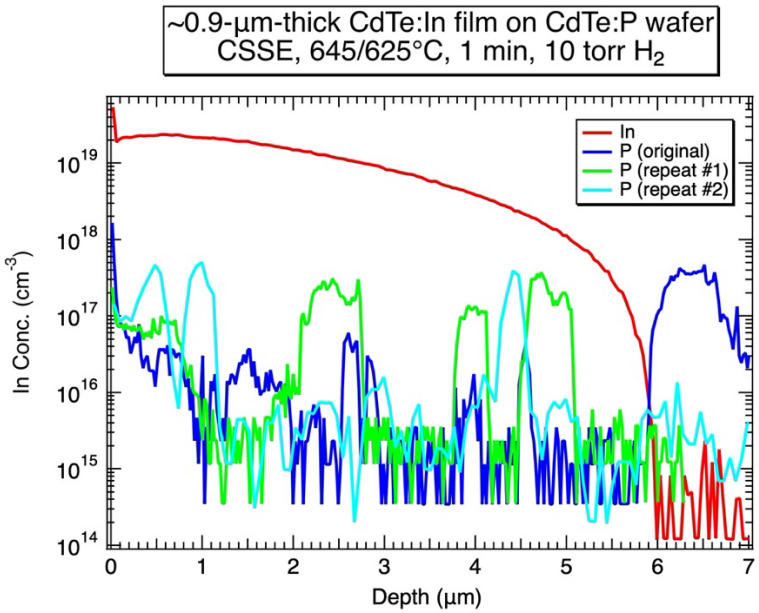


Figure 7: SIMS depth profile of ~0.9 µm thick CdTe:In film grown on a CG168 CdTe:P wafer. Indium diffusion to several µm depth occurs during film growth.

6.2.2 CdSeTe:In films

Hall measurements were performed on Cd(Se)Te:In films to determine the carrier concentration and mobility of these films. In the case of the thicker films, soldered In contacts were used. Pressed In contacts were used for thinner films (those <500 nm) to prevent thermal damage to the films. Hall results for CdSeTe:In films are shown in Figure 8 and summarized in Table 5.

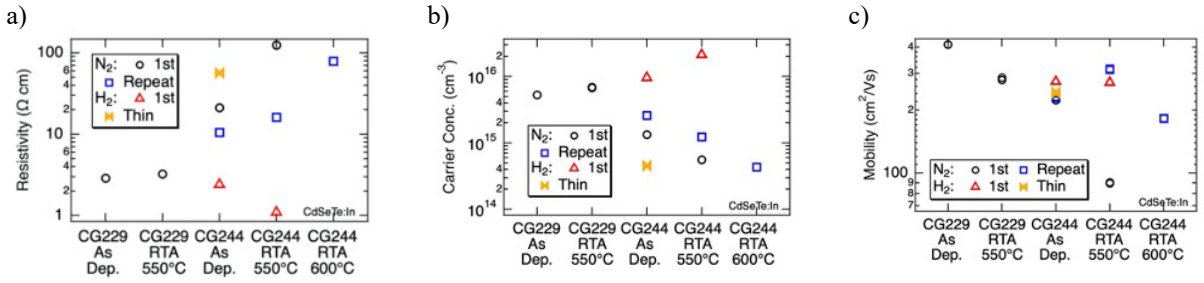


Figure 8: Hall results for CdSeTe:In films grown by CSSE on high-resistivity CdTe wafers, as described above.

6.2.3 CdTe:I films

CdTe:I films were deposited onto insulating CdTe wafers by close-spaced sublimation epitaxy (CSSE) using source material sieved to an approximate particle size of 250-1100 µm. The growth chamber was backfilled to 20 torr H_2. The temperature of the source was ramped to 665°C while the substrate (wafer) was ramped to 625°C. Deposition times of 15 min resulted in film thicknesses of 30-35 µm. After growth, some films were subjected to additional rapid thermal annealing (RTA) to determine whether the iodine dopant could be further activated. These anneals were performed in Ar ambient for 5 min at a temperature of 600°C using a 1 min ramp from room temperature to the setpoint.

Hall measurements were performed on CdTe:I films grown on insulating CdTe wafer substrates to determine their carrier concentration and mobility using soldered In contacts. Hall results for CdTe:I films grown from sources with three I levels are shown in Figure 9.

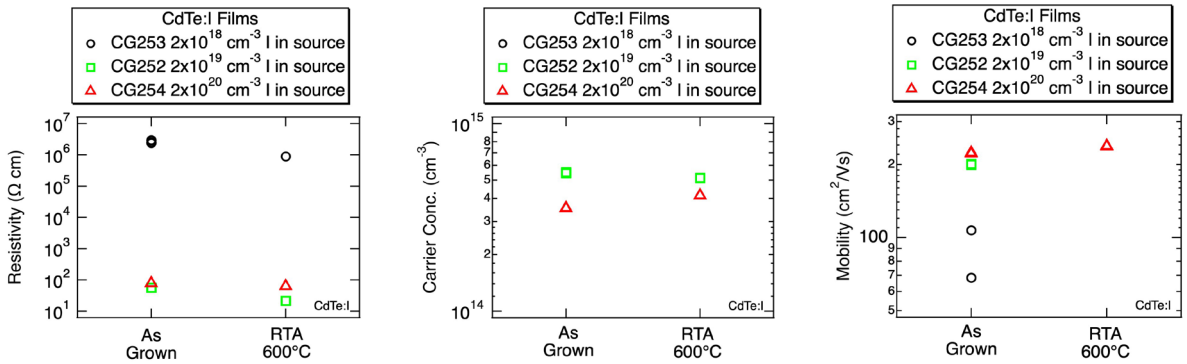


Figure 9: Hall results for CdTe:I films grown by CSSE. Resistivity, n-type carrier concentration, and carrier mobility are shown for as-deposited and RTA-treated films. Films with three levels of I dopant incorporated before crystal growth are indicated.

The film resistivity (Figure 9a) was found to be several orders of magnitude higher for the film grown using the source of lowest I concentration. This high resistivity prevented definitive carrier concentration and mobility values from being obtained for films grown from the source prepared using 2×10^{18} cm^{-3} I. The higher-concentration sources, however, enabled Hall measurements in most cases. Electron concentrations remained limited, however, to the mid-10^{14} cm^{-3} range, with electron mobility values of around 200 cm^2/V·s. Verification of the I content of the films is required before an estimate of carrier activation can be calculated. Rapid thermal annealing at

600°C did not result in any significant differences in carrier concentration, and associated carrier activation.

Secondary Ion Mass Spectrometry (SIMS) was conducted to measure the incorporation of iodine in thick films (Figure 10). Films made from all three iodine concentrations in the crystal were measured, as indicated in Table 4. The GDMS measurements indicate 5-10% of the iodine from the batch incorporates into the crystal. SIMS measurements indicate that, of the iodine in the crystal, 2-22% incorporate into the films. The moderate iodine content (CG253) has the highest film incorporation, and seems to behave the best electrically as a crystal (see section on CdTe:I crystals).

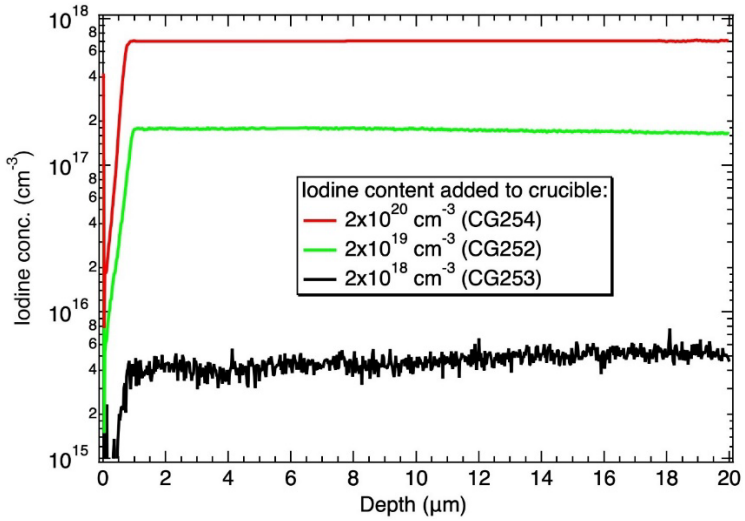


Figure 10: SIMS measuring iodine concentration in CdTe:I films

Table 4: CdTe:I film thicknesses and concentrations per SIMS compared to crystal concentrations

Wafer Name	Film source material	I dopant in melt (cm^{-3})	I dopant in crystal per GDMS (cm^{-3})	I dopant in film per SIMS (cm^{-3})	Film Thickness (μm)
CG236 AS3-2	CG253 heel CdTe:I	$2x10^{18}$	$2x10^{17}$	~$4x10^{15}$	29.0
CG236 AS3-3	CG252 heel CdTe:I	$2x10^{19}$	$9x10^{17}$	~$2x10^{17}$	33.1
CG236 AS3-4	CG254 heel CdTe:I	$2x10^{20}$	$9x10^{18}$	~$7x10^{17}$	35.3

6.2.4 Two-Photon Time Resolved Photoluminescence (2PE-TRPL)

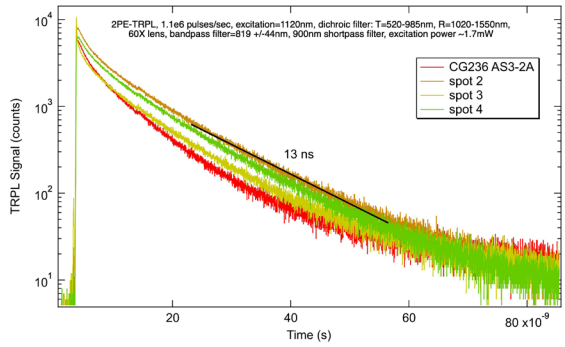
Two-photon time-resolved photoluminescence (2PE TRPL) measurements were conducted by Steven Johnston at NREL to estimate carrier lifetime. Measurement parameters used were: 1120 nm excitation wavelength, 1.7-10 mW power, $1.1x10^6$ pulses/s, using a bandpass filter centered at 819 nm. 2PE TRPL measurements were conducted on films of >10 μm thickness to enable the focus to be placed in the film, reducing contributions from film surfaces and the substrate; the vertical sampling distance of the technique is on the order of several μm; the vertical sampling distance of the technique is on the order of several μm. Lifetime estimates for all measured films are summarized in Table 5. Lifetimes for the CdTe:In CG245 films grown in N_2 are the longest measured. Examples of the raw data, here for CdTe:I films, are shown in Figure 11.

Table 5: CdTe:In, CdSeTe:In, and CdTe:I film parameters as measured by 2PE TRPL and Hall effect at NREL.

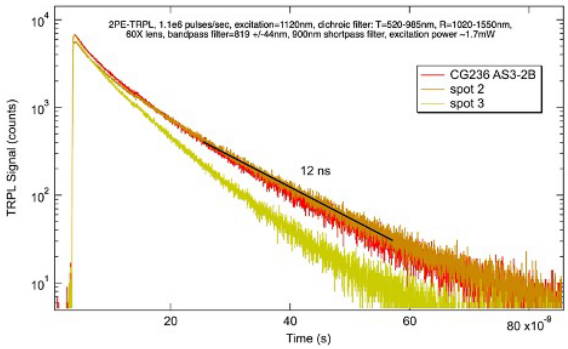
Sample	Substrate Wafer Name	Growth Ambient	Film Thick. (µm)	Processing	2PE TRPL Lifetime (ns)	Carrier conc. (cm^{-3})	Mobility (cm^2/Vs)
CG244 CdSeTe:In	CG224 AS3-3B	N_2	16.3	As deposited	51	$2.6x10^{15}$	232
CG244 CdSeTe:In	CG224 AS3-3C	N_2	20.1	RTA 550°C, 5 min	51	$1.2x10^{15}$	312
CG244 CdSeTe:In	CG224 AS3-2A	H_2	42.1	As deposited	53	$9.5x10^{15}$	274
CG244 CdSeTe:In	CG224 AS3-2D	H_2	42.1	RTA 550°C, 5 min	49 to 52	$2.1x10^{16}$	270
CG244 CdSeTe:In	CG242 AS5-4A	H_2	0.47	As deposited	-	$4.6x10^{14}$	240
CG245 CdTe:In	CG224 AS3-6B	N_2	20.7	As deposited	260 to 330	$1.6x10^{15}$	202
CG245 CdTe:In	CG224 AS3-6C	N_2	21.7	RTA 550°C, 5 min	230 to 560	$2.1x10^{15}$	380
CG245 CdTe:In	CG176 H4-7A	H_2	42.2	As deposited	51	$8.4x10^{15}$	244
CG245 CdTe:In	CG176 H4-7B	H_2	42.0	RTA 550°C, 5 min	54	$7.5x10^{15}$	247
CG245 CdTe:In	CG242 AS5-2B	H_2	0.46	As deposited	-	$5.7x10^{15}$	341
CG253 CdTe:I	CG236 AS3-2A	H_2	32.3	As deposited	13	$3.1x10^{10}$	88
CG253 CdTe:I	CG236 AS3-2B	H_2	35.4	RTA 600°C, 5 min	12	-	-
CG252 CdTe:I	CG236 AS3-3A	H_2	30.1	As deposited	65	$5.5x10^{14}$	200
CG252 CdTe:I	CG236 AS3-3B	H_2	30.4	RTA 600°C, 5 min	18	$5.1x10^{14}$	570
CG254 CdTe:I	CG236 AS3-4A	H_2	37.5	As deposited	35, 50	$3.5x10^{14}$	223
CG254 CdTe:I	CG236 AS3-4B	H_2	35.6	RTA 600°C, 5 min	40	$4.1x10^{14}$	238

NOTE: For wafer name, CGXXX is the WSU crystal growth number, AS# or H# is the position in the growth (axial section, heel, respectively), and -#letter is the sub-portion of the wafer used by NREL for the particular film

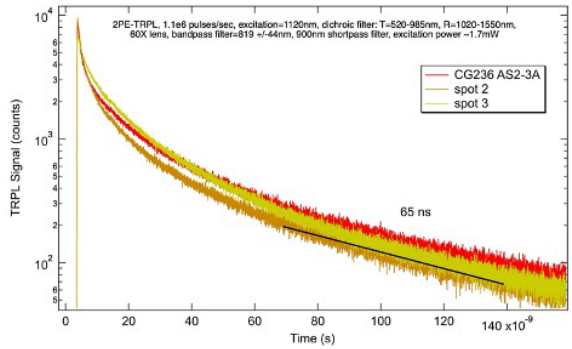
a) CG253, I conc. 2×10^{18} cm^{-3}, as dep.



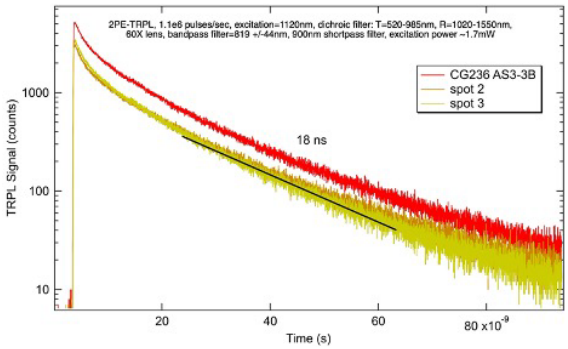
b) CG253, I conc. 2×10^{18} cm^{-3}, RTA 600°C



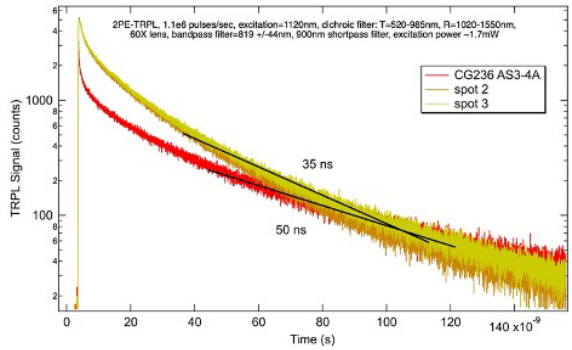
c) CG252, I conc. 2×10^{19} cm^{-3}, as dep.



d) CG252, I conc. 2×10^{19} cm^{-3}, RTA 600°C



e) CG254, I conc. 2×10^{20} cm^{-3}, as dep.



f) CG254, I conc. 2×10^{20} cm^{-3}, RTA 600°C

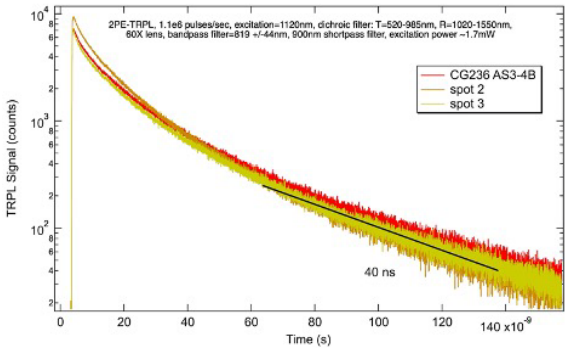


Figure 11: 2PE TRPL measurements and carrier lifetime fits for CdTe:I films as deposited and following a 600°C RTA. Iodine concentrations shown are batched intended concentrations in the crystals.

6.2.5 EBSD on Films Grown in H_2 Ambient

The electron backscatter diffraction (EBSD) technique was used to verify epitaxy of thin (< 1 µm) and thick (~50 µm) films grown onto CdTe wafer substrates. These substrates were either single crystalline or large-grain polycrystalline (with grain sizes on the order of several mm). Crystal orientation of the wafers was not known at the time of film growth. The orientations of both the wafers and films were identified when EBSD measurements were performed.

Three films grown under a CSSE atmosphere of 10-20 torr H_2 were examined. One thick film with a matte appearance and two thin films, one with a matte appearance and one with a specular

appearance, were the subjects of this study (Figure 12). For each sample, plan view SEM and EBSD were performed. Cross-sectional imaging was also performed for the matte samples.

a) CdTe:In film (matte, 42-68 µm), wafer CG176 H4-7

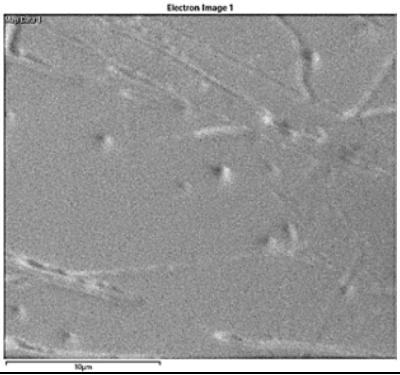
b) CdTe:In film (matte, 0.3-0.6 µm), wafer CG242 AS5-2

c) CdTe:In film (specular, 0.5-1.0 µm), wafer CG242 AS5-8

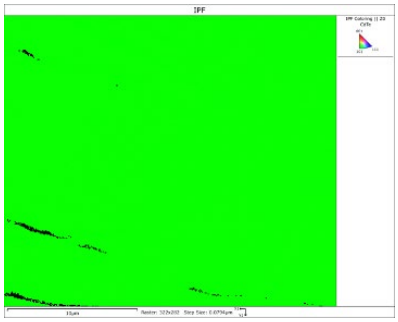
Figure 12: CdTe:In films grown by CSSE onto undoped CdTe wafer substrates.

The substrate for the thin specular film (Figure 13c) had a few macro-scale features as shown by SEM (Figure 13a). The substrate was indexed (Figure 13c) to an orientation near (101). After film growth (Figure 13, d-f), the inverse pole Figure and map match those of the substrate, indicating epitaxial growth of the CdTe:In film onto the CdTe wafer. Though CSSE films have been found to be epitaxial in the past (Colegrove et al., 2020), most have been tens of µm thick. This work confirms that much thinner epitaxial CSSE films can be grown.

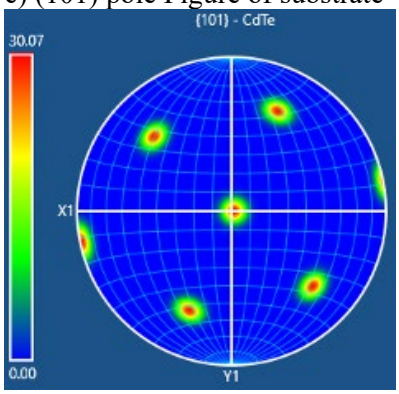
a) SEM plan view image of substrate



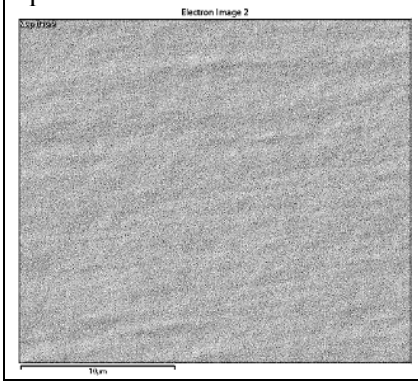
b) Inverse pole Figure map of substrate



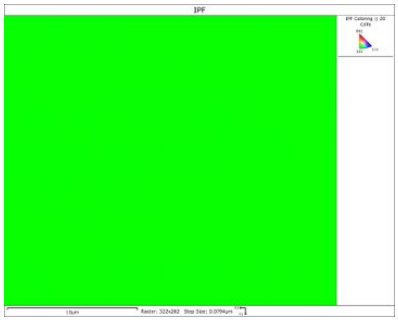
c) (101) pole Figure of substrate



d) SEM plan view image of thin specular film



e) Inverse pole Figure map of thin specular film



f) (101) pole Figure of thin specular film

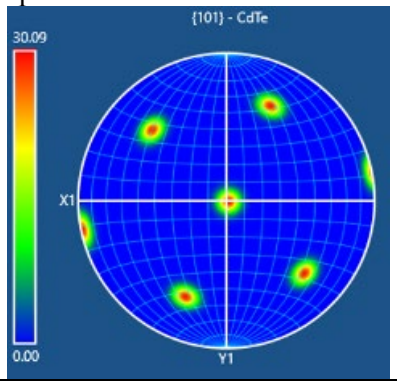


Figure 13: SEM and EBSD results for the thin specular film. Scale bars are 10 µm. The substrate is oriented ~1.1° off of (101). The film grows epitaxially on the substrate.

For comparison, a thin film of matte appearance was also characterized (Figure 14). The wafer upon which this film was grown was found to have a crystal orientation near (213). This matte film was found to have significantly higher roughness than the specular film, as seen in plan-view SEM (Figure 14d). Because of this roughness and the accompanying shading that occurred during measurement, the inverse pole Figure map (Figure 14e) includes non-imaged areas. Areas that were imaged, however, match the orientation of the substrate, implying that the matte-textured thin film grew epitaxially. To verify this, cross-sectional analysis was also performed (Figure 14, g-i). No interfaces are evident in the cross-sectional inverse pole Figure map (Figure 14h) and no misorientation is observed in the region of interest (Figure 14i), verifying epitaxial growth.

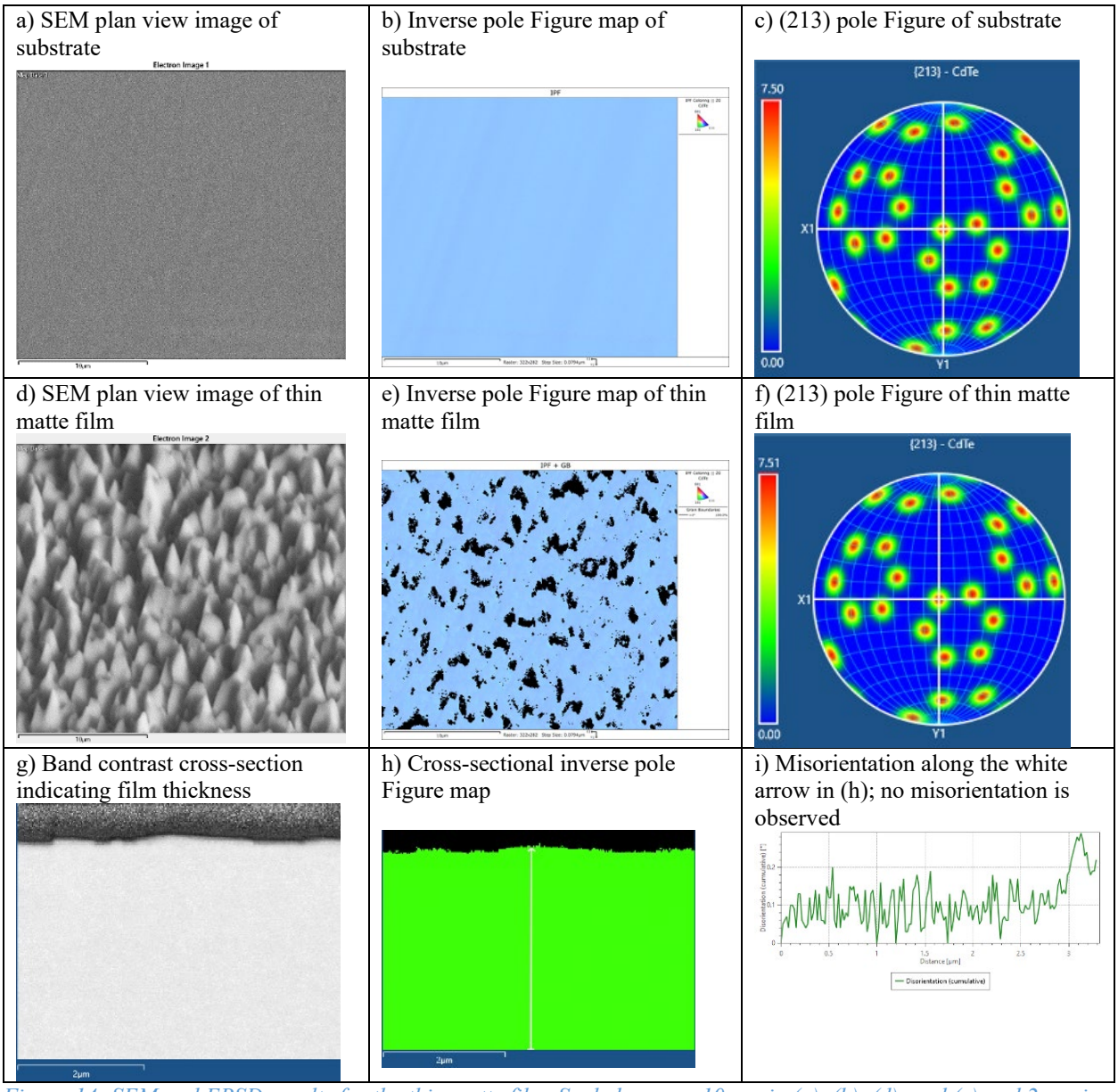


Figure 14: SEM and EBSD results for the thin matte film. Scale bars are 10 µm in (a), (b), (d), and (e) and 2 µm in (g) and (h). The substrate is oriented ~0.4° off of (213). The film grows epitaxially on the substrate. The black-colored areas in (e) denote areas that were not imaged due to shadowing from roughness.

A thick (> 50 µm) matte film was also examined (Figure 15). In this case, the substrate crystal orientation was found to be near (223). The roughness of this film was significantly higher than that of the thin matte film (Figure 15d). Again, the plan view inverse pole Figure map is incomplete because of shading during the measurement, but the area that can be imaged maintains a similar orientation to the substrate, implying epitaxial growth. A small-angle rotation between the substrate and film was suspected as a result of plan view measurements; cross-sectional measurements were performed to verify this behavior. An interface is visible in the band-contrast image (Figure 15g) between the film and substrate. The resolution of the inverse pole Figure map is insufficient to show this interface, but the misorientation profile from substrate to film (Figure 15i) shows a rotation of ~0.7° between substrate and film. Despite the angle offset, the film retains strong epitaxy.

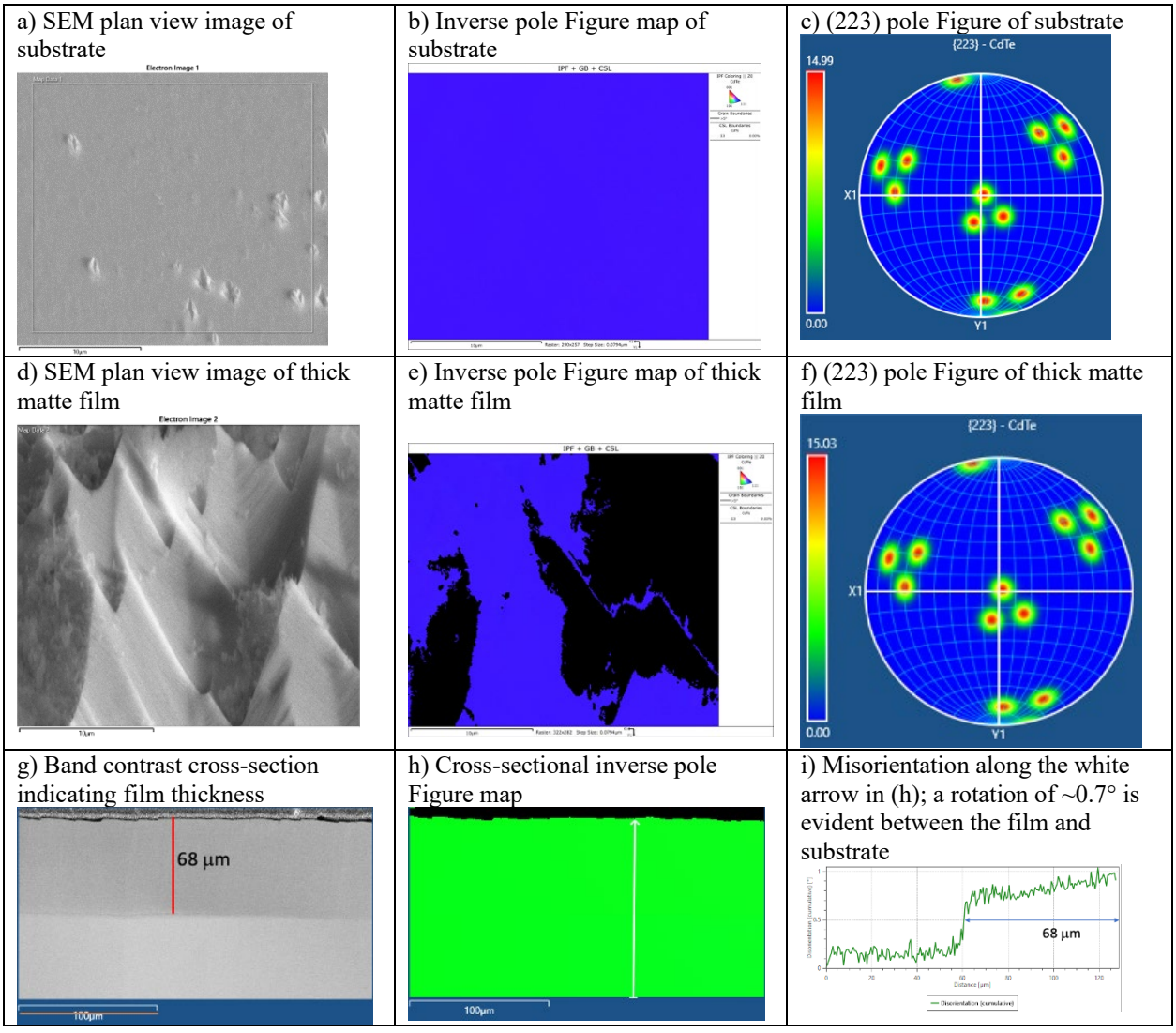


Figure 15: SEM and EBSD results for thick matte film. Scale bars are 10 µm in (a), (b), (c), and (e) and 100 µm in (g) and (h). The substrate is oriented ~1.8° from (223). The film grows epitaxially on the substrate with a misorientation of 2.4° from (223), implying a slight rotation between the film and substrate. The black-colored areas in (e) denote areas that were not imaged due to shadowing from roughness. Cross-sectional EBSD verified the ~0.7° rotation between film and substrate.

EBSD measurements were also performed on films grown in N_2 CSSE ambient (not shown). These films were also found to grow epitaxially. Homojunction devices were primarily fabricated using films grown under H_2 ambient, however, because initial work indicated higher Hall carrier concentration values for films grown under H_2.

6.3 Comparison of films and crystals: carrier concentration and lifetime

Below is a compilation and comparison of measured carrier concentrations and time-resolved photoluminescence (TRPL) measurements, the latter performed at NREL (see previous report for most of the data). In Figure 16 (all data) and Figure 17 (individual datasets) below, the blue line refers to the radiative limit assumption $\tau_R=1/(Bn)$, where τ_R is the recombination lifetime as measured by two-photon excitation (2PE) TRPL, $B = 1x10^{-10}$ cm^3/s, and n is the measured carrier concentration in cm^{-3} (see (Swain et al., 2019) for details). The datapoints show the measured values of n and τ_R from this project.

It can be seen that in most cases the RTA helps the carriers get closer to the radiative limit, but to date we do not know exactly what the RTA is doing, whether it is affecting the surface state and hence the ability to achieve good contacts for the carrier density measurement or whether it is changing dopant concentration or activation near the surface or something else. For CG245 crystals (CdTe:In, orange circles) the effect of RTA brings the points on the radiative limit line (in one case over the line). The CdSeTe as grown is very close to the line and with RTA is on the line.

For the N_2 grown films, the RTA does not seem to change the carrier behavior much, but there is a H_2 films it seems to improve carrier concentration a little. The films are still well below the recombination limit. The CdTe:In films shown are those investigated by the SIMS shown previously, so at least in the bulk of the film sampled by 2PE TRPL the measured indium concentration is much higher than the measured carrier concentration.

In can be seen also that in general the films have inferior carrier properties to the crystals relative to the radiative limit (Figure 17). This is apparent in the comparisons of CdTe:In (CG245), CdSeTe:In (CG244), and CdTe:I (CG254). The only possible exception is the CG252 CdTe:I, which behaved ‘out of family’ for the other tests as well. In general, the CdTe:I results were far away from the radiative limit, but as shown in the next section the Cd annealing greatly improved the carrier concentration, but lifetime is not yet measured for these samples.

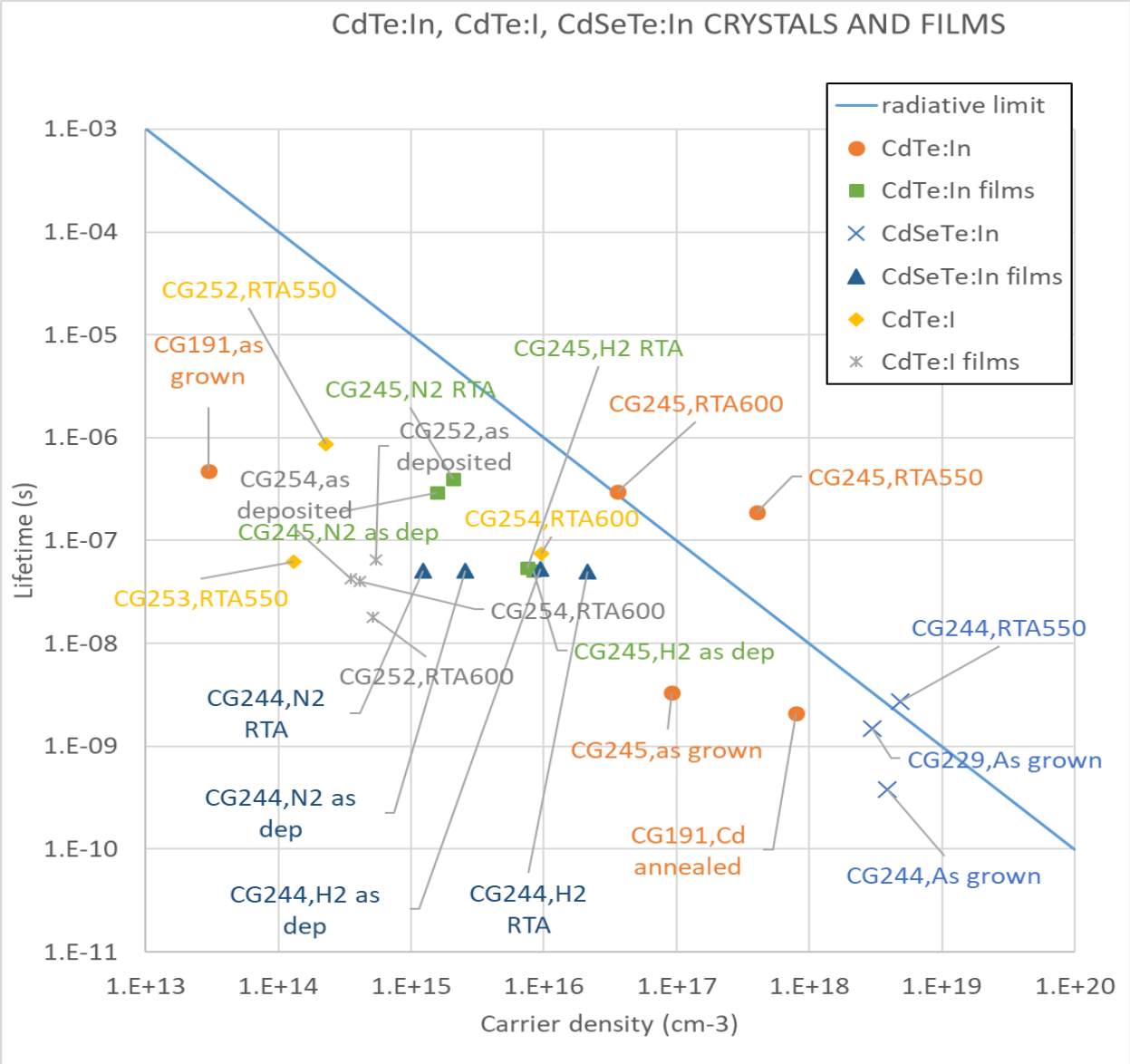


Figure 16: All data: Lifetime versus carrier density compared to the radiative limit (blue line). CdTe:In crystals are circles (CG245, CG191), CdTe:In films are squares (CG245), CdSeTe:In crystals are "X" symbols (CG229, CG244), CdSeTe:In films are triangles (CG244), CdTe:I crystals are diamonds (CG252, CG253, CG254), CdTe:In films are starts (CG253, CG254)

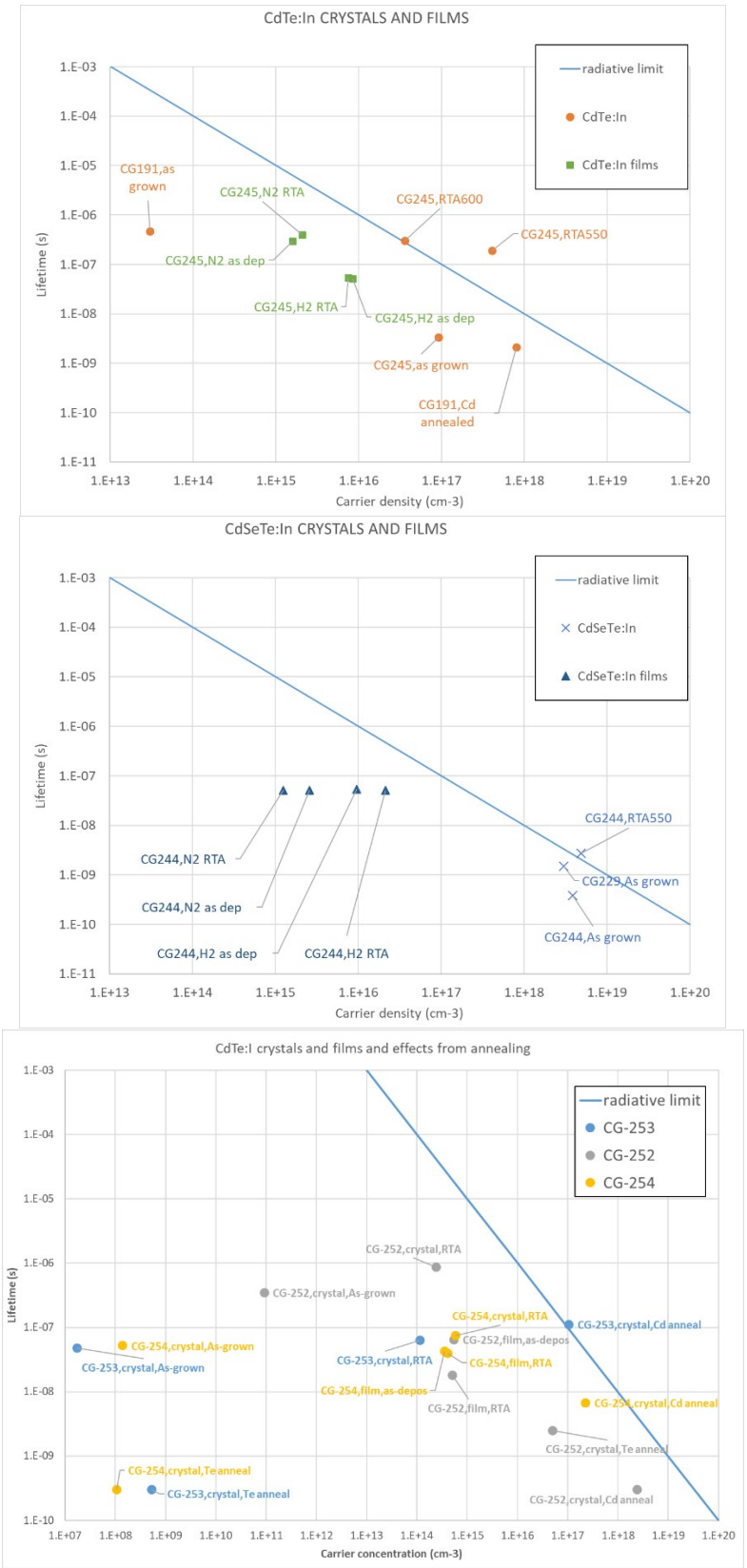


Figure 17: Separated data: Lifetime versus carrier density compared to the radiative limit (blue line).

6.4 Crystal growth: summary (CdTe:I, CdTe:In and CdSeTe:In crystals)

The results on the CdTe:I crystals were being written up in the MS Thesis in Materials Science & Engineering of student Samuel Bigbee-Hansen, who defended in May 2022.

Table 6 shows the summary of the n-type doped crystals grown at WSU, including the batched dopant concentration, measured concentrations by GDMS, and other growth details.

Table 6: Summary of crystal growth conditions and GDMS

Sample		**Dopant**	**[Dopant]-batched, cm^{-3}**	**[Dopant]-GDMS, cm^{-3}**	**Year grown**	**Incorporation (%)**	**Notes**
CG191	CdTe	In	$\approx 10^{19}$	$\approx 10^{18}$ (89,000 ppba)	2016	~10%	No crucible
CG245	CdTe	In	$\approx 10^{20}$	$\approx 10^{19}$ (610,000 ppba)	2021	~10%	No crucible
CG229	$CdSe_{0.4}Te_{0.6}$	In	$\approx 10^{19}$	$\approx 10^{18}$ (83,000 ppba)	2019	~10%	pBN crucible
CG244	$CdSe_{0.4}Te_{0.6}$	In	$\approx 10^{20}$	$\approx 10^{19}$ (1,000,000 ppba)	2020	~10%	No crucible
CG248	$CdSe_{0.4}Te_{0.6}$	In	$\approx 10^{19}$	n.m.	2021	n.m.	No crucible
CG256	$CdSe_{0.4}Te_{0.6}$	In	$\approx 10^{19}$	n.m.	2021	n.m.	No crucible, ACRT
CG237	$CdSe_{0.4}Te_{0.6}$	None	n.a.	n.a.	2020	n.a.	ACRT
CG249	$CdSe_{0.4}Te_{0.6}$	None	n.a.	n.a.	2021	n.a.	ACRT
CG253	CdTe	I	$\approx 2x10^{18}$	$\approx 2x10^{17}$ (17,000 ppba)	2021	~12%	No crucible
CG252	CdTe	I	$\approx 2x10^{19}$	$\approx 9x10^{17}$ (62,000 ppba)	2021	~5%	No crucible
CG254	CdTe	I	$\approx 2x10^{20}$	$\approx 9x10^{18}$ (640,000 ppba)	2021	~5%	No crucible

n.m. indicates not measured. n.a. indicates not applicable. ACRT is accelerate crucible rotation technique.

6.4.1 CdTe:In crystals

CG191 and CG245 were grown MVB furnace (electrodynamic gradient freeze furnace, EDG). Growth charges were prepared in a class 1000 clean room environment where CdTe of 99.9999% (6N5) purity material was measured in appropriate quantities and also taken In as dopant with concentration $8.82x10^{18}$ ($\sim 10^{19}$) cm^{-3} for CG191 and $1.15x10^{20}$ ($\sim 10^{20}$) cm^{-3} for CG245, respectively. The measured CdTe and In material were loaded into fused quartz tube. Before charging materials, quartz tube etched with hydrofluoric acid (HF) and dried at high temperature. An etched cap was inserted into the ampoule for sealing purposes. The ampoule was evacuated down to 10^{-8} mbar according to the pumping system and baked at ~300°C for a 24 h to remove residual gas and moisture. The ampoule was fused by rotatory burner torch. The sealed ampoule was then loaded onto the furnace after checking the vacuum seal on the ampoule. The furnace temperature was uniformly increased above the CdTe melt. After melting, the charge was soaked for 24 h and then temperature gradient moved from bottom to top by segment. The crystal growth rate was applied 2 mm/h for CG191 and CG245. The cool down process was started after crystallize the entire charge. Ingots were cooled down in steps. When the grown ingot reached room temperature, the ampoule was taken out from the furnace and the ingot was easily extracted.

As grown crystal and slice wafer are shown in Figure 18 for CG191 and Figure 19 for CG245, respectively.

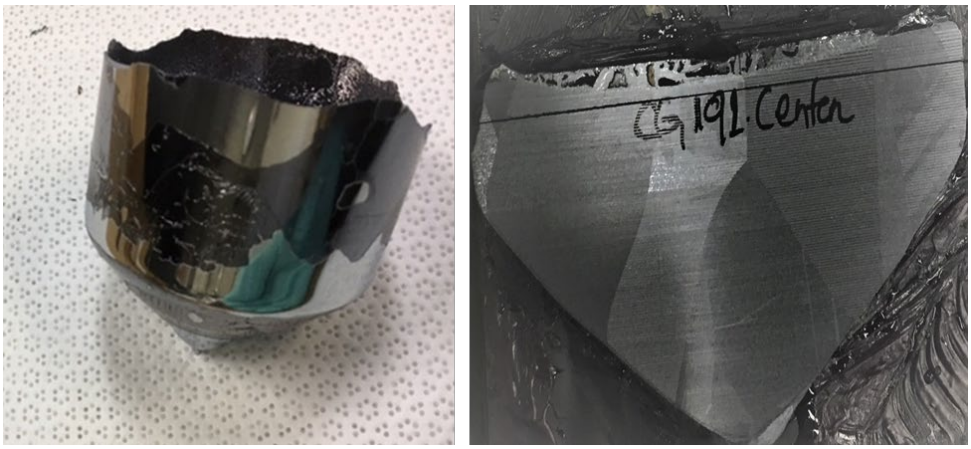


Figure 18: CG-191 ingot and wafer slice

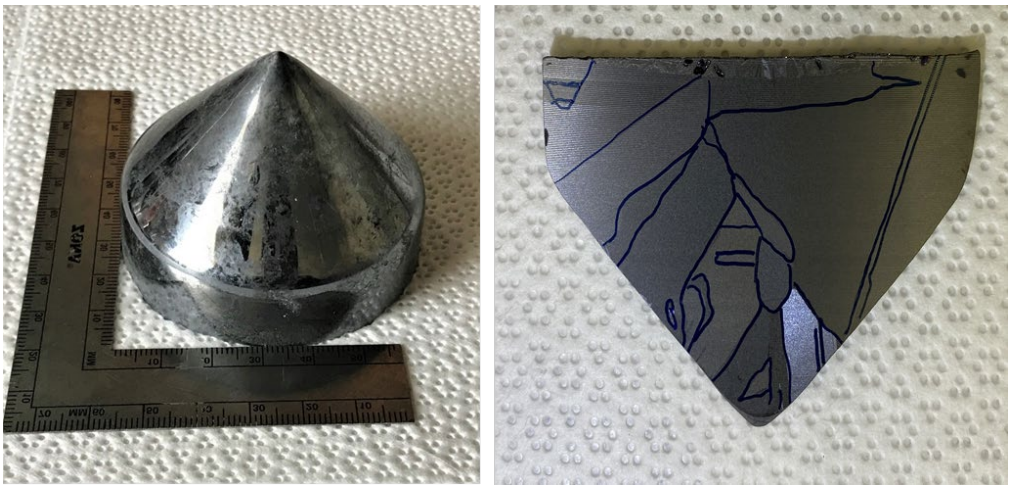


Figure 19: CG-245 ingot and wafer slice

The highly In doped (~10^{20} cm^{-3} as-batched, CG245) CdTe sample were cut and polished with 5x5x1 mm dimensions for Hall measurement. Hall measurement were carried out for three sample with varies conditions with soldered In contacts applied for the measurement. Some samples were processed with a rapid thermal annealing (RTA) (550°C or 600°C) before Hall measurement. The measured Hall values (resistivity, carrier concentration and mobility) are shown in Figure 20. The resistivity value is lower for the RTA samples compare to un-annealed as-grown sample. The carrier concentration is the same for both annealed samples, 3.5x10^{17} cm^{-3}. The mobility also increased for RTA at 600°C sample when compared to RTA at 500°C. Rapid thermal annealing improves the dopant activation by factor ~4 from the unannealed, qualitative activation percentage is ~1% based on GMDS concentration of In of ~10^{19} cm^{-3}. Further activation is expected from Cd overpressure annealing, similar to what was observed and published for CG191 (Swain et al., 2019).

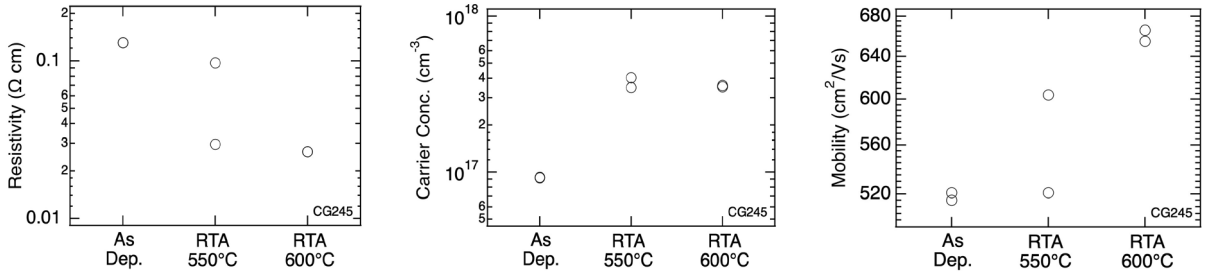


Figure 20: Hall measurements, CG245, performed at NREL as a function of RTA.

Additionally, Hall measurement were obtained at WSU using a different system, before and after Cd annealing. An indium contact was applied for CG191 and gold contact for CG245. It can be seen that the values with the Au contact are not likely reasonable due to the nature of Au as a Schottky contact on *n*-type CdTe (e.g., excessively high mobility, low carrier concentration). The CG191 BC2-8 and CG191-BC2-2 samples were annealed with Cd overpressure at 700°C for 16 h, and then samples were immediately quenched in water. Before annealing, the measured the resistivity, carrier concentration and mobility values were $1x10^{5}$ Ω·cm, $6x10^{12}$ cm^{-3}, and 10 $cm^2/V·s$, respectively. After annealing, resistivity, carrier concentration, and mobility are $1.4\ x10^{-2}$ Ω·cm, $1.4x10^{18}$ cm^{-3} and 300 $cm^2/V·s$, respectively. As seen in Table 7, The carrier density increased drastically after Cd annealing. Additionally, comparison with the NREL measurement shows the effect of the electrical contacts, where for the same as-grown crystal, NREL measured more than an order of magnitude higher carrier concentration, a more reasonable mobility, and lower resistivity. Cd annealing on CG245 appeared to decrease the conductivity, affecting mostly the mobility.

Table 7: Hall data for CG191 and CG245, measured at WSU and NREL

	CG 245 (no anneal) (In soldered contact, NREL)	**CG 245 (no anneal) (Au contact)**	**CG 245 (Cd anneal @700°C 16 h (Au contact)**	**CG 191 (no anneal) (In contact)**	**CG 191 (Cd anneal @700°C 16 h) (In contact)**
All MVB (no ACRT)	**CdTe:In**	**CdTe:In**	**CdTe:In**	**CdTe:In**	**CdTe:In**
Batched In (cm^{-3})	$\approx10^{20}$	$\approx10^{20}$	$\approx10^{20}$	$\approx10^{19}$	$\approx10^{19}$
GDMS In (cm^{-3})	$\approx10^{19}$	$\approx10^{19}$	$\approx10^{19}$	$\approx10^{18}$	$\approx10^{18}$
ρ (Ω·cm)	$1x\ 10^{-1}$	$6x\ 10^{0}$	$7x\ 10^{1}$	$1\ x10^{5}$	$1.4\ x10^{-2}$
n (cm^{-3})	$9x10^{16}$	$5x10^{15}$	$8x10^{15}$	$(6\text{-}30)\ x10^{12}$	$10^{17}\text{-}10^{18}$
μ ($cm^2/V·s$)	518	2000	76	~10	300-850

The resistivity in CdTe CG245 is and it increases after annealing. One of the probable reasons is the formation of some closed-to mid-bandgap point defects, which is formed after annealing and may causing the pining of the Fermi level and hence a change in resistivity. CG191 annealing cause a big drop ~10^7 orders in resistivity. Cd overpressure causes compensation in vacancies as well as A-centers which cause a drop-in resistivity. The mobility data for the single crystals are higher or almost the same order as polycrystalline samples.

In Cd annealed CG191, the mobility is improved after annealing from 300 $cm^2/V·s$ to 850 $cm^2/V·s$. Most probably some traps are annealed-out, which may increase the lifetime and mobility of the charge carriers. In case of CG245 the material seems more *p*-type, annealing decreases the hole

mobility as well. As mentioned before, the low-temperature additional phase formation is more likely. It may be In_2Te_3 phase around 400°C, due to excess of In and Te. One more chance is the formation of more hole traps, called A-centers. As a result, as compared to CG191, the decrease in the mobility and a negligible change in the hole density. Overall the carrier density increased after annealing.

IR- spectroscopy was performed for CG245 ~10^{20} cm^{-3} In, and CG191 (before and after annealing at 700°C@16h). CG245 (Figure 21, Figure 22) sample behaved differently than CG191 (Figure 23). Instead of solid shaped Te- inclusions, some diffuse inclusions were observed in CG245. This may be the additional low-temperature InTe-related phase generated on cooling during crystal growth of 10^{20} cm^{-3} In growth. The IR patterns may be due to extra absorbance or scattering due to the new induced phases during the growth, which may have reduced the IR transmission at 941 nm.

To study the effect of heating on these phases, some annealing at 700°C for 12 h with Cd overpressure has been performed for CdTe:In CG245 (Figure 21 and Figure 22) as compared to CG191 (Figure 23) with an order of magnitude less In. After annealing CG245, the diffuse Te phases (or other highly absorbing phases) are reduced in size, or break down to small pieces. Some areas are clean and no defect can be seen (Figure 22). Comparing the two levels of In dopants, it can be seen clearly that lower level has clear IR signal and Te inclusions, while the second has unclear and diffuse patterns. In addition, the inclusions in both cases are annealed out to some extent.

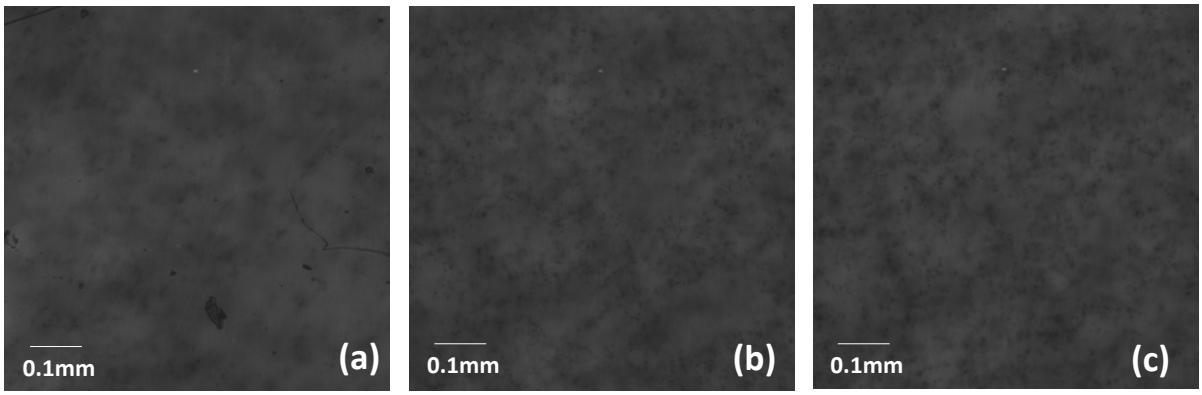


Figure 21: IR images for the CG245-AS2-3, a) as-grown sample and b), c) at two different depths.

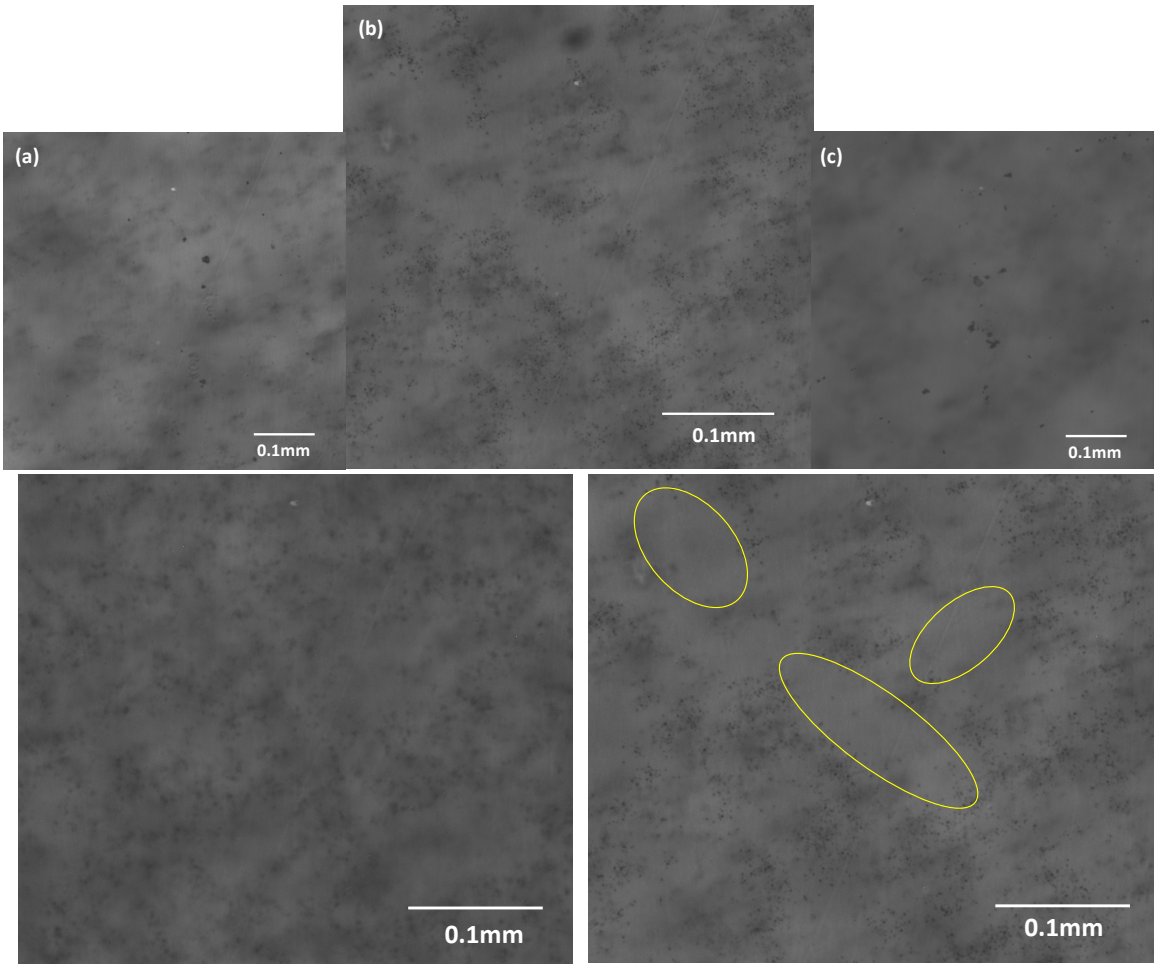


Figure 22: IR images for the CG245-AS2-3, CdTe:In, annealed at 700@12h. a) and c) are surfaces, and c) is in the middle of the sample, small fogy phases in b), and pure- Te inclusions at the surfaces; bottom: IR images for the CG245-AS2-3, CdTe:In, (left) as grown and (right) annealed with Cd overpressure 700°C@12 h. Te- annealed out are in yellow regions.

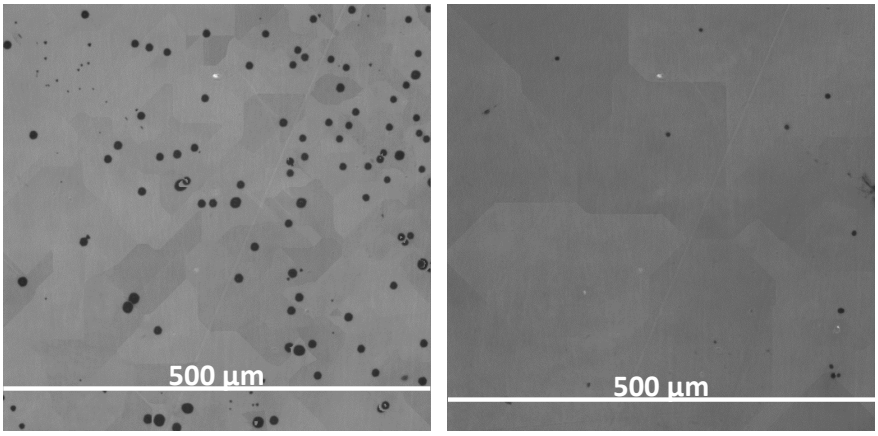


Figure 23: IR images for the CG191-AD2-5, CdTe:In, as grown sample a) Annealed at 700°C@16h (from (Swain et al., 2019))

2PE-TRPL (Figure 24) was performed at NREL using 1120 nm excitation, ~8 to 10 MW, 1.1x10^6 pulses/sec, dichroic R=1020-1550 nm, T =520-985, bandpass filter centered 819 nm, and 60x lens. Lifetimes increased from 2.9-3.8 ns (as-grown, CG245-AS2-9A) to 170-210 ns (RTA, 550°C, CG245-AS2-9B) to 280-320 ns (RTA, 600°C, CG245-AS2-9C). The significance of these results is currently being reviewed. Note for example the short lifetime component and additional long lifetime component one spot in the as-grown sample in Figure 24. The post-RTA behavior shows lifetimes approach radiative limit depending on the carrier concentration assumed.

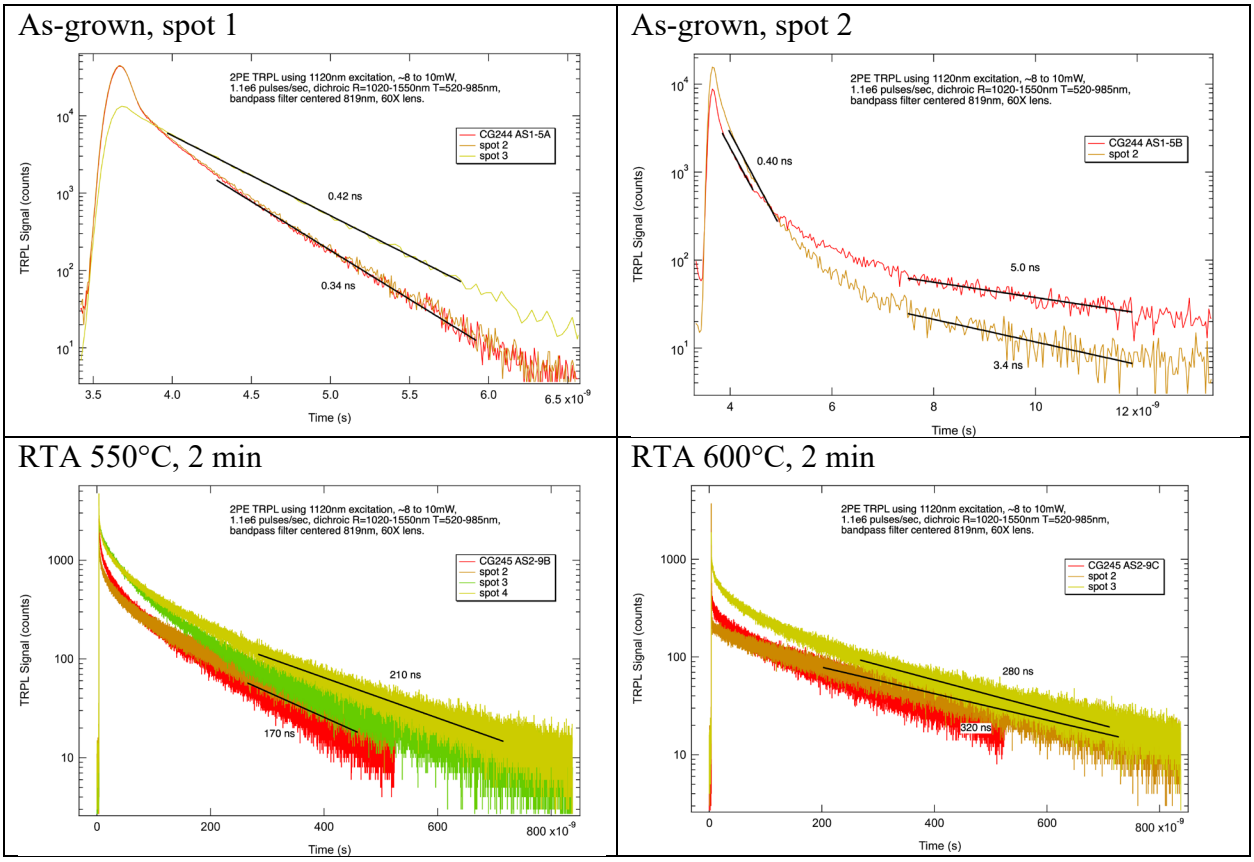


Figure 24: TRPL on CdTe:In, CG245 as-grown and RTA conditions.

6.4.2 *CdSeTe:In crystals*

Bulk single crystals of $CdSe_{0.4}Te_{0.6}$:In (CST) were grown by using the Modified Vertical Bridgman Method (MVB) by adding elemental indium (In), with dopant level from ~1×10^{18} to 1.5×10^{20} cm^{-3}, to CdTe and CdSe. 6N (99.9999%) high purity binary compounds and dopants were used for the crystal growths. In the class 1000 clean room facility, the charge preparation was done in an Ar flow bags. Ampoules, lids and crucible were etched with 20% HF solution for 20 minutes. The crucibles were sealed under high vacuum of ~10^{-8} torr. The ampoule sealing was checked by using cross polarizers. When the ampoule was ready, it was carefully aligned and loaded into the MVB-furnace. One of the temperature profiles employed for the crystal growth is shown in Figure 25. The maximum temperature was kept at 1150°C. The diameter and length of the ingots grown are

typically 62 mm, and 100 mm, respectively. The MVB crystal growth takes 10 to 13 days depending on the crystal growth rate, e.g., 1-2 mm/h. The list of the CdTe and CdSeTe crystal growths is provided in
Table 8.

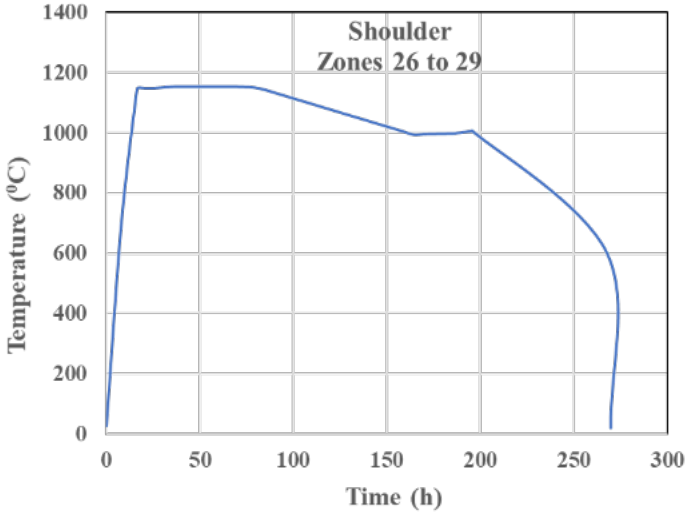


Figure 25: Typical temperature profile used for the CST and CdTe crystal growths.

CG237 is an undoped CST, and the same parameters were used to produce a new crystal as CG249. Similarly, CG229 was CST:In-1x10^{19} cm^{-3} and a new crystal was grown as CG245 for this project. All the growths which are used in the current project are shown in Figure 26. The undoped CST crystal quality was comparatively uniform and homogeneous than the doped one.

- CG256 (CST:In) was mostly polycrystalline. In addition, crystals were more porous as compared to CG244.
- CG248 (CST:In) ingot had mixed (i.e., large and medium) sized grains. The crystal growth quality was good as compared to CG256 and CG244, with some porous region at the tip.
- CG244 (CST:In) again has a mixed grain size. The crystal growth quality was comparatively poor compared to CG237.
- CG191 (CdTe:In) had large and medium sized grains. The twins along the growth direction can be seen in Figure 26. The crystal growth quality was uniform and homogeneous.
- CG245 (CdTe:In) had some big grains. The crystal growth quality was comparatively uniform and homogeneous.

Comparing the crystal quality of all these growths, it is concluded that the use of pBN inside the quartz ampoule improves the quality of the crystal by improving the homogeneity and uniformity, which as a result increases the single crystal yield.

In CdTe crystal growth, the quality of the crystals is better than for CST ingots. Although Se has uniformity along the growth and has a smaller segregation coefficient than Zn in CZT (Roy et al., 2014). However, our CST crystal quality is not as high as those reported by Brookhaven National Lab (e.g., above); however, these crystals had at most 10% Se, not 40% Se as our growths.

Table 8: List of *n*-type CST crystal growths. (*) are pre-project growths.

Growth	Compound	Crystal Growth
CTS		
237	CST-undoped	ACRT-MVB with pBN crucible (*)
249	CST-undoped	ACRT-MVB (re-growth of CG237)
229	CST: In-10^{19} cm^{-3}	MVB with pBN crucible (*)
248	CST: In-10^{19} cm^{-3}	MVB (re-growth of CG229)
256	CST: In-10^{19} cm^{-3}	ACRT-MVB
244	CST: In-10^{20} cm^{-3}	MVB

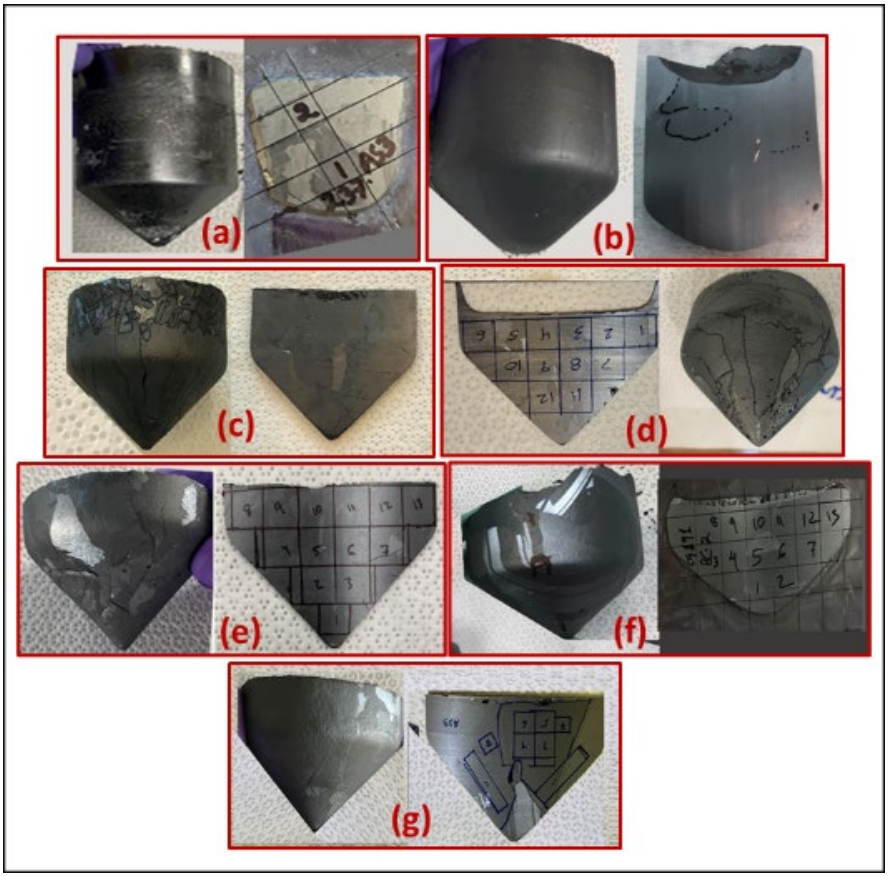


Figure 26: Pictures of ingots and axial wafers. All CST unless otherwise noted. a) CG237, b) CG229, c) CG256, d) CG248, e) CG244, f) CG191 (CdTe:In), and g) CG245 (CdTe:In).

Crystal ingots, after sand blast and cleaning, were cut into ~2 mm thick, axial as well as radial wafers, by using the programmed electric wire saw. Each wafer was further cut into ~10x10x2 mm^3 samples, which were polished with Al_2O_3 particles solution by using electric spinners and particular grid papers. Wafers were further clean with deionized water and ethanol/ methanol. For bulk electrical crystal characterization, polishing was done on all 6 sides, while for use as substrates or for structure and morphology characterizations, only 2 sides were polished. On bulk wafers, contacts were fabricated by using different procedures, including sputtering and different time-temperature recipes on a hotplate. For Hall experiments, the 4-point contacts were ~1 mm at the corners, either Au or In dot contacts.

CST and CdTe crystals and devices were tested for crystal quality and performance by using variety of characterization experiments. The techniques included current-voltage (IV), infrared (IR) microscopy, photoluminescence (PL) mapping, Hall measurements, X-ray diffraction (XRD), 2PE-TRPL, and scanning electron microscopy (SEM) with energy dispersive spectroscopy (EDS) and electron backscatter diffraction (EBSD). The details are as follows.

The resistivities, shown in Table 9 for the CST growths are evaluated from the IV characteristic plots. Planar samples with 1-2 mm thickness were fabricated by sputtering Au on two planar sides. Other measurements were obtained by NREL on CG244 using Hall effect with pressed or soldered indium contacts. Considerable differences are seen depending on the contacts, with lower resistivities measured for indium contacts.

Table 9: Resistivity data obtained for the CST crystal growths, WSU and NREL, contacts indicated. WSU measurements are through-thickness resistivity, NREL measurements are Hall effect

		Resistivity (□-cm)		
Growth	**Compound**	**WSU (Au, sputtered)**	**NREL (In, pressed)**	**NREL (In, soldered)**
237	CST	$6x10^{6}$	n.m.	n.m.
229	CST: In-10^{19} cm^{-3}	$<10^{0}$	n.m.	n.m.
256	CST: In-10^{19} cm^{-3}	n.m.	n.m.	n.m.
248	CST: In-10^{19} cm^{-3}	n.m.	n.m.	n.m.
244	CST: In-10^{20} cm^{-3}	$<10^{-1}$	$2.2x10^{-3}$	$2.3x10^{-3}$

n.m. indicates not measured

It has been reported previously that In doping of CdTe is associated with self-compensation, depending on the In concentration. In our doped crystal growths, it was observed that 10^{20} cm^{-3} In level makes no improvement in charge carrier density. To improve the carrier density and mobility in the doped crystals, some annealing experiments under Cd- and Se- over pressure were performed.

Annealing under Se and Cd overpressure was performed on CG229. It was observed that annealing improved the resistivity as well as other charge transport properties. As-grown undoped CdTe crystal are typically *p*-type due to Cd vacancies, whereas as-grown undoped CdSe is known to be *n*-type due to Se vacancies.

To test this, CG229 samples were annealed under a Se overpressure condition in an evacuated and sealed quartz ampoule. The Se source was maintained at a temperature of 500°C, whereas the temperature of the $CdSe_{0.4}Te_{0.6}$:In sample was kept at a higher temperature of ~570°C to avoid elemental Se deposition on the sample surface. The Se overpressure was $\sim 5x10^{-2}$ atm, corresponding the temperature of the Se source. The resistivity increased from 0.9 to 75 Ω·cm.

In order to confirm that the observed *n*-type conductivity in CdSeTe:In is due to indium and not due to Se vacancies, an undoped CST crystal (CG237) was grown with the same Se composition as CG229, CdSeTe:In. The undoped crystals showed a resistivity of $\sim 6\times10^{6}$ Ω·cm compared to <1 Ω·cm for CdSeTe:In, suggesting that Se vacancies cannot account for the high electron

concentration in CdSeTe:In. A comparison of IV charateristic plots and resistivity is shown in Figure 27.

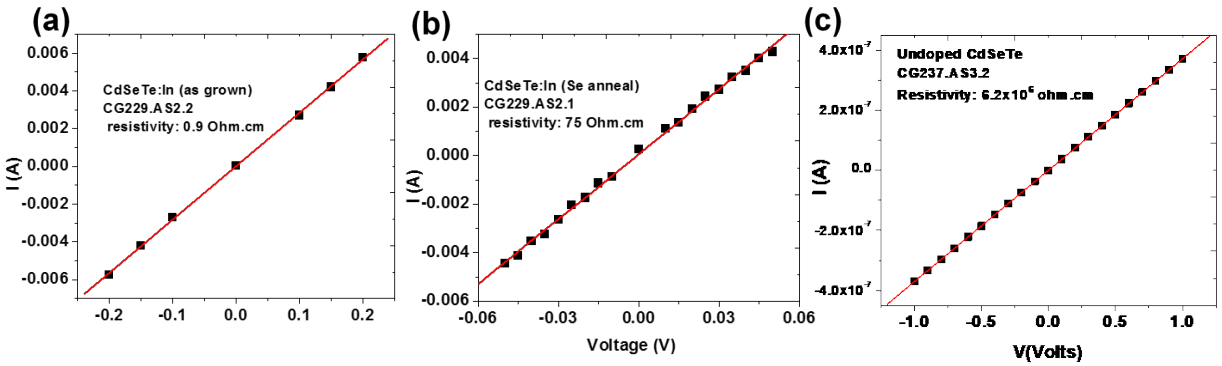


Figure 27: Two probe I-V measurements on (a) $CdSe_{0.4}Te_{0.6}$:In, as-grown (CG229); (b) CdSeTe:In, Se overpressure annealed (CG229); and (c) undoped $CdSe_{0.4}Te_{0.6}$ (CG237).

For CG244, rapid thermal annealing (RTA), same conditions as previously described, was performed at NREL. Data is shown in Figure 28. It appears that the RTA did not have sigificant effects, positive or negative, on the carrier properties of highly In doped CST.

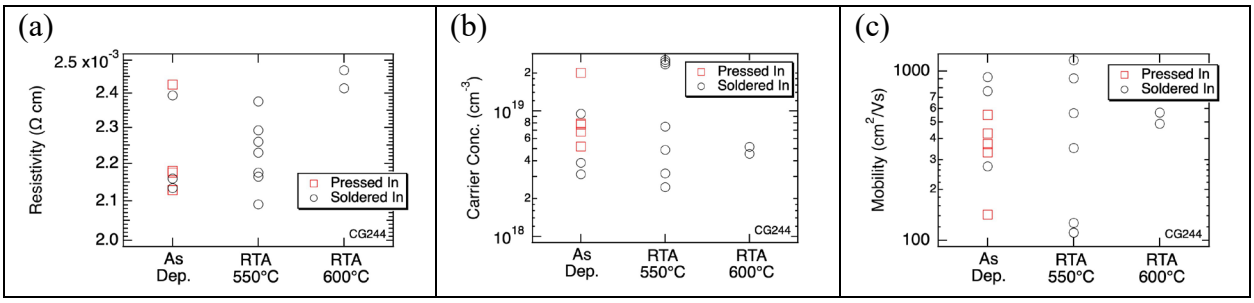


Figure 28: Hall effect on CG244, CdSeTe:In high doped, showing resistivity, carrier concentration, and mobility.

Hall experiments were performed at WSU on CST crystals, observed as "single" or "polycrystalline." Au sputtered contacts were used for these measurements. The data is recorded in
Table 10. GDMS was also performed to compare the In density with the incorporated dopant level during the growth. The comparison of In indicated that during the growth only about 10% of the batched indium is incorporated in the crystal, similar to CdTe. Resistivity data from Hall measurements shows that polycrystalline samples have higher resistivity values as compared to the single crystal samples, as expected. It seems crystals are becoming more conducting with increasing In incorporation. In the undoped CST sample, the Se-annealing may generate additional Cd vacancies and material becomes more resistive (Figure 27b).

CG244, due to its higher *n*-typed dopant level, is more conducting and has comparatively higher mobilities of ~ 232 $cm^3/V{\cdot}s$. CG237 the undoped polycrystalline CST have the lowest ~ 0.6 $cm^2/V{\cdot}s$, in all CST. Note that all measurements with Au contacts will have to be rechecked with other contacts which are likely to be more ohmic. Values with the Au contact may not be reasonable due to the possible nature of Au as a Schottky contact on *n*-type CdTe. Particularly suspect are data obtained on CG237.

Table 10: CST:In and effect on resistivity, mobility and free- carrier concentrations. Measurements performed at WSU with Au contacts.

Description	CG237		CG229		CG244	
	Poly-crystalline	Single Crystal	Poly-crystalline	Single Crystal	Poly-crystalline	Single Crystal
Batched (cm^{-3})	Undoped		$\approx 10^{19}$		$\approx 10^{20}$	
GDMS (cm^{-3})	n.a.		$\approx 10^{18}$		$\approx 10^{19}$	
In- incorporation	n.a.		~10%		~10%	
ρ (Ω-cm)	3.82×10^{7}	2.02×10^{7}	6.27	6	0.28	0.08
μ ($cm^2/V \cdot s$)	0.622	6.19	104	2×10^{3}	85	232
Density (cm^{-3})	9.87×10^{21}	5.80×10^{10}	1.27×10^{16}	5×10^{15}	1.58×10^{17}	1.94×10^{18}

The wafers used for the PL mapping are shown in Figure 29. In mapping for CG237 wafer, a 635 nm excitation wavelength with a 50 μm step size was used to collect the spectra. As for mapping, the individual frames were ~2 mm, corresponding to about 4 microns per pixel, with a total of 384x512 pixels. Only a single peak was observed in CG237 wafer. The energy and intensity PL images for CG237 are shown in Figure 30. The energy variation is between 1.390 to 1.392 eV, which indicates the material homogeneity and uniformity. The intensity mapping shows large grains a few twins along the growth direction, which are emerging from the lower right side of the wafer.

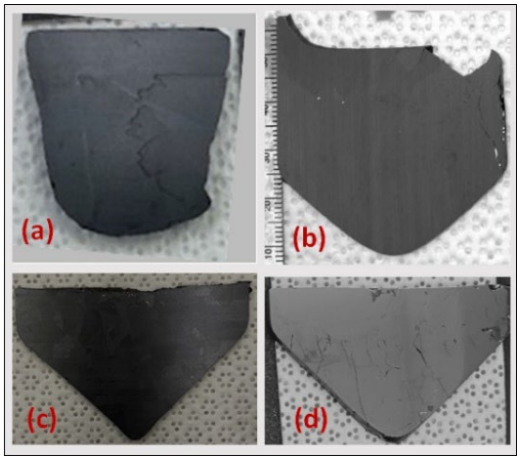


Figure 29: Wafers used for PL mapping and EDS and EBSD of CTS, a) CG237, b) CG229, c) CG244, and d) CG248.

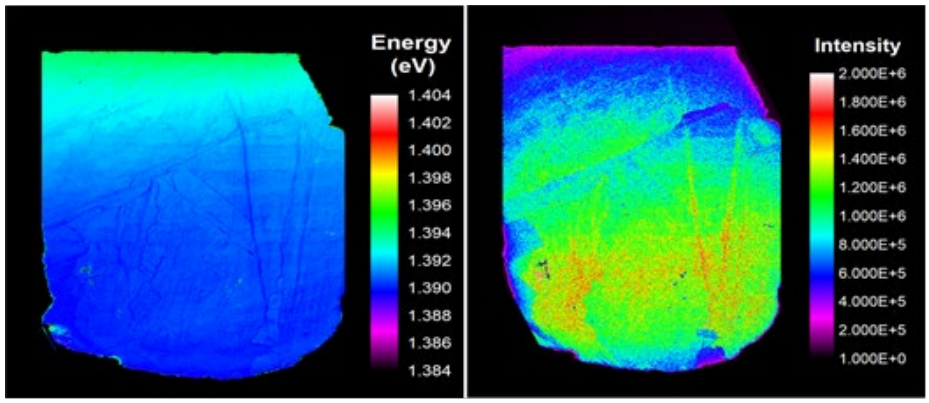


Figure 30: CG237 (undoped CTS) PL mapping for energy (left) and intensity (right) distributions.

In CG229, the maps show complex behavior, with very sharp changes appearing in the energy maps. The intensity maps suggest some form of defect like twins aggregating along grain boundaries. PL mapping is shown in Figure 31. In the energy map a small region in the tip and most of the heel region are homogeneous. The conical region has a mix of single and polycrystalline material.

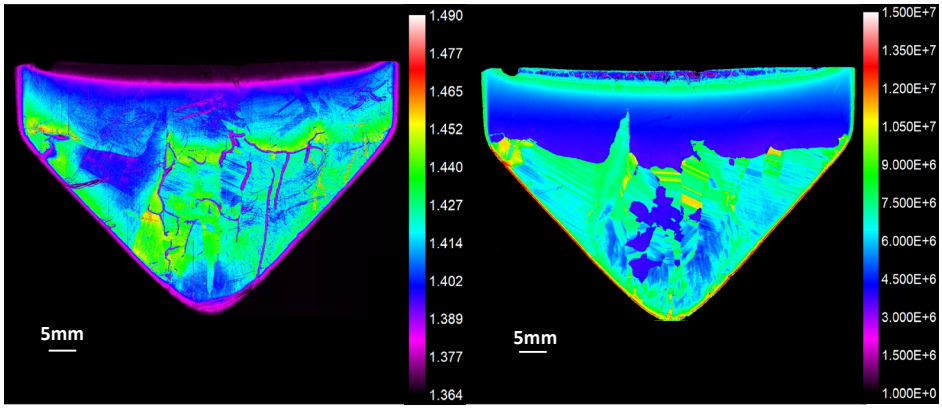


Figure 31:. CG229 (CdTe:In), PL mapping for energy (left) and intensity (right) distributions.

In CG244 PL mapping shown in Figure 32, a 635 nm excitation wavelength, with a 50 µm step size was used to collect 1,080,755 spectra. Three peaks were identified. Fitting was done with two bi-Gaussian functions and a Gaussian function. In the energy map, the tip and heel regions show mostly ~1.41 eV. The conical region has mixed energy distribution but has homogeneity along the middle axial direction. The intensity map has no twins or dislocations but suggests a few structural defects (the yellow, high intensity area) which may be the porosity generated during crystal growth.

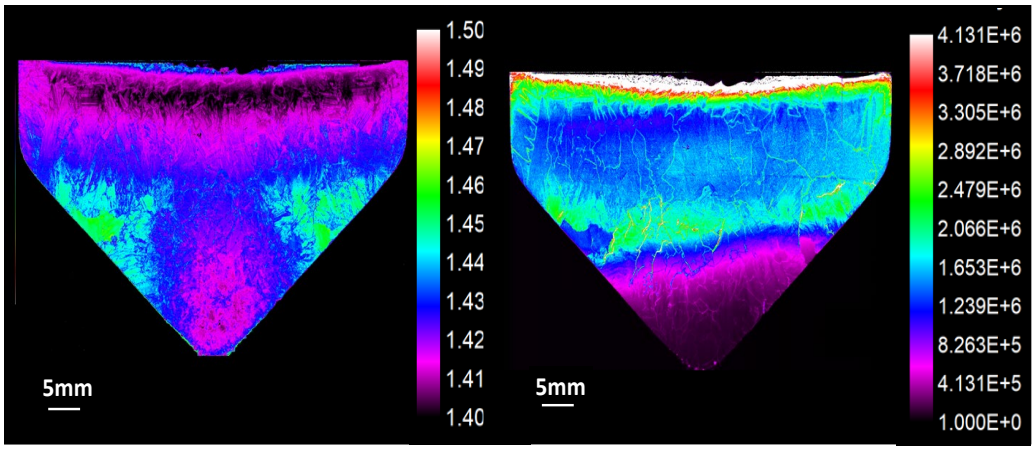


Figure 32: CG244 (CTS:In) PL mapping for energy (left) and intensity (right) distributions.

EDS and EBSD analysis was performed for the samples shown in Figure 29. The wafers were etched in 1% Br methanol solution for 2 minutes. Measurements were made at different positions roughly 5 mm away from each other, along the growth direction for each wafer.

The Se K-alpha and Se K-beta peaks were identified in these wafers. The EDS data for the elements in in each growth are shown as insets in Figure 33. The plots provide rough elemental segregation along the growth direction from first to freeze to last to freeze regions. Comparing the EDS data for three growths, Cd has almost a homogeneous distribution along the ingot. Te slightly increases from first-to-freeze to last-to-freeze, while Se is roughly homogeneous but closed to the heel, it decreases in concentration. Indium as the dopant has roughly homogeneous distribution along the ingot growth.

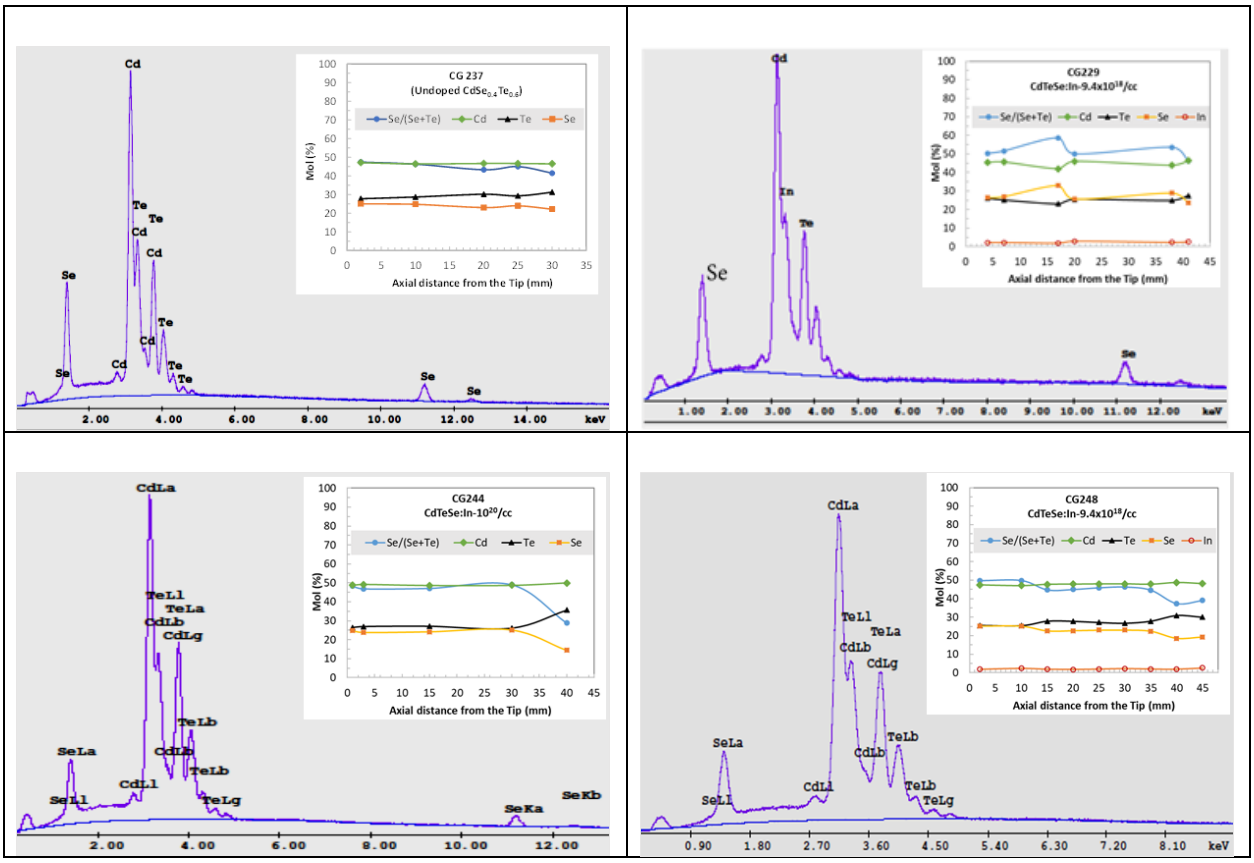


Figure 33: EDS data in molar weight for the elemental distribution in ingots; a) CG237, b) CG229, c) CG244, and d) CG248.

An attempt was made to correlate the PL energy with selenium concentration in the PL maps, using the relationship x(Se mol fraction)=A(E_{gap}(CdTe)-E_{PL}), as suggested by (Peiris et al, *J Electr. Mater*, 33, 724, 2004). Here A=2.596 and E_{gap}(CdTe) was found on the PL system to be 1.502 eV. The results are shown in Figure 34 (CG248) and Figure 35 (CG244). The calculated Se concentration variations seemed high, so a confirmatory large back scatter electron (BSE) map was collected to confirm that these PL differences were really Se concentration differences. The results suggested that the Se concentration was quite uniform, and a small region with electron probe microanalysis (EPMA) and wavelength dispersive spectroscopy (WDS) on CG248 confirmed a weak concentration difference in a similar region with observed features from the PL map, but nowhere near the variation in concentration as suggested by the PL map calculation alone. (EPMA 4 sec/pixel map, with detection limits well below 0.1%; sample area spanned a large range of brightness levels in the PL image). It appears, then, there may be another contribution to the PL energy shift other than Se concentration. Also, there currently appears to be a disagreement between the semi-quantitative EDS (showing some Se segregation) and the quantitative WDS (showing no segregation).

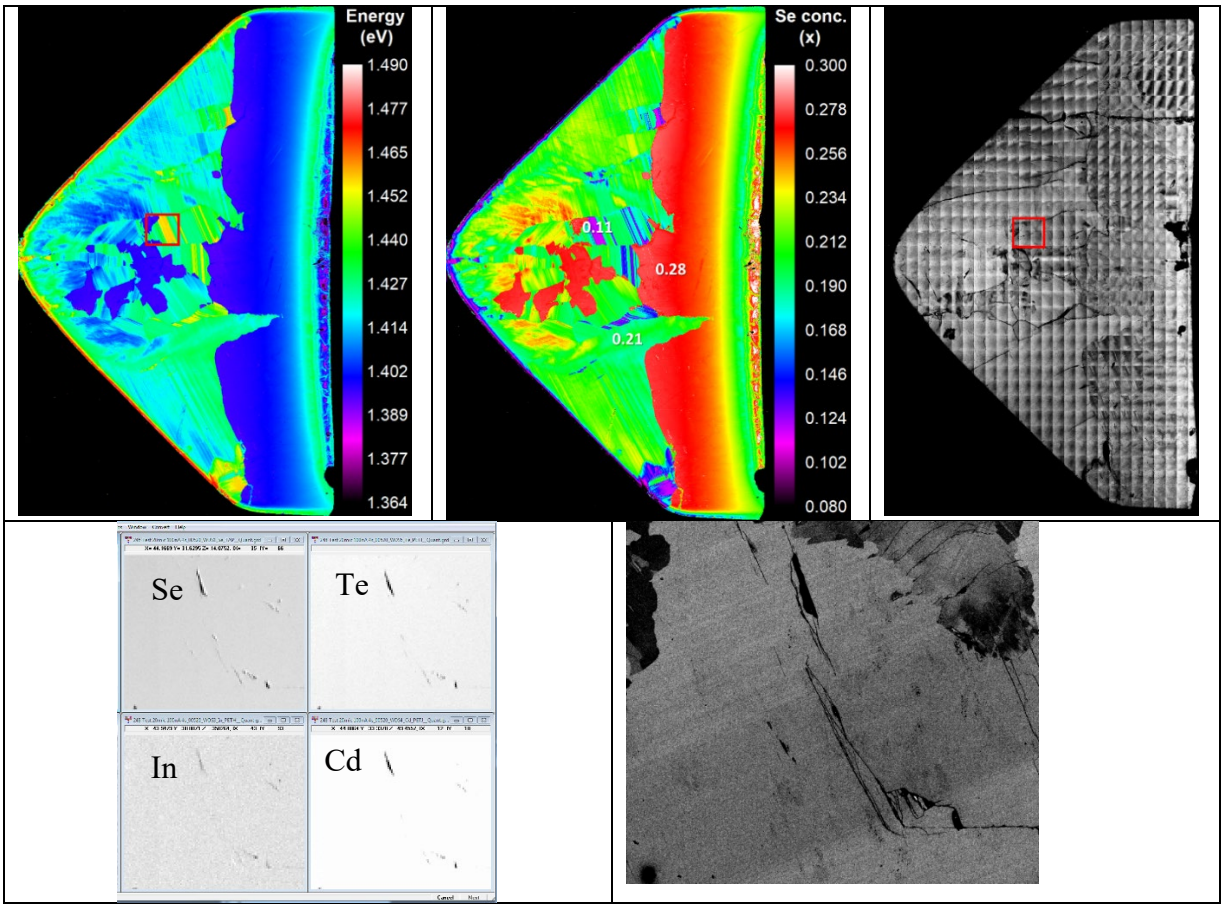


Figure 34. CG248, extracted Se concentration spatially from PL energy, compared to stitched BSE image (region of interest shown in red box). For the boxed region, the EMPA maps on the bottom left show essentially homogeneous Se, Te, In, and Cd, while the BSE map on the bottom right shows weak contrast in the same region

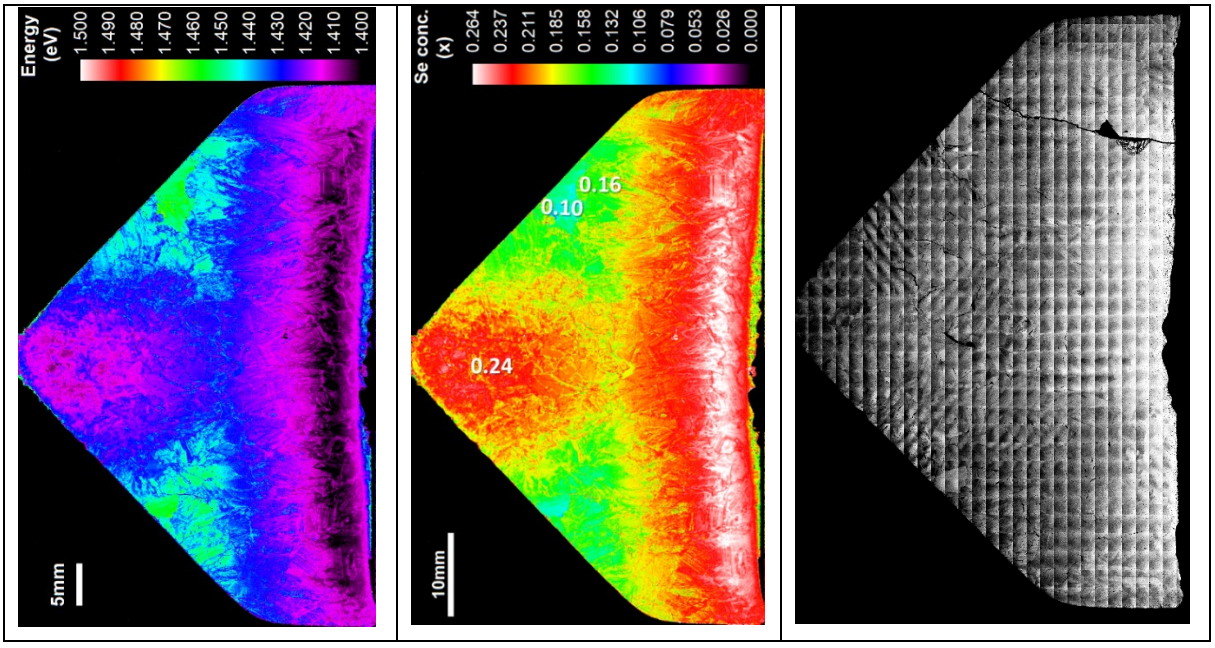


Figure 35. CG244, extracted Se concentration spatially from PL energy, compared to stitched BSE image

EBSD data was collected for the four growths, on same wafers in Figure 29. The crystallographic mapping was done assuming a cubic CdTe-structure crystal. The data is shown in Figure 36. CG237 is mostly {101} orientations. CG229 data was collected at three locations. The tip region is mostly mixture of the {001} and {111} orientations. The middle, bulk region is multi oriented while the heel is mostly {111} with traces of {001} and {101}. The CG244 is mainly {101} with some unknown orientations unrecognized by the system. In the case of CG248, the crystals are mixture of different orientations, with {101} the dominant orientation.

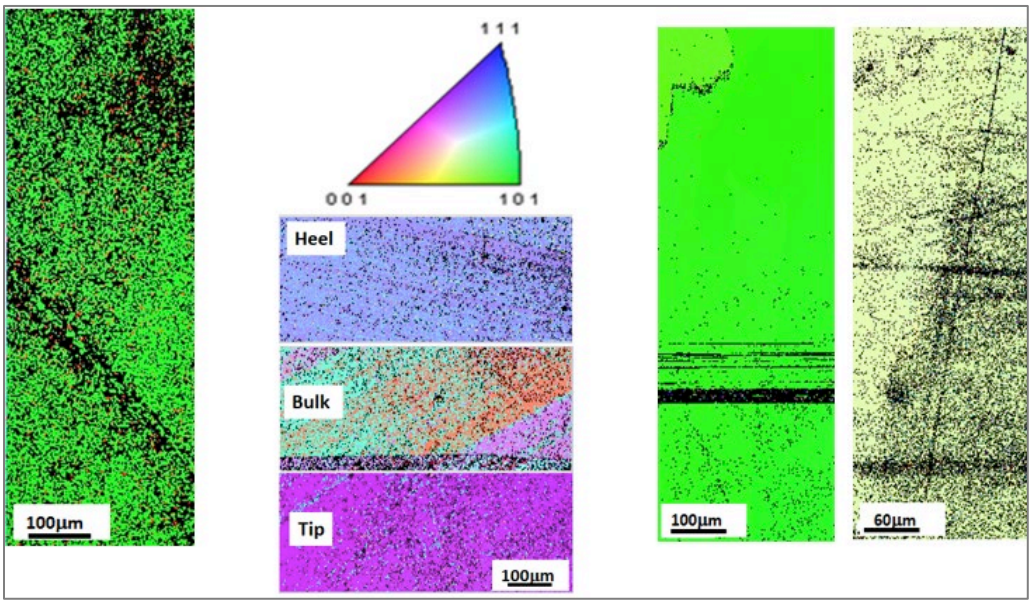


Figure 36: EBSD images for (L to R): CG237 middle region, CG229 Tip and Heel, CG244 heel, CG248 Tip

Transmission measurements were performed to measure the band gap of an undoped $CdSe_{0.4}Te_{0.6}$ (CG237) and doped $CdSe_{0.4}Te_{0.6}$:In (CG229, CG244) as shown in Figure 37. In the indium doped crystals, the bandgap is estimated to be ~1.24 eV, about 70 meV lower than the undoped CTS with the same composition (Figure 38). The reduction in the bandgap may be caused by absorption due to an impurity band.

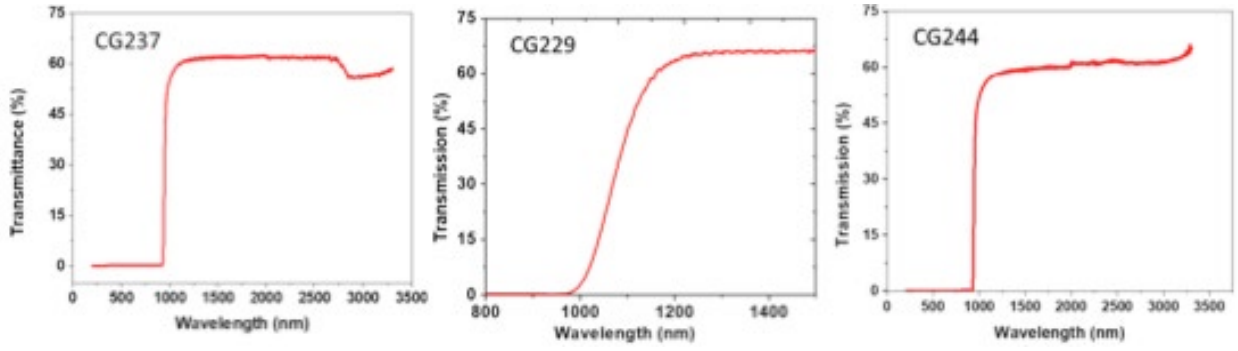


Figure 37*: Transmission measured for CG237, CG229 and CG244, 1mm thick samples.*

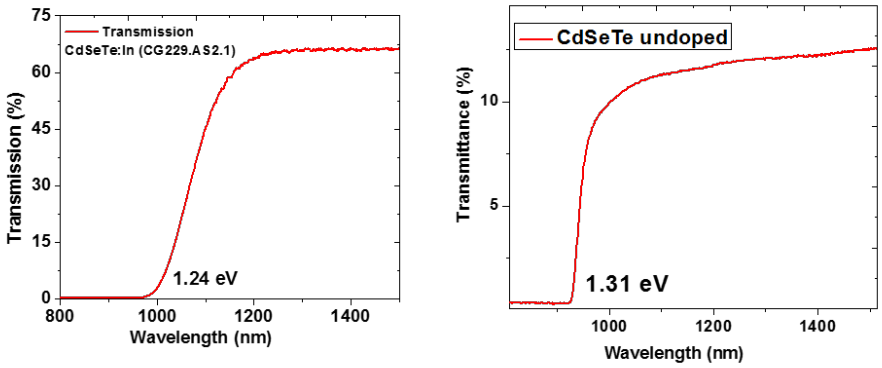


Figure 38: Transmission for $CdSe_{0.4}Te_{0.6}$: In (low doped In, CG229) and undoped $CdSe_{0.4}Te_{0.6}$ (CG237). Estimated bandgap is ~1.24 eV and 1.31 eV respectively.

Transmittance was measured for the annealed CG229 as well. The bandgap reduced from 1.36 eV to 1.24 eV on annealing, but the same time the transmittance is improved further into the infrared (Figure 39). These results are still under investigation for their interpretation.

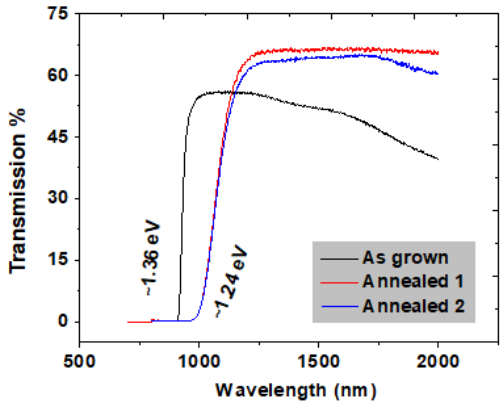


Figure 39:Transmittance data for CG229, comparison of as- grown and annealed samples.

For the CdSeTe:In crystal (CG229), we performed X-ray diffraction (XRD) to determine the phases, since it is known to exist in sphalerite (cubic), wurzite (hexagonal), or mixed phases, depending on the composition and cooling condition. CdSeTe with 40% CdSe freezes from the melt in a hexagonal phase and undergoes a phase transition to the cubic phase ~800-850°C, according to the phase diagram. In our case, the material shows mixed phases. This is likely due to incomplete transformation of the hexagonal phase to the cubic phase. Long cooling times after growth are expected to achieve a complete cubic phase. In II-VI materials like CdSeTe, ZnS, and group V SiC, the close energy between cubic (zincblende structure) and hexagonal (wurtzite structure) often results in repeating mixed cubic/hexagonal stacking sequences known as polytypes.

We have grown an undoped CdSeTe crystal (CG237) with the same composition (40% CdSe) as CdSeTe:In, and cooled slowly to room temperature. The X-ray diffraction (XRD) sample obtained does not look like the CdSeTe:In pattern. We have also measured a 10^{20} cm^{-3} target indium CdSeTe:In (CG244), and it appears similar to the undoped sample. We therefore believe that the pattern suggestive of a polytype in CG229 is likely a region in the crystal where the transformation

from hexagonal wurtzite at high temperautre to cubic zincblende at room temperature was arrested, forming the polytype. However, given all the other results (e.g., PL mapping) suggesting heterogeneity, there may be regions of the crystal with mixed structures. Whether this is significant for production of films after crushing source material remains to be seen.

To assess the importance of these signatures, a large number of samples of CdTe and CST, doped and undoped, from our archive were measured with XRD. We conclude from this that it is possible that the patterns represent instead stacking faults (i.e. hexagonality) (McCloy et al., 2009), and not true polytypes. The extreme heterogeneity of CST in particular, and heavily doped CST (HPB7, CG239), is apparent in Figure 40, particularly in the 22-26° 2θ range. CST:In appears to be more variable than CST:As. One speculation is that this is due to the similar atomic number of Cd and In and a greater interaction than with As. The only crystallographic irregularities in CST:As appear at the highest As concentrations. Even undoped CST appears highly irregular, however, and variable with location even for the same crystal. By contrast, CdTe crystals are very homogeneous and almost all are similar and have very similar peak locations.

TRPL measurements were performed at NREL, for all the CTS:In CG244 (Figure 41). The ~0.34-0.42 value for the as-grown and one of the relaxations in the RTA sample is ~15% of the radiative limit. The long lifetime appears to be in excess of the radiative limit and is under investigation. For comparison, CG229 CTS:In at lower In concentration was previously measured having lifetime 1.5 ns.

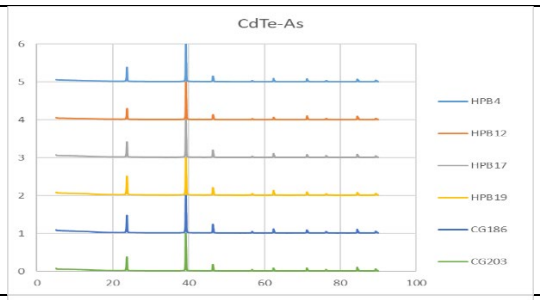
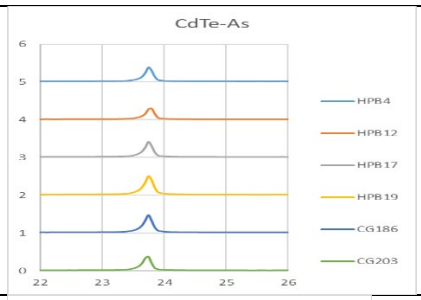
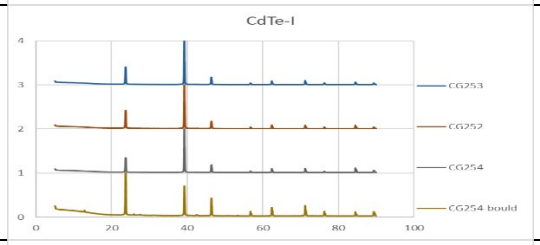
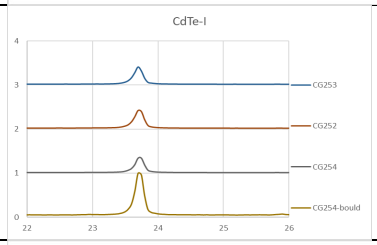
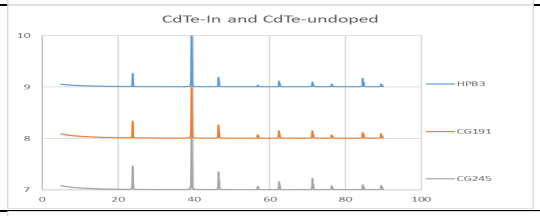
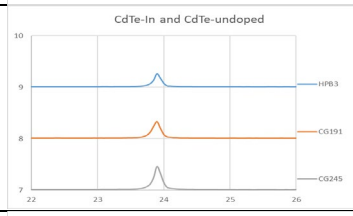
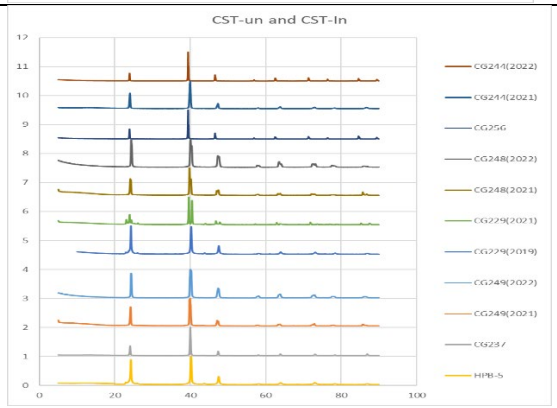
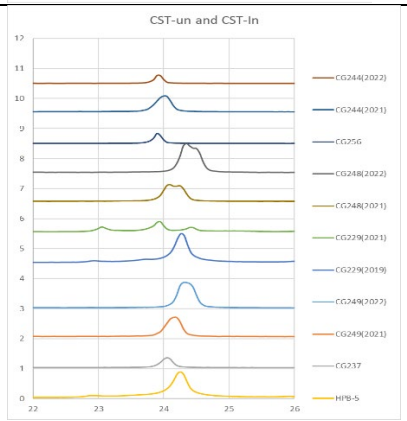
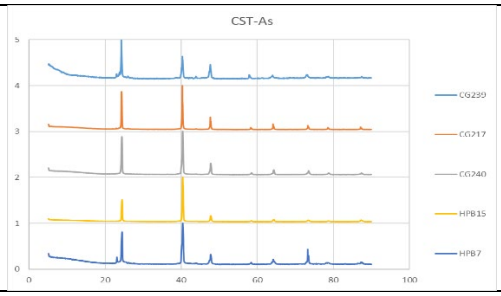
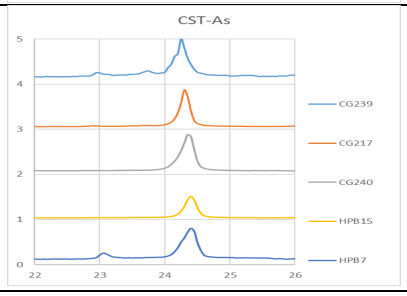
CdTe:As		
CdTe:I		
CdTe:In		
CST:un and CST:In		
CST:As		

Figure 40. XRD comparison for a large number of CdTe and CST samples. X-axis in all cases is angle 2θ (Cu Kα X-rays), and Y-axis is intensity normalized to the peak and offset. CG and HPB numbers are WSU internal reference numbers.

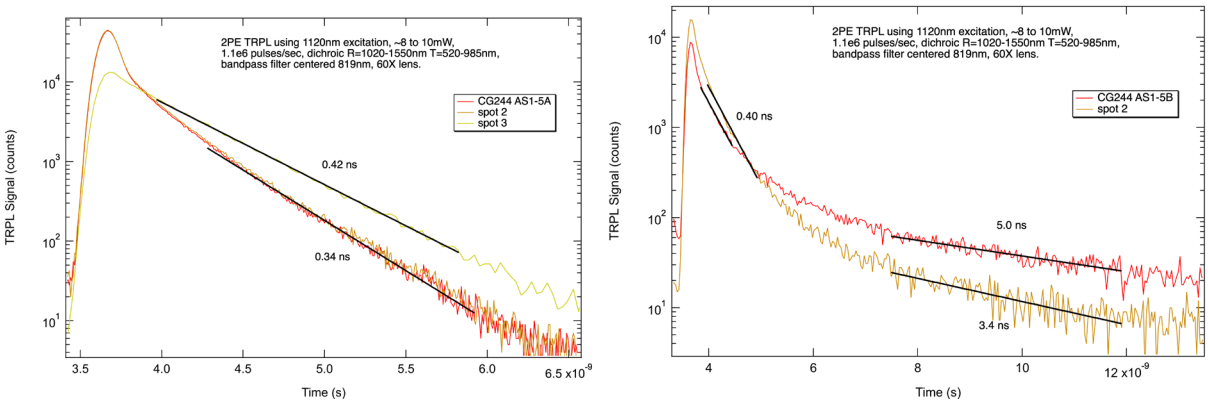


Figure 41: TRPL data for CG244, CTS:In, as-grown (left) and RTA 550°C-2 min (right)

For all the 2PE TRPL for CdTe:I, CdTe:In, and CST:In, the data is compared with the theoretical calculated values by using the formula,

$$\tau = 1 / (B_{eff} * n)$$

τ = carrier lifetime
B_{eff} = effective radiative recombination coefficient, for CdTe, ~1.1×10^{-10} cm^3/s
n = carrier density

The source for the B_{eff} value is (Burst et al., 2016). Surface recombination may be a factor, despite the 2PE TPRL method. Another option is that the carrier concentration may be non-uniform. These possibilities are still under investigation for the crystals and the films.

6.4.3 CdTe:I crystals

CdTe:I growths were performed in the modified vertical Bridgman (MVB) set up at WSU. Batch sizes were 750 g of CdTe with dopant added to that. Photographs of the crystals are shown in Figure 42.

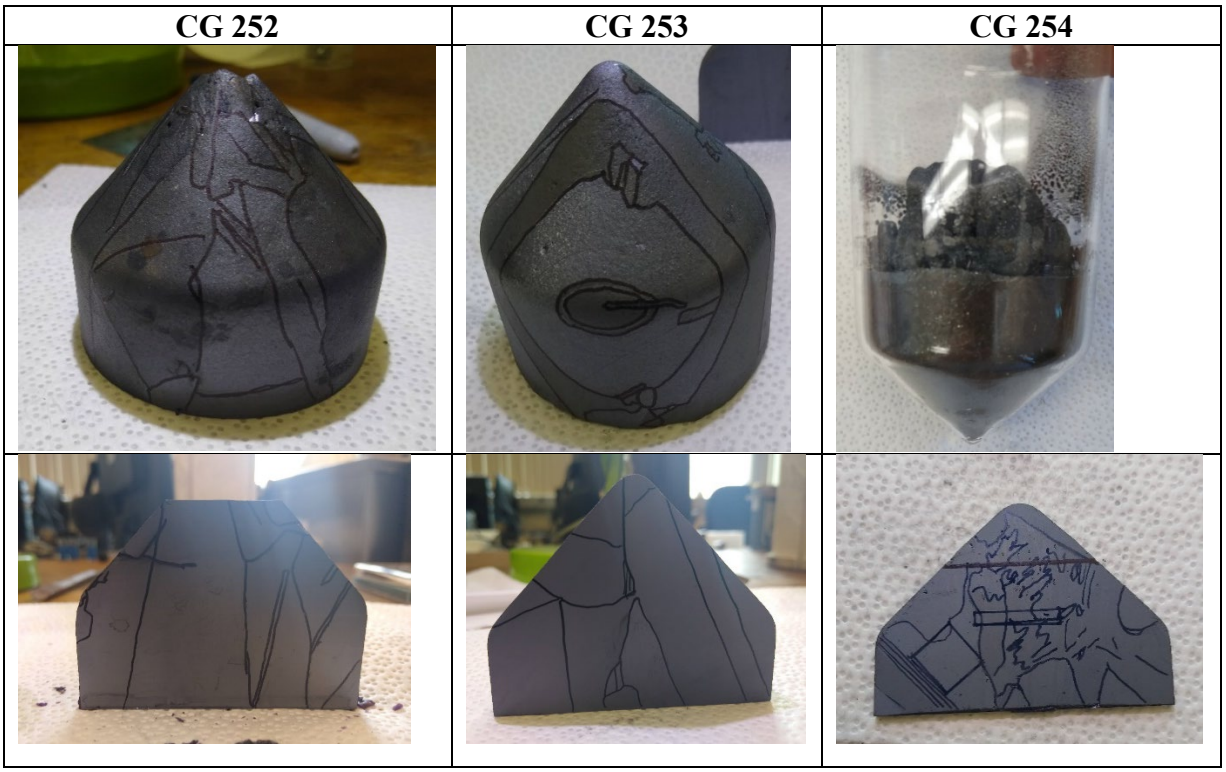


Figure 42: Photographs of the three CdTe:I growths.

Measured impurities and dopant concentrations, as determined from glow discharge mass spectrometry (GDMS), are shown in Figure 43. The GDMS trends fit with the growth profile concentrations where the grey series has the most iodide followed by the blue and then the orange. However, the orange series had proportionately a large amount of zinc and iron compared to the iodide.

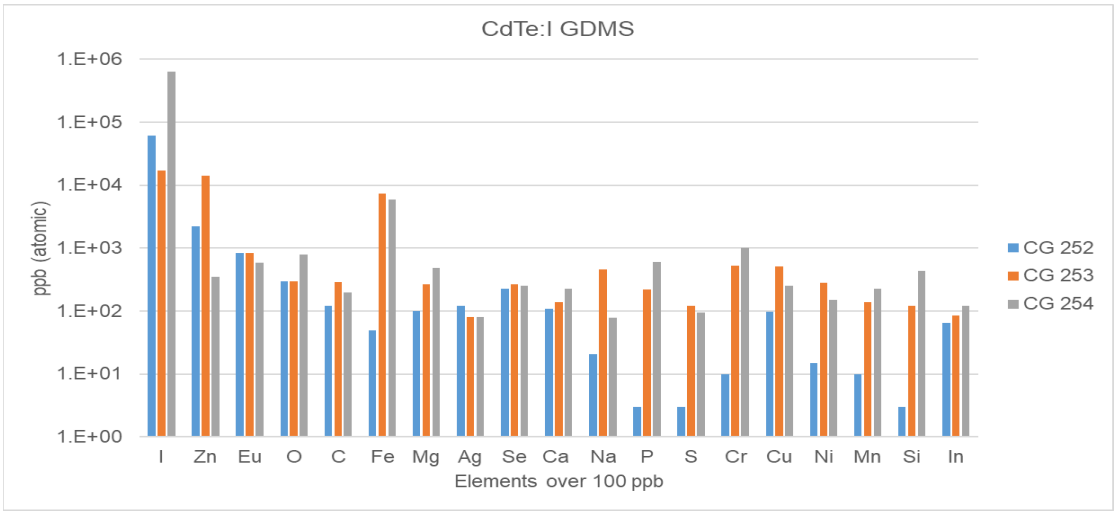


Figure 43: GDMS data from National Research Council, Canada.

The X-ray diffraction (XRD) data (Figure 44) we collected showed the expected CdTe spectrum, except for the unusual growths that were from the "boulders" (abnormal growth) that grew on top of CG 254. The additional peaks around 2θ = 8° and 27° are attributed to cadmium iodide (CdI_2) which was not incorporated into CdTe.

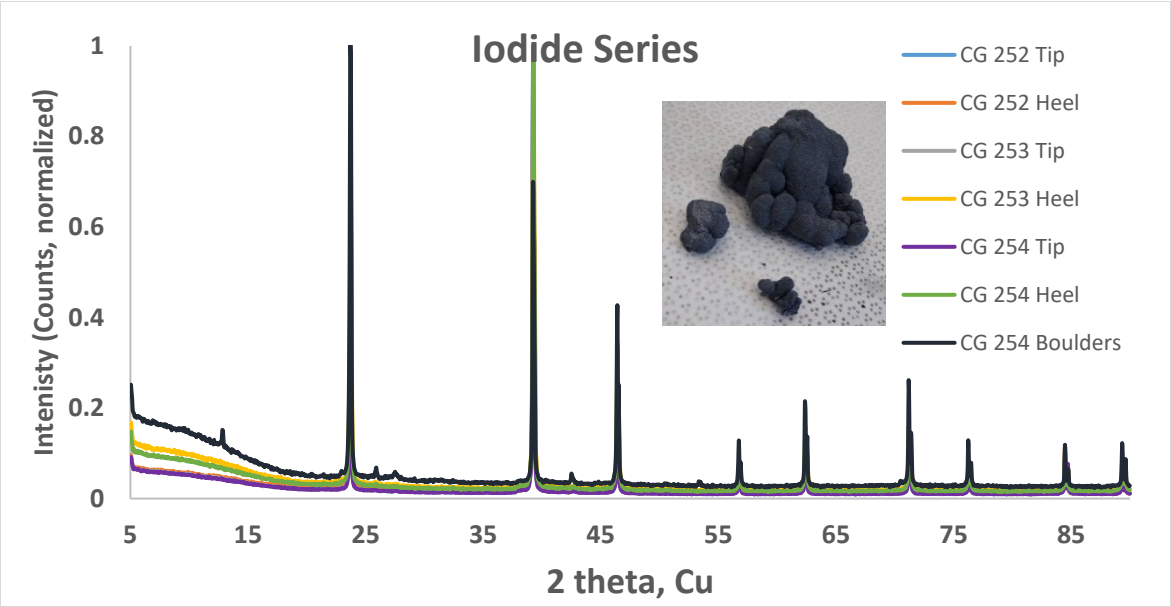


Figure 44 XRD on powdered CdTe:I. Inset shows the 'boulders' which formed at the heel of CG 254.

A trend was determined when examining the transmission spectrum (Figure 45) of the doped samples. Increase of iodide concentration decreases the band gap. The above graph CG 150 is undoped CdTe, with increasing iodide in the order of CG 253, 252, and 254.

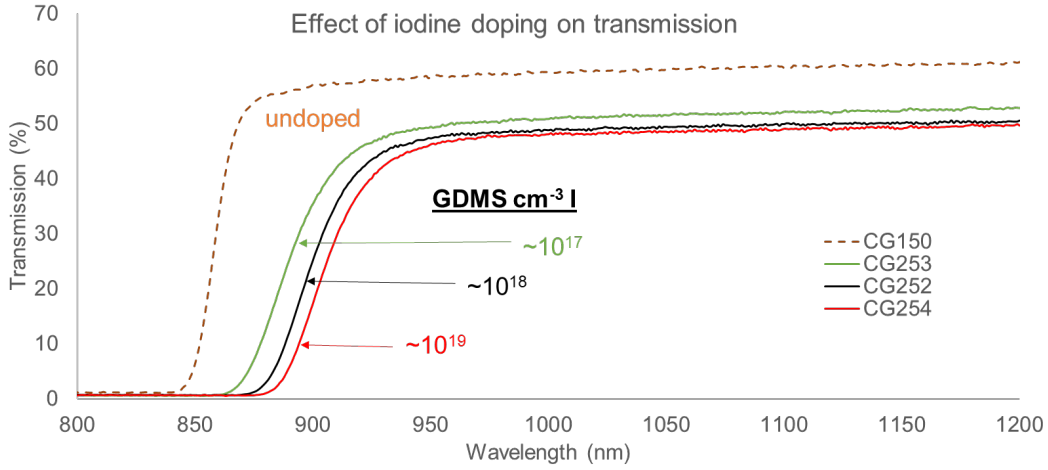


Figure 45. Near infrared transmission spectrum of CdTe and CdTe:I

To look at possible heterogeneities, photoluminescence (PL) mapping was performed on axial slices at Klar Scientific (Figure 46 and Figure 47), specifically on CG 252 and CG 253, using a 635 nm laser excitation and a 50 μm spatial step size. About 1.1-1.3 million spectra were collected and fitted for each sample.

Heterogeneities in peak energy, full-width half-maximum (FWHM) and energy are observed. We are still in the process of understanding the significance of these results, but it is apparent that individual grains can have different signatures, as can the tip region which may be more highly stressed and possibly have compositional differences.

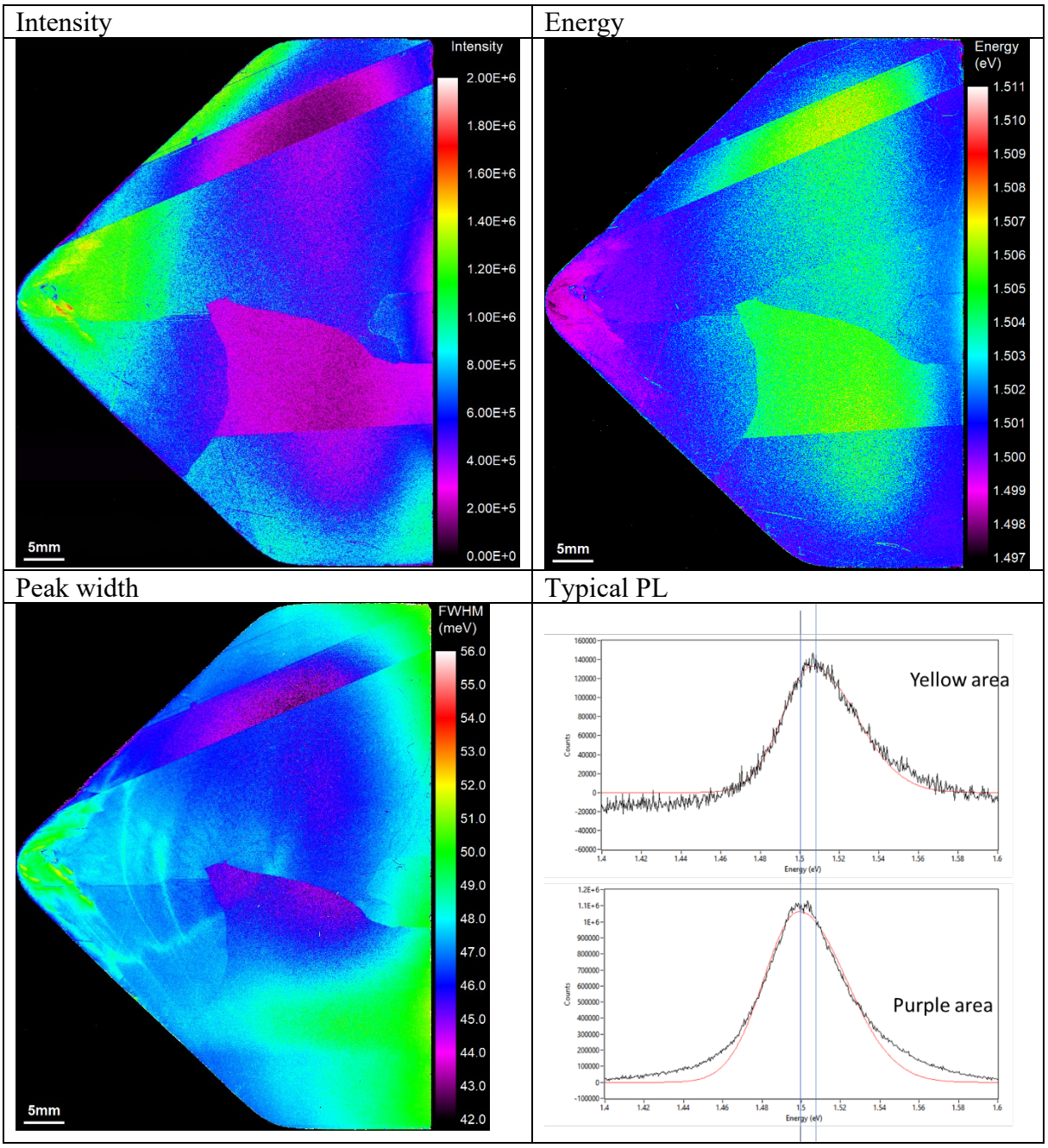


Figure 46: PL mapping of CG 253 AS1

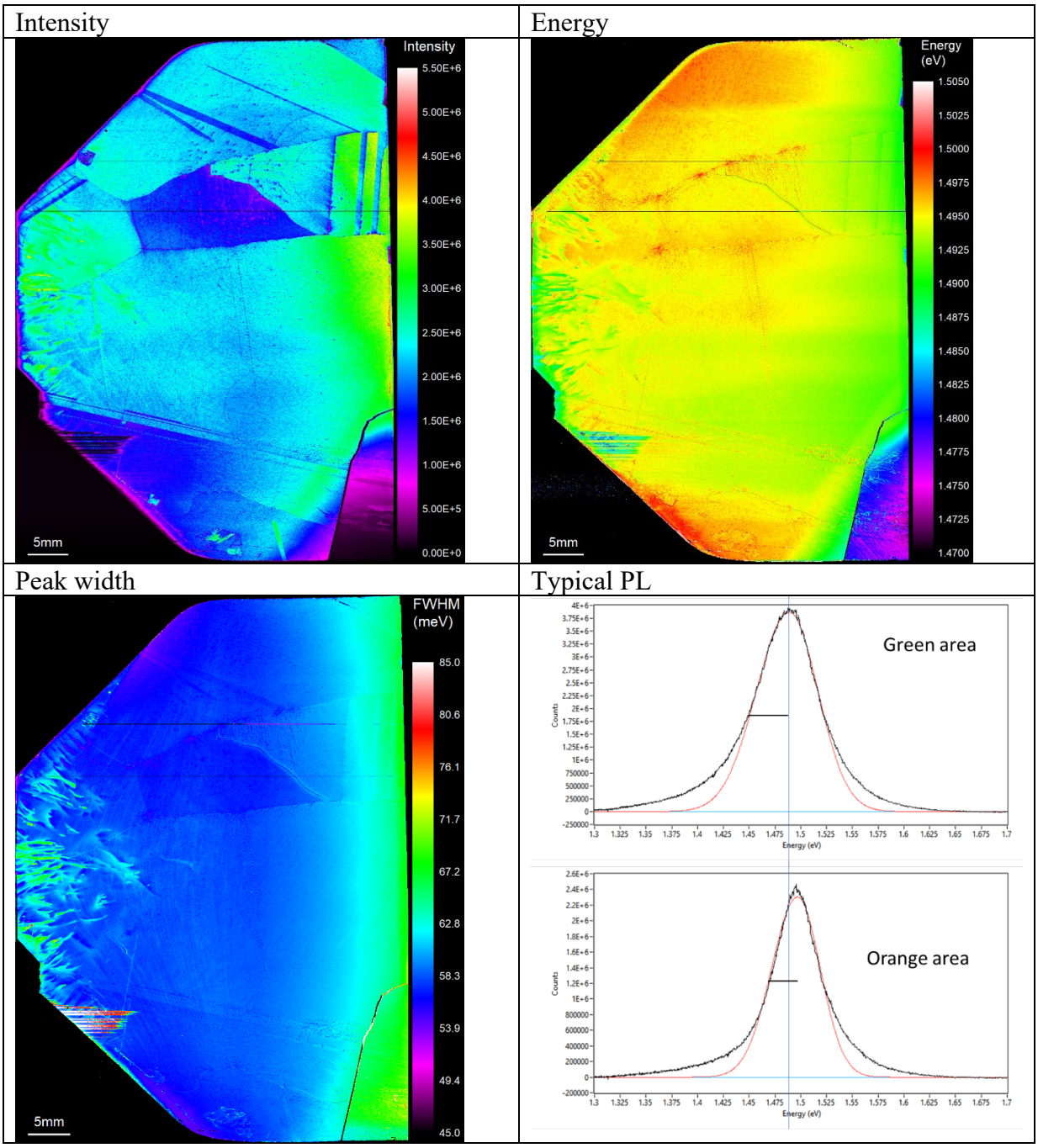


Figure 47: PL mapping of CG 252 AS1

Hall effect measurements (Figure 48) were performed on cut and polished substrates at NREL. The samples were too resistive, except CG 254, to measure any voltages using the Hall effect prior to a rapid thermal anneal (RTA). The RTA was performed as a 1 min ramp from room T to the setpoint (here 550°C or 600°C) then a 5 min hold, all in flowing Ar ambient; no intentional cooling was performed after hold (~4 min to 60°C). There was not a clear trend dependent upon doping concentrations, but in general the RTA showed increased carrier concentrations increasing concentrations.

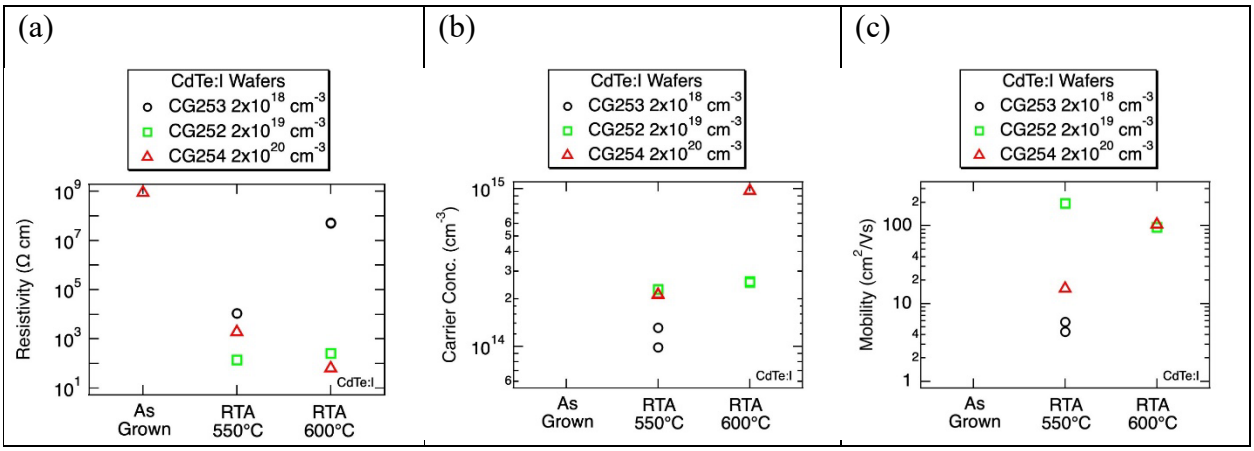


Figure 48: Hall effect on CdTe:I crystals, showing resistivity, carrier concentration, and mobility.

Infrared (IR) microscopy was performed on CG252, using 941 nm diode array for imaging. As shown in Figure 49, before annealing the sample contains dark inclusions, likely Te, as typically seen in Cd-Zn-Te samples.

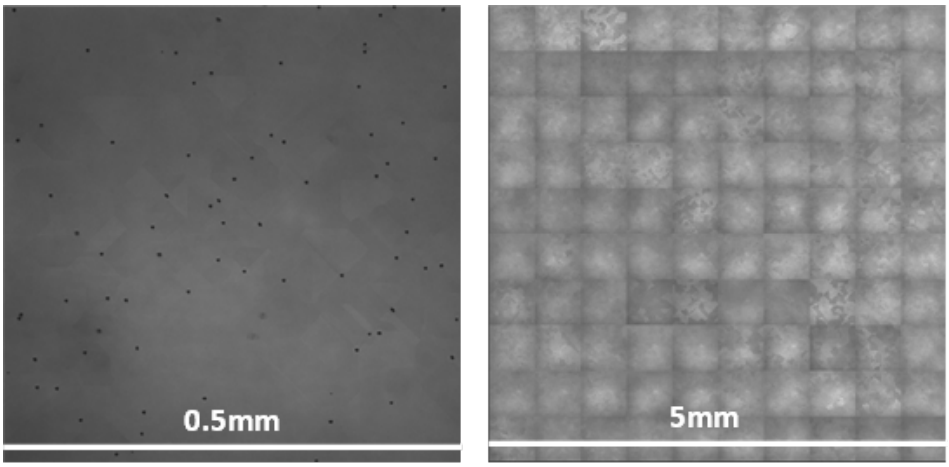


Figure 49: IR images for the CG252-AS2-2: CdTe:I. as grown. On left is single image and on right is stitched image showing larger area.

2PE-TRPL (Figure 50) was performed at NREL using 1120 nm excitation, ~8 to 10 MW, 1.1×10^6 pulses/sec, dichroic R=1020-1550 nm, T =520-985, bandpass filter centered 819 nm, and 60x lens. These measurements are currently being analyzed.

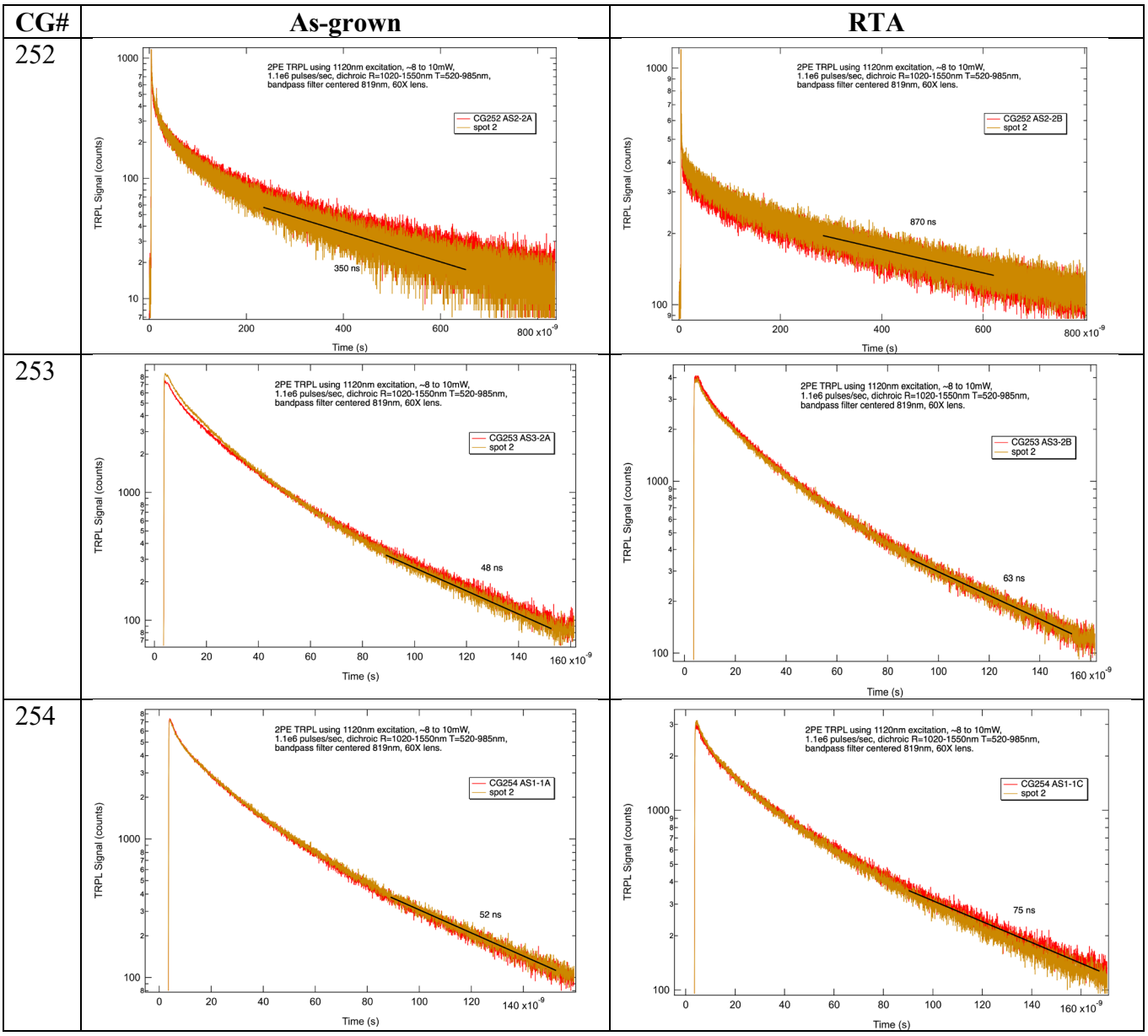


Figure 50: TRPL results for CdTe:I samples.

The results of the Hall effect measurements (at WSU) on the Te- and Cd-annealed samples are shown in Figure 51. In general, the RTA decreased the measured resistivity and carrier concentration of all the compositions. The Te-anneal slightly decreased the resistivity (and concomitantly increased the carrier concentration) for all but the moderately doped composition (CG252), where the resistivity was decreased dramatically. We believe this to be a real effect, as the CG252 is an outlier, and this sample behaves differently in visible transmittance after Cd annealing compared to the other samples (Figure 52).

In general Te annealing does not seem to change the apparent band gap (E_{opt}) from the as-grown sample, as determined from the first derivative of the transmission spectrum (Figure 52). In CG252

Cd annealing increases the apparent bandgap (makes it more transparent in the near-infrared). While Cd annealing does not increase infrared losses for CG252, Te annealing does. Originally, we thought this reduction in transmission (for CG253 Cd anneal and CG252 Te anneal) was due to free carrier absorption. However, this is not consistent with the other high carrier concentration samples, so it may be that this represents scattering due to an increasing size of some precipitate. We hope that infrared microscopy can answer this question.

Interestingly, the mobility of all the Te annealed samples increased from as-grown or RTA measurements. For the Cd annealing, all samples showed reduced resistivity and increased carrier concentration. Unexpectedly, the mobility scales with iodine concentration, not the expected inverse.

Carrier concentration in the Cd-annealed CdTe:I crystals (and the Te-annealed CG252) is 10^{16}-10^{18} cm^{-3}, presumably due to the removal of the acceptor traps which in CdTe are A-centers consisting of ($V_{Cd} \cdot I_{Te}$) complexes, though it is not clear if the Te-annealing mechanism for CG252 can be seen be the same mechanism for creating high carrier concentration.

TRPL results were obtained for the Cd- and Te-annealed samples are were shown in combined with the measured carrier concentrations in Figure 16.

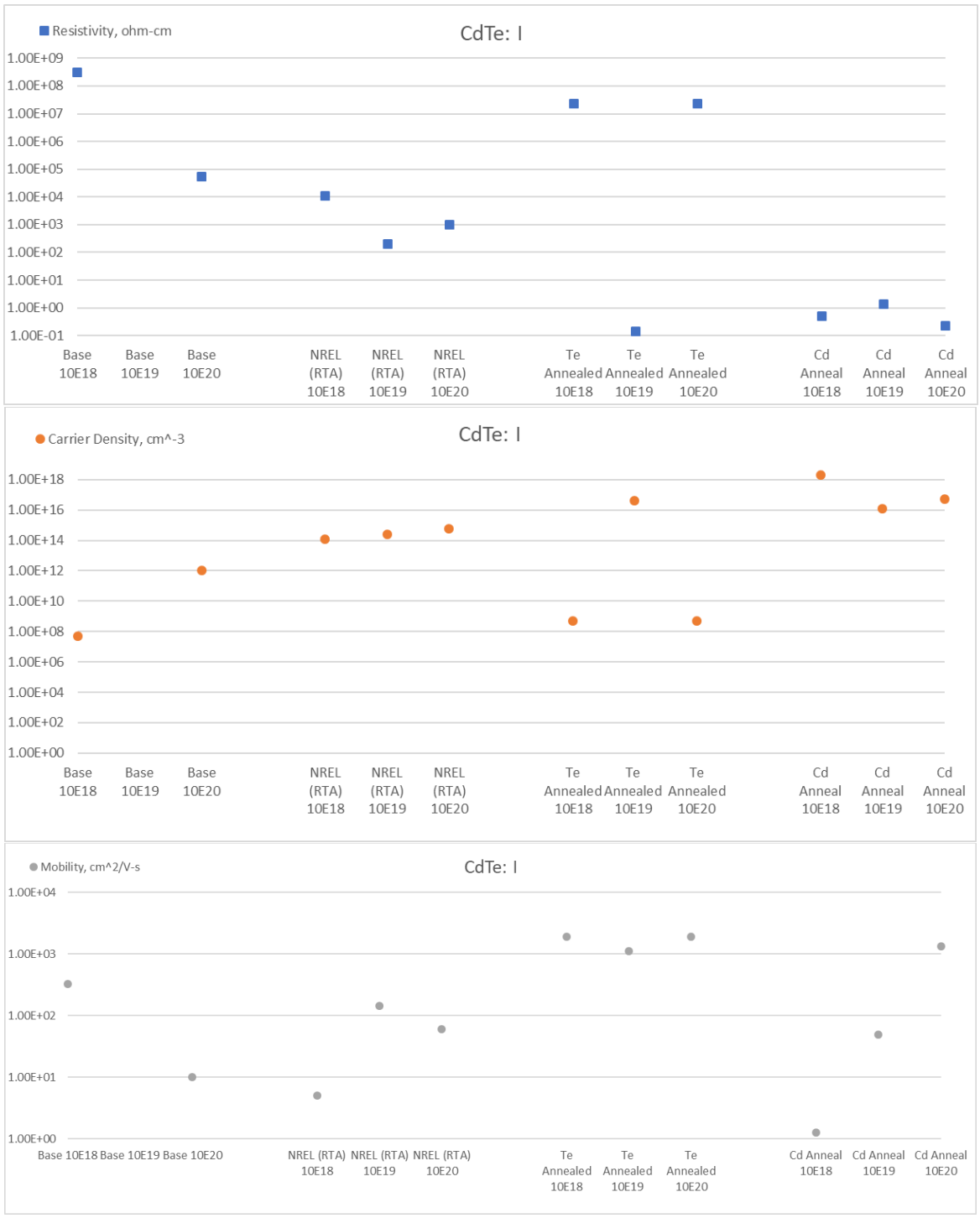


Figure 51: Hall effect results from CdTe:I crystals, target I concentration shown; all measurements at WSU except the RTA data; all heat treatments before contact placement. Comparing: as-grown ("Base"); RTA; Te-anneal, Cd-anneal. Three plots are: 1) resistivity, 2) carrier concentration, 3) mobility

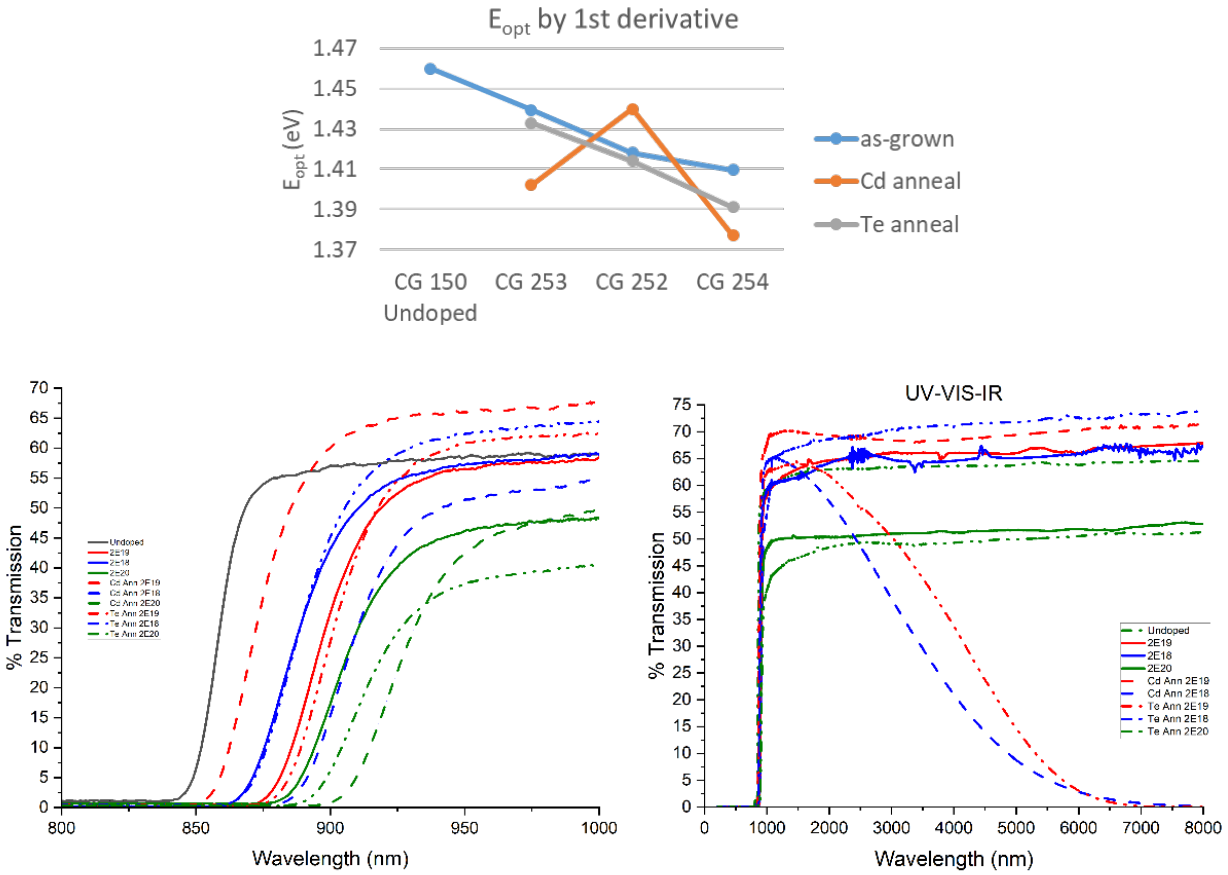


Figure 52: Transmission of as-grown, Cd anneal, and Te annealed CdTe:I materials. A) apparent optical gap determined from first derivative of transmission graph near band edge. B) near-infrared band edge transmission cut-on. C) stitched data for transmission in near- and mid-infrared. For B) and C), blue is CG253 (target ~10^{18} cm^{-3} I), red is CG252 (target ~10^{19} cm^{-3} I), and green is CG254 (target ~10^{20} cm^{-3} I); solid lines are as-grown, dashed lines are Cd-annealed, and dash-dot lines are Te-annealed.

6.5 Homojunction devices

6.5.1 Initial attempts

Homojunction device structures were fabricated in the following manner. *P*-type wafers of hole concentration ~2x10^{15} cm^{-3} (CG 168, CdTe:P) were diced to ~ 1 cm x 1 cm x 2 mm size and polished on both faces. Before film growth, the wafer was immersed in a 1% solution of Br in methanol for 1 min. A Cd(Se)Te:In film was then grown by CSSE as described above. Next, edges of the wafer were masked and a ~200-nm-thick layer of indium tin oxide (ITO; 10 wt.% SnO_2) was deposited by RF magnetron sputtering in an ambient of 0.3% O_2 in Ar at room temperature. To form the back contact, the opposite side of the wafer was masked, followed by RF magnetron sputtering of 1-3 nm of Cu and DC magnetron sputtering of 500 nm of Mo, both at room temperature in Ar.

Devices were characterized using current density-voltage (JV) measurements under simulated one-sun AM1.5 illumination. Capacitance-voltage (CV) measurements were performed at 50 kHz in the dark from 0.5 V forward bias to 1.5 V reverse bias.

JV data for initial PV devices are shown in Figure 53. Device performance is limited to low overall power conversion efficiency. We suspect that there are several reasons for this. The low current observed for devices containing Cd(Se)Te:In is likely due to low carrier concentration in the Cd(Se)Te:In film layer. Short-circuit current density (J_{sc}) is slightly higher for the thicker CdTe:In film, despite the opposite relation expected, as shown in Figure 53. This thicker film may contain a greater number of free carriers, which may slightly increase the electric field strength present in the junction region, leading to slightly greater current collection, its value, however, remains severely limited. The device with ITO only (no Cd(Se)Te:In) shows significantly higher J_{sc}; the ITO carrier concentration is expected to be in the low-mid 10^{20} cm^{-3} range and can thus lead to an increased electric field in the junction region. It is likely, however, that the surface recombination velocity is high at the ITO-CdTe:P interface and the band alignment may be poor, leading to the overall low V_{oc} and poor device performance. The observed strong JV rollover also indicates a non-ohmic back contact. Next steps that are being considered are discussed below.

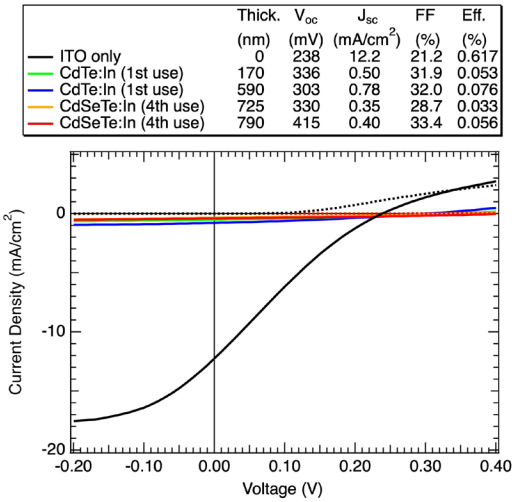


Figure 53: JV measurements from selected devices with various thicknesses of Cd(Se)Te:In as shown in the inset. One device without a Cd(Se)Te:In layer is shown for comparison.

CV measurements were also collected for these devices (Figure 54). The black curve shows a flat profile that is well-behaved, with a net acceptor density at zero bias in the high 10^{14} cm^{-3} range. This is near the expected hole concentration in the CdTe:P wafer of ~$2x10^{15}$ cm^{-3}. Depletion widths for all of the other devices are higher, consistent with a lower electric field strength and the poorer current collection observed in Figure 53. CV data for the CdTe:In devices are not considered to be reliable in terms of carrier concentration; note that the zero-bias points are not indicated here. The CdTe:In device with the thicker emitter layer does appear to have a lower depletion width, consistent with a slightly higher electric field strength.

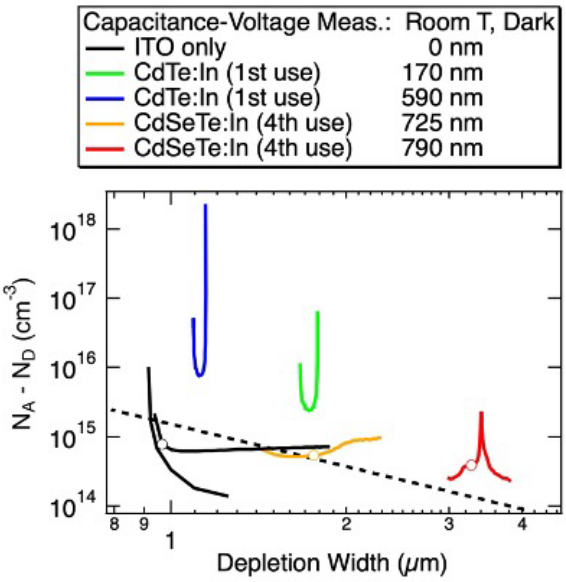


Figure 54: CV measurements for the devices shown in *Figure 53*. The dashed line indicates the expected position of net acceptor density (N_A-N_D, where N_A is the acceptor density and N_D is the donor density) as a function of the depletion width for a one-sided junction with an n-type region of electron density that exceeds the hole density of the p-type absorber layer. The open circles along the CV traces indicate the zero-bias position in the data collection range from +0.5 to -1.5 V (forward to reverse bias, respectively).

Device work then proceeded to focus primarily on using films grown from CdTe:In source material. Film growth when using CdTe:In rather than CdSeTe:In has seemed to offer enhanced reproducibility. Differences in vapor pressures present in the growth chamber with the addition of Se may lead to additional complications. Second and third uses of a particular allocation of source material also enabled enhanced reproducibility in resultant film thickness. An open question remains as to the amount of dopant remaining in the source material on uses subsequent to the first; we are planning to evaluate these differences using SIMS.

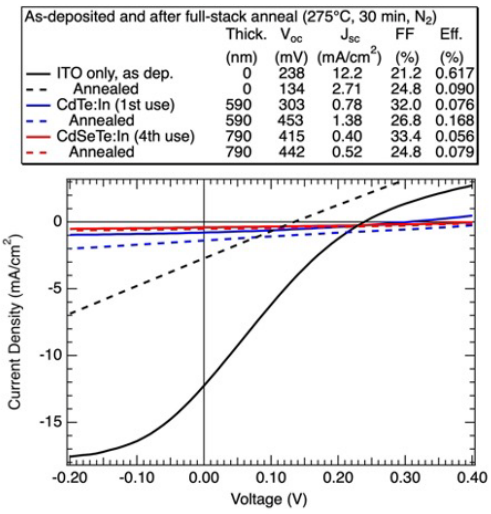
Controlling CdTe:In film growth to thicknesses < 1 µm, as required for use in homojunction devices, remains difficult. Experiments in which H_2 pressure was changed to 10 torr in an effort to enhance film uniformity were performed, but results remained unclear. Film thickness control was enhanced by reducing the source temperature from 665°C to as low as 640°C while maintaining the substrate temperature at 625°C, but some irreproducibility remained.

6.5.2 Assessing the importance of contacts and substrate wafer

As a follow-up to previous work, completed homojunction devices with CdTe:In films deposited onto CdTe:P wafers, with both front indium tin oxide (ITO) and back Cu/Mo contacts applied, were annealed at 275°C for 30 min in flowing N_2. This was performed to investigate whether an anneal at this temperature could aid in, for example, healing sputter damage incurred from applying the front and back contacts. Performance for devices with CdTe:In increased in short-circuit current (J_{sc}) only slightly, while fill factor (FF) decreased to ~25% (Figure 55a). A test structure with an ITO front contact only (no CdTe:In film), while having significantly higher initial J_{sc}, showed a significant decrease in J_{sc} after annealing. Indium from the CdTe:In layer may have diffused into the p-type wafer to the extent that there was no longer significant diode behavior both

with and without the CdTe:In layer. Annealing a device structure after applying the ITO front contact, but before applying the back contact, showed similar results, suggesting that the back contact was not responsible for this behavior.

a)



b)

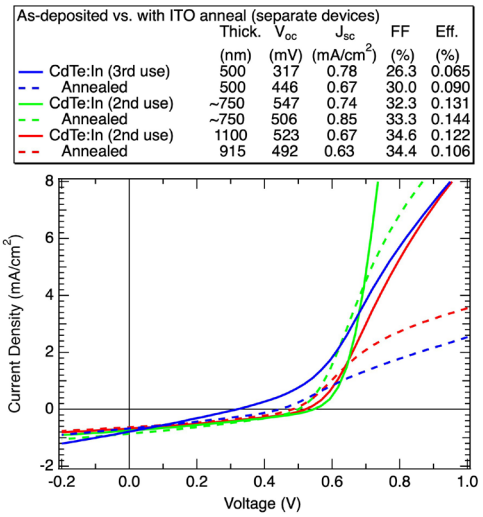


Figure 55:. a) Post-fabrication annealing of full devices. b) Devices in which the ITO front contact was annealed before application of the Cu/Mo back contact.

As an aid to determine reasoning behind the poor performance of devices containing CdTe:In layers, a series of devices were fabricated with several variations in device structure. In all cases, the front transparent conducting oxide (TCO) was changed from ITO, as had been used in previous devices, to a bilayer of 100 nm ZnO and 120 nm ZnO:Al, as has been used in CIGS polycrystalline devices and single-crystal (SX) CdTe devices. In addition, 60-nm-thick CdS:In films, previously used in SX devices, were included in selected structures.

Figure 56a shows JV curves and JV parameters for these devices. The blue curves show a device with CdTe:In deposited onto a CG168 CdTe:P wafer followed by deposition of a ZnO/ZnO:Al TCO bilayer, with and without a 30 min 335°C anneal after deposition of the bilayer. It is seen that while the anneal improves device performance, enhancement is minimal; J_{sc}, in particular, remains extremely low, as has been observed for previous devices containing a CdTe:In layer. Adding a CdS:In layer between the CdTe:In and TCO led to a significant V_{oc} improvement, but J_{sc} again remains low. As a test of whether a CSSE-grown film in general or a CdTe:In film in particular leads to J_{sc} limitations, a device structure was grown in which a CdTe:As film, rather than a CdTe:In film, was incorporated. This was followed by CdS:In and TCO layers. While the overall performance of this structure remains limited, J_{sc} values are considerably higher than those observed for devices incorporating a CdTe:In layer, suggesting that the CdTe:In layer itself is a significant limitation. In this CdTe:As device, the post-TCO anneal decreases the J_{sc} somewhat, but the J_{sc} is not limited to the extent of that in a CdTe:In device.

The last comparison in Figure 56a is the structure used in NREL/WSU high-V_{oc} SX CdTe device work of several years ago (Duenow et al., 2016), incorporating CdS:In and ZnO bilayer TCO layers. Best performance parameters for the CG168 wafer in the past were limited to V_{oc} of ~960 mV and efficiency of ~15%. While these parameters of the current devices are limited in

comparison, J_{sc} values are much higher than those observed for devices incorporating CdTe:In, and V_{oc} values exceed 900 mV, indicating that the CG168 wafers used in this work, with the accompanying CdS:In and TCO layers, are sufficient so as to not be the primary limitation of devices incorporating CdTe:In.

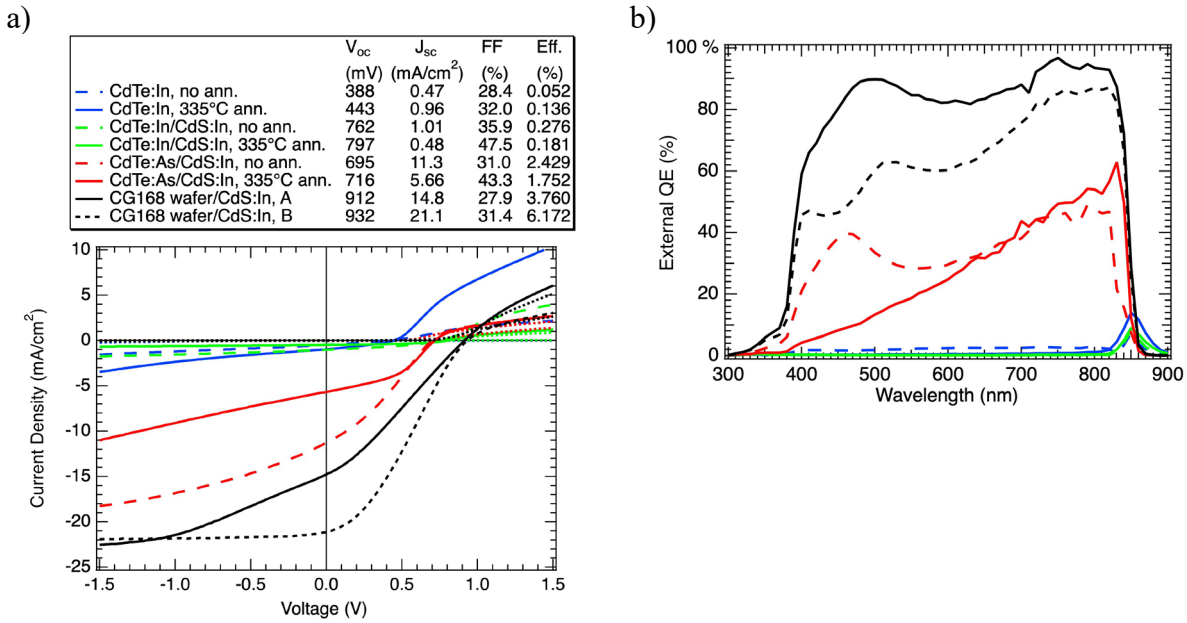


Figure 56: Several device structures used in determining limiting factors of CdTe:In homojunction devices. a) JV curves. b) External quantum efficiency.

More information is provided by examining external quantum efficiency (EQE) data for these devices (Figure 56b). The highest EQE values are observed for the high-V_{oc} structures that also show the highest J_{sc} values in Figure 56a. The junction, in this case, is expected to be near the interface of the n-type CdS:In and p-type CdTe:P wafer. Next, the device structures incorporating a p-type CdTe:As thin film, rather than a CdTe:In thin film, show a somewhat lower J_{sc}, as expected from the JV curves. The junction here is expected to be between the n-type CdS:In and p-type CdTe:As film, so impinging light is not required to pass through the CdTe:As film layer to reach the junction in this case. However, in the device structure containing CdTe:In, the junction is expected at the interface between the CdTe:In film and CdTe:P wafer. In this case, light is required to pass through the highly absorbing CdTe:In film to reach the p-n region to enable charge separation.

In examining the EQE data for the CdTe:In-containing structures, it is seen that the EQE signal is nearly 0 for wavelengths below 800 nm, with only a small "spike" visible near the band edge of the CdTe. This *behavior is often observed in the case of a buried homojunction*, where the p-n junction occurs in a device at a depth at which insufficient charge separation and collection occurs. This could occur because most of the incident light is absorbed in the part of the absorber layer that the light encounters first, as would be the case with an *excessively thick* n-type side of the homojunction (in this case, CdTe:In). Another contributing factor could be *poor carrier lifetime* in the CdTe:In film. If charge separation were to occur, but the carrier lifetime in the CdTe:In film were low, then separated carriers could recombine before being extracted to the electrodes on either side of the device structure. Though we have measured 2PE TRPL on thick CdTe:In films

and found them to have reasonable lifetime values, characterizing the lifetime in a thin film is more difficult because of confounding effects with surfaces. A *large interface recombination velocity* could also contribute toward excessive carrier recombination and low overall carrier extraction.

In other device growth investigations, we also considered whether a $CdCl_2$ heat treatment after deposition of the CdTe:In film onto a CdTe:P wafer could offer any benefits. In Figure 57a, four devices with $CdCl_2$-treated CdTe:In films are shown, with and without a CdS:In layer between the CdTe:In and TCO, and with and without an anneal after the TCO deposition. While J_{sc} values do improve slightly relative to the case without $CdCl_2$, the J_{sc} remains far below that which was observed in device structures without CdTe:In in Figure 56a. CV data (Figure 57b) show that, after the 310°C anneal following deposition of the TCO, hole concentration values of the absorber are near the expected ~1×10^{15} cm^{-3}, whereas devices without the anneal appear to be depleted.

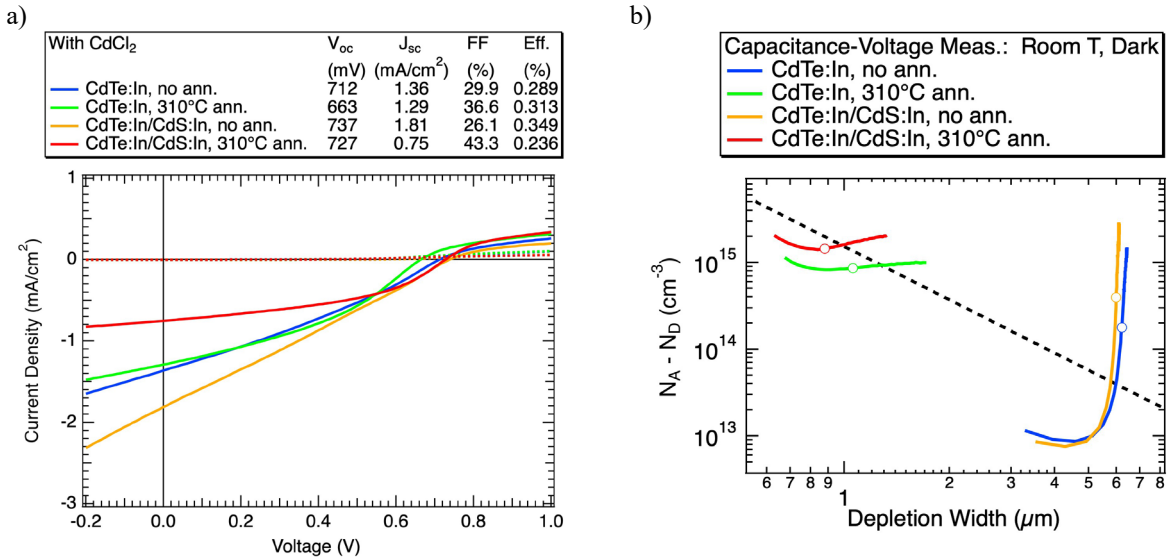


Figure 57: Device structures with $CdCl_2$-treated CdTe:In. a) JV. b) CV.

6.5.3 Assessing band alignment, CSSE deposition distances, n-layer dopant, diffusion

Several sets of homojunction PV devices were fabricated as follow-up to previous device work. In the first case shown here, devices were fabricated using thinner CdTe:In layers than had previously been used (Figure 58). These devices were fabricated both with and without an additional CdS:In layer between the CdTe:In and ZnO/ZnO:Al transparent conducting contact because of the potential band offset benefits of including the CdS:In layer. Despite reasonable V_{oc} values of >800 mV observed when incorporating the additional CdS:In layer, J_{sc} values remained low. External quantum efficiency (QE) values were low for the lowest wavelengths, increasing slightly for longer wavelengths, and exhibiting a spike at the CdTe band edge near 825 nm. This QE behavior is typical of a buried homojunction, where only the longest-wavelength light, of greatest penetration depth, reaches the n-p junction region without first being absorbed, in this case, in the n-type region upon which sunlight is incident.

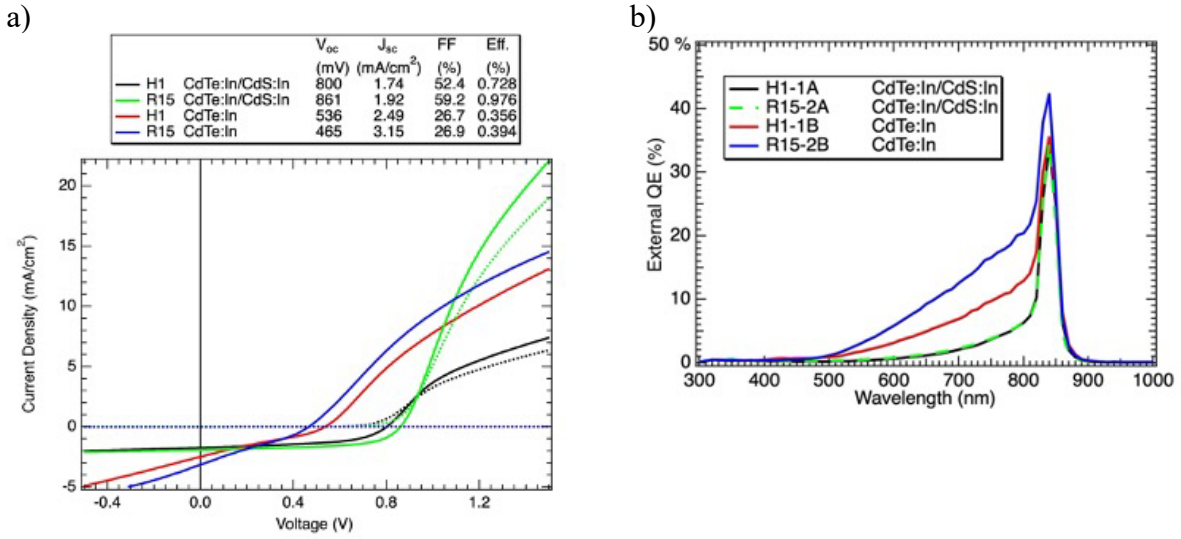


Figure 58: a) JV data and b) QE data for PV homojunction devices with thinner CdTe:In layers than previously used (H1 devices with CdTe:In of 100-230 nm thickness; R15 with 150-180 nm thickness). Evidence of a buried homojunction is shown in QE data.

In another experiment, the CSSE source-to-substrate distance was increased from the typical 3 mm to 7 mm in an attempt to reduce the coupling between source and substrate temperatures (Figure 59). While the CSSE technique has the benefit of relatively fast deposition (~µm/min rates) because of the close spacing between source and substrate, this geometry can also lead to challenges. Due to the close spacing, the substrate temperature rises significantly as the source material is heated to its deposition temperature of ~625°C, rising to 500-550°C during a film deposition using 3 mm spacing despite a substrate setpoint of 200°C. Increasing this spacing resulted in similar ultimate substrate temperatures. Film thickness was controlled to <100 nm, to which the greater spacing may have contributed. The device implementing the additional CdS:In layer that may offer band alignment benefits enables reasonably high V_{oc} of 841 mV coupled with the highest J_{sc} value to date, though J_{sc} remains limited. The buried-junction behavior remains evident in QE data.

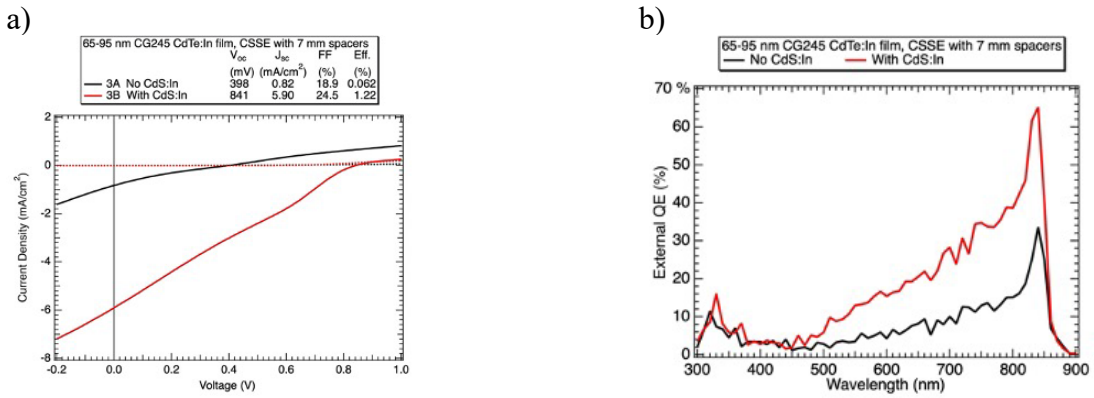


Figure 59: a) JV and b) QE for PV homojunction devices fabricated by CSSE using greater source-substrate distance of 7 mm instead of the typical 3 mm. CdTe:In film thicknesses are also < 100 nm. Despite these differences from previous processing, evidence of a buried homojunction is shown by QE.

In the next experiment, the CdTe:In thin film was replaced with a **CdTe:I** film (Figure 60). Because diffusion and activation of I may differ from those of In, this alternate dopant was also investigated. Device behavior, however, was similar to that of devices incorporating In-doped films. The device containing CdS:In shows reasonable V_{oc} and a somewhat higher J_{sc} compared to earlier results, but J_{sc} again remains limited. QE data show buried homojunction behavior.

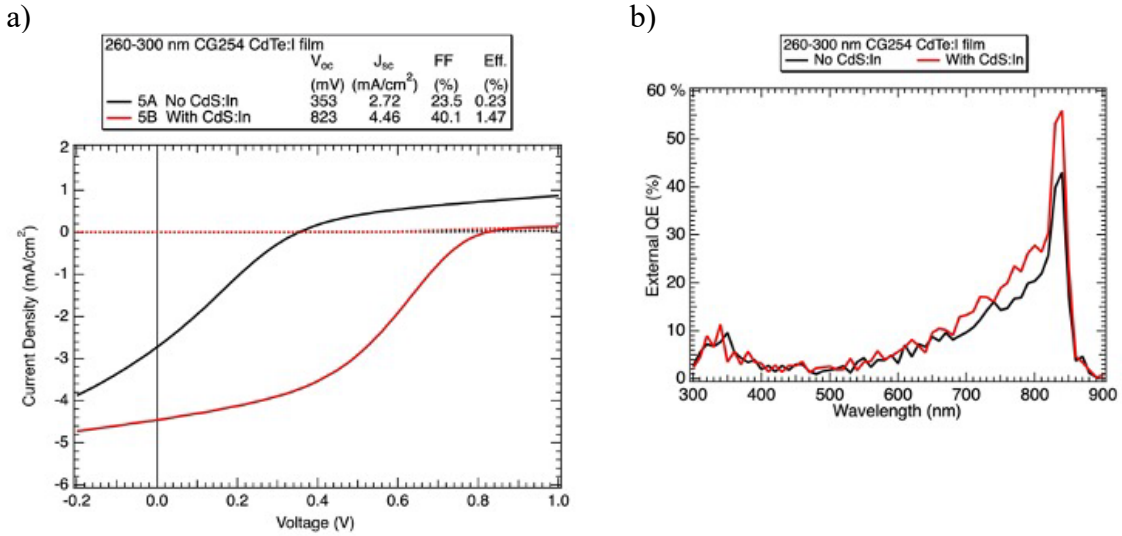


Figure 60: JV and QE for PV homojunction devices with a CdTe:I film. Evidence of a buried homojunction is shown by QE.

Because of the known diffusion issues in depositing doped CdTe films to form the homojunction, an alternative approach was attempted for comparison. In this case, undoped CdTe films of two thicknesses were deposited onto CdTe:P wafers. Then, a 5-nm-thick In layer was deposited onto the film surface by RF magnetron sputtering. Next, the structure was subjected to a thermal anneal at 115-180°C in a tube furnace in flowing He to drive In into the CdTe layer. Device fabrication omitting the CdS:In layer but including the ZnO/ZnO:Al front contact bilayer followed, but the typical 250-300°C thermal anneal following the front contact deposition was omitted. For comparison, 5 nm of In was also deposited directly onto a CdTe:P wafer and subjected to the same thermal anneal. One of these wafer-only structures also included the CdS:In layer. Despite what was expected to be limited In diffusion into the undoped CdTe film, J_{sc} values remained low (Figure 61) and QE showed buried homojunction behavior for the devices incorporating the undoped CdTe layer.

In contrast, the devices in which the In was diffused directly into the CdTe:P wafer showed significantly higher, though limited, J_{sc} (Figure 61). QE, in this case, did not show the typical buried homojunction behavior, but rather showed fairly constant QE across the wavelength spectrum, with the additional superposition of interference fringes due to the front contact films. SIMS data regarding the diffusion depth of In in these samples are discussed below. The limited performance of the devices incorporating the undoped CdTe layers may also be evidence that carrier lifetime values in the films may be quite limited and interfering with carrier collection. Verifying carrier lifetime values for these thin films is challenging. To reduce the effects of surface recombination, surface passivation is required. However, most common techniques, such as deposition of an Al_2O_3 passivating layer, also require a $CdCl_2$ heat treatment as follow-up for

reasonable passivation. This treatment would irrevocably change the film to the extent that the measurement would no longer be providing the desired information. Temporary passivation techniques for CdTe surfaces are being developed at NREL, but, at this time, have shown greater success on polycrystalline thin films than on single crystal surfaces such as wafers or epitaxially-grown films.

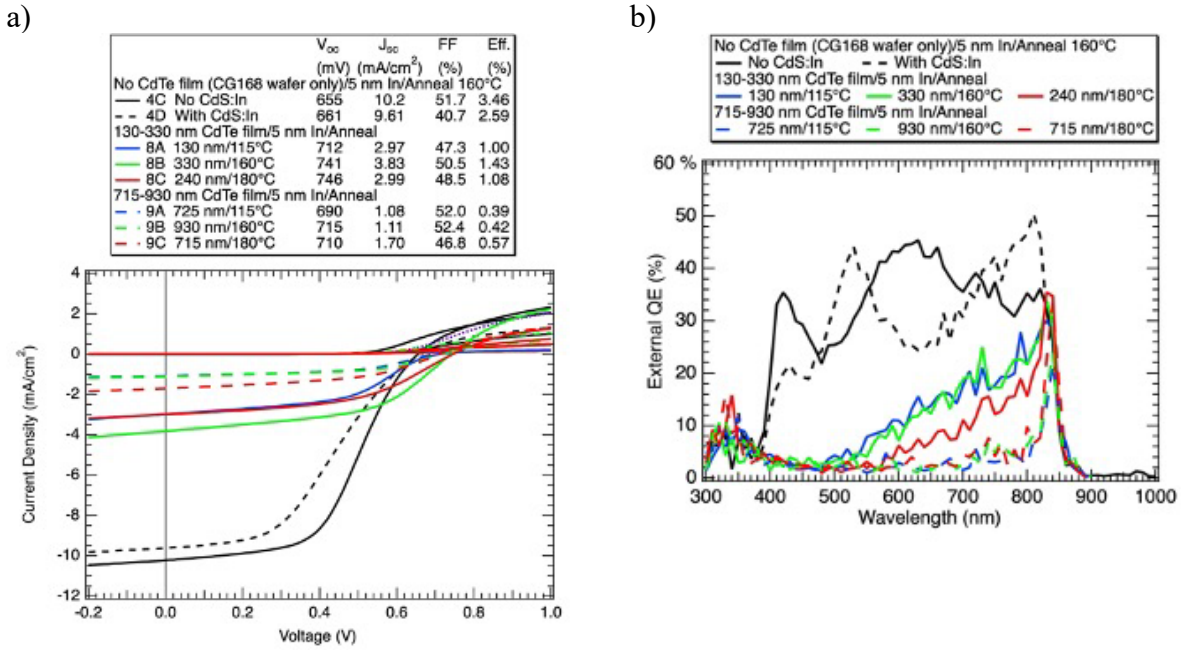


Figure 61:. JV and QE for PV homojunction devices with diffused In into either undoped CdTe film (8A-C film thickness 130-240 nm, 9A-C film thickness 715-930 nm) or directly into CdTe:P wafer (no film). Evidence of a buried homojunction is shown by QE for devices containing the undoped CdTe film but not the devices without the undoped CdTe film.

Additional devices with In diffused into a CdTe:P wafer were processed at different thermal anneal temperatures so as to observe any differences in device behavior with tuning of the depth of In diffusion. Two additional devices with diffused In layers were fabricated for comparison with previous results (Figure 62). In these devices, 5 nm of In was sputtered onto the surface of a CdTe:P wafer with a subsequent anneal at 120°C and 170°C, respectively. This fabrication procedure produced devices with considerably higher J_{sc} values than those observed previously for devices incorporating deposited film layers. In addition, external quantum efficiency (QE) appeared reasonably uniform across the wavelength spectrum (though affected by, as is typical, the superposition of the interference fringes of the front contact layers). In comparison, a device incorporating an *n*-type CdTe:In film (Figure 62, red trace) showed low QE for the shortest wavelengths, increasing slightly for longer wavelengths up to the CdTe band edge near 825 nm. This QE behavior is typical of a buried homojunction, where the longest-wavelength light, of greatest penetration depth, preferentially reaches the *n-p* junction region without first being absorbed, in this case, in the *n*-type region upon which sunlight is incident. An additional device with a CdTe:I layer experienced front contact delamination issues; this condition was repeated in the following experimental set.

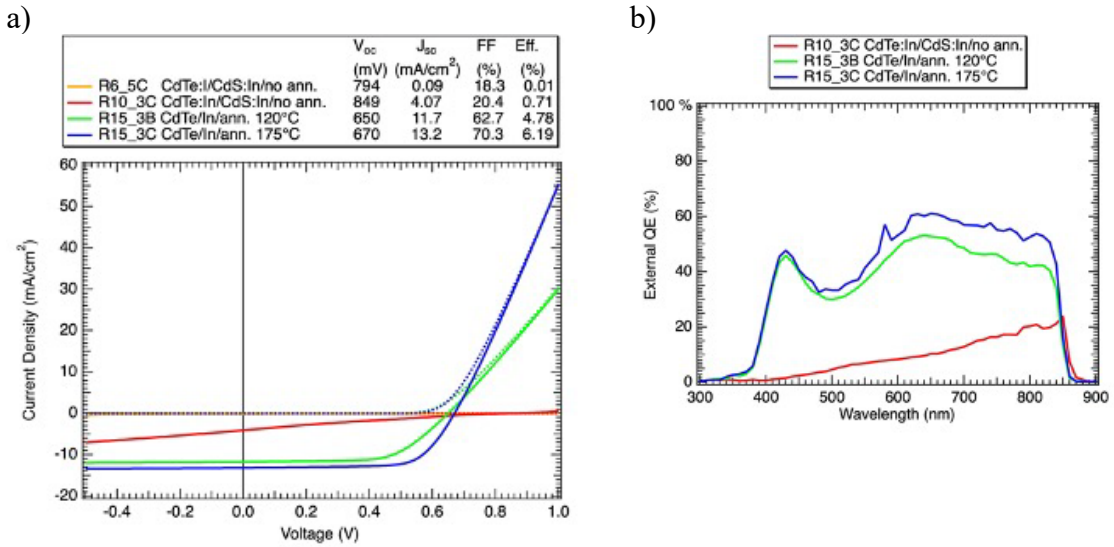


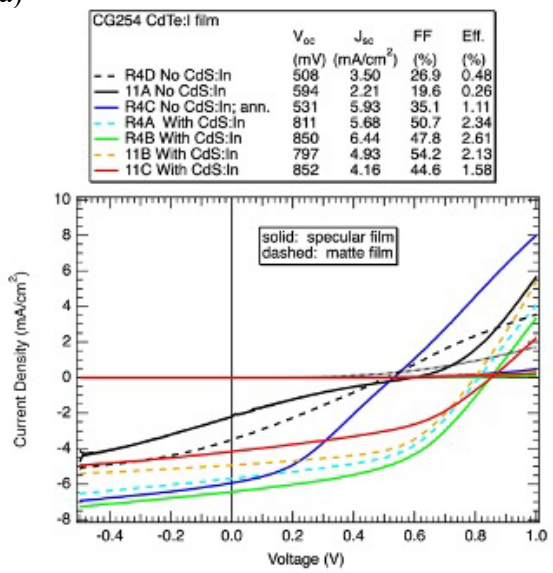
Figure 62: a) JV data and b) QE data for PV homojunction devices. Through the device with a deposited CdTe:In film layer (red trace) showed evidence of a buried homojunction in QE data, this effect is absent in the diffused In devices (blue and green traces).

In the last set of homojunction devices, we implement a CdTe:I film that includes a CdS:In layer that may have band alignment benefits; in this case, the front contact was not be annealed to prevent convolution of I and In doping. CdTe:I film thicknesses were constrained to <200 nm (Table 11) to enable sufficient light transmittance to the junction region. Device performance (Figure 63) was particularly limited for the devices in which a ZnO/ZnO:Al bilayer was deposited directly onto the CdTe:I layer. Annealing this front contact stack at 270°C for 30 min improved the J_{sc} (potentially by enabling interface improvements through, for example, healing of sputter damage at the ZnO/CdTe:I interface) but did not have a significant effect on V_{oc}. The addition of a CdS:In layer improved both V_{oc} and J_{sc}. The CdS:In layer may offer band alignment benefits that can lead to these improvements. No annealing was performed after deposition of the CdS:In layer to prevent possible In diffusion from this layer from confounding effects of the CdTe:I film layer. In general, the device with the thinnest CdTe:I layer, which enables the greatest light transmittance to the *p-n* junction, showed the highest J_{sc}. The CdTe:I film appearance on the surface of the CdTe:P wafer, specular vs. matte, was also considered. It was found previously that films having a matte appearance exhibit significantly higher roughness than specular films. This apparent roughness, however, was not found to correlate strongly with device performance in this limited set.

Table 11: CdTe:I film thicknesses for devices shown in Figure 63.

Name	Film thick. (nm)
R4D	20-200
11A	74
R4C	Not applic.
R4A	130
R4B	60
11B	155
11C	140

a)



b)

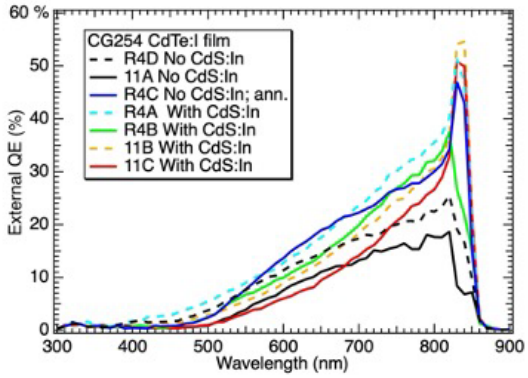


Figure 63: a) JV and b) QE for PV homojunction devices incorporating CdTe:I films. Despite the thin CdTe:I films used, the signature of a buried homojunction remains for all devices in QE data.

6.5.4 SIMS on devices

Secondary ion mass spectrometry (SIMS) measurements were performed to verify the depth of In diffusion for a thin *n*-type CdTe:In film (~0.9 µm) deposited onto a *p*-type CdTe:P wafer, matching the general structure that was used in homojunction devices (though this test structure did incorporate a somewhat thicker CdTe:In film than that typically used in devices). Rather than the In being primarily limited to the thickness of the CdTe:In film, In was found to diffuse to a depth of several µm (Figure 64a). This is consistent with the observed buried homojunction behavior observed in JV and QE data. Ideally, the *n*-type layer in a CdTe:In/CdTe:P homojunction device would be limited to ~200 nm or less to enable sufficient light to reach the main *n*-*p* junction and generate a sufficient number of carriers which, if extracted, could enable high J_{sc}. These data indicate that, even for a CdTe:In film with a thickness nearer 100-200 nm, the diffusion depth of In will likely preclude high carrier generation in the junction region, with the majority of light being absorbed exclusively within the broadened In-doped n-type layer before it reaches the junction region.

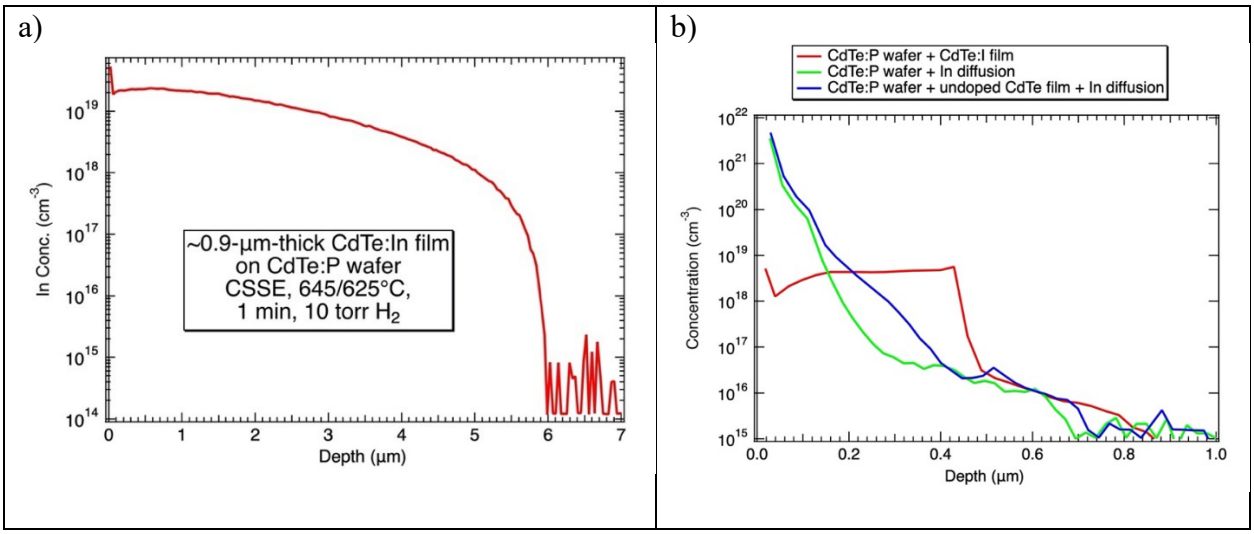


Figure 64: a) SIMS depth profile of ~0.9 µm thick CdTe:In film grown on a CG168 CdTe:P wafer. Indium diffusion to several µm depth occurs during film growth. b) Depth profile for three additional films, with structures i) CdTe:P wafer/CdTe:I film, ii) CdTe:P wafer with 5 nm In layer subjected to a diffusion anneal at 160°C for 30 min, iii) CdTe:P wafer with ~400-nm-thick undoped CdTe film and similar 5 nm diffused In film.

In a follow-up experiment, additional films were analyzed by SIMS (Figure 64b). In the first, a CdTe:I film of thickness ~250 nm was deposited onto a CdTe:P wafer. This same film was used for the homojunction PV devices shown in Figure 60. The I concentration is found to be in a range suitable for *n*-type doping, but the extent of the high concentration region is greater than ideal, consistent with the buried homojunction behavior observed. The ~0.45 µm I depth does appear to be limited in comparison to the several µm of In diffusion shown in Figure 64a, however. Further homojunction device work with CdTe:I films may be worthy of investigation.

The other profiles in Figure 64b are a comparison of diffusing a 5-nm-thick In film into the surface of a CdTe:P wafer vs. into a CdTe:P wafer with a ~400-nm-thick undoped CdTe layer deposited by CSSE. The indium diffusion profiles in these cases appear similarly shaped, with the wafer+film structure showing higher In concentrations from the surface to a depth of ~400 nm. The significant difference in JV and QE behavior between the devices with and without the undoped CdTe film suggests that there may be other device performance limitations beyond the In concentration at depth. The film layer may have a short carrier lifetime, for example, or interface recombination may also be high, enabling poor carrier extraction.

6.5.5 Final comments on devices

The growth of n-type CdTe:In layers using the CSSE method leads to excessive diffusion of In and PV devices that act as buried homojunctions. Despite lesser dopant diffusion observed for CdTe:I films, devices implementing these CdTe:I films have also behaved as buried homojunctions.

The significant difference between device performance in devices without a CSSE film (CdTe:P wafer only with diffused In and polycrystalline front contact layers) and similar structures that incorporate doped CdTe films grown by CSSE suggests that there may be carrier lifetime limitations in these CSSE films or high recombination velocity at the film interfaces. Measuring

the carrier lifetime in the thin films is difficult because of the high surface recombination velocity at the free surface of the film.

If this free surface could be passivated effectively, it might be possible to clarify the lifetime in the thin film. Most of the known CdTe passivation techniques (for example, deposition of an Al_2O_3 film followed by a $CdCl_2$ heat treatment) would alter a thin film significantly. NREL is developing a temporary CdTe surface passivation technique, but it currently has been most effective for polycrystalline thin films and has had limited effect for single-crystal surfaces and films, and thus requires further development. The additional interfaces present when depositing the doped CdTe film layer may themselves present significant additional complications. Despite epitaxial growth of the thin doped CdTe films, as confirmed previously with electron backscatter diffraction, interfacial defects may remain prevalent, requiring addition mitigation.

7 Suggestions for Future Work and Path Forward

At this point in the project we have identified that CdTe is likely to be more successful than CdSeTe for film production due to problems with differential element incorporation in films, despite the advantage in CdSeTe for being closer to the radiative limit without Cd annealing treatments in its as-grown crystalline form. The data so far show that incorporating enough dopant into the crystal and into the film is not the issue. Activation by Cd annealing treatments leads to large carrier concentrations in CdTe:I, and rapid thermal annealing allows high carrier concentration and performance near the radiative limit in CdTe:In, even without Cd annealing. However, the performance of as-deposited films is still poor. It may be that Cd annealing treatments are required after film deposition. This will likely improve carrier concentration but may also reduce the lifetime, depending on whether it is limited in the films by carriers or by defects.

The devices perform as if they have a *buried junction*, thus the window layer is too thick or lifetime is short. It may be that there is interdiffusion between In and P such that the thin layer of CdTe:In is depleted. It appears that P diffuses a little, but the substrates may have had inhomogeneous P concentration. Iodine may diffuse less than indium, but the diffusion may or may not be the primary issue in poor device performance. If a significant amount of In is diffusing from the CdTe:In layer, it could lead to a low electric field in the p-n junction region and the poor carrier collection observed. More careful determination of where the *p-n* junction lies in our device structures would be helpful in determining reasons behind the poor J_{sc} observed. We will consider electron-beam induced current (EBIC) and Kelvin Probe Force Microscopy (KPFM) measurements for more information.

The growth of *n*-type CdTe:In layers using the CSSE method leads to *excessive diffusion of In* and PV devices that act as buried homojunctions. Based on recently acquired SIMS data, CdTe:I films, should they be controllable to thicknesses < ~200 nm, may have greater promise. However, even thinner films apparently have issues with either bulk lifetime or (more likely) interface recombination effects. Some of the iodine crystals showed high concentrations of metallic impurities, and if reduced these could improve carrier properties. The significant difference between device performance in devices without a CSSE film (CdTe:P wafer only with

polycrystalline front contact layers) and similar structures that incorporate doped CdTe films grown by CSSE suggests that *there may be carrier lifetime limitations in these CSSE films or high recombination velocity at the film interfaces*. Measuring the carrier lifetime in the thin films is difficult because of the high surface recombination velocity at the free surface of the film.

Passivation techniques for the sake of measurement of the bulk lifetime may be possible, and atomic layer deposited (ALD) Al_2O_3 could be tried. We could work to determine whether 1-photon TRPL measurements on any of our structures would be informative. We will also consider whether a passivated structure (for example, with Al_2O_3) could enable information about carrier lifetime in thin CdTe:In films to be gleaned. Al_2O_3 passivation, when optimized, typically requires a $CdCl_2$ treatment subsequent to the Al_2O_3 film deposition, however, which may affect In diffusion in a sample.

Some adjustments could be made to the substrate, such as a higher hole concentration CdTe:P (e.g., CG155), or even switching the homojunction to try a *p*-type CSSE layer on a highly doped *n*-type CdTe:In crystal substrate. Additionally, surface treatments prior to CSSE could be explored, such as comparing cleaved, mechanically polished, chemo-mechanically polished, peroxide treatment, and very thin (<500 μm) substrates. These surfaces could be measured by positron annihilation spectroscopy, which has previously shown large differences in sub-surface damage in CdTe with these different surface treatments.

Finally, it may be possible to improve the thermal isolation between the substrate and the CSS source, somewhat slowing down any dopant diffusion. Film thickness control remains limited for CSSE. Further consideration of methods that might enable enhanced control is required. *Improved modeling* may enable distinction between effects due to film thickness, dopant profile, bulk film lifetime, surface recombination, and interface recombination.

8 Impact and Conclusions

<u>High-level cumulative results for the project:</u>

- Initial device modeling has set specifications for desirable thickness ranges of the *n*-type layer, <200 nm.
- 3 different crystals were grown with iodine doping of CdTe at target levels 2×10^{18} cm^{-3}, 2×10^{19} cm^{-3}, and 2×10^{20} cm^{-3} iodine. Between 5-10% of the intended iodine was incorporated into the crystal. As-grown electrical properties are not outstanding, but annealing in Cd improves conductivity in all compositions, resulting in carrier concentrations in the 10^{16}-10^{18} cm^{-3} range in the crystals. The best performing crystal is CG252, with the middle iodine doping level.
- Thick (10-40 μm) close space sublimation epitaxy (CSSE) films of CdTe:In, CdSeTe:In, and CdTe:I were grown on insulating CdTe or $Cd_{0.9}Zn_{0.1}Te$ substrates (CG176, CG224, or CG236) to measure Hall effect, EBSD, and 2PE-TRPL. Films were grown in N_2 or H_2 ambient and subjected to additional rapid thermal anneal (RTA). These variations resulted in different electrical properties. Indium levels up to 3×10^{19} cm^{-3} and iodine levels up to 7×10^{17} cm^{-3} were achieved in the CdTe films.
- Over 40 *p*-*n* junction devices were deposited on CdTe:P single crystals to assess the important parameters in the device fabrication. Thickness control of CSSE for the thin layers was a challenge. Several parametric experiments have suggested that the device performance

problems are not due to the back contact or the doping level in the *p*-type substrate, but rather poor external quantum efficiency (QE) in the *n*-type layer due poor charge transport. The results suggest a buried junction, which could be due to excessive thickness, poor lifetime, or diffusion of the dopants.

- Further experiments suggested that the buried junctions were due at least in part to diffusion of the *n*-type dopant from the film into the substrate, making the actual junction deeper than desired for the device. However, a contribution of the carrier lifetime in the *n*-type film cannot be ruled out as influencing the poor device performance. Diffusion of iodine during the CSSE process may be less than for indium.

9 Budget and Schedule

Period of Performance: 3/1/2021 – 8/31/22.
Originally the project was scheduled to end 2/28/22, but a no-cost extension to the 08/31/22 and was approved. The reason for the request was the delayed progress at NREL due mainly to equipment issues and availability of staff.

This work was a Cooperative Agreement. The budget summary is below. Cost share was provided by the Washington State University Institute of Materials Research and the federal funds were spent.

Federal share	$189,912
Cost share (20% of total)	$75,097
Total	$265,009

10 Products and Publications resulting from this work

Full Author List	Paper title	Conference	Location	Date
John S. McCloy, Rubi Gul, Magesh Murugesan, Marc Weber, Santosh Swain, Saketh Kakkireni, Samuel Bigbee-Hansen	II-VI Materials Growth and Characterization at the WSU IMR	US Workshop on the Physics and Chemistry of II-VI Materials	Chicago, IL	10/26-29/2021
Samuel Bigbee-Hansen	Cadmium Telluride: a Study on the Effects of Iodine Doping	MS Thesis, Materials Science & Engineering	Pullman, WA	6/3/2022

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