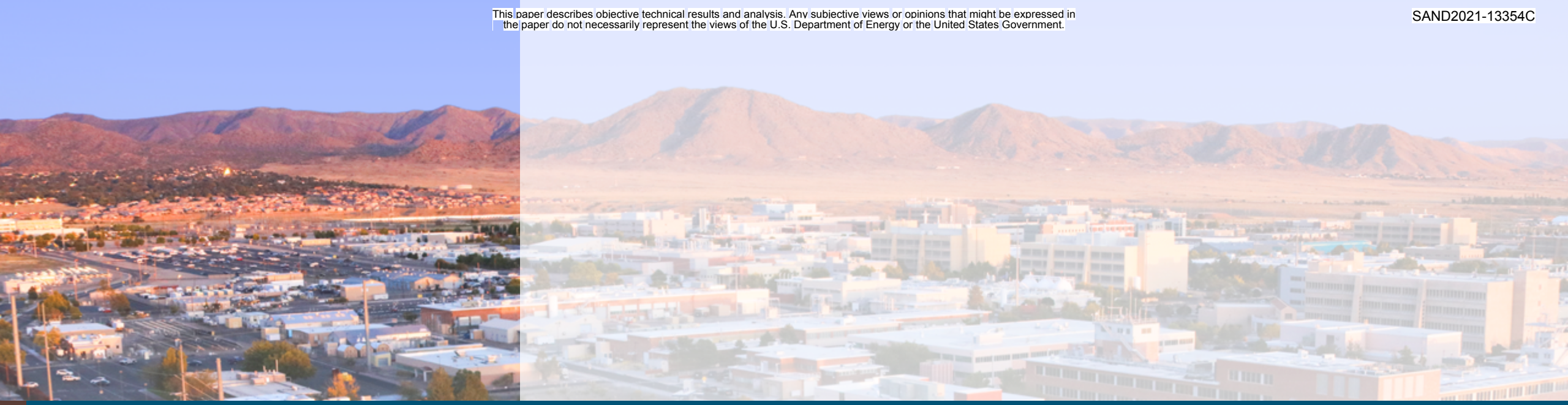
SAND2021-13354C



Digital electronics at the atomic scale

Shashank Misra

Sandia National Laboratories

AVS Symposium (2021)

This work was supported by the Laboratory Directed Research and Development Program at Sandia National Laboratories, and was performed, in part, at the Center for Integrated Nanotechnologies, an Office of Science User Facility operated for the U.S. Department of Energy (DOE) Office of Science. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. A-0003525

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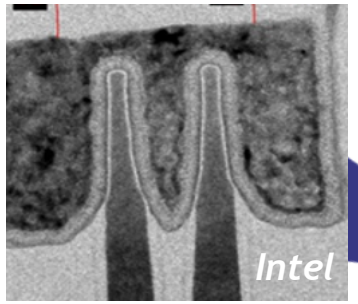
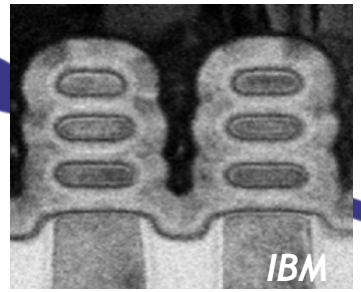
Interruption of virtuous cycle in semiconductor manufacturing

FINFET



22 – 7 nm

GAA-FET



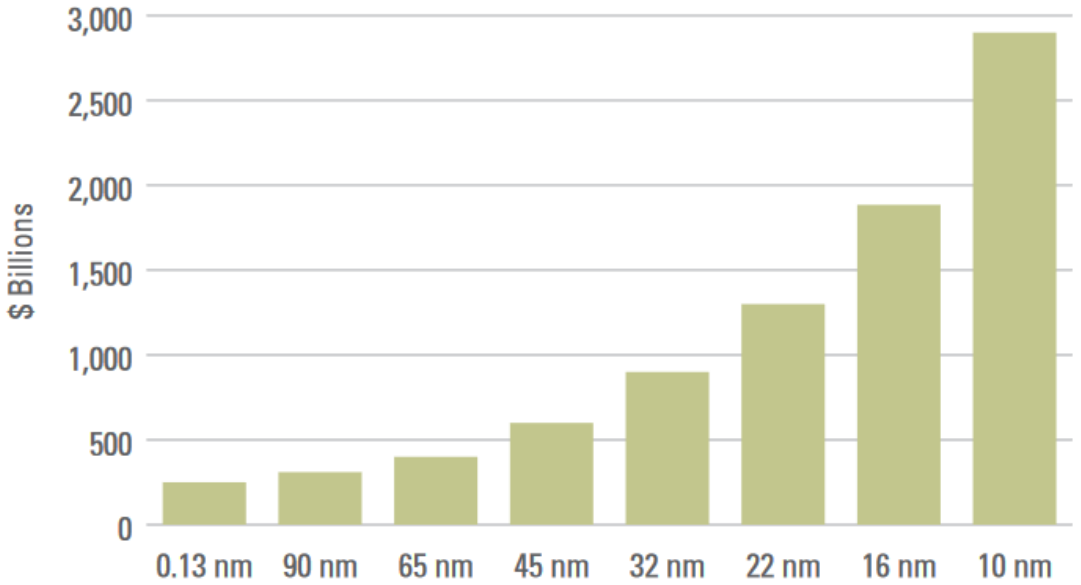
5-2 nm

What's next??

< 2 nm

What do I need to know?

Figure 5: Process Technology Development Costs by Node (US$ billions)



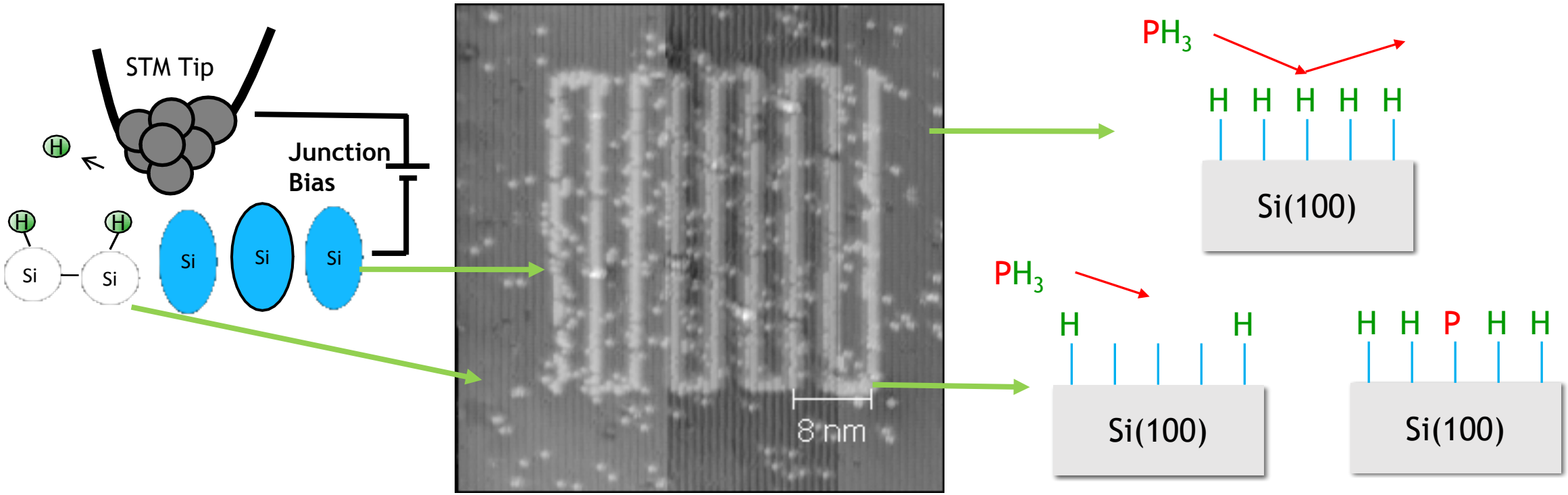
Source: Common Platform Technology Forum 2012 and AlixPartners analysis

Decreasing node sizes include radical changes – not just scaling.

R&D costs are increasing exponentially.

Relax manufacturing requirement and look for opportunities from the perspective of the atomic limit.

What is atomic precision advanced manufacturing (APAM)?



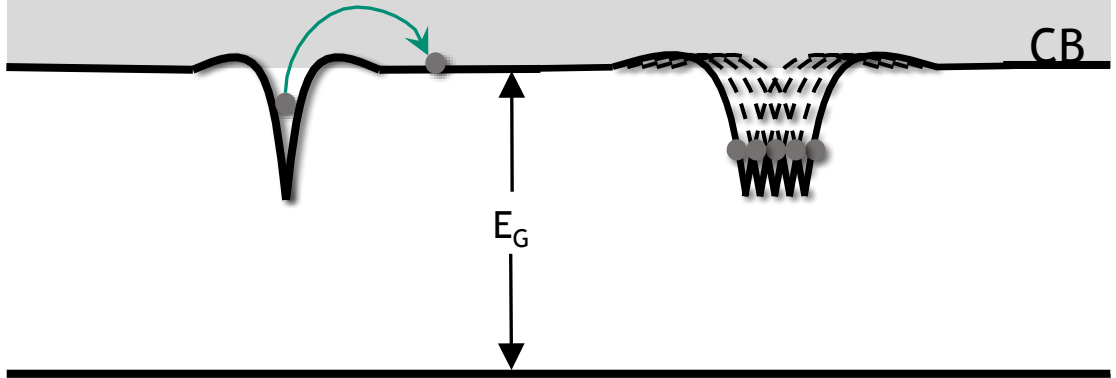
Chemical contrast at the surface of silicon

- Reactive unterminated Si
- Unreactive H-terminated Si

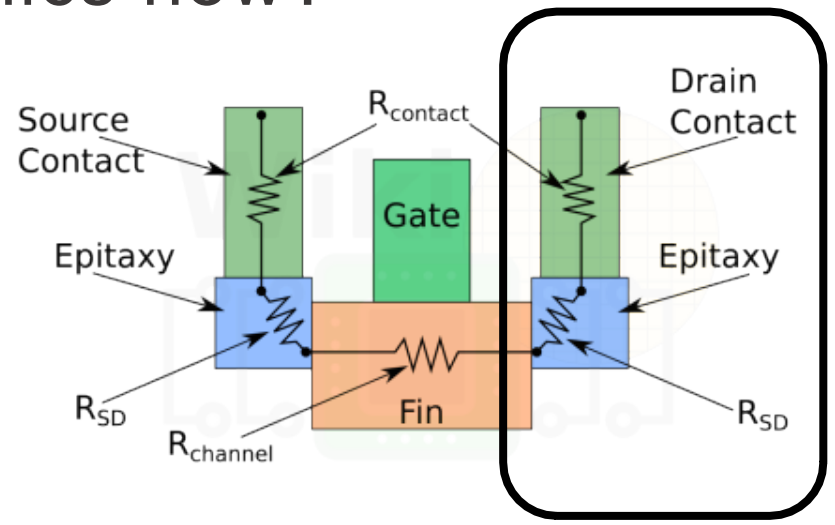
Selectively react with dopant precursor

What can APAM do for microelectronics now?

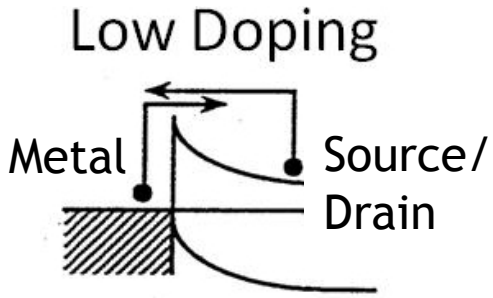
Normal doping:
Dopant donates electron to silicon

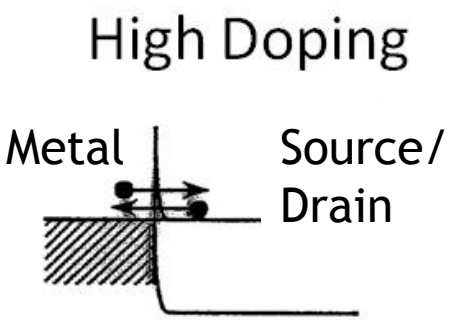


Ultra-doping:
dopant potentials overlap significantly



As transistors shrink, channel resistance goes down, but contact resistance goes up

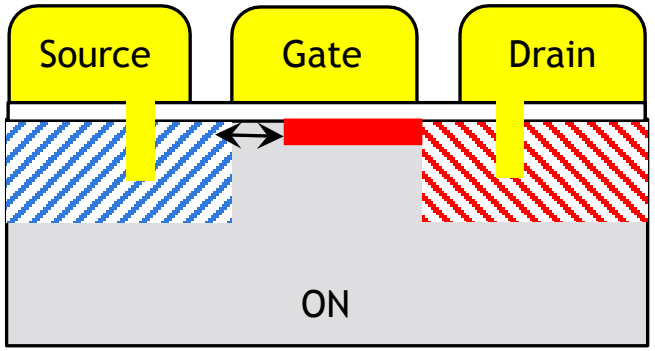


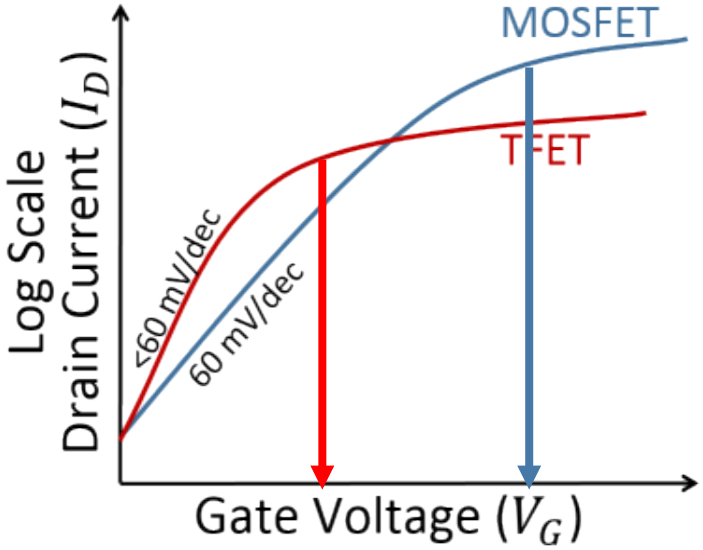


Dramatic control over material properties … better CMOS contacts

What can APAM do for microelectronics in the future?

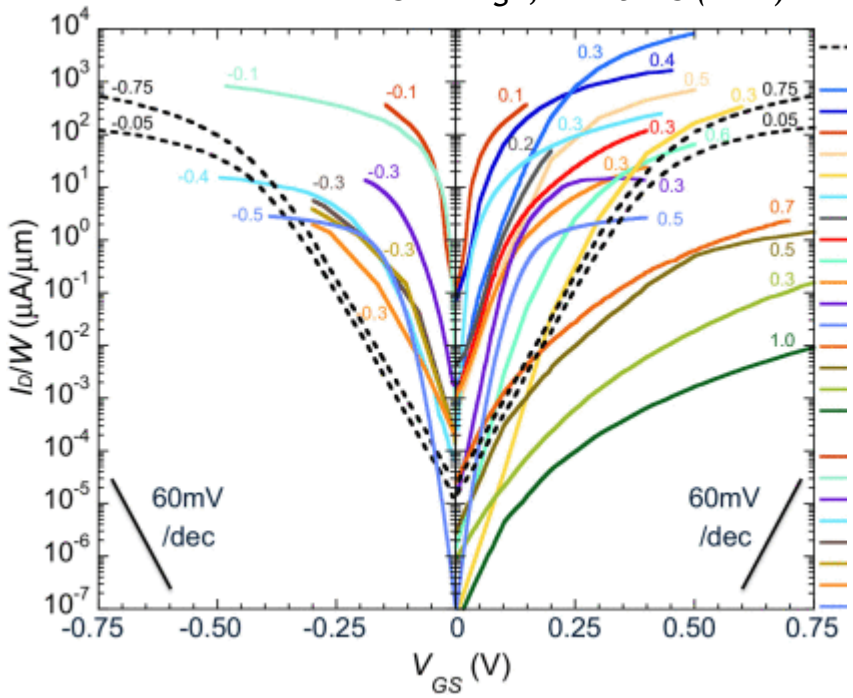
Tunnel field effect transistor (TFET)





TFETs 10x energy efficiency in theory

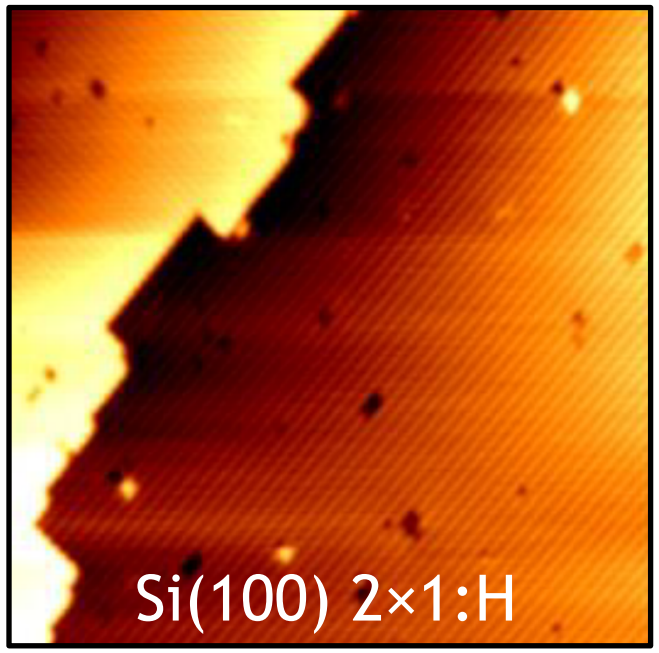
Lu & Seabaugh, IEEE JEDS (2014)

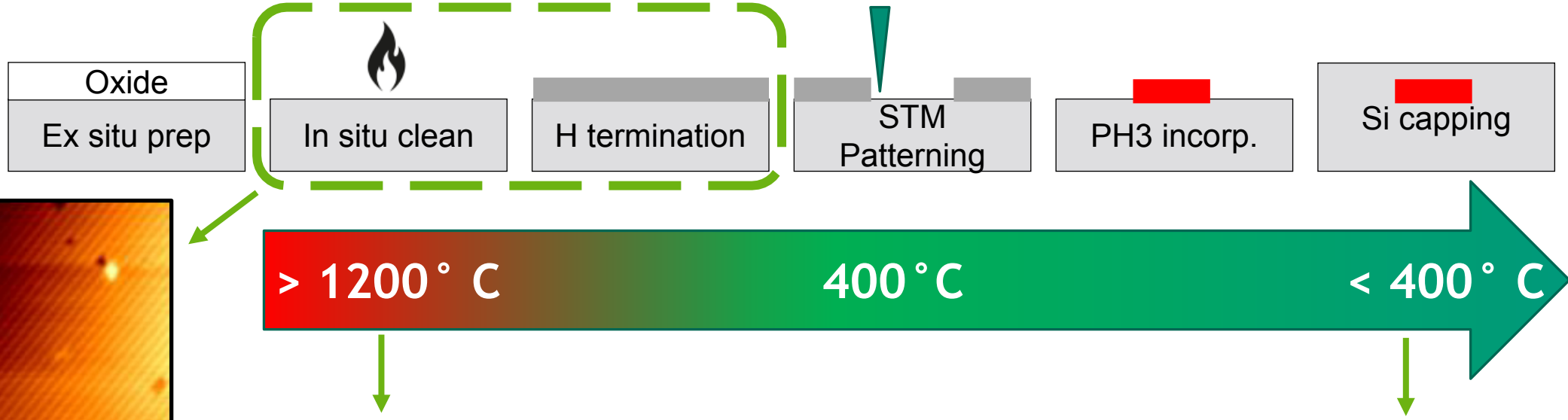


TFETs have not realized their promise in practice

What can you learn with atomic-scale degree of control?

Why has APAM not been used in this space?





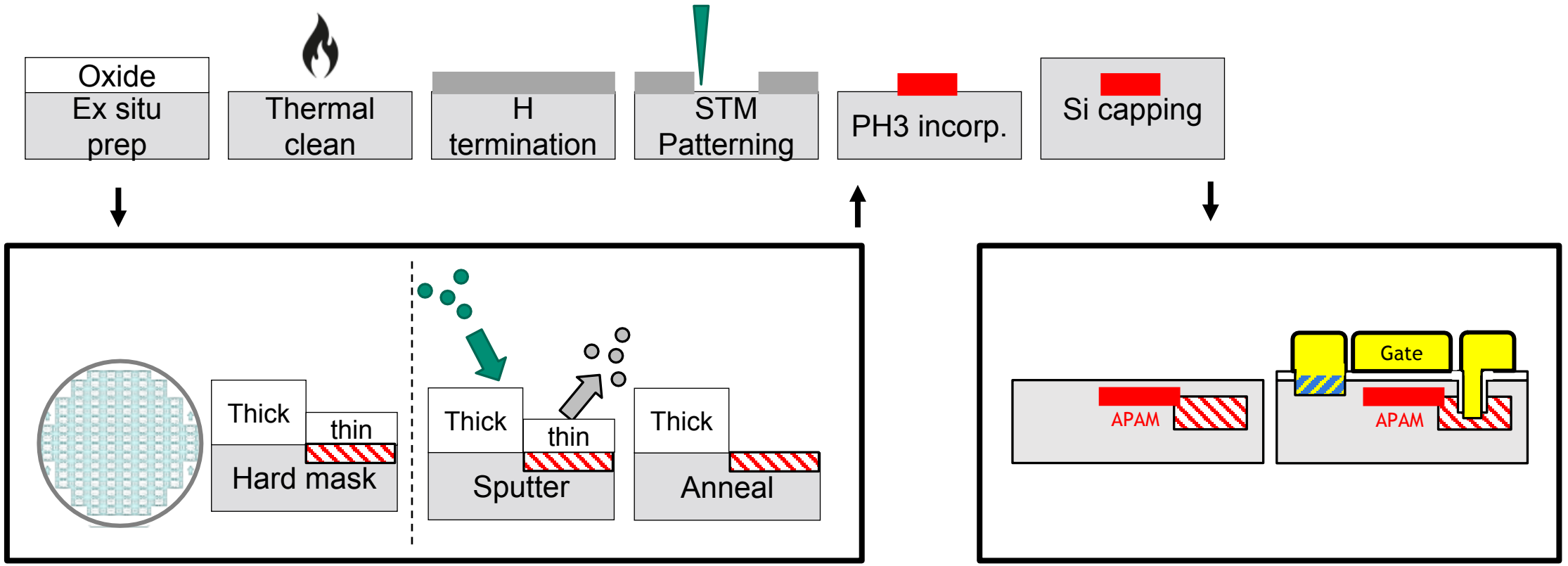
Too hot – creating an APAM-compatible surface will destroy everything else

Too cold – can't add much to chip after APAM without diffusing donors

Thermal budget issues preclude leveraging past investments in microelectronics

- APAM devices are simple (donors only)
- Devices only work at cryogenic temperature
- No path to manufacturability, etc.

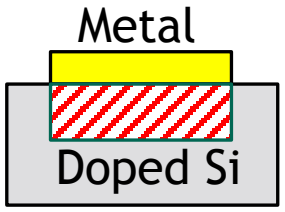
Outline – Digital electronics at the atomic scale

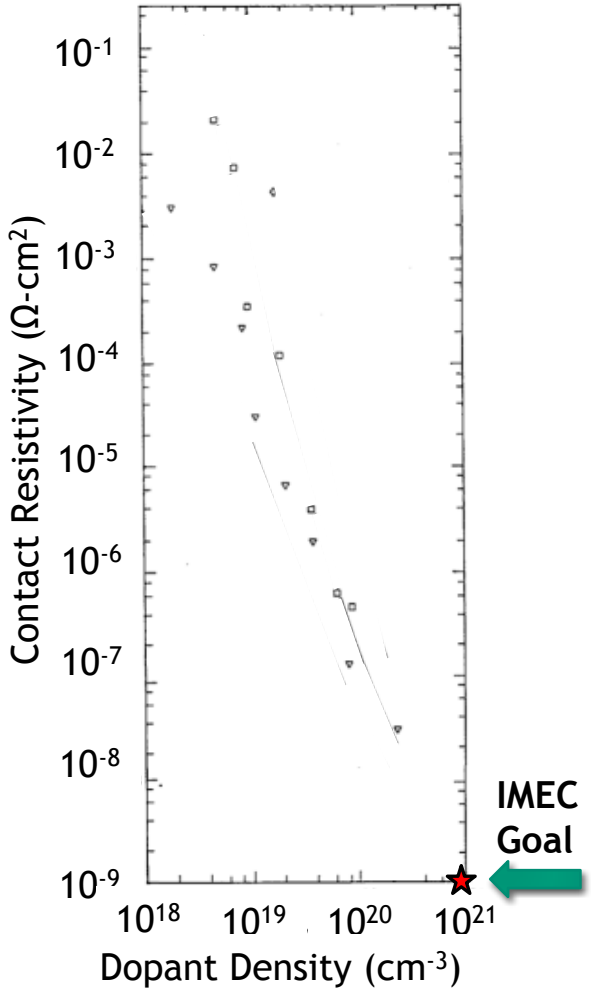


1. Integration with CMOS (contacts)
- Do no harm to parent CMOS
- Wafer-scale high-throughput APAM
- APAM robustness vs. CMOS

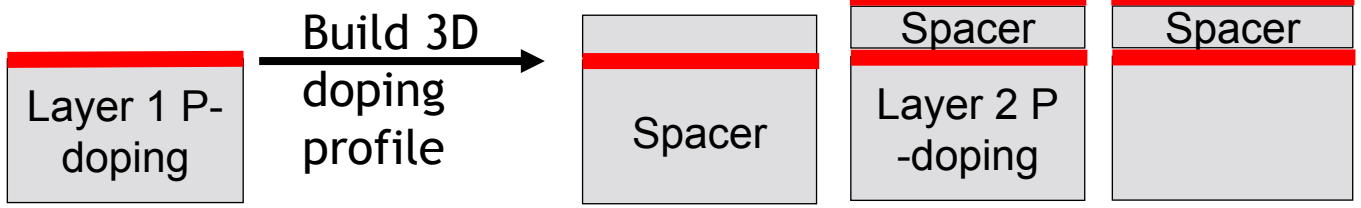
2. Sophisticated devices (TFET)
- Added features must preserve APAM
- Quality of APAM & other device elements

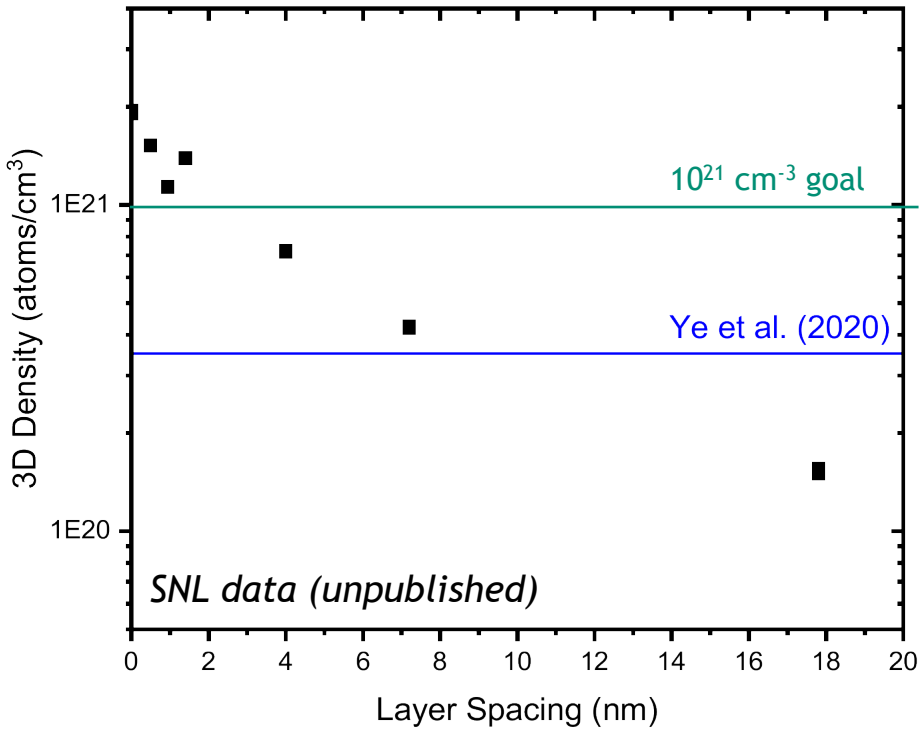
Why are APAM-enabled contacts interesting?





Single layer 4K magnetotransport:
n = 1.7 x 10^{14} cm^{-2}
μ = 50 cm^2/V-s
t = 1-2 nm





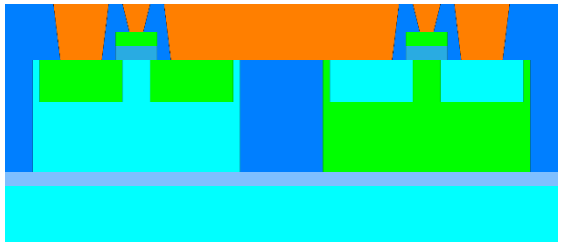
APAM beats state of the art in doping density

Working w/ K. Jones (Florida) on quantifying impact to contact resistance.

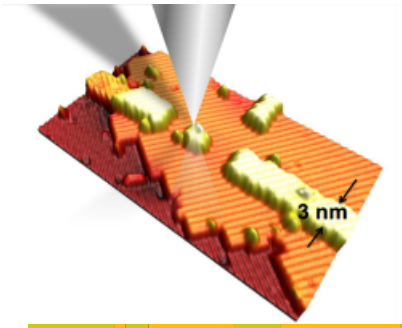
Can APAM be integrated into CMOS manufacturing?

Is it compatible with CMOS process flows?

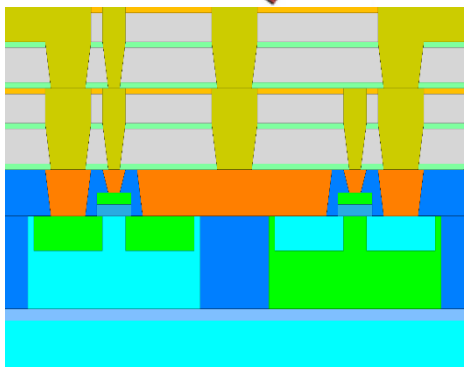
Transistors



APAM



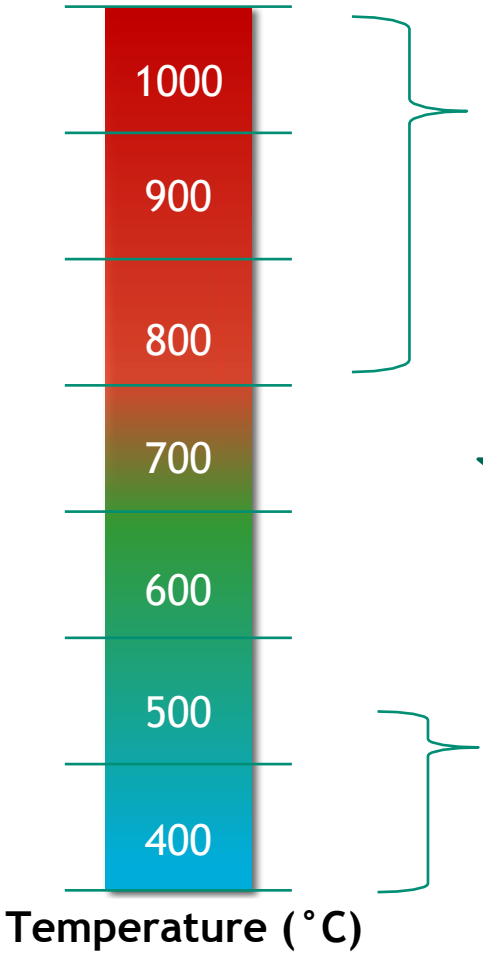
Metallization

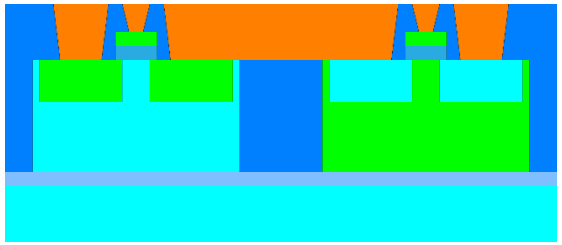


Can it be scaled?

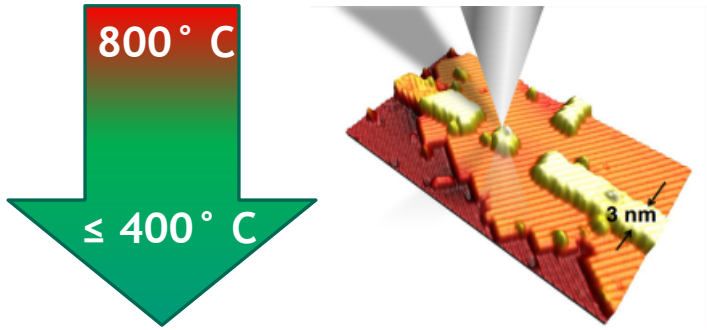
Does it hold up in accelerated lifetime testing?

APAM – CMOS integration

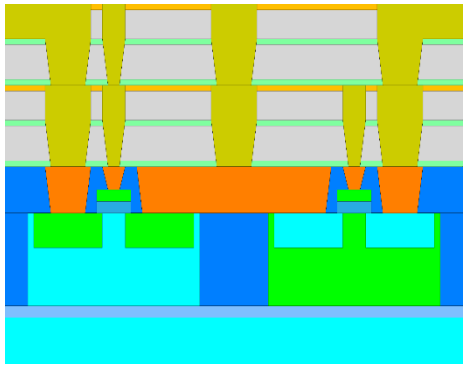




CMOS:
Front-End-Of-Line (FEOL)
Transistor generation



APAM Addition



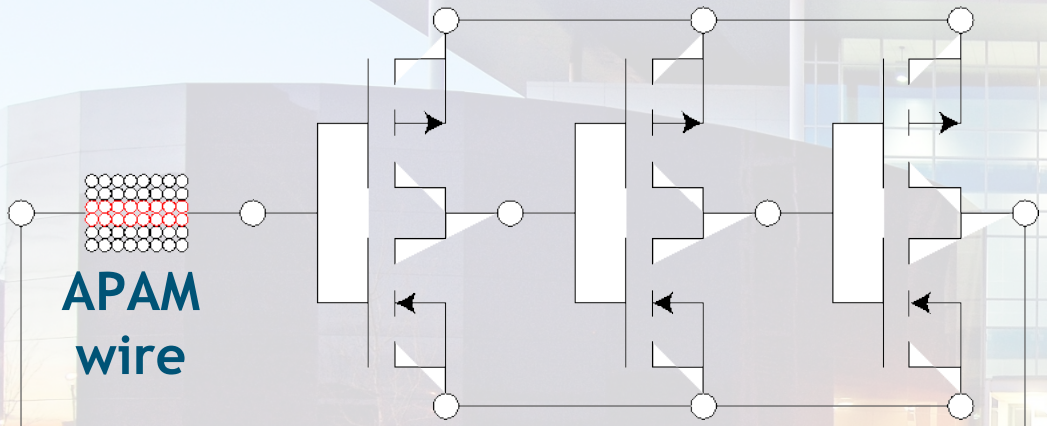
CMOS:
Back-End-Of-Line (BEOL)
Metal layers

APAM can do no harm to CMOS - thermal budget challenge

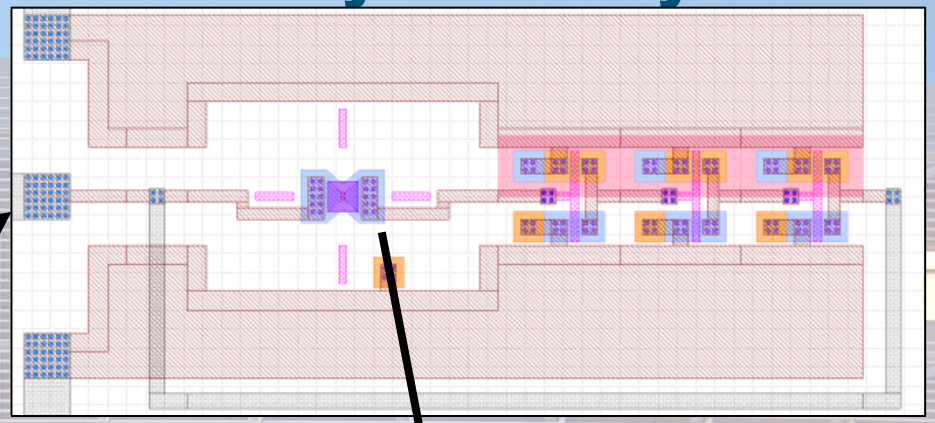
Design simple test of APAM + CMOS on the same chip

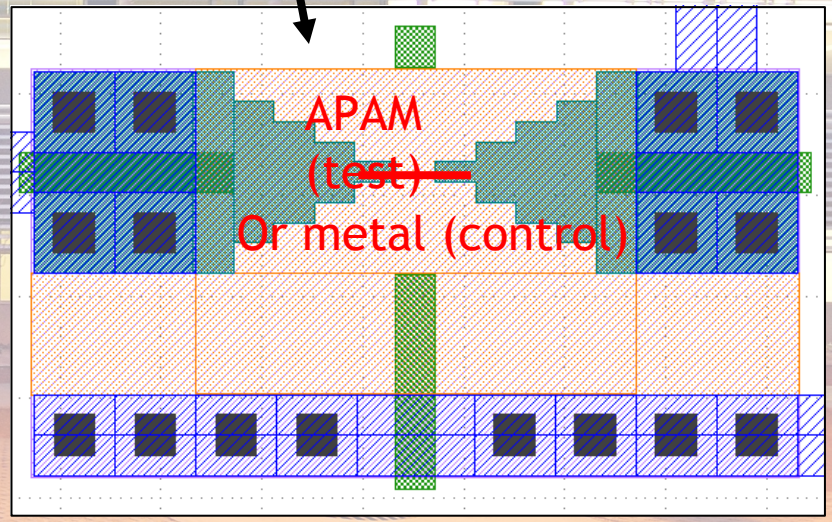
Circuit editor

CMOS Ring Oscillator



Physical Layout

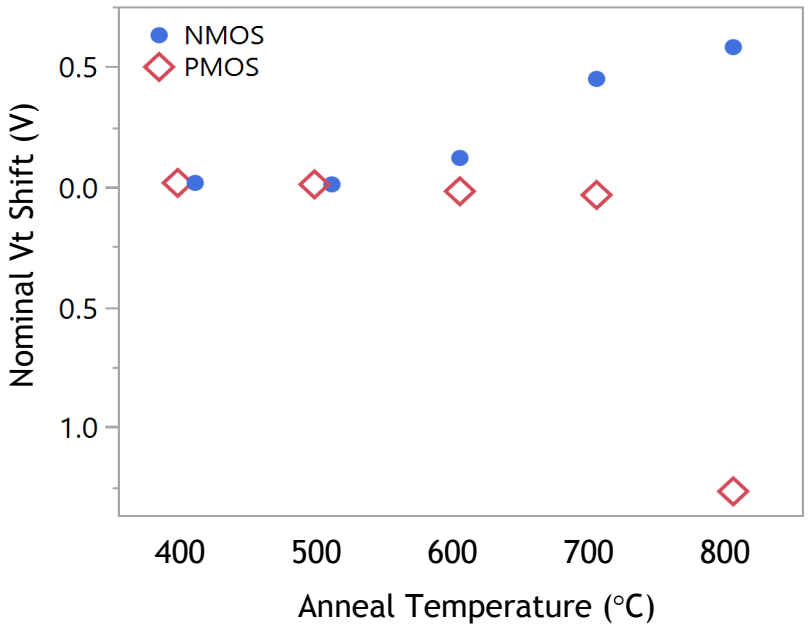




Easily able to design new APAM + CMOS circuits

Can we fully integrate APAM with CMOS? YES!!

Temperature effects on threshold voltage



Threshold shifts at T>650 C

Cleaning Condition	2D Carrier Concentration ($x10^{14} cm^{-2}$)	Carrier Mobility ($cm^2V^{-1}s^{-1}$)
Flash clean (1000 C, 1 hr) Oxide Ex situ prep Thermal clean	1.7	50
Sputter and anneal (650 C, 15 sec) Oxide Sputter Anneal	1.2	58

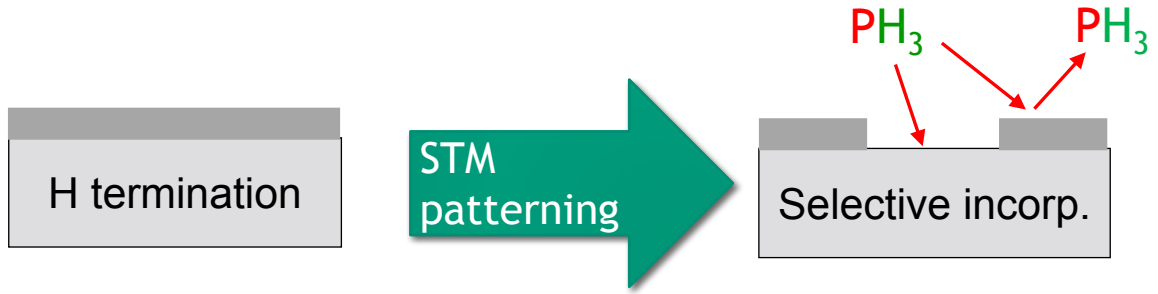
Punchline: Atomic scale processing session

CMOS-compatible processing of atomic-precision donor devices

DeAnna Campbell

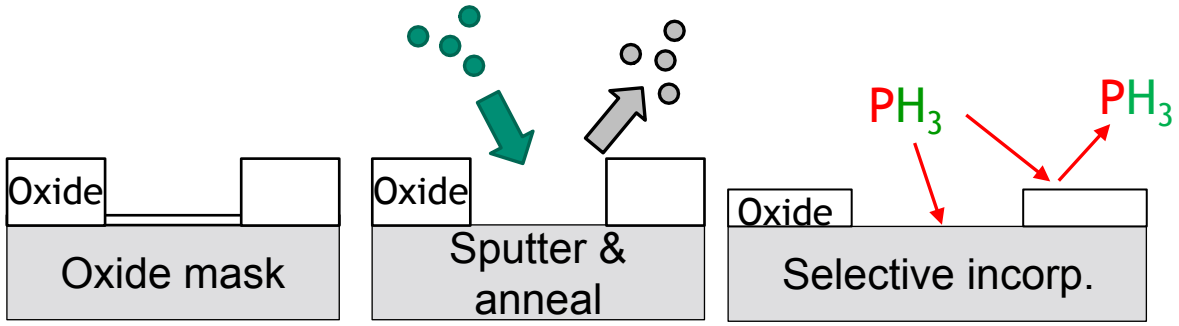
Wafer-scale high-throughput APAM using hard masks

Hydrogen lithography

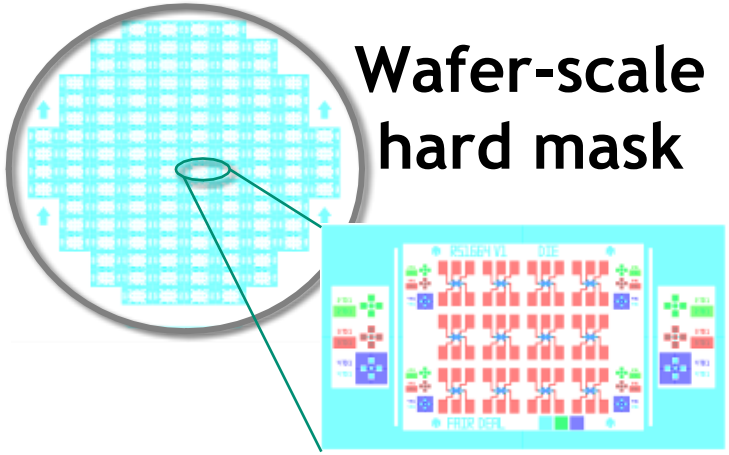


Low-throughput atomically precise process

Hard mask



High-throughput wafer-scale process



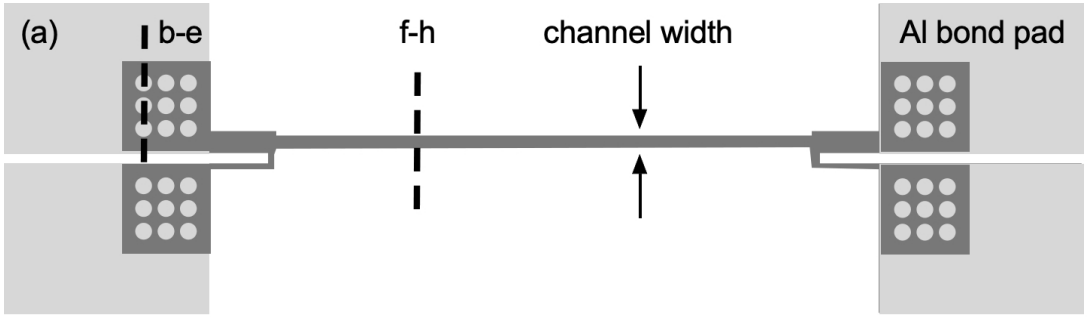
Wafer-scale hard mask

Process	2D Carrier Concentration ($x10^{14} cm^{-2}$)	Carrier Mobility ($cm^2V^{-1}s^{-1}$)
Hydrogen lithography	1.7	50
Hard mask	1.0	40

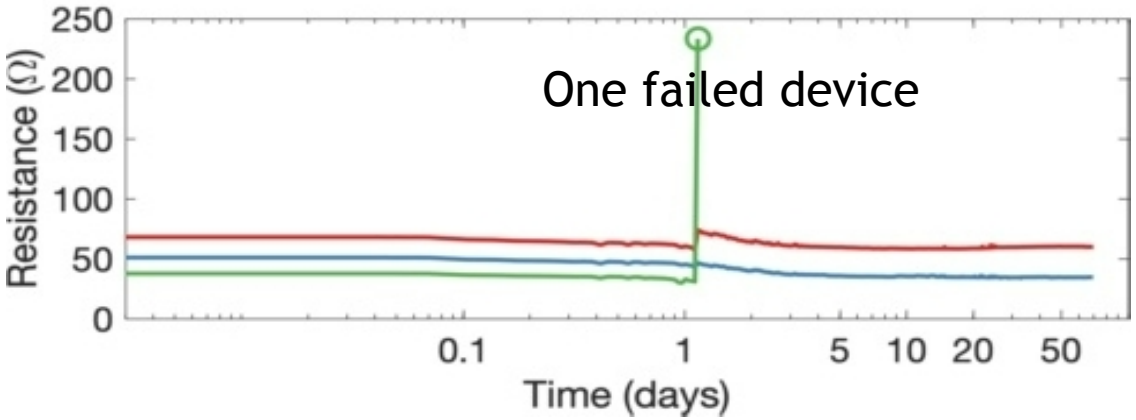
Need a wafer-scale tool for chemistry/ growth

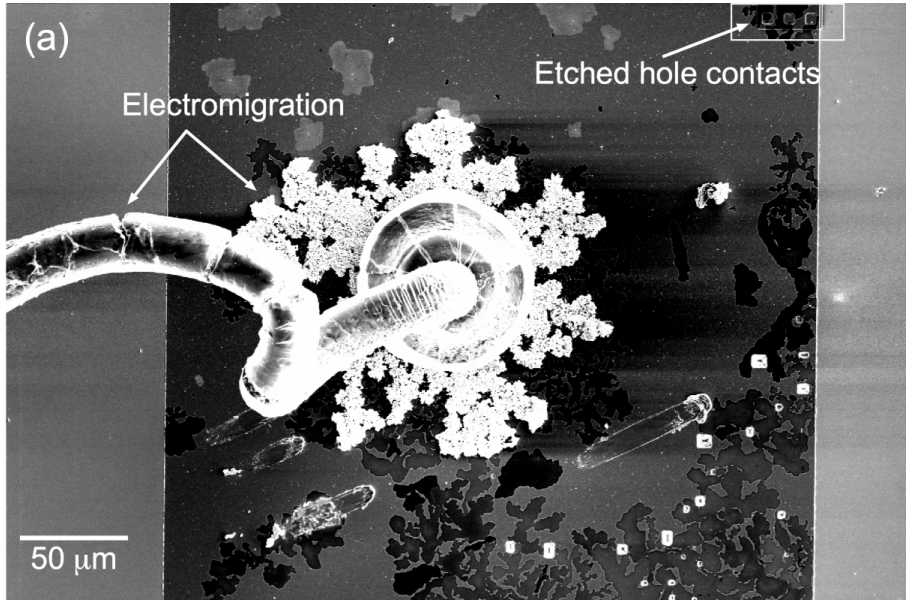
Accelerated lifetime testing

- Heat sample to 300 C
- Current density 5-10 MA / cm^2 (metal fails ~ 1 MA/cm^2)



- Monitor sample for months
- Analyze failed parts





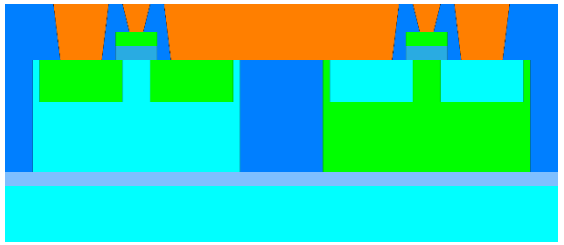
Failures never associated with APAM, always with electromigration

C. Halsey, "Accelerated lifetime testing and analysis of delta-doped silicon test structures", submitted.

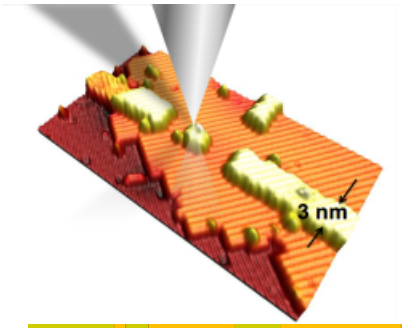
Can APAM be integrated into CMOS manufacturing?

Is it compatible with CMOS process flows?

Transistors



APAM



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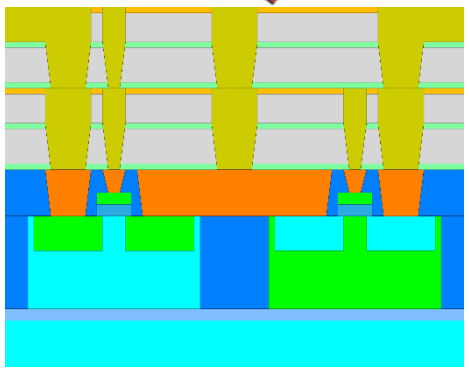


Yes

Can it be scaled?

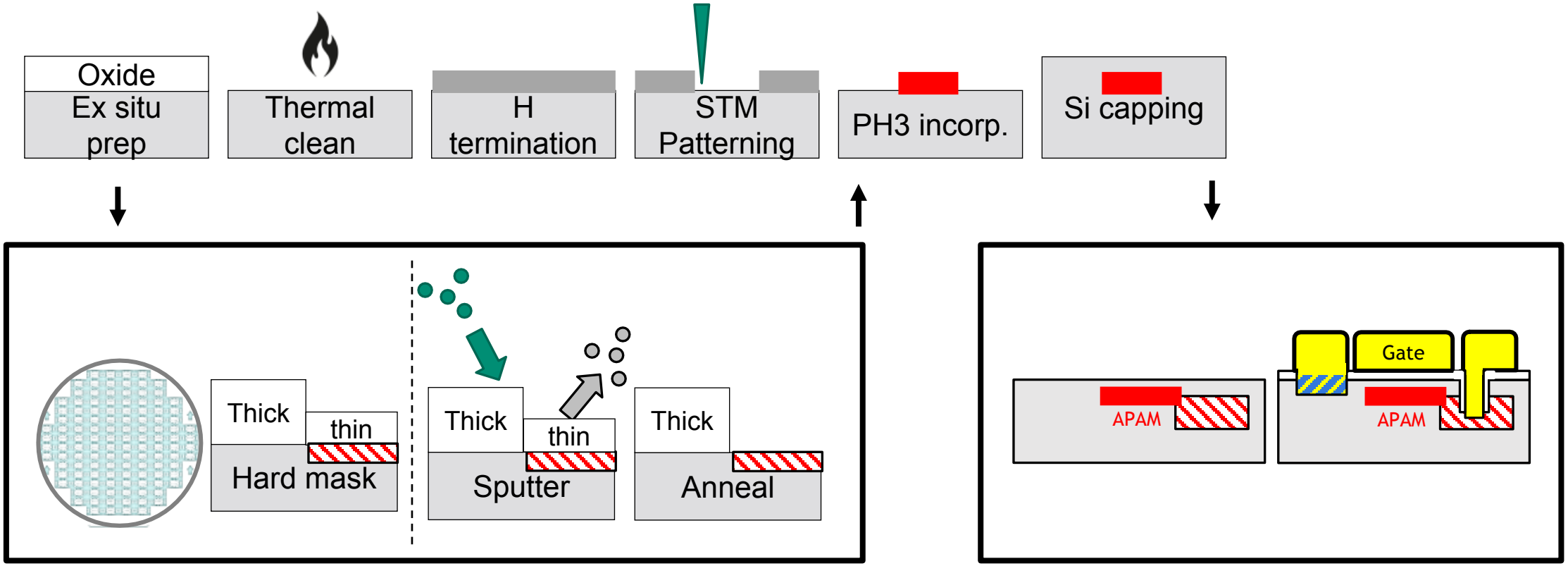
Yes, but…

Does it hold up to accelerated lifetime testing?

Yes

Outline – Digital electronics at the atomic scale

We have overcome the thermal budget issues with APAM, opening the door to microelectronics applications.



1. Integration with CMOS (contacts)
- Do no harm to parent CMOS
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- APAM robustness vs. CMOS

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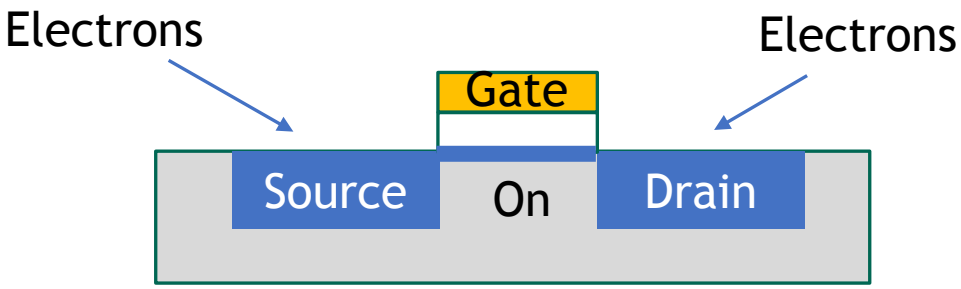
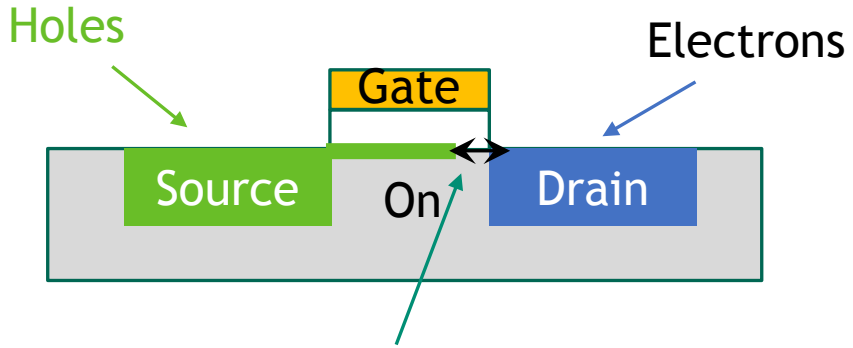
- Added features must preserve APAM
- Quality of APAM & other device elements

Why are APAM-enabled TFETs interesting?

MOSFET

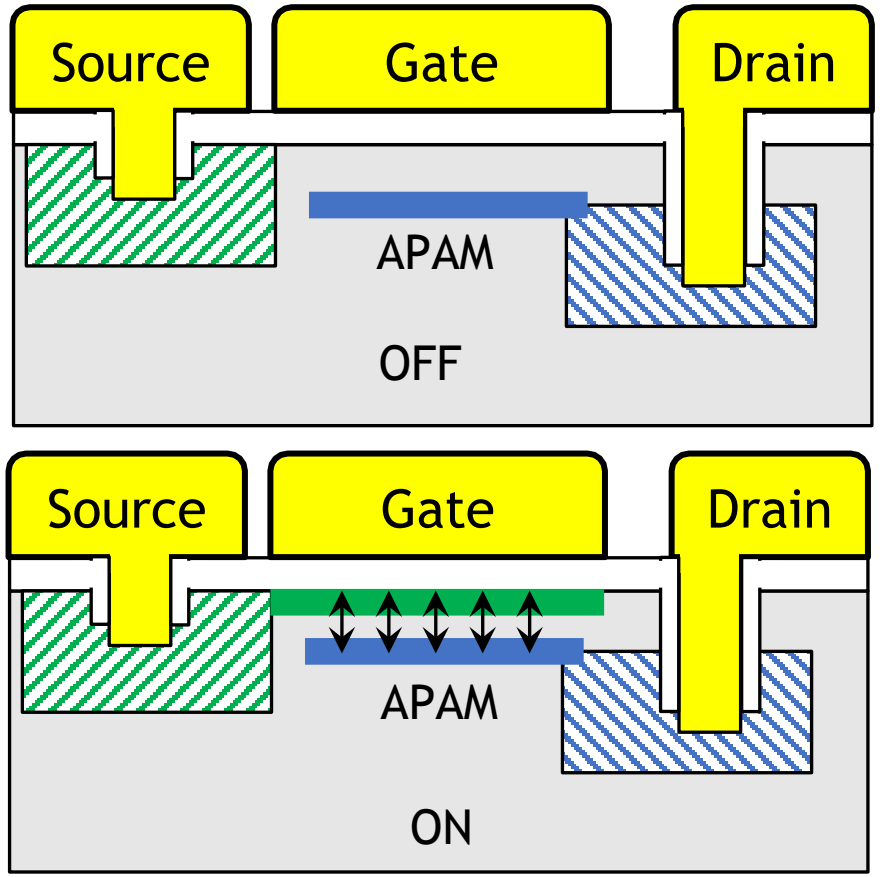


TFET



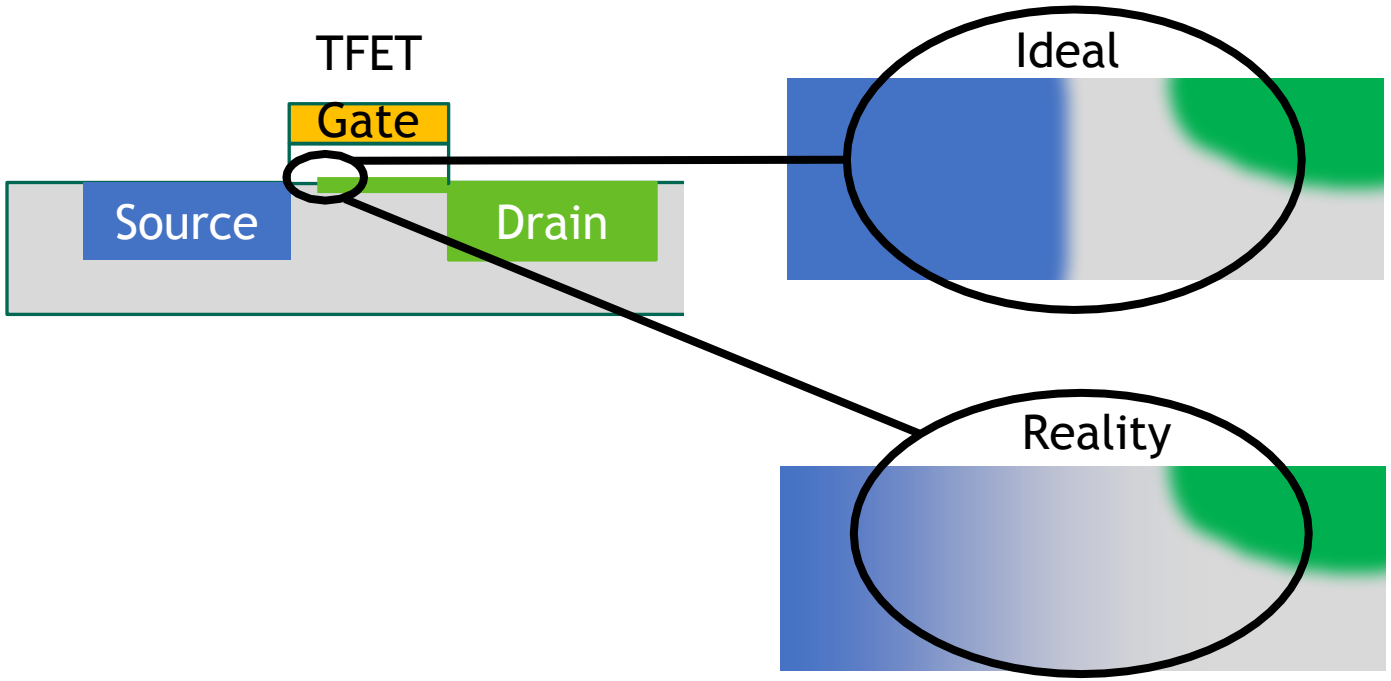
Tunneling makes the device energy efficient, but also introduces a speed bump reducing current

APAM confinement enables vertical geometry

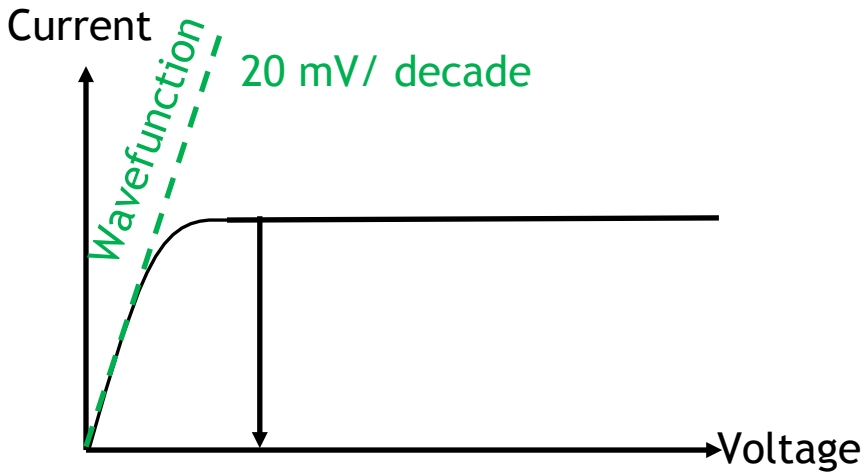


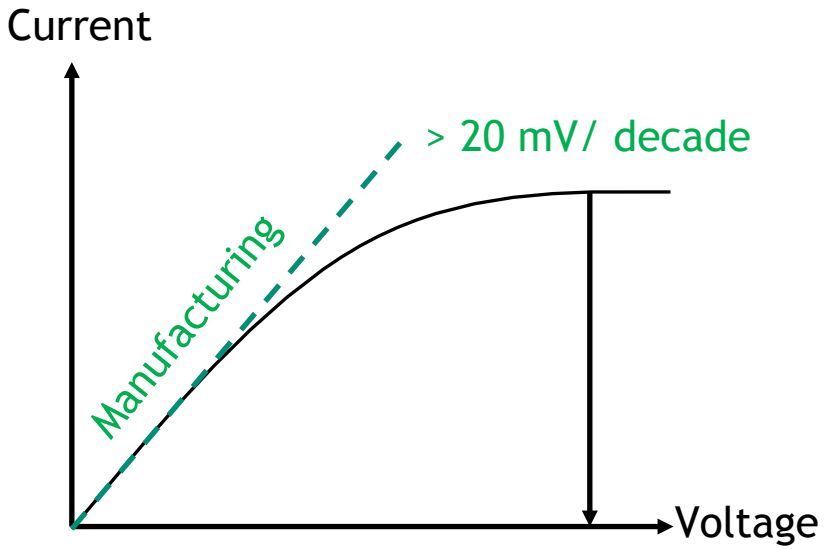
Vertical geometry potentially circumvents TFET limitations on current

Why are APAM-enabled TFETs interesting?



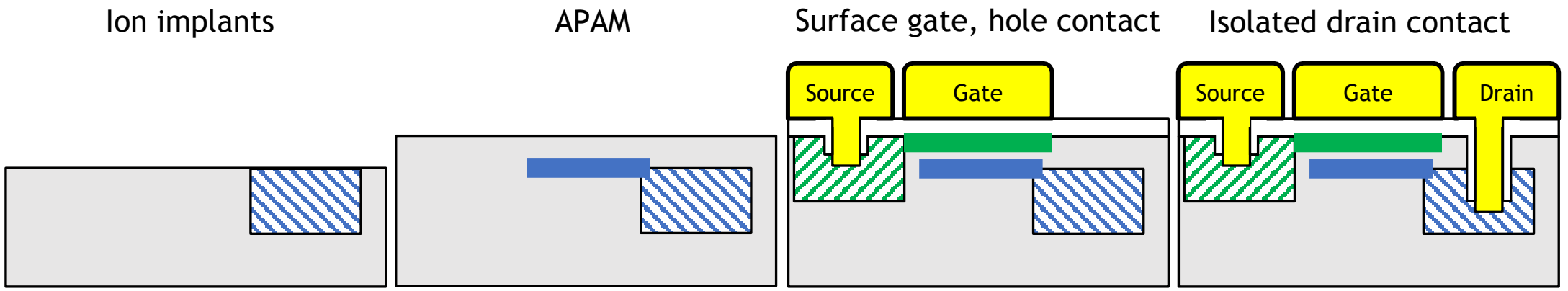
High temperature → diffusion



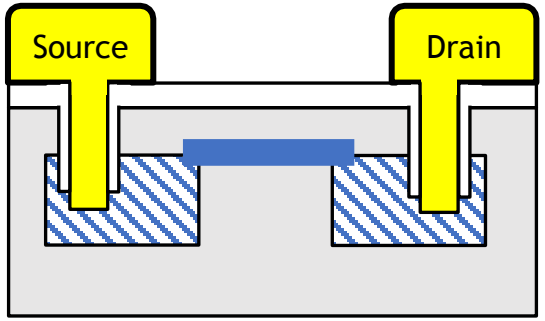


Atomically abrupt doping profiles may circumvent manufacturing limitations to TFET energy efficiency

How do you make an APAM vertical TFET?

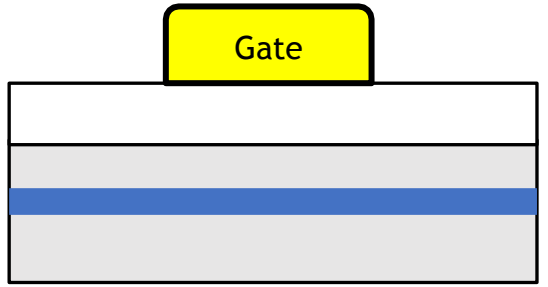


1. Isolated contacts



Electrons stay confined to APAM layer

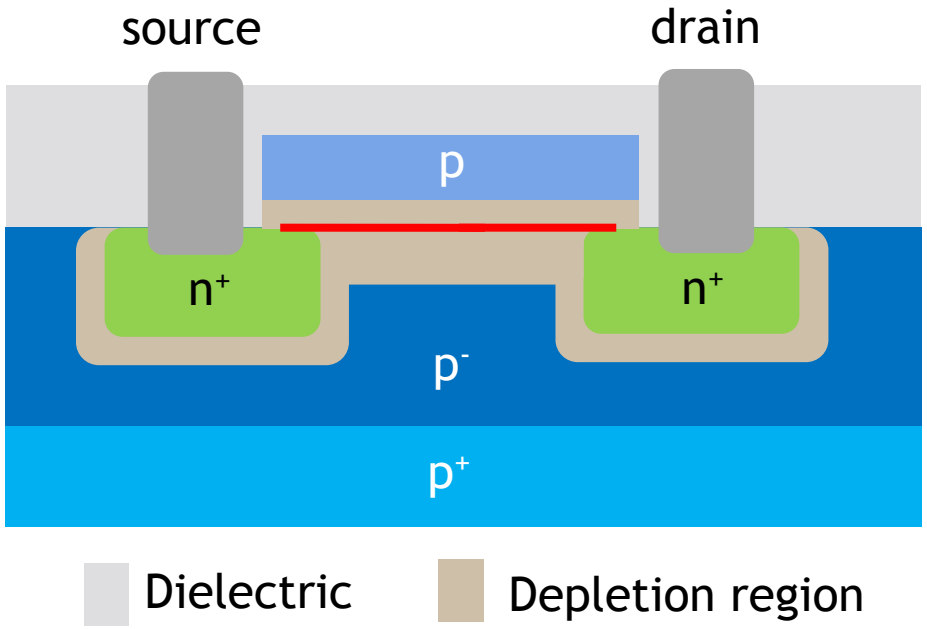
2. Surface gate



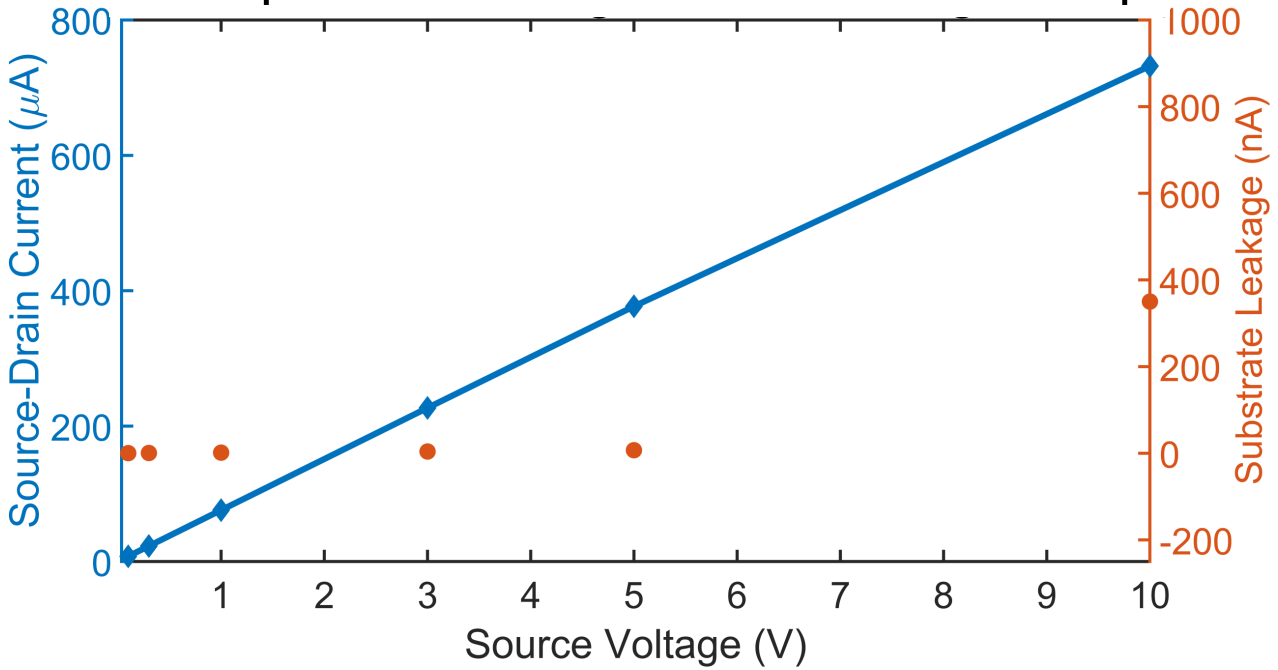
Need low density of charge traps & APAM layer to stay in place

APAM layer provides strong confinement, even at room temp.

P-N junctions pinch off leakage paths



Transport: 500 nm nanowire at room temp



Preserving doping profiles is a challenge

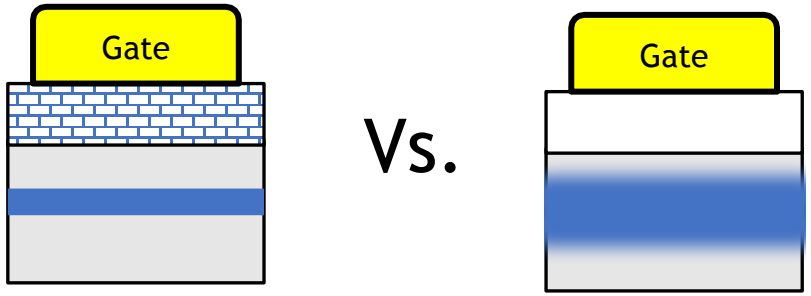
Current density > 30 MA/cm^2

[Whole story: Atomic scale processing session]

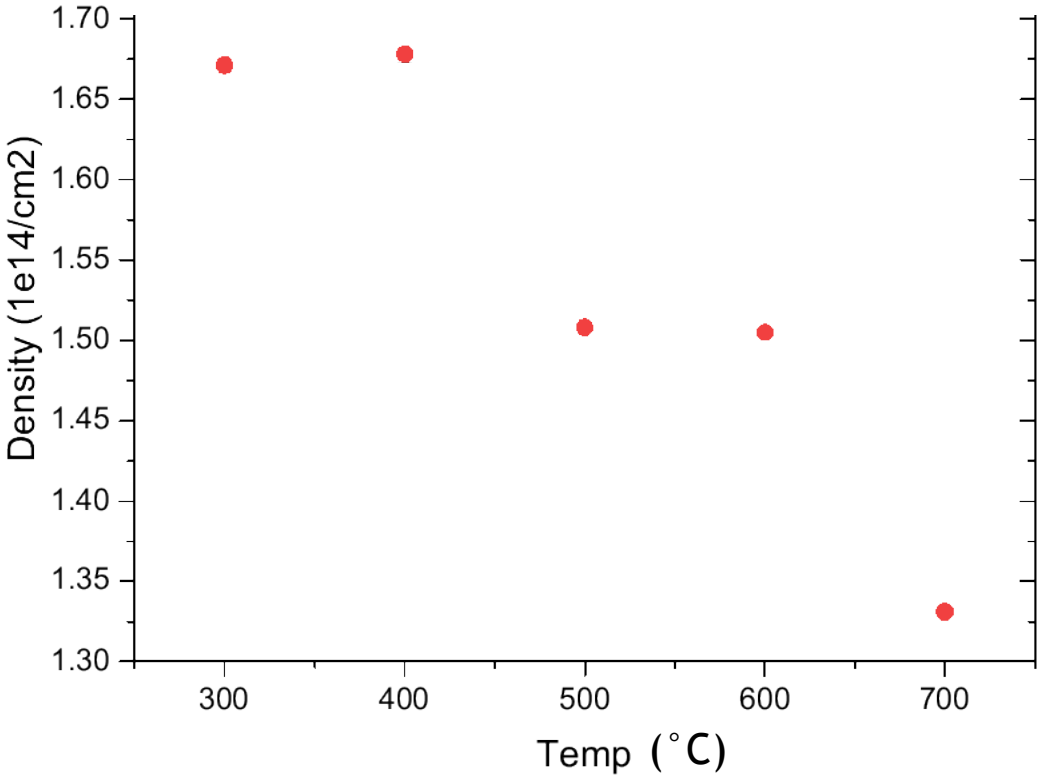
Room Temperature Operation of Donor-Based Atomically Precise Devices

Jeff Ivie

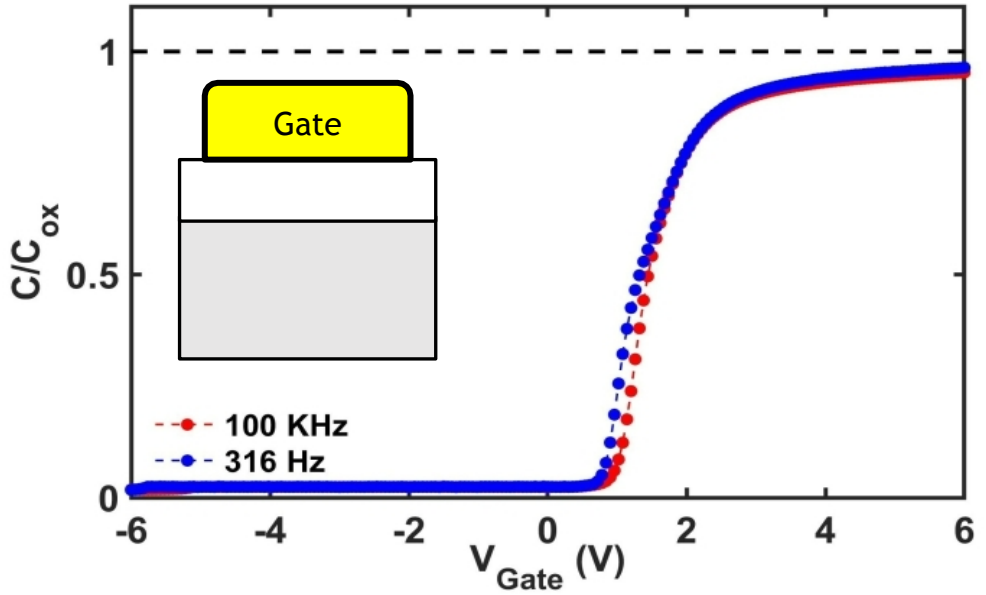
APAM-compatible surface gate



Vs.



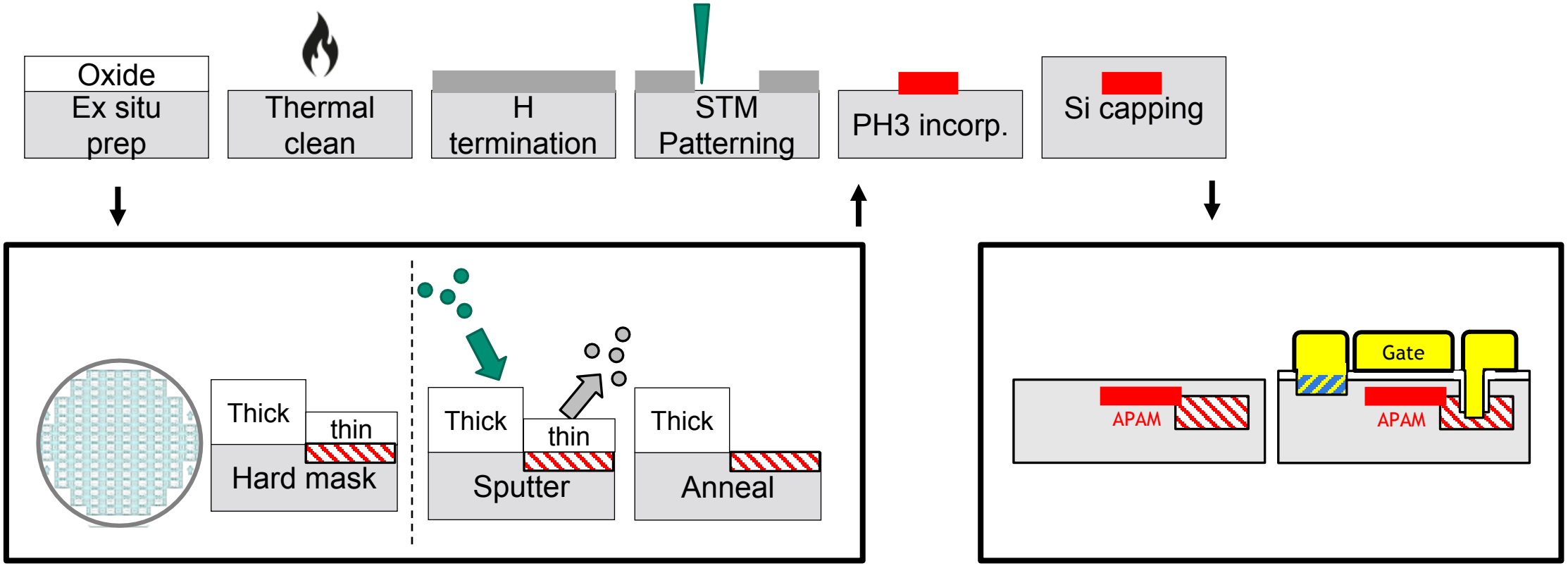
Reasonable trap density: 7 x 10^{11} $cm^{-2}eV^{-1}$



Whole story: Atomic scale processing session
Development of low thermal budget SI epitaxy and high-k/metal gate for APAM
Evan Anderson

Conclusion – Digital electronics at the atomic scale

We have overcome processing issues with APAM, opening the door to microelectronics applications.



1. Integration with CMOS (contacts)
   - Measure contact resistance improvement

2. Sophisticated devices (TFET)
   - Making our first TFETs!!

Questions? Shashank Misra: smisra@sandia.gov

Who	Section	Title
DeAnna Campbell	Contributed on-demand Atomic Scale Processing – 25	CMOS-compatible processing of atomic-precision donor devices
Jeff Ivie	Contributed on-demand Atomic Scale Processing – 28	Room temperature operation of donor-based atomically precise devices
Evan Anderson	Contributed on-demand Surface Science - 1	Development of low thermal budget SI epitaxy and high-k/metal gate for APAM
Dhamelyz Silva Quinones	Contributed on-demand Surface Science - 67	Reactions of Boron-containing molecules with H- and Cl-terminated Si(100)
James Owen	Contributed on-demand Atomic Scale Processing – 40	Towards ultraprecise bipolar 2D devices using APAM

Measurement: Lisa Tracy, Tzu-Ming Lu, Albert Grine, Connor Halsey, Ping Lu, Aaron Katzenmeyer, Chris Allemang

Microfabrication: Andrew Leenheer, DeAnna Campbell, Mark Gunter, Phillip Gamache

Modeling: Denis Mamaluy, Juan Granado, William Lepkowski, Andrew Baczewski, Quinn Campbell, Steve Young

Surface Science: Scott Schmucker, Evan Anderson, Jeff Ivie, Ezra Bussmann, Fabian Pena, Aaron Katzenmeyer, Esther Frederick, David Wheeler

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